# ECE3700J Introduction to Computer Organization

Homework 8

# Assigned: October November 29, 2022

**Due: 2:00pm on December 6, 2022 Submit a PDF file on Canvas**

1. (20 points) Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows parameters for a two-level cache memory.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Size | Miss Rate | Hit Time |
| L1 | 16 KB | 7.3% | 1.18 ns |
| L2 | 1 MB | 1.5% | 5.34 ns |

* 1. What is the AMAT for the computer? (10 points)

AMAT= L1 hit rate \* L1 hit time + L1 miss rate \* (L2 hit rate \* L2 hit time + L2 miss rate \* Mem access time)= 92.7%\*1.18+7.3%\*(98.5%\*5.34+1.5%\*70)=1.554ns

* 1. Assuming the L1 hit time determines the cycle times and a base CPI is 1.0 without any memory stalls, what is the total CPI? (10 points)

Total CPI=(1.18+36%\*7.3%\*(98.5%\*5.34+1.5%\*70))/1.18=1.14

1. (30 points) In this exercise, we will examine how replacement policies impact miss rate. Assume a 2-way set associative cache with 4 blocks. Following table gives addresses for memory access.
   1. Assuming an LRU replacement policy, how many hits does this address sequence exhibit? (10 points)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Block Address of memory | Hit/Miss | Evicted Block | Contents of Cache | | | |
| Set 0 | | Set 1 | |
| 1 | M |  |  |  | 1 |  |
| 3 | M |  |  |  | 1 | 3 |
| 5 | M | 1 |  |  | 5 | 3 |
| 1 | M | 3 |  |  | 5 | 1 |
| 3 | M | 5 |  |  | 3 | 1 |
| 1 | H |  |  |  | 3 | 1 |
| 3 | H |  |  |  | 3 | 1 |
| 5 | M | 1 |  |  | 3 | 5 |
| 3 | H |  |  |  | 3 | 5 |

3 hits

* 1. Assuming an MRU (most recently used) replacement policy, how many hits does this address sequence exhibit? (10 points)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Block Address of memory | Hit/Miss | Evicted Block | Contents of Cache | | | |
| Set 0 | | Set 1 | |
| 1 | M |  |  |  | 1 |  |
| 3 | M |  |  |  | 1 | 3 |
| 5 | M | 3 |  |  | 1 | 5 |
| 1 | H |  |  |  | 1 | 5 |
| 3 | M | 1 |  |  | 3 | 5 |
| 1 | M | 3 |  |  | 1 | 5 |
| 3 | M | 1 |  |  | 3 | 5 |
| 5 | H |  |  |  | 3 | 5 |
| 3 | H |  |  |  | 3 | 5 |

3 hits

* 1. Simulate a random replacement policy by flipping a coin. For example, “heads” means to evict the first block in a set and “tails” means to evict the second block in a set. How many hits does this address sequence exhibit? Note: you should flip the coin yourself, not by computer. (10 points)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Block Address of memory | Hit/Miss | Evicted Block | Contents of Cache | | | |
| Set 0 | | Set 1 | |
| 1 | M |  |  |  | 1 |  |
| 3 | M |  |  |  | 1 | 3 |
| 5 | M | 1 |  |  | 5 | 3 |
| 1 | M | 5 |  |  | 1 | 3 |
| 3 | H |  |  |  | 1 | 3 |
| 1 | H |  |  |  | 1 | 3 |
| 3 | H |  |  |  | 1 | 3 |
| 5 | M | 1 |  |  | 5 | 3 |
| 3 | H |  |  |  | 5 | 3 |

4 hits

1. (50 points) Virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. The following is a stream of virtual byte addresses used to access memory. Virtual addresses (in decimal): 12648, 45419, 46824, 16975, 40004, 12707, 52236

Assume 4 KB pages, a 4-entry fully associative TLB, and LRU replacement. If pages must be brought in from disk, increment to the next largest page number.

TLB:

|  |  |  |
| --- | --- | --- |
| Valid | Tag | Physical Page Number |
| 1 | 11 | 12 |
| 1 | 7 | 4 |
| 1 | 3 | 6 |
| 0 | 4 | 9 |

Page Table:

|  |  |
| --- | --- |
| Valid | Physical Page Number |
| 1 | 5 |
| 0 | Disk |
| 0 | Disk |
| 1 | 6 |
| 1 | 9 |
| 1 | 11 |
| 0 | Disk |
| 1 | 4 |
| 0 | Disk |
| 0 | Disk |
| 1 | 3 |
| 1 | 12 |

* 1. Given the virtual address stream, and the initial TLB and page table states shown above, show the final state of the system. Also list for each reference if it is a hit in the TLB, a hit in the page table, or a page fault. (15 points)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Addr(d) | Addr(h) | VPN | TLB hit | Page table | TLB change |
| 12648 | 0x3168 | 0x3 | y |  |  |
| 45419 | 0xb16b | 0xb | y |  |  |
| 46824 | 0xb6e8 | 0xb | y |  |  |
| 16975 | 0x424f | 0x4 | n | hit | 4th entry valid bit set to 1 |
| 40004 | 0x9c44 | 0x9 | n | Page fault | 2nd entry: <1, 9, 13> |
| 12707 | 0x31a3 | 0x3 | y |  |  |
| 52236 | 0xcc0c | 0xc | n | Page fault | 1st entry: <1, 12, 14> |

The final TLB:

|  |  |  |
| --- | --- | --- |
| Valid | Tag | Physical Page Number |
| 1 | 12 | 14 |
| 1 | 9 | 13 |
| 1 | 3 | 6 |
| 1 | 4 | 9 |

The final Page Table:

|  |  |
| --- | --- |
| Valid | Physical Page Number |
| 1 | 5 |
| 0 | Disk |
| 0 | Disk |
| 1 | 6 |
| 1 | 9 |
| 1 | 11 |
| 0 | Disk |
| 1 | 4 |
| 0 | Disk |
| 1 | 13 |
| 1 | 3 |
| 1 | 12 |
| 1 | 14 |

* 1. Repeat question (1), but this time use 16 KB pages instead of 4 KB pages. (15 points)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Addr(d) | Addr(h) | VPN | TLB hit | Page table | TLB change |
| 12648 | 0x3168 | 0 | n | hit | 4th entry: <1, 0, 5> |
| 45419 | 0xb16b | 2 | n | Page fault | 1st entry: <1, 2, 13> |
| 46824 | 0xb6e8 | 2 | y |  |  |
| 16975 | 0x424f | 1 | n | Page fault | 2nd entry: <1, 1, 14> |
| 40004 | 0x9c44 | 2 | y |  |  |
| 12707 | 0x31a3 | 0 | y |  |  |
| 52236 | 0xcc0c | 3 | y |  |  |

The final TLB:

|  |  |  |
| --- | --- | --- |
| Valid | Tag | Physical Page Number |
| 1 | 2 | 13 |
| 1 | 1 | 14 |
| 1 | 3 | 6 |
| 1 | 0 | 5 |

The final Page Table:

|  |  |
| --- | --- |
| Valid | Physical Page Number |
| 1 | 5 |
| 0 | 14 |
| 0 | 13 |
| 1 | 6 |
| 1 | 9 |
| 1 | 11 |
| 0 | Disk |
| 1 | 4 |
| 0 | Disk |
| 0 | Disk |
| 1 | 3 |
| 1 | 12 |

* 1. What would be some of the advantages and disadvantages of having a larger page size? (5 points)

Larger page size may decrease the page fault rate but increase the page fault penalty, and also reduces the flexibility of pages storage in main memory.

* 1. Show the final contents of the TLB if it is 2-way set associative. (15 points)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Addr(d) | Addr(h) | VPN | Index | Tag | TLB hit | Page table | TLB change |
| 12648 | 0x3168 | 0x3 | 1 | 1 | n | hit | 4th entry: <1,1,1,6> |
| 45419 | 0xb16b | 0xb | 1 | 5 | n | hit | 3rd entry: <1,1,5,12> |
| 46824 | 0xb6e8 | 0xb | 1 | 5 | y |  |  |
| 16975 | 0x424f | 0x4 | 0 | 2 | n | hit | 1st entry: <0,1,2,9> |
| 40004 | 0x9c44 | 0x9 | 1 | 4 | n | Page fault | 4th entry: <1,1,4,13> |
| 12707 | 0x31a3 | 0x3 | 1 | 1 | n | hit | 3rd entry: <1,1,1,6> |
| 52236 | 0xcc0c | 0xc | 0 | 6 | n | Page fault | 1st entry: <0,1,6,14> |

The final TLB:

|  |  |  |  |
| --- | --- | --- | --- |
| Index | Valid | Tag | Physical Page Number |
| 0 | 1 | 2 | 9 |
| 1 | 6 | 14 |
| 1 | 1 | 1 | 6 |
| 1 | 4 | 13 |