**ECE3700J Introduction to Computer Organization Homework 7**

**Assigned: November 14, 2023**

**Due: 2:00pm on November 21, 2023**

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1. (50 points) For a direct-mapped cache design with a 32-bit byte address, the following bits of the address are used to access the cache.

| **Tag** | **Index** | **Offset** |
| --- | --- | --- |
| 31–9 | 8–5 | 4–0 |

1. What is the cache block size (in words)? (2 points)
2. How many blocks does the cache have? (2 points)
3. What is the ratio between total bits required for such a cache implementation over the data storage bits? (3 points)

    Beginning from power on, the following byte addresses for cache references are recorded.

| **Address** | | | | | | | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0x10 | 0x04 | 0x20 | 0x74 | 0xEC | 0x0A | 0x711 | 0x1D | 0x9C | 0xD1C | 0xF6 | 0x878 |

1. (25 points) For each reference, list
   1. its tag, index, and offset
   2. whether it is a hit or a miss, and
   3. How many blocks were replaced (if any)?

*(you may find following table useful for answering this part of the problem)*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Byte Address | Tag | Index | Offset | Hit or Miss | Blocks replaced |
|  |  |  |  |  |  |
| .  .  . |  |  |  |  |  |
|  |  |  |  |  |  |

1. What is the hit ratio? (3 points)
2. Show the final state of the cache by completing the following table. (15 points)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Index | Valid | Tag | Word0 | … |
|  |  |  |  |  |
| .  .  . |  |  |  |  |
|  |  |  |  |  |

**NOTE: the following problems are optional and won’t be graded.**

1. Below is a list of memory address references, given as simplified word addresses:

0x03, 0x04, 0x05, 0x03, 0xBE, 0xBF, 0x58, 0x5C, 0xB0, 0x2C, 0xBA, 0xED

1. For each of these references, identify the tag and the cache index given a direct-mapped cache with 8 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.
2. For each of these references, identify the tag and the cache index given a direct-mapped cache with two-word blocks and a total size of 4 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.
3. You are asked to optimize a cache design for the given references. There are three direct-mapped cache designs possible, all with a total of 8 words of data: design C1 has 1-word blocks, design C2 has 2-word blocks, and design C3 has 4-word blocks. In terms of miss rate, which cache design is the best? If the miss stall time is 45 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles, and C3 takes 5 cycles, which is the best cache design?
4. In general, cache access time is proportional to its capacity. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for caches attached to each of two processors, P1 and P2.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Size | Miss Rate | Hit Time |
| P1 | 16KB | 5.1% | 1.25 ns |
| P2 | 32KB | 2.4% | 2.42 ns |

1. Assuming that the cache hit time determines the cycle times for P1 and P2, what are their respective clock rates?
2. What is the AMAT for P1 and P2? AMAT (Average Memory Access Time) is defined as follows: AMAT = Hit time + Miss rate × Miss penalty.
3. Assuming a base CPI of 1.0 without any memory stalls, what is the actual CPI for P1 and P2? Which processor is faster?