**ECE3700J Introduction to Computer Organization Homework 8**

**Assigned: November 21, 2023**

**Due: 2:00pm on November 28, 2023**

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1. (50 points) Given the following byte addresses for memory access:

33, 130, 34, 35, 165, 79, 138, 14, 189, 47, 186, 252

1. Show the final cache contents for a 3-way set associative cache with two-word blocks and a total size of 24 words. Use LRU replacement. For each reference identify the index bits, the tag bits, the offset bits, and if it is a hit or a miss. You may find the following tables useful. (20 points)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Set Index | Valid | Tag | Data | |
| Word0 | … |
|  |  |  |  |  |
| .  .  . |  |  |  |
| .  .  . | .  .  . |  |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Byte Address | Binary | Tag | Set Index | Word Offset | Byte Offset | Hit/Miss |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
| .  .  . |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |

1. Show the final cache contents for a fully associative cache with one-word blocks and a total size of 8 words. Use LRU replacement. For each reference identify the index bits, the tag bits, and if it is a hit or a miss. You may find the following table useful. (10 points)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Byte Address | Binary | Tag | Byte Offset | Hit/Miss |
|  |  |  |  |  |
|  |  |  |  |  |
| .  .  . |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

1. What is the miss rate for a fully associative cache with two-word blocks and a total size of 8 words, using LRU replacement? What is the miss rate using MRU (most recently used) replacement? You may find the following table useful. (20 points)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Byte Address | Binary | Tag | Word Offset | Byte Offset | H/M (LRU) | H/M (MRU) |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
| .  .  . |  |  |  |  |  |  |
|  |  |  |  |  |  |  |

LRU: miss rate = \_\_\_\_\_\_\_\_\_\_\_\_\_\_

MRU: miss rate = \_\_\_\_\_\_\_\_\_\_\_\_\_\_

**NOTE: the following problems are optional and won’t be graded.**

1. For a 2-way set associative cache with a 32-bit address and write back mechanism, the partition of the 32 bits are as follows:

* Offset: bit 7 to 0
* Index: bit 11-8

1. What is the size of the cache?

Starting from power on, the following byte addresses were used to access the cache memory: 0, 33, 20, 156, 332, 64, 1004, 301, 149, 3002, 160, 2314

1. What is the hit rate?
2. Show the final state of the cache. You may find the following tables useful.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Hit/Miss | Byte Address | Binary | Tag | Set Index | Word Offset | Byte Offset |
|  |  |  |  |  |  |  |
| .  .  . |  |  |  |  |  |  |
|  |  |  |  |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Set Index | Valid | Dirty | Tag | Data |
|  |  |  |  |  |
| .  .  . |  |  |  |
| .  .  . | .  .  . |  |  |  |

1. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows parameters for a two-level cache memory.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Size | Miss Rate | Hit Time |
| L1 | 16 KB | 7.3% | 1.18 ns |
| L2 | 1 MB | 1.5% | 5.34 ns |

1. What is the AMAT for the computer?
2. Assuming the L1 hit time determines the cycle times and a base CPI is 1.0 without any memory stalls, what is the total CPI?
3. In this exercise, we will examine how replacement policies impact miss rate. Assume a 2-way set associative cache with 4 blocks. Following table gives addresses for memory access.
4. Assuming an LRU replacement policy, how many hits does this address sequence exhibit?
5. Assuming an MRU (most recently used) replacement policy, how many hits does this address sequence exhibit?
6. Simulate a random replacement policy by flipping a coin. For example, “heads” means to evict the first block in a set and “tails” means to evict the second block in a set. How many hits does this address sequence exhibit? Note: you should flip the coin yourself, not by computer.

You may find following table useful:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Block Address of memory | Hit/Miss | Evicted Block | Contents of Cache | | | |
| Set 0 | | Set 1 | |
| 1 |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |
| 5 |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |
| 1 |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |
| 5 |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |