
JOINT INSTITUTE
交大密西根学院

ECE2700J Introduction to Logic Design

# Lab 1
# Design of a Full Adder
## - A Tutorial on Vivado and Multisim

UM-SJTU Joint Institute
Shanghai Jiao Tong University
May 2022

## 1. Objective

- To draw and simulate simple logic circuits the software tool.
- To install Xilinx Vivado software on your computer supporting digital circuit prototyping on FPGA.
- To become familiar with Digilent Basys 3 FPGA Training Board

## 2. Setup Basys 3 FPGA board

Basys 3 board is a Field Programmable Gate Array (FPGA) digital circuit development platform that we will use to implement digital circuits in this class, as shown in Figure 1. The board is centered around a Xilinx Artix-7 FPGA chip. It also provides rich I/O resources for users to test/implement a digital device. These include switches, LEDs, pushbuttons, seven-segment displays, VGA output, USB port, etc. The switches and pushbuttons can be used to provide digital input signals and the LEDs can be used to capture the digital outputs. There are also four seven-segment displays (SSDs) for outputs. All these I/O resources are physically connected to the FPGA chip.

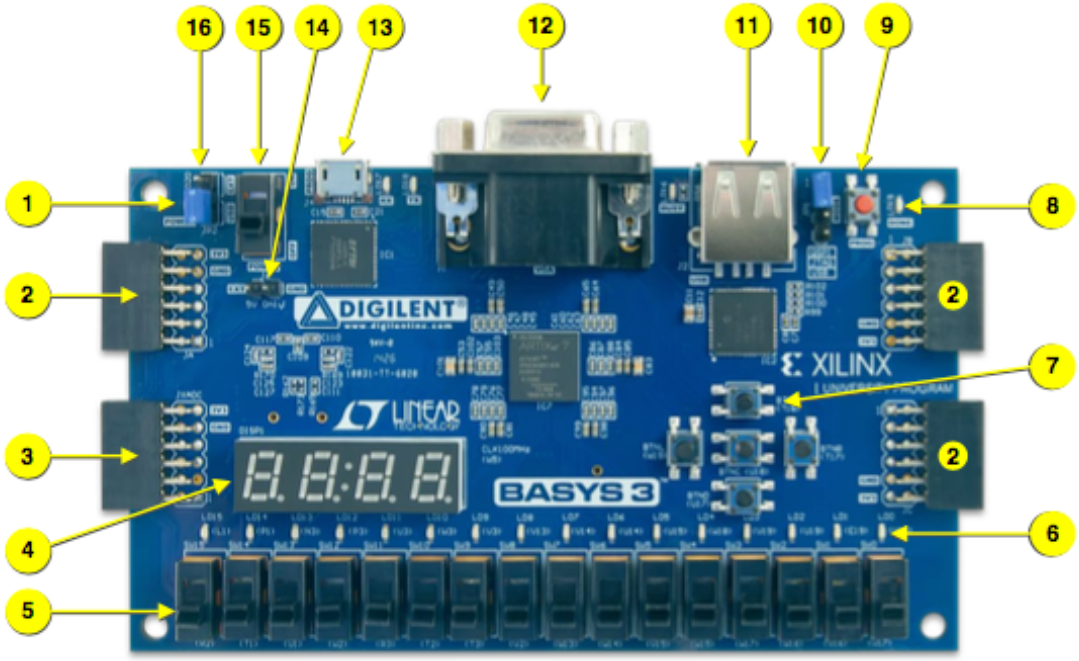


**Figure 1. Basys 3 FPGA Board**

Connect your Basys 3 board to your computer with the USB cable (at 13). Put the jumper (at 10) on the middle two pins (JTAG option). Turn on the board (at 15).

## 3. Draw schematic in Multisim

Multisim is an advanced, industry-standard, in-class SPICE simulation environment. We use this software in this class to capture simple schematics of your designed digital circuit, simulate the circuit, and verify the functions of the circuit.

In this section, you will draw the schematic of a simplified full adder as shown in Figure 2.

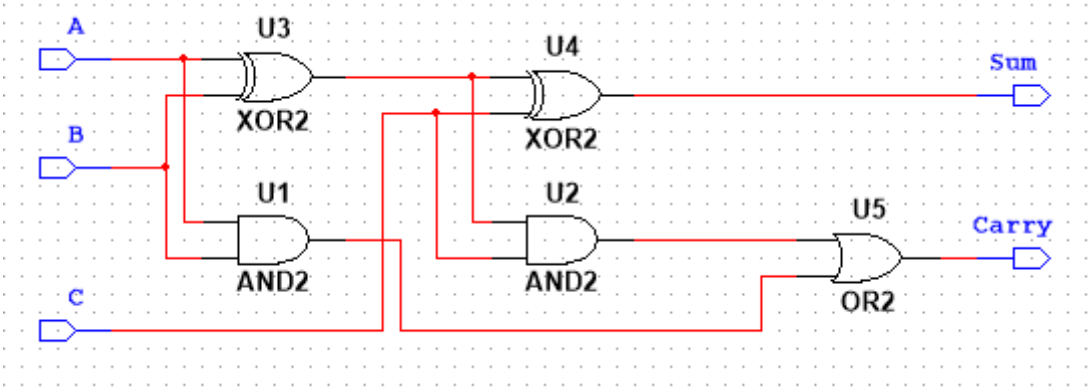


**Figure 2. Full Adder Gate-Level Schematic**

- Launch Multisim
- In Multisim, File → New → select "PLD design…" → Create, to create a new file;
- In the "New PLD Design – Step 1 of 3" window, select "Digilent Basys 3" → Next, to choose the FPGA board that your want to implement your circuit in;
- In the "New PLD Design – Step 2 of 3" window, give a name to your PLD design;
- In the "New PLD Design – Step 3 of 3" window, check the I/O resources on the Basys 3 FPGA board that you plan to used for the inputs and outputs of your circuit; in this lab, we will use SW0, SW1, SW2 for the three inputs A, B, C, and LED0 and LED1 for the two outputs Sum and Carry, as shown in Figure 3;
- Finish;

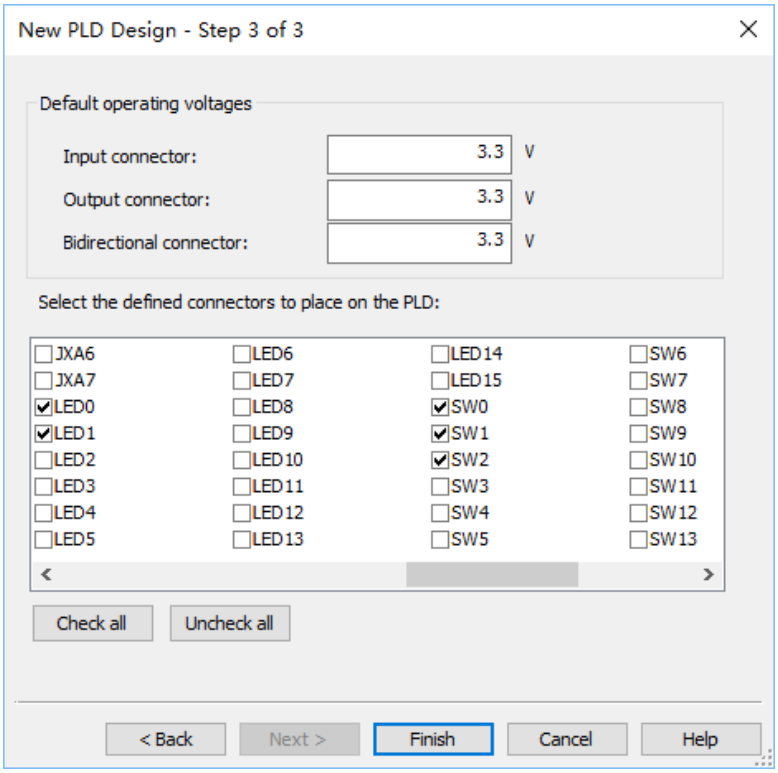


**Figure 3. Choosing I/O resources on an FPGA board**

- From the drop down menu: Place → New hierarchical block, to create a block of circuit on the work sheet;
- In the "Hierarchical Block Properties" window, give a name to the block you are creating, and specify the number of inputs and outputs; obviously we will create a 3 input and 2 output circuit block, as shown in Figure 4;
- Click OK;

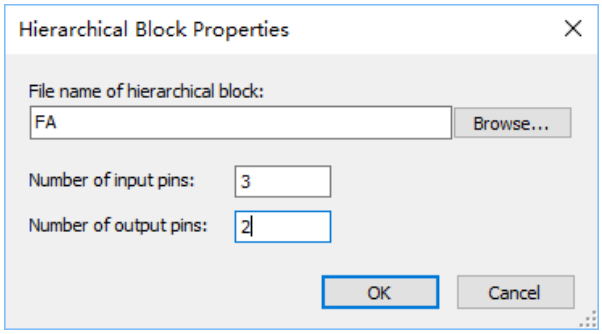


**Figure 4. Creating a hierarchical block**

- Double click on the block
- In the "Hierarchical Block/Subcircuit" window, click "Open subsheet", then you will come to a new schematic work sheet with 3 inputs and 2 outputs as you have specified, rename the inputs and outputs by double click on the ports; draw the schematic shown in Figure 2.
- From the drop down menu: Place → Component, to place necessary digital/analog components;
- In the "Select a Component" window, select appropriate gates to place on the work sheet from "PLD Logic" group and "LOGIC_GATES" family, where "AND2" means two-input AND gate, "INV" means invertor, and so on;
- Connect the components with wires using the mouse;
- Save your files;

Now your schematic should look like the one shown in Figure 2.

- Go back to the first schematic work sheet;
- Connect the switches (SW) and LEDs (LED) to the inputs and outputs of the block;

Now your schematic should look like the following figure.

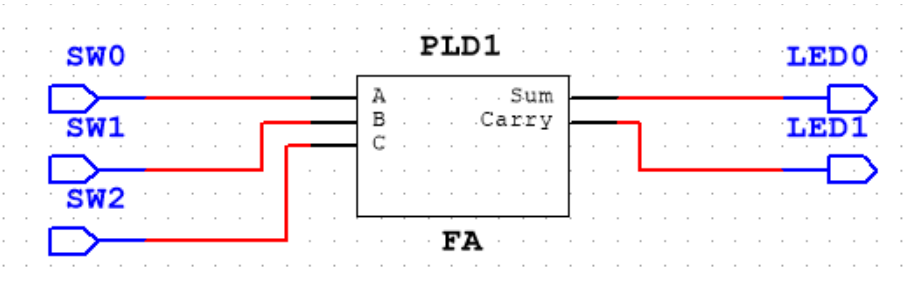


**Figure 5. Completed circuit**

## 4. Simulate your circuit in Multisim

One of the benefits of creating a hierarchical block is that it can be reused as many times as you want.

- From the drop-down menu: File → New → select "Blank" → Create, to create a new file and schematic work sheet;
- From the drop-down menu: Place → Hierarchical block from file;
- Select the file for the hierarchical block you just created;
- Click OK on the next window;
- Place the block on the new work sheet;
- From the drop-down menu: Place → Component;
- In the "Select a Component" window, select input sources from "Sources" group and "DIGITAL_SOURCES" family, use "INTERACTIVE_DIGITAL_CONSTANT", one for each of the 3 inputs, A, B, and C;
- In the "Select a Component" window, select probes to capture the outputs from "Indicators" group and "PROBE" family, use one for each of the two outputs, Sum and Carry;
- Connect the components with wires using the mouse
- Save your file;

Now your schematic should look like this:

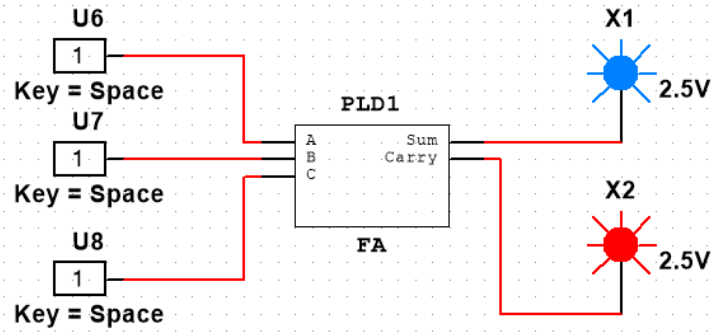


**Figure 6. Completed schematic for simulation**

- From the drop-down menu: Simulate → Run, to simulate your circuit;
- Click on the input sources to toggle digital value, to provide "1" or "0" inputs to the circuit;
- Observe the changes on the probes to verify the function of your circuit. Complete the following truth table for the circuit. Have it checked by one of the TAs before you go to the next step.

| A | B | C | Sum | Carry |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

## 5. Xilinx Vivado installation

Skip this section if you have already had the Vivado software installed.

Vivado is an industrial strength electronic system design software tool provided by Xilinx Inc. In this lab, Vivado will be used to convert the virtual schematic in Multisim to a real circuit, and implement the circuit in the Basys 3 FPGA board.

Download Vivado HL WebPACK Edition from Xilinx Website (xilinx.com). Vivado HL WebPACK Edition is free to use, but you need to sign up at xilinx.com.

Install Vivado WebPACK with the downloaded installer. You may choose the tools you need, but default tools are enough for our labs in this class.

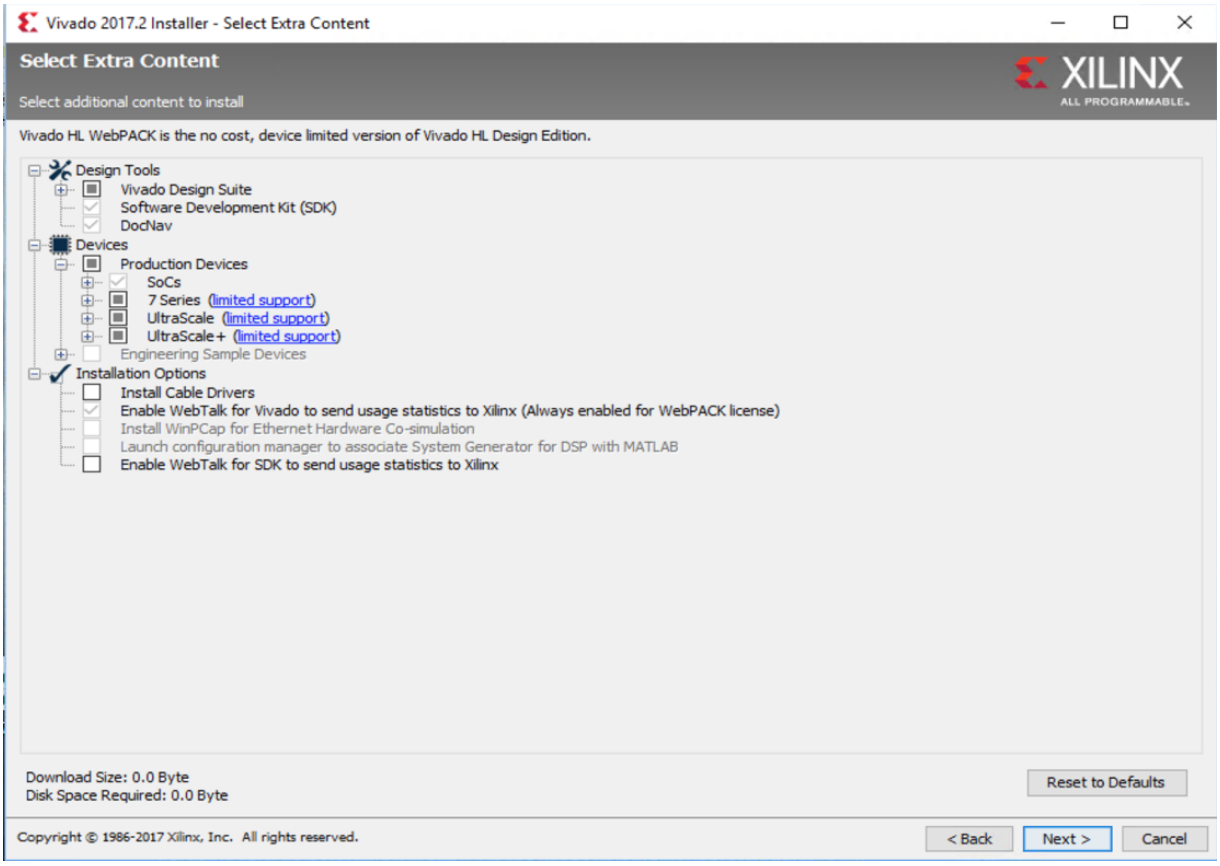


**Figure 7. Choose necessary tools to install for Vivado**

## 6. Implement your circuit with Multisim and Vivado

In this section, you will implement the circuit that you have created above using Multisim together with Vivado software.

- Go back to the schematic shown in Figure 5.
- From the drop-down menu: Transfer → Export to PLD, to download your circuit to the Basys 3 FPGA board;

- In the “PLD Export – Step 1 of 2” window, select “Program the connected PLD”, and check “Save generated programming file”; Next;
- In the “PLD Export – Step 2 of 2” window, make sure Xilinx Vivado Design Suite is the selected tool to use; Finish; **Note: in this step, you must select the path as: “ ….\Vivado\2017.2”,** this is because Multisim only checks whether there is a directory named “\bin” inside;
- Wait… (this may take a few minutes), when the process is finished, the DONE LED on the FPGA board ( 

in Figure 1) should be lit;
- Verify the function of your circuit on the board against the above truth table.

## 7. Deliverable

This is a 1-week lab. The full score for this lab is 100 points.

1) Demonstrate your board to the TAs before your lab session ends.
2) Upload source files on Canvas by **10:00pm, May 21, 2022**.