

Problem Statement/Introduction

The work presents the automation of the linting process for UVM testbench files using the AMIQ Verissimo tool, integrated within an automation framework. The automation is structured into three distinct phases to streamline and standardize the lint flow. The define phase, involves specifying all necessary parameters for the linting process. These parameters are defined based on their nature and role within the flow, setting the foundation for subsequent steps. The setup phase, focuses on generating the required configuration, run scripts, and support files. Once these files are prepared, the Verissimo tool will be invoked to initiate the linting operation, ensuring the automation environment is fully configured. The final phase is the execute phase, during which setup scripts are executed.

Proposed Methodology/Advantages

The proposed methodology has three phases namely define, setup and execute where each phase runs sequentially meeting the requirements and necessary specifications.

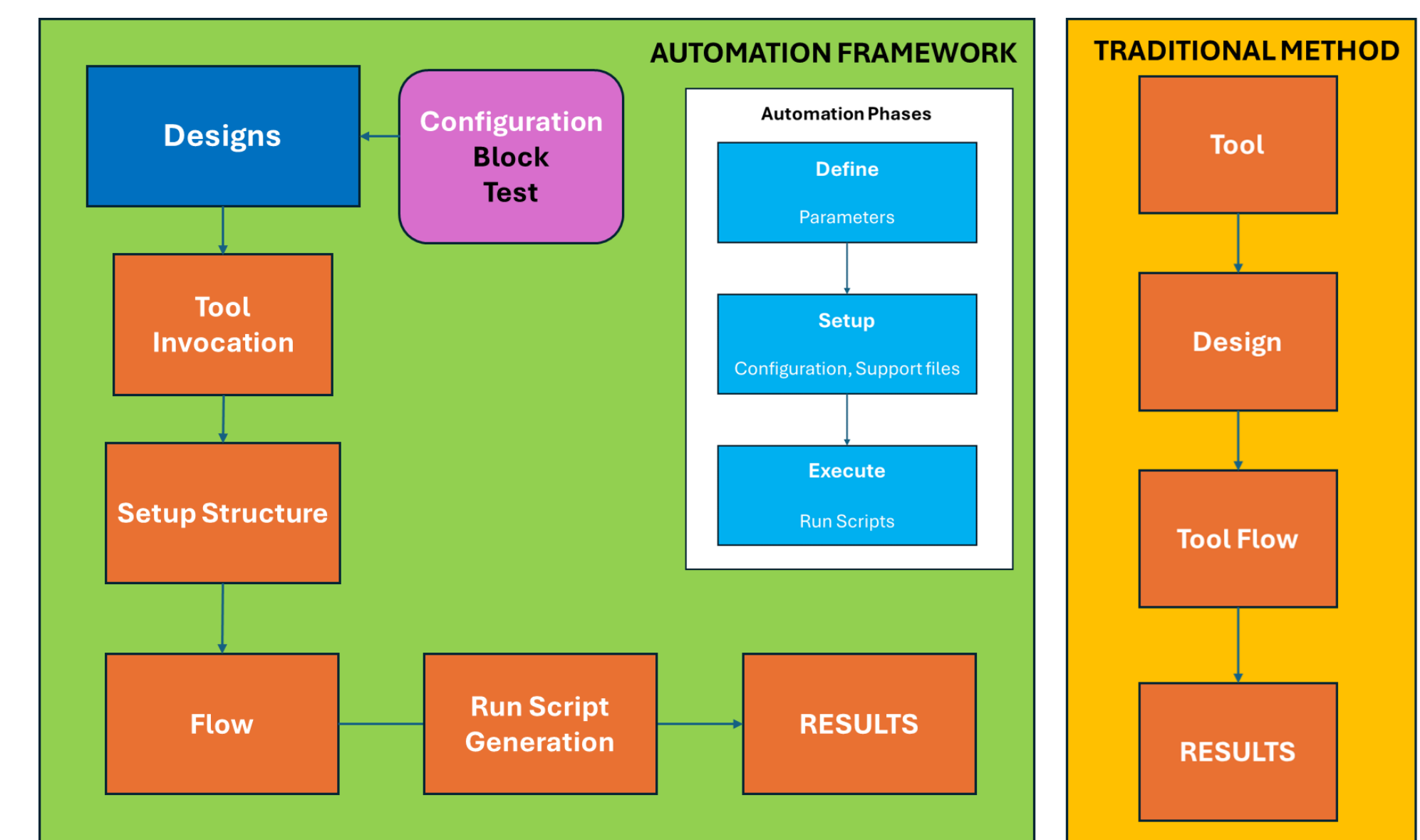


Figure 1 Automation Framework and Traditional Flow

To eliminate manual effort, enforce consistency, and accelerate the linting process for UVM testbenches using AMIQ verissimo, by developing a modular, scalable, and fully automated framework that supports both CLI and GUI workflows.

Implementation Details/Diagram

There are files which are generated in the automated flow which are required in the flow.

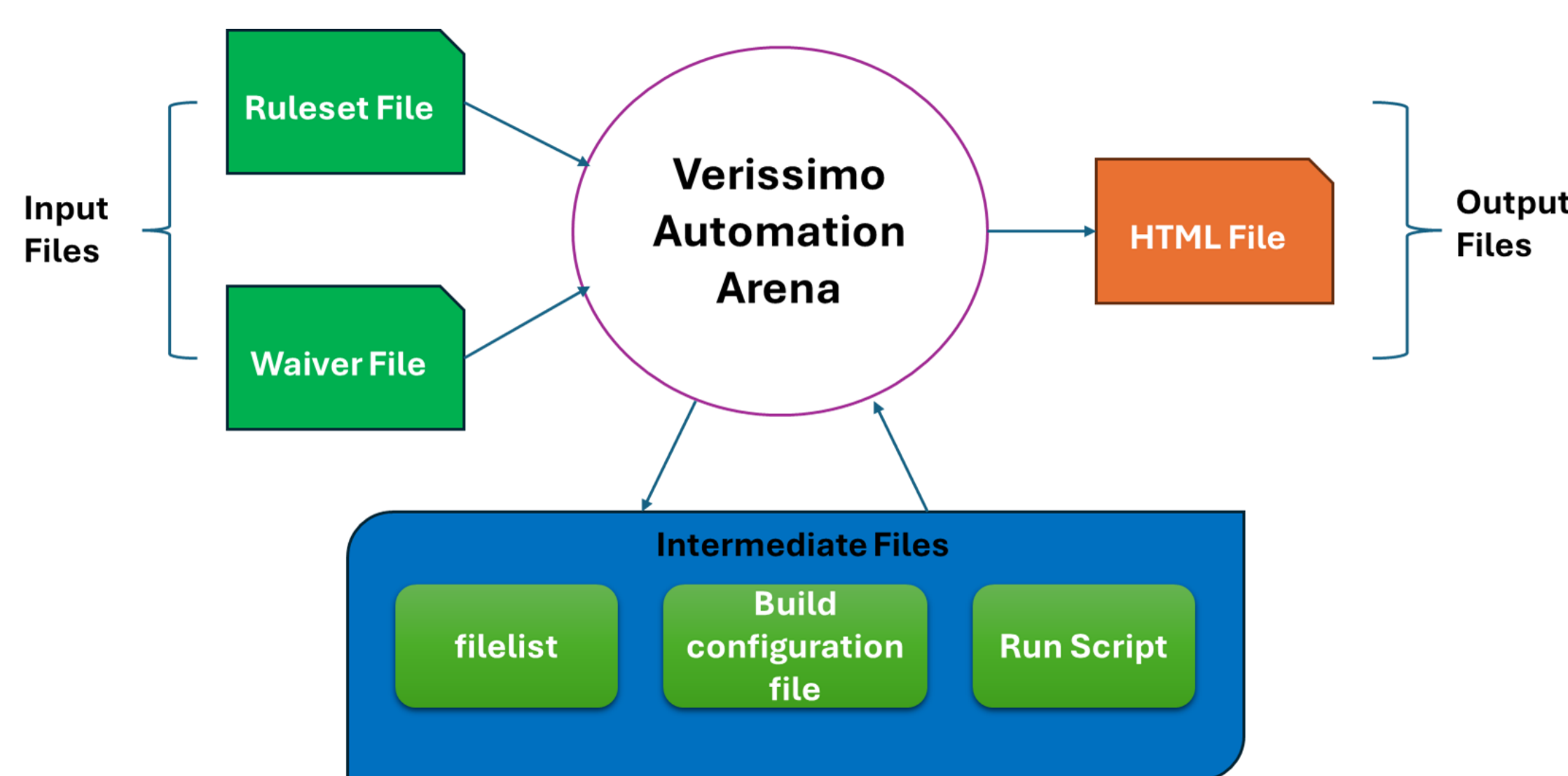


Figure 2 Inputs and outputs of Automation Framework

The input files ruleset and waivers are fetched from custom or standard directories. A set of intermediate files are created, which includes testbench filelist, build configuration file containing top block and uvm package information, and a run script to track information of all parameters. This setup allows for a flexible and automated verification lint flow tailored for UVM-based environments.

Implementation Details/Flow Chart

The implementation has been done covering complete flow of lint run and it covers error handling parts included. The file generation and execution along with verissimo automation flow is shown below.

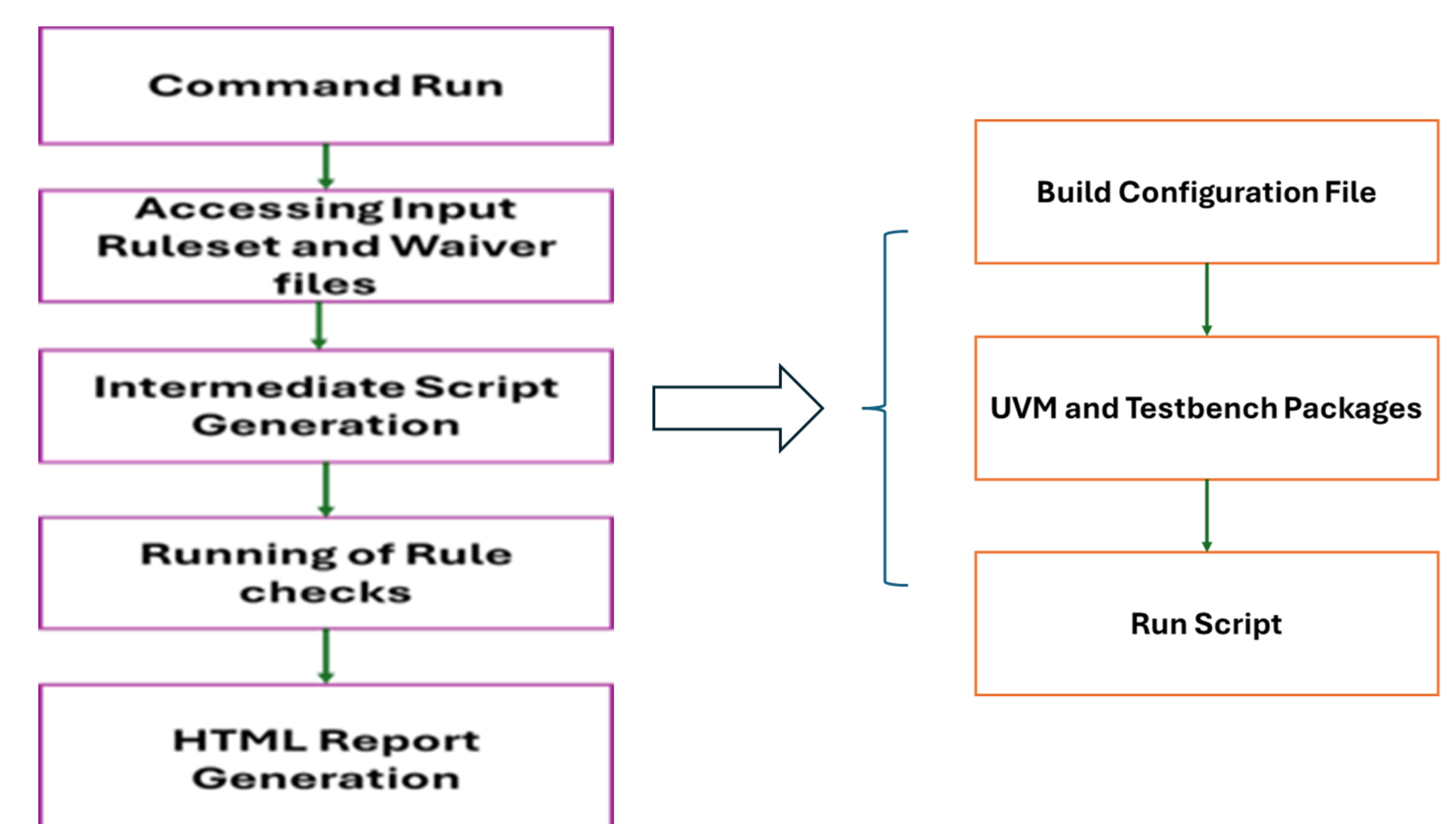


Figure 3 Verissimo Automation Flow

Results

The automation framework wraps the UVM testbench lint flow, providing an interface to user that facilitates the tool setup, execution and report results in standard location, the automation eliminates the manual tool setup and automates 100% the lint execution flow. The automation framework has been implanted in a way that can be escalated from IP to SOC level and used by different projects across design verification teams. The framework supports both command-line interface (CLI) and graphical user interface (GUI) modes, making it flexible and user-friendly. The verissimo tool report is generated in HTML format as the same format as running the verissimo tool standalone. Given the increasing complexity of UVM-based designs, this automated approach ensures consistent enforcement of coding guidelines, thereby enhancing code quality and maintainability.

Conclusion

The automation framework is developed in a modular way, internally it will run three-phases, from setup to execute the verissimo tool for UVM testbench lint checks. Enabled full integration with CLI and GUI, supporting diverse user needs and streamlines the design verification process. The tool setup has been fully automated to reduce the manual effort and increased consistency of linting across design verification projects to improve code quality by enforcing UVM standard guidelines. It has been demonstrated adaptability across multiple design at different levels without the need for reconfiguration. In the future the tool automation can be integrated in continuous integration and continues delivery pipelines and adding support for additional static analysis tools and advance rule customization.

References

- [1] <https://eda.amiq.com>
- [2] <https://www.chipverify.com>
- [3] <https://vlsiverify.com>