Next-Gen Low Power Verification: Empowering Shift-Left Predictive Analysis with Virtual Instrumentation

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ABSTRACT

Power is one of the important parameters impacting today's electronic designs and with increasing complexities in the power structure and complex power domain definitions, the need to minimize dynamic and static power consumption creates verification challenges.

For all low power designs, power intent/UPF is a key and generating a clean UPF helps throughout the design flow and reduces the overall turnaround time of projects. For complex SoCs, due to increase in physical partitions and supply rail restrictions for various partitions, can make UPF generation challenging, i.e. the UPFs that are being generated need to be physical implementation aware. These generated UPF needs to be validated thoroughly to make sure UPF is clean from syntax, schematics, consistency w.r.t to power state tables and Implementation aspects and if any issues in the UPF constructs then it's better to be caught earlier at the RTL stage itself so that issues can be fixed sooner and faster without involving implementation phase/cycle.

VC LP static low power verification solution includes UPF Consistency Checks, Structural Power/Ground (PG) Checks and Functional checks and Architectural checks. Traditional use models of VC LP allow to make sure UPF consistency w.r.t power state tables are clean at RTL stage and at Netlist stage, low power cells are correctly inserted that makes design structurally and electrically correct. There is an increasing demand to catch and verify various Netlist stage low power issues at the RTL stage itself. This will shift left the static verification of low power issues.

Virtual instrumentation-based flow in VC LP shifts left the low power verification by instrumenting the isolation and level shifter cells in the design based on the UPF strategies which subsequently leads to the more accurate verification of the design and save a lot of verification time at RTL and Netlist.

[Key words: Low Power, RTL, Isolation, Level Shifter UPF, PST]

I. INTRODUCTION

New electrical issues introduced in design after multi voltage cells (ISO/LS) insertion due to synthesis are caught only at post synthesis which comes very late in the verification cycle. Implementing synthesis level instrumentation (such as DC/FC) in static tools itself is not feasible because it is highly error prone, takes a lot of runtime/memory and library cell availability is not guaranteed.

Traditionally at the RTL stage, VC LP checks do not instrument ISO/LS cells and due to this verification done through VC LP is not accurate and many times, it results in several false and missing violations. Then as shown in Figure 1, design synthesis is done by Synopsys tool DC which instruments all the power management cells. After that, VC LP is again run at Netlist stage which exposes more electrical bugs in the design.

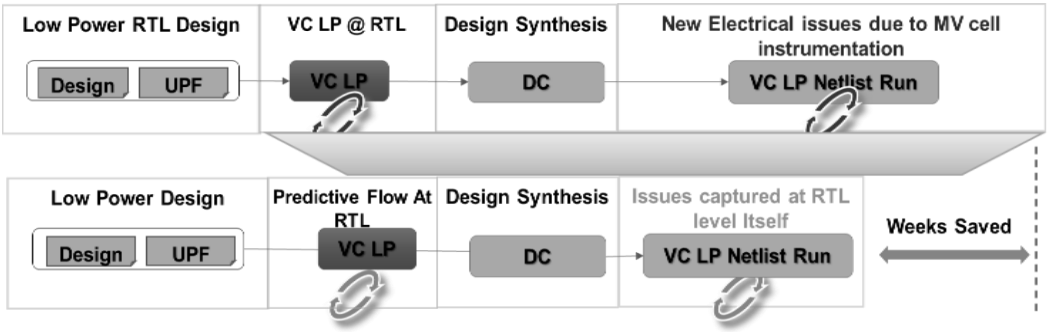

Fig. 1

By default, VC LP checks do not consider cross impact of ISO and LS strategies at RTL stage which leads to **noise/missing violations** at RTL. There is an increasing demand to catch netlist level LP issues at the RTL stage itself and reduce noise by predicting post-synthesis behavior. Major requirement is to catch netlist level low power issues at the RTL stage itself by mimicking the Isolation and Level Shifter cells in the design. **This will lead to better turn-around time in the verification cycle as shown in Fig 1.**

Fig 2 shows an example in which the design issue caught at Netlist which could have been caught at RTL. At RTL, as there is no instrumented isolation strategy but as shown below, when Isolation cell is synthesized, it generated the need of the Level Shifter in the design which has to be now fixed at Netlist. This issue could have been easily caught at RTL with the virtual instrumentation flow. Therefore, this flow is very helpful and necessary.

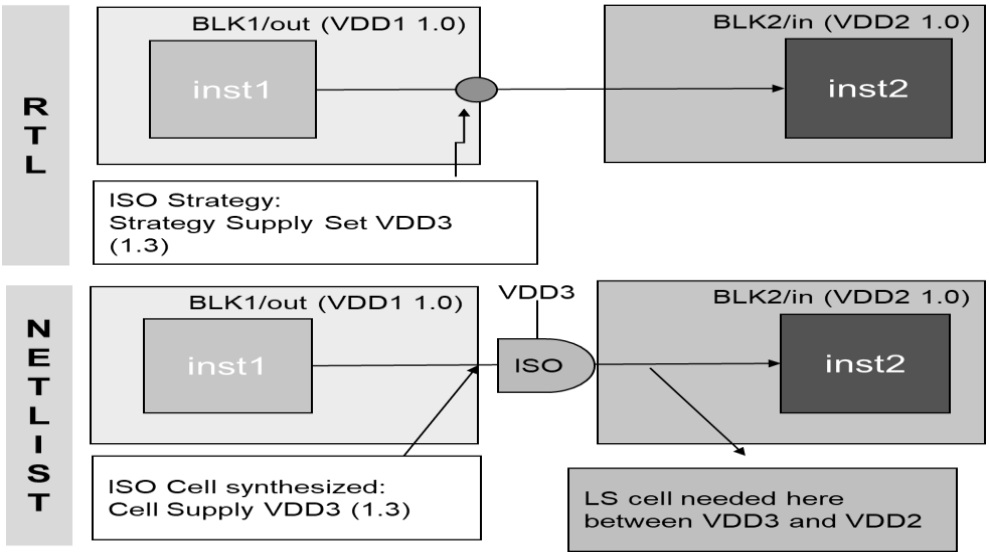

Fig. 2

II. RELATED WORK

Currently there is no related work in this area.

III. ARCHITECTURE

a) VC LP architecture (Figure 3)

Design files such as Verilog/VHDL and supplementary files such as UPF (Unified Power Format) are inputs to the VC LP. First design analysis & elaboration is done and then UPF analysis is done for the power model to be annotated on the design.

VC LP does its path-by-path analysis on an internal sub-graph (known as crossover DB). Crossover DB sub graph is built upon the Flat Netlist Model.

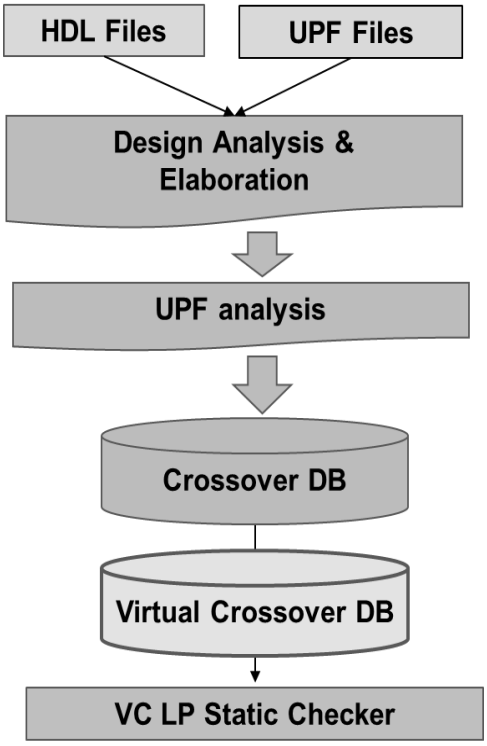

Fig. 3

b) Virtual Instrumentation

Solution proposed in this paper only modifies the crossover DB to insert virtual Isolation and Level Shifter cell. Supply annotation is done on virtual nodes and actual Netlist model is intact.

Virtual Instrumentation supports Isolation, Level Shifter, and ELS (ISO + LS). Also location specified in UPF strategy is used to infer net for virtual node. And supply specified in UPF strategy is annotated on the virtual node.

Example:

set_isolation ISO1 -domain PD1 -elements {inst1/out1} -isolation_supply_set SS2 -location parent

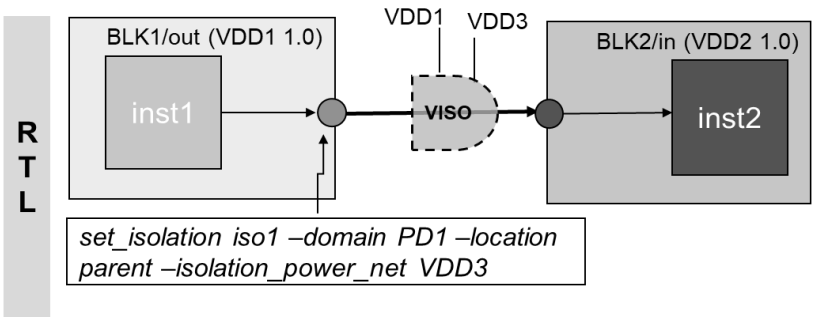

Fig. 4

Consider the above example shown in Figure 4. There is a crossing from inst1/BLK1/out and inst2/BLK2/in and a virtual isolation is inserted on the path in the crossover DB.

- **Original Path created in the crossover DB:**
  BLK1/inst1/out -> BLK1/out → BLK2/in → BLK2/inst2/inc

- **Modified Path created in the crossover DB:**
  BLK1/inst1/out -> BLK1/out → VISO/IN → VISO/OUT → BLK2/in → BLK2/inst2/in

- VC LP will flag **LS_STRATEGY_MISSING** violation between VISO/OUT and BLK2/inst2/in due to voltage difference.

Another more complex example (Figure 5 & 6) in which instrumentation is needed for both Isolation and Level shifter.

Isolation instrumentation is done first in the flow and then Level Shifter is instrumented based on the new segments and LS needs. As we can see, there are two segments on which LS need can be there. One is between inst1/out → isolation input and other is isolation output → inst2 input. As per Power state table, there is a LS need between VDD3 and VDD2. Power state table information is shown in Figure 6 which shows the supply information among supplies in the design.

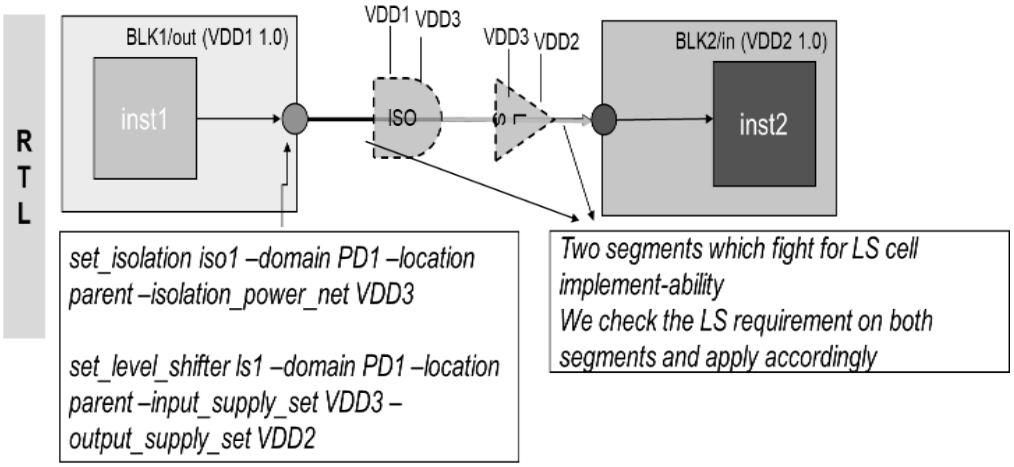

Fig. 5

VDD1	VDD2	VDD3
1.0	1.0	1.3
OFF	1.0	1.3

Fig. 6

c) Novelty of the Solution

Various checks such as Location feasibility, Supply availability/mismatch, electrical issues can be caught with this infrastructure. This flow will Shift-left Netlist Low Power verification at RTL without needing actual design instrumentation and liberty information. There will be no methodology changes required at the customer end. It requires minimal memory and runtime overhead with no such solution at competition.

IV. EXPERIMENTAL RESULTS

Let's start with a customer case study. The below figure shows the noise at RTL stage without new flow. This used to take a lot of time for analyzing and waiving. Predictive flow has caught this issue at RTL itself and suppressed the noise. Figure 7 shows RTL stage and corresponding noise:

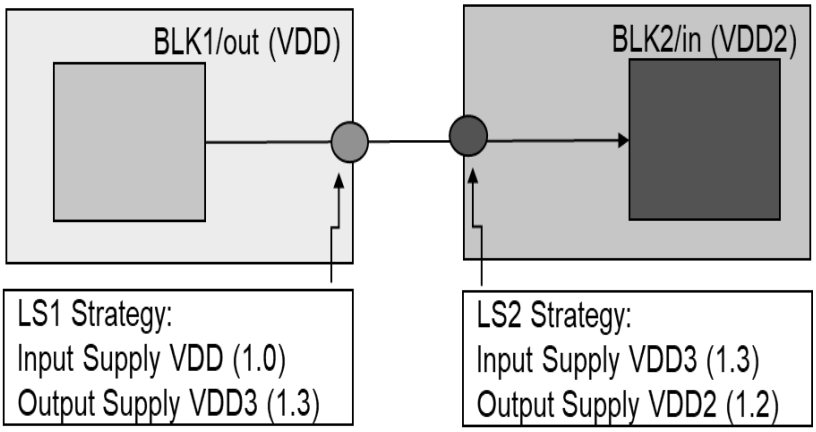

Fig. 7

At RTL, LS Strategies compare the input/output supplies with actual source/sink supplies to check whether they are correct or not electrically.

LS1: input supply with BLK1/out: No violation

LS1: output supply with BLK2/in:
LS_SUPPLY_MISMATCH ← **Inaccurate**

LS2: input supply with BLK1/out
LS_SUPPLY_MISMATCH ← **Inaccurate**

LS2: output supply with BLK2/in: No violation

Figure 8 shows instrumented RTL and how issue is fixed:

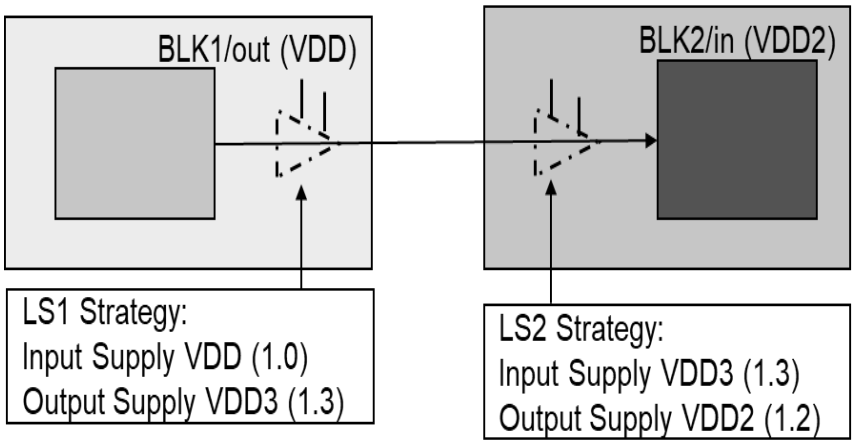

Fig. 8

LS Strategies consider the input/output supplies of the adjacent LS strategies.

LS1: input supply with BLK1/out: No violation
LS1: output supply with LS2/in: **No violation**
LS2: input supply with LS1/out: **No violation**
LS2: output supply with BLK2/in: No violation

- Customer got excellent results with the latest predictive VC LP flow at their RTL design.
- **~99% accuracy** in predictive checks w.r.t post synthesis run at customer design by reducing noise

VC LP TAGS	Default Flow RTL	Predictive Flow RTL	Change	Percentage
LS_STRATEGY_MISSING	156521	512	-156009	99.67%
LS_SUPPLY_MISMATCH	68537	1501	-67036	97.81%
ISO_CONTROL_VOLTDIFF	113	49	-64	56.64%
UPF_SPADRIVER_STATE	24775	416	-24359	98.32%
UPF_SPARECEIVER_STATE	118160	473	-117687	99.60%
UPF_SPASUPPLY_VOLTAGE	21424	315	-21109	98.53%
LS_ASSOC_DIFFER	25132	24	-25108	99.90%
LS_STRATEGY_REDUND	9872	5	-9867	99.95%
Total	**424534**	**3295**	**-421239**	**99.22%**

Table 1

Table 1 shows significant violation accuracy with respect to Netlist stage at customer design.

V. FUTURE WORK

- Debuggability through TCL and GUI.
- Control path virtual instrumentation.
- PG pin connectivity for the MV cells.
- Already commercialized as Elite feature in VC LP.
- Deploy at 3-4 more accounts in near future.

VI. REFERENCES

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