CURRICULUM VITAE

Personal:

Name : **Dr.D.Nirmal M.E, Ph.D.,**

Date of Birth : 20.01.1984

Sex : Male

Nationality : INDIAN

Office Address : Associate Professor and Post Graduate Program coordinator,
Department of Electrical Technology,
Karunya University, Coimbatore, India - 641114.

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Academic History:

Ph.D Faculty of Information and Communication Engineering, Highly Commended.
(specialisation in Nano Device Modelling)
Anna University, Chennai- 2012

Mater of Engineering
(Specialization in VLSI Design)
Karunya University, India- 2007

Bachelor of Engineering
(Specialisation in Electrical and Electronics)
Anna University, Chennai-2005

Post Graduate Diploma in Higher Education
Indira Gandhi National Open University, India- 2015.

Employment Record:

Type of Employment- **Associate Professor**
Place-Karunya University(Electronics and communication Engineering Department)
Period- July 2013- Till Date.

Type of Employment- **Assistant Professor**
Place-Karunya University(Electronics and communication Engineering Department)
Period- June 2009- June 2013

Type of Employment- **Lecturer**
Place-Karunya University(Electronics and communication Engineering Department)
Period- June 2007- May2009

Type of Employment- **Teaching Research Associate**
Place-Karunya University(Electronics and communication Engineering Department)
Period- June 2006 - May 2007

Research Experience:

- Position-**Teaching and Research.**

  Place – VLSI center of excellence, Karunya University.

  Period – July 2007 to Till Date.

Administrative Experience:

- Position- **Co-ordinator Post Graduate programm**

  Place- Department of Electrical Technology(EEE,ECE,E&I and Media) Karunya University.

  Period- June 2016- till date.

- Position- **IEEE Student branch counsellor**

  Place- Karunya University.

  Period- June 2016- till date.

- Position- **Department Library In-charge**.

  Place- Electronics and communication engineering, Karunya University.

  Period- June 2007 to 2013.

Campus Life Experience:

- Position-**Joint Chief Warden**.

  Place- Men's Hostel, Karunya University.

  Period- January 2013- Till Date

- Position-**Warden**.

  Place- Men's Hostel, Karunya University.

  Period- June 2007 to December 2010

  Experience- 3 years and 6 months..

Projects Handled:

- Bachelor of Engineering- (Many Projects in Electronics and Communication Engineering)
- Master of Engineering – (More than 25 VLSI Design)
  - 1(Nanotechnology)

Honors & Awards:

- IEEE Madras Section **Professional Achievement** in the year 2016.
- IEEE Electron Device Coimbatore **Chapter Chair**.
- **Best Researcher Award** from Karunya University in the year 2014.

- Shir.P.K.Das Memorial **Best Faculty Award** in the Year 2013 by Nehru College of Educational and Charitable Trust.
- **Best Research Paper Award** with high impact factor from Karunya University in the year 2012.
- Received **Shiksha Rattan Puraskar Award** 2012 from Indian International friend ship Society.
- Distinction in Master of Engineering (VLSI DESIGN)

Professional Society Activities:

- Life Member of ISTE(Indian Society for Technical Education)LM-56881
- Senior Member of IEEE (Institute of Electrical and Electronics Engineering)SM-92838928.
- Life Member of SSI(Semiconductor Society of India)
- Member of Institute of Engineers (India)M-1544705.
- Member of IETE (The Institution of Electronic and Telecommunication Engineers) M-215257
- Life Member of IAENG(International Association for engineers)
- Member of IACSIT(International Association Of Computer Science And Information Technology)
- Member of ACCENT (Association of Computer Communication Education for National Triumph Social and Welfare Society)

Subjects Handled:

- VLSI Design.
- CMOS VLSI Technology.
- Nanoelectronics.
- Solid State Device Modeling.
- Microelectronics.
- Solid State Electronics.
- Electron Devices.
- Microwave and Optical Engineering.

Research Interests:

- MOS insulators: Study of MOS insulators, including high-k dielectrics
- Novel MOS devices for ULSI applications: Transistors with high-k dielectrics

Review Assignments for Scientific Journals/ Societies:

- IEEE Electron Device Letters.
- International journal of Microelectronics (MJS) Elsevier.
- International Journal of Microelectronics Reliability Elsevier.
- International journal of Superlattices and Microstructures Elsevier.
- All IEEE Young Engineer's Humanitarian Challenge 2016- Jury member.

Editorial Member for Journal:

- Editor- Microelectronics Journal(Elsevier)
- Guest Editor - IEEE Trans on Nanotechnology.
- Editorial Board member of Journal of Nanoscience,Nano Engineering& Applications (JoNSNEA).
- Editorial Board member of Journal of Semiconductor Devices and Circuits.
- Editorial Board member of Journal of Solid State Electronics and Devices.
- Editorial Board Member of International Journal of Advanced Computer Research(IJACR)
- Editorial Board Member of International Journal of Scientific Engineering and Technology(IJSET)

International Advisory committee: Several.

University Collaboration:

Collaborative research work is going on with Mumbai University Nanoscience and Nanotechnology Centre from January 2013.

International/National Universities, College Visited For Research Activity:

- Nanyang Technical University, Singapore.
- IIT Bombay,India.
- IIT Chennai, India.
- Manipal University, India.
- Anna University,India.
- Indian Institute of Science,Bangalore, India.
- SRM University, India.
- Bharathiar University,India.
- P.S.G Tech,Coimbatore, India.
- Noorl Islam University, India.

Research Publications in International Journals:

[1]. J. Ajayan and **D. Nirmal**, "20 nm high performance enhancement mode InP HEMT with heavily doped S/D regions for future THz applications " *Superlattices and Microstructures* DOI: 10.1016/j.spmi.2016.10.011 **(Impact factor: 2.117)**

[2]. P.Prajoon, **D. Nirmal,** Anuja Menokey and J.Charlespravin, "Temperature dependant efficiency droop analysis of In GaN MQW light emitting diode with modified ABC model.", *J Comput Electron* , Vol 16 (2016) pp 1511–1520. **(Impact factor – 1.104).**

[3]. J. Ajayan and **D. Nirmal**, "20-nm enhancement-mode metamorphic HEMT with highly doped InGaAs source/drain regions for high frequency applications" *International Journal of Electronics* DOI: 10.1080/00207217.2016.1218066 **(Impact factor:0.414)**

[4]. J. Ajayan and **D. Nirmal**, "20-nm T-gate composite channel enhancement-mode metamorphic HEMT on GaAs substrates for future THz applications" *J Comput Electron* Vol 16(2016), pp 1291–1296. **(Impact factor:1.104)**

[5]. Charles Pravin J, **D.Nirmal** , Prajoon P and Anuja Menokey M., "A New Drain Current Model for Dual Metal Junctionless Transistor for Enhanced Digital Circuit Performance" **IEEE** Trans. Electron Devices**,** VOL. 63, NO. 9 pp 3782-3789**. (Impact Factor – 2.207).**

[6]. Prajoon P, **D. Nirmal,** AnujaMenokey M, J Charles Pravin "Efficiency Enhancement of InGaN MQW LED Using Compositionally Step Graded InGaN Barrier on SiC Substrate" **IEEE** J. Display Technology, DOI: 10.1109/JDT.2016.2570814, (2016) 1117 - 1121. (**Impact Factor – 1.925).**

[7]. P.Prajoon, **D .Nirmal,** AnujaMenokey and J.Charlespravin, "A Modified ABC Model in InGaN MQW LED Using Compositionally Step Graded Alternating Barrier for Efficiency Improvement", *Superlattices and Microstructures*, 96 (2016) 155-163. **(Impact factor – 2.097).**

[8]. J. Charles Pravin, **D. Nirmal**, P. Prajoon and J. Ajayan, "Implementation of nanoscale circuits using dual metal gate engineered Nanowire MOSFET with high-k dielectrics for low power applications" *Physica E* 83 (2016) 95–100. **(Impact Factor: 2.00).**

[9]. J. Ajayan and **D. Nirmal**, "A review of InP/InAlAs/InGaAs based transistors for high frequency applications" *Superlattices and Microstructures* 86 (2015) 1–19. **(Impact factor: 2.097)**

[10]. Binola k Jebalin, ShobhaRekh, Prajoon, N.Mohankumar and **D.Nirmal ,"**The influence of high-k passivation layer on breakdown voltage of schottky AlGaN/GaN HEMTs" *Microelectronics Journal. Vol. 46 (12), (2015), 1387–1391.* **(Impact factor: 0.836).**

[11]. Binola k Jebalin, ShobhaRekh, Prajoon, N.Mohankumar and **D.Nirmal, "**Unique model of polarization engineered AlGaN/GaN Based HEMTs for high power applications" *Superlattices and Microstructures* 78(2015)210-223**. (Impact factor: 2.097).**

[12]. B. Padmanaban, R. Ramesh, **D. Nirmal** and S. Sathiyamoorthy, "Numerical modeling of triple material gate stack gate all-around (TMGSGAA) MOSFET considering quantum mechanical effects" Superlattices and Microstructures 82 (2015) 40–54.(**Impact factor: 2.097**)

[13]. **D. Nirmal**, P. Vijayakumar , Shruthi and N.Mohan Kumar, "Nanoscale Channel Engineered Double Gate MOSFET for Mixed Signal Applications using High-k Dielectric", International journal of circuit theory and applications, Volume 41, Issue 6, pp 608-618,2013. **(Impact Factor: 1.759).**

[14]. **D. Nirmal**, P. Vijayakumar , D. Divya and N.Mohan Kumar , "Subthreshold Performance of Gate Engineered FinFET Devices and circuit with High-k Dielectrics", Microelectronics Reliability, 53 (2013) 499–504**. (Impact factor: 1.167).**

[15]. **D. Nirmal**, P. Vijayakumar , Shruthi and N.Mohan Kumar, " A review of Nanoscale channel and Gate Engineered FINFETS for VLSI mixed signal applications using Zirconium – di- oxide dielectrics" Journal of Engineering sciences and Technology Review Volume7(2) 2014, 119-124.

[16]. I.Flavia Princess Nesamani, V.LakshmiPrabha,Aswathy Paul and **D.Nirmal**, "Synthesis and Dielectric Studies of Monoclinic Nanosized Zirconia", International journal of Advances in Condensed Matter Physics, Vol. 2014. http://dx.doi.org/10.1155/2014/828492 (**Impact Factor: 1.175).**

[17]. Surya A , D. **Nirmal,** "CMOS Based Instrumentation Amplifier For Neural Recording System" *IJCIC* Volume5, Issue 1,pp 51-55,2013.

[18]. **D. Nirmal**, P. Vijayakumar , Patrick Chella Samuel and N.Mohan Kumar, "Subthreshold analysis of nanoscale FinFETs for ultra-low power application using high-k materials", International Journal of Electronics, Vol. 100, Issue 6,pp 803-817,2013. **(Impact factor: 0.440).**

[19]. Cyril Robinson Azariah, B.Nalini and **D.Nirmal,**"Fabrication and Characteristics of Flexible Thin Film Depletion Mode Field Effect Transistor (FET) using High-κ Dielectric Nano Zirconia" International Journal of Emerging Trends in Engineering and Development, Issue 3, Vol.2 pp.295-299. (March 2013).

[20]. **D.Nirmal** and P.Vijayakumar ,"Fin Field Effect Transistors Performance in Analog and RF for High-k Dielectrics" Defence Science Journal, Vol. 61, No. 3, pp. 235-240, May 2011. **(Impact factor:0.304)**

[21]. **D.Nirmal**, Shruti .K, Divya Mary Thomas, Patrick Chella Samuel, P.Vijayakumar and N.Mohan Kumar,"Impact of Channel Engineering on FINFETs using High-k dielectrics" International Journal of Micro and Nano Electronics, Circuits and Systems, 3(1), pp. 7-11, 2011.

[22]. **D. Nirmal**, B.Nalini and P. Vijayakumar, "Nano sized High K Dielectric Material for FINFET", Integrated Ferroelectrics, Vol. 121, Issue 1, pp. 31-35, 2010. **(Impact Factor: 0.264)**

[23]. **D.Nirmal**, P. Vijayakumar and Sam Jebaraj, "NAND Gate Using FINFET for Nanoscale technology", International Journal of Engineering Science and Technology Vol.2 (5), pp. 1351-1358, 2010.

[24]. **D.Nirmal and** P.Vijayakumar, "Gate Engineering on the Analog Performance of DM-DG MOSFETs with High K Dielectrics", International Journal of Advanced Science and Technology Vol. 25, pp. 1-6, December, 2010.

Research Publications in International / National conferences:

International conference:

[1]. AnujaMenokey, **D Nirmal**, Prajoon P**,** J Charles Pravin, "Green InGaN/GaN LEDs with n-GaN Interlayer for efficiency droop improvement" International Conference on Devices, Circuits and Systems (ICDCS'16), Karunya University, Coimbatore, pp-216-219, 3 March-2016.

[2]. Charles Pravin**., D.Nirmal**, PrajoonP., Altrin Sharma., AnujaMenokey M "Impact of Gate Length on the Performance of a Junctionless Dual Metal Transistor with High-k dielectrics", International Conference on Devices, Circuits and Systems (ICDCS'16), Karunya University, Coimbatore, pp-291-294, 3 March-2016.

[3]. S sreeram, J Ajayan, K Vivek, **D. Nirmal** and V Rajesh " A high speed 256-bit carry look ahead adder design using 22 nm strained silicon technology" IEEE Sponsored 2nd international conference on electronics and communication system ICECS-2015, Karpagam College of Engineering, Coimbatore, Tamil Nadu,26-27 Feb. 2015 pp 174 – 179.

[4]. Jerrin K. Joy, **D. Nirmal** and P. Prajoon "Effect of quantum well thickness and molar concentration for obtaining different wavelength using AlGaAs/GaAs single quantum well LASER" IEEE sponsored 2nd international conference on electronics and communication systems (ICECS 2015), of IEEE International Conference on Electronics and Communication System ICECS'14, Karpagam College of Engineering, Coimbatore, Tamil Nadu Vol-3, (2015) pp:1738-174.

[5]. Surya A, **D. Nirmal** and Charles Pravin "Performance enhancement of Junctionless Gate transistor with high ON/OFF ratio" International Conference on Innovation in Information, embedded and

communication systems (ICIIECS-2015), Karpagam College of Engineering, Coimbatore, Tamil Nadu 19 Mar - 20 Mar 2015 pp 1-4.

[6]. J. Ajayan, **D. Nirmal**, D. Sivaranjini, S. Sivasankari and M. Manikandan " High Performance Low Leakage power Full adder Circuit Design Using Rate Sensing Keeper" Proceedings of International Conference on Electronics and Communication Systems-ICECS-2014, Karpagam College of Engineering. Coimbatore, Tamilnadu, Feb.13, 14. pp.55-59.

[7]. J. Ajayan, **D. Nirmal,** S. Sivasankari, D. Sivaranjini and M. Manikandan " High speed Low Power Full adder Circuit Design Using Current Comparison Domino" proceedings of Second International Conference on Device Circuits and Systems-ICDCS-2014. Karunya University, Coimbatore, Tamilnadu, pp.10-14, March-6-8, 2014.

[8]. Prajoon.P, **D. Nirmal,** Aldona Mathew, AbinGeorge"Enhancement Mode GaN Based HEMT UsingPolarization Engineering Technique" proceedings of International Conference on Innovations in Information Embedded and Communication Systems ICIIECS'14, Karpagam College of Engineering, Coimbatore, Tamil Nadu, March 2014 pp 208-211.

[9]. A.Persiya, **D. Nirmal,**C.T.Sruthi "Investigation on the optical and structural properties of Thermally Evaporated tin selenide thin films for Phase Change Memory application" proceedings of International Conference on Innovations in Information Embedded and Communication Systems ICIIECS'14, Karpagam College of Engineering, Coimbatore, Tamil Nadu, March 2014 pp 482-484.

[10]. T.D.Subash, Dr.T.Gnanasekaran, J. Jagannathan, **D. Nirmal** "Intend and portrayal of InSb QWFET for RF application" proceedings of International Conference on Innovations in Information Embedded and Communication Systems ICIIECS'14, Karpagam College of Engineering,Coimbatore,Tamil Nadu, March 2014 pp 787-790.

[11]. Abin George, **D. Nirmal,**Prajoon.P,Aldona Mathew "Design and Simulation of Schottky-Source/Drain GaN/AlGaN HEMTs for Breakdown Voltage Improvement" proceedings of IEEE International Conference on Electronics and Communication System ICECS'14,Karpagam College of Engineering, Coimbatore, Tamil Nadu, February 2014 pp 187-189.

[12]. Aldona Mathew, **D. Nirmal,**Prajoon.P, Abin George "Modelling of HEMT for High Power Switching Application using Polarization Engineering Technique" proceedings of IEEE International Conference on Electronics and Communication System ICECS'14,Karpagam College of Enginnering,Coimbatore,TamilNadu,February 2014 pp 149-152.

[13]. Surya, **D. Nirmal,**J.Beulah, D.Rubavathy, Daphne and J.David " CMOS Based Instrumentation Amplifier For Neural Recording System" in First International Conference on Communication , Computation and Control held in Christian College of Engineering and technology from 11th- 13th April 2013.

[14]. Annie, **D. Nirmal,**SajithaSoman, Praba , Kingsly "Analysis of Gate Engineered SOI MOSFET FOR VLSI Applications" proceedings of IEEE International Muti Conference on Automation, Computing, Contral, Communication and Compressed sensing , iMac4s-2013, St. Joseph's College of Engineering and Technology. pp 498 - 501 Palai, Kottayam, March 2013.

[15]. Praba, **D. Nirmal,**SajithaSoman, Annie , Kingsly "Design and Simulation of GaN/AlGaN HEMTs with Low Leakage Current and High ON/OFF Current Ratio" proceedings of IEEE International Muti Conference on Automation, Computing, Contral, Communication and Compressed sensing , iMac4s-2013, St. Joseph's College of Engineering and Technology. PP 490 - 493 Palai, Kottayam, March 2013.

[16]. SajithaSoman, **D. Nirmal,**Praba, Annie , Kingsly "Analysis of Drain Current in Short Channel Drain ExtentedTripal Gate FinFETs" proceedings of IEEE International Muti Conference on Automation, Computing, Contral, Communication and Compressed sensing , iMac4s-2013, St. Joseph's College of Engineering and Technology. PP 494 - 497 Palai, Kottayam,March 2013.

[17]. **D. Nirmal,**Vijayakumar, DoreenJoy, Binola k Jebalin, and N.Mohankumar "Nanoscale Tri Gate MOSFET for Ultra Low Power Applications Using High-k Dielectrics " 5th IEEE International Nanoelectronics Conference, IEEE INEC 2013 held in Singapore, Page 12-16, on 2nd – 4th January 2013

[18]. **D. Nirmal,**ShevinBobinVarughese, DoreenJoy, FlaviaPrincess and P.Vijayakumar "Design and simulation of ALGaN/GaN HFET" 2012 International Conference on Devices, Circuits and Systems (ICDCS) Proceedings, Karunya university Page. 199-201,2012.

[19]. **D. Nirmal,**DoreenJoy, ShevinBobinVarughese, FlaviaPrincess, and P.Vijayakumar "Low power analysis of triple gate MOSFET" 2012 International Conference on Devices , Circuits and Systems (ICDCS) Proceedings, Karunya university Page. 126-129,2012.

[20]. FlaviaPrincess, P.Sindhu,M.Manikandan,V.LaksmiPrabha and **D.Nirmal** "Mixed mode simulation of SRAM FINFETs" 2012 International Conference on Devices , Circuits and Systems (ICDCS) Proceedings,Karunya university Page. 280-283,2012.

[21]. **D. Nirmal,** P.Vijaya Kumar, Patrick Chella Samuel, Shruti K, Divya Mary Thomas & N. Mohankumar "Analysis Of Dual Gate Mosfets Using High K Dielectrics" 2011 3rd IEEE International Conference on Electronics Computer Technology (ICECT 2011)Proceedings, page VI:22-25.

[22]. **D. Nirmal,**P.Vijaya Kumar, Shruti K, Divya Mary Thomas, Patrick Chella Samuel & N. Mohankumar "Analysis Of Single Halo Double Gate Mosfets Using High-K Dielectrics" 2011 3rd IEEE International Conference on Electronics Computer Technology (ICECT 2011)Proceedings, page VI:26-30.

[23]. **D. Nirmal,**P.Vijaya Kumar, Divya Mary Thomas, Shruti K, Patrick Chella Samuel & N. Mohankumar "Impact of Gate Engineering on Double Gate MOSFETs using High-k Dielectrics" 2011 3rd IEEE International Conference on Electronics Computer Technology (ICECT 2011)Proceedings, page VI:31-34.

[24]. **D. Nirmal,**Divya Mary Thomas, Shruti K, Patrick Chella Samuel, Vijaya Kumar& N. Mohankumar " Analysis of Dual Material FinFETs using High-k Dielectrics" International Conference on Communication and Signal processing ICCOS 2011 Karunya University, Coimbatore-641 114. 17-18, March 2011

[25]. **D.Nirmal,**Nalini, Vijayakumar "Nanosized High K Dielectric Material For Finfet" *ICE (International conference for Electro ceramics)* , Delhi University, India, 13-17, Dec 2009.

[26]. **D.Nirmal,**Vijayakumar, Rekha, Soumya "Impact Of High-K Dielectrics On Device Performance Of SOI FinFETS" *ISCO (4th international conference on intelligent systems and control)*, karpagam college of engineering, India, 4th and 5th , Feb 2010.

[27]. **D.Nirmal,**Vijayakumar, Rekha "High-K Dielectrics On FinFETs Device Performance Using TCAD" *International Conference on Emerging Trends in Engineering Technologies ICETS*, Noorul Islam university,India, 25 & 26, March 2010.

[28]. **D.Nirmal,** Vijayakumar, Soumya "Device Design And Optimization Of Nanoscale FinFETs Using TCAD" *International Conference on Emerging Trends in Engineering Technologies ICETS*, Noorul Islam university, India, 25 & 26, March 2010.

National conference:

[1]. **D. Nirmal**, Vijayakumaret,al. " ANALYSIS OF ANALOG PARAMETERS USING MULTI GATE FET" *3rd National Conference on Signal Processing, Communications and VLSI Design (NCSCV '11)* Anna university of Technology coimbatore.6th & 7th May 2011. pp. 35-39.

[2]. **D. Nirmal,**Vijayakumar, Samjebaraj, Christopher, Arockia, Sunil "FinFETs For Future Nano Scale Technology" *National Conference on the theme 'Emerging trends in RF and Signal Processing* FISAT , Kerala,India, 25-27, March 2010,pp. 161-165.

[3]. **D. Nirmal,**Vijayakumar, Samjebaraj, Christopher, Arockia, Sunil "CMOS logic design with Double Gate Transistors" National Conference on VLSI,Image processing and Wireless communication ARASU Engineering College, India 20th March 2010,pp.1-7.

[4]. **D. Nirmal,** Vijay "Implementation of Low Power Circuits Using FinFETs" National Conference on Microwave and Optical Communication, Alagappa Chrttiar College Of Engineering And Technology, India, 2009.

[5]. **D. Nirmal,**Jackuline Moni "Floorplanning Based on Btree* and simulated Annealing" *National conference on Modeling, Analysis and Simulation of Computer and Telecommunication systems* Government College Of Engineering Salem, India, 2007.

Ongoing Research Projects:

- "A compact modelling of GaN Based FP-HEMT Device for High power microwave Applications" is approved in DRDO for 21.98 Lakhs.

Grant Fetched:

- Grand-in–aid for organizing **International conference on Devices, Circuits and Systems** from DRDO for the year 2012 with Rs 40,000.
- Grand-in–aid for organizing **National workshop on Electronics system Design and Manufacturing(ESDM)** from DIT for the year 2012 with Rs 30,000.

International Conference Resource Person:

- Session Chair in the " **IEEE Sponsored International conference on Innovations in Electrical ,Electronics, Instrumentation and Media Technology**" held in Karunya University, India 4th , February 2017.
- Session Chair in the **IEEE Sponsored International conference on Inventive systems and Control** Organized by JCT College of Engineering and technology, India on 19th January 2017.
- Session Chair in the **2017 International Conference on Computer Communication and Informatics**(ICCCI 2017) Organized by Sree Shakthi Institute of Engineering and Technology - Coimbatore, India on 7th January 2017.

- Session Chair in the **IEEE International Conference on Communication and Electronics Systems**(ICCES 2016) Organized by PPG Institute of Technology - Coimbatore, India on 21st October 2016.
- Session Chair in the **IEEE International Conference on Inventive Computation Technologies**(ICICT 2016) Organized by RVS Technical Campus- Coimbatore, India on 26 th to 27th August 2016.
- Session Chair in the IEEE EDS and IETE sponsored 3rd **International Conference on Devices, Circuits and Systems** Organized by Karunya University, India on 3rd to 5th March 2016.
- Session Chair in the IEEE sponsored International **conference on Electronics and Communication Systems** Organized by Karpagam College of Engineering, India on 25th February 2016.
- Session Chair in the **International conference on Systems, Science, Control, Communication, Engineering and Technology** Organized by Karpagam Institute of Technology, India on 10th August 2015.
- Session Chair in the **International conference on Networks, Electronics, Communication and Control** Organized by Cape Institute of Technology, India on 5th and 6th March 2015.
- Session Chair in the IEEE **9th International conference on Intelligent Systems and Control"** Organized by Karpagam college of Engineering, India on 9th and 10thJanuary 2015.
- Session Chair in the IEEE **SSCS Sponsored Conference On "Solid State Circuits"** Organized by SaintGits college of Engineering, India on 29th August 2014.
- I have served as a organizing secretary of 2nd International **conference on Devices, Circuits and Systems** sponsored by **IEEE EDS INDIA** and **IETE INDIA** March 6th to 8th 2014.
- Session Chair in the **International Conference Innovations in Information, Embedded and Communication systems** Organized by Karpagam college of Engineering, India on 13th and 14th of March 2014.
- Session Chair in the International **Conference on Devices circuits and systems** Organized by Karunya University, India on 6th to 8th March, 2014.
- Session Chair in the **International Conference on Electronics and Communication Systems** Organized by Karpagam college of Engineering, India on 13th and 14th of February 2014.
- I have served as a organizing secretary of **International conference on Devices,Circuits and Systems** sponsored by **IEEE EDS INDIA** and **IETE INDIA**March 15th and 16th 2012.
- Session Chair in the International**Conference on Innovations in Intelligent Instrumentation, Optimization and Signal** Organized by Karunya University, India on 1st March 2013.
- Session Chair in the **IEEE International Multi Automation, Computing, Control, Communication and Compressed Sensing** Organized by St. Joseph's College of Engineering and Technology,Kerala, India on 22th and 23th March 2013.
- Session Chair in the 2013 **IEEE International Conference on Emerging Trends in Computing, Communication and Nanotechnology** Organized by Infant Jesus College of Engineering, India on 25th and 26th March 2013.

National Conference Resource Person:

Session Chair in the Fourth National Conference on Communication, Computation, Control and Automation, CCCA 2014 Organized by Sri Ramakrishna Institute of Technology, India on 28th and 29th March 2014.

Workshop Organized:

- Organized One day IEEE ED Coimbatore Chapter sponsored workshop "**National Workshop on Semiconductor device modeling and applications"** in Karunya University, 9th October 2015.
- Organized One day IEEE ED Coimbatore Chapter sponsored workshop "**National Workshop on semiconductor memories"** in Karunya University, 18th September 2015.
- Organized two day workshop on "**National Workshop on circuit simulation on TANNER EDA Tool"** in Karunya University, 25th and 26th March 2011.
- Organized one day DIT sponsored workshop on "**Electronic System Design Manufacturing**" in Karunya University, 14th October 2012.

International / National Resource Person:

- Keynote address on **"Current Trends in Junctionless Transistors for Ultra Low power Applications"** in IEEE Sponsored International conference on Inventive systems and Control Organized by JCT College of Engineering and technology, India on 19th January 2017.
- Delivered a Talk on "**Semiconductor Devices and Applications** " in One day IEEE ED Coimbatore Chapter sponsored workshop " **2nd National Workshop on Semiconductor device modeling and applications"** in Karunya University, 11th January 2017.
- Guest Lecture on " **NPN and PNP Junctions**" in FDTP ON Electron Devices organized by Karpagam Institute of Technology , Coimbatore on 23th December 2016.
- Invited talk on " **Semiconductor Nano Electronic Devices and its applications for Future Electronics**" in National seminar on MEMS and Nano Electronic Devices held on 19th and 20th December 2016 in Bharathiar University, India
- Delivered a Keynote address on "**Nanoscale Junctionless Transistor Design and Its Applications** " in the IEEE International Conference on Communication and Electronics Systems(ICCES 2016) Organized by PPG Institute of Technology - Coimbatore, India on 21st October 2016.
- Resource person in the TEQIP-II sponsored faculty development program on "**Multiscale modelling and simulation of Nanoelectronic Devices- A research Perspective**" on 28th July 2016 in PSG college of Technology.
- Delivered a Keynote address on "**GaN based High Electron Mobility Transistor (HEMT): Trends and applications"** in the IEEE sponsored International **conference on Electronics and Communication Systems** Organized by Karpagam College of Engineering, India on 25th February 2016.
- Resource person for a seminar on "**Research paper writing: Methodology & Aspect**" held on 17th February, organized by Department of Electronics and communication Engg ECHO association, Karunya University.

- Delivered a Keynote address on "**Emerging trends in Nanotechnology and Integrated circuits**" in National Level Workshop on Recent trends of Nanotechnology in Electronics held at Arasu Engineering College, India on 8th February 2016.
- Delivered a Technical Talk on "Introduction **to High Power & Low Power Devices in Nanotechnology**" in Alva's Institute of Engineering and Technology, India on 06thNovember 2015.
- Resource person for IEEE EDS Coimbatore chapter sponsored workshop on "**National Semiconductor device modeling and applications**" in Karunya University, 9th October 2015.
- Delivered a lecture on "VLSI **Technologies and research Trends**" in Royal college of Engineering and technology, India on 14th August 2015.
- Keynote address in the **"International conference on Systems, Science, Control, Communication, Engineering and Technology" on** Next Generation Electronics and its Applications Organized by Karpagam Institute of Technology, India on 10th August 2015.
- Keynote address in the **"International conference on Networks, Electronics, Communication and Control" on** Heterostructure based MOSFETs in Nano electronic Regime Organized by Cape Institute of Technology, India on 5th and 6th March 2015.
- Keynote address in the "**IEEE 9th International conference on Intelligent Systems and Control" On** Advanced high power semiconductor devices and its application Organized by Karpagam college of Engineering, India on 9th and 10th January 2015.
- Delivered a plenary talk in the IEEE **SSCS Sponsored Conference On "Solid State Circuits"** Organized by SaintGits college of Engineering, India on 29th August 2014.
- Resource person for IEEE India EDS chapter sponsored workshop on "Nano **Electronics Device Modelling**" in Mahendra Engineering College on 14th July 2014.
- Delivered a Talk on "Nano **electronics in recent trends**" in Reva ITM,Bangalore India on 24th March 2014.
- Delivered a Special Guest lecture on "VLSI **Design**" in Pavai College of Technology, India on 28th January 2014.
- Delivered a Guest lecture in IETE Student forum inauguration on "**Nano electronics in Communication systems**" in Karpagam college of Engineering, India on 30th September 2013.
- Delivered a special lecture in One day seminar on "**Advanced Research Methodologies in VLSI System**" in Cape Institute of Technology, India on 12th August 2013.
- Delivered a Keynote Talk in **2013 IEEE International Conference on Emerging Trends in Computing, Communication and Nanotechnology** Organized by Infant Jesus College of Engineering, India on 25th and 26th March 2013.
- Resource person in "**Workshop for Writing Journal Papers**" at Karunya University, Coimbatore on 6th March 2013.
- Guest Lecture on " **Emerging Trends in Nano Electronics for VLSI Applications**" in Paavai College Of Engineering, Namakkal on 12th February 2013.

- Technical Talk On **"Emerging Engineering Technologies Using FinFETwith High-K Dielectrics"** in the IEEE INDIA EDS chapter workshop on FinFET Circuit Design-An Alternate for CMOS Design conducted in Muthayammal Engineering College, Rasispuram, India 2012.
- Guest lecture in National workshop on **"Low power VLSI methodologies"** organized by Hindustan Institute of Technology, Coimbatore conducted on 24th April 2010.
- Resource person for National Workshop **"Find your way with Wonder Chip: VLSI"** organized by Karunya University conducted from 19th of September 2009 to 21st of September 2009.
- Delivered an Invited lecture on the topic "**INTRODUCTION TO SYNOPSYS"** in Karunya University.

International Courses / Seminars Attended:

- Participated in " IEEE Sponsored International conference on Innovations in Electrical ,Electronics, Instrumentation and Media Technology" held in Karunya University, India on 3rd and 4th , February 2017.
- Completed the course on "Crosscheck for conferences- Plagiarism Detection Tool" from IEEE on September 1st 2016.
- Participated in the IEEE Volunteer Leadership Training programme (VOLT) Program Graduate 2015.
- Participated in pre-conference workshop in "International Conference on signal processing, Image processing and pattern Recognition" on Lab View held on 6th February 2013 at Karunya University.
- Attended the International workshop and IEEE EDS Mini-colloquia on "The past & future of Integrated Circuits Technologies" held during November 4-5, 2009 at S.K.P Engineering college, Tiruvannamalai.
- Advanced International Workshop on "NANOSCIENCE AND TECHNOLOGY" Organized by Anna University Chennai on 2009.

National Courses / Seminars Attended:

- Participated in " National seminar on MEMS and Nano Electronic Devices 2016" held on 19th and 20th December 2016 in Bharathiar University, India.
- Attended faculty development workshop on "Effective teaching Learning Methodology for Engineers" Organized by Department of Electrical Technology,Karunya University on 23th June 2016 .
- Attended one day National level conclave on IOT for smart city on 16th April 2016 in karunya university.
- Participated in "Virtual Labs Workshops" conducted at Karunya University on 20th February 2016.
- Attended one day workshop on "Intellectual Property Rights" on 15th September, 2016 in Karunya University.

- Attended a faculty development program on "Team building and Leadership skill" Organized by Dept. of ECE Karunya University on 6th September 2014.
- Attended a workshop on "COMSOL Multiphysics Modeling" organized by Electronics and Instrumentation Engineering Department, Karunya University on February 14, 2014.
- Attended the one day "Workshop on Project Proposal Writing" in Karunya University, Coimbatore, February 13th 2013.
- Attended the one day National Workshop on "Recent trends in RF Design" in Anna University of Technology Coimbatore, 09th October 2010.
- Underwent the one day training program in center for VLSI & Nanotechnology in S.K.P Engineering College, Tiruvannamalai, 24 September 2010.
- Attended the 3rd INUP (Indian Nano electronics User Program) training program on Nanofabrication Technologies, IISC, Bangalore, 15-16 April 2010.
- Attended the One day Hands-on-training program on "VLSI Back-end tools" organized by Kumaraguru college of Technology on 20th February 2010.
- Attended the workshop on "ASIC Design using SYNOPSYS" Organized by Karunya University collaboration with D'gipro Design Automation and Marketing Pvt.Ltd., on 2009.
- Attended a "Research Workshop on Nanochemistry" Organized by Karunya University under KRWG scheme on January 28 &29, 2009.
- Work shop cum seminar on "RESEND TRENDS IN VLSI DESIGN & VERIFICATION-AN INDUSTRY PERSPECTIVE" at Manipal Centre for Information Science, Manipal University in 2008.
- Attended the one week "PEDAGOGIC TRANING" in Karunya University in 2007.
- AICTE sponsored National seminar on "EMERGING TRENDS IN VLSI DEVICES USING EMBEDED SYSTEMS" conducted by NICE Kumaracoil in 2007
- Underwent one week in-plant training in "Madurai Power Corporation Pvt.Ltd" in 2003.

Reference:

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Declaration:

I hereby declare that all the information presented above are true and correct to the best of my

knowledge and belief.

(**D NIRMAL**)