



## Chapter - 4

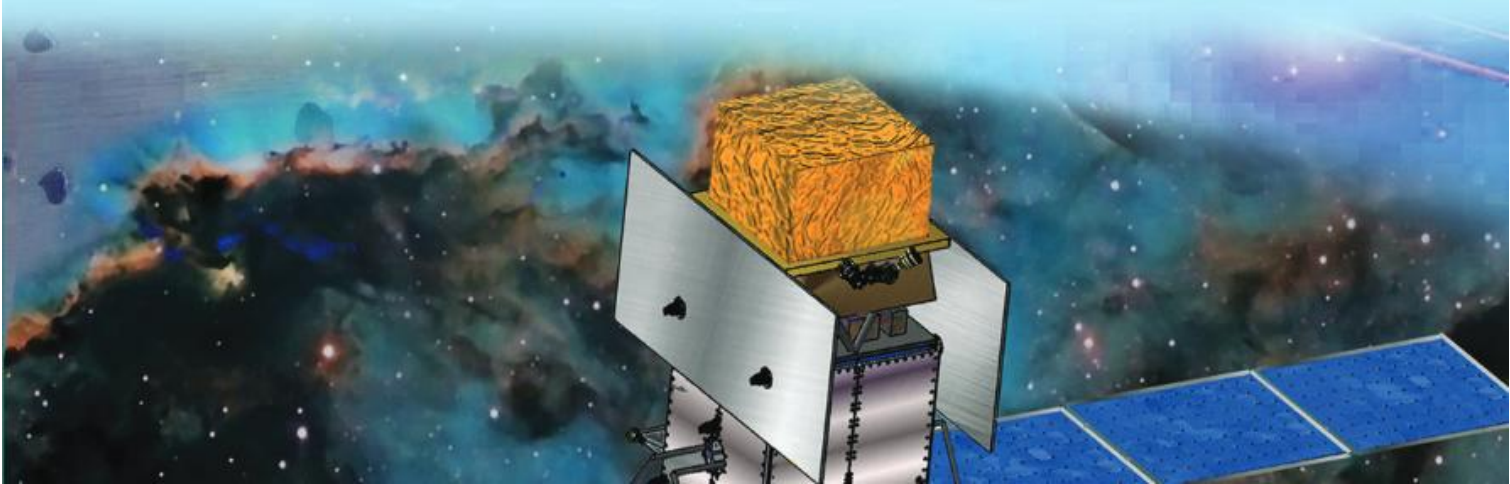
# LOGIC GATES

❖ *Introduction to Boolean algebra* ❖

❖ *Digital logic gates* ❖

❖ *OR gate* ❖ *AND gate* ❖ *NOT gate* ❖

❖ *XOR gate* ❖ *NOR gate* ❖ *NAND gate* ❖



## 4.1 INTRODUCTION

The electronic circuits are of two types. They are analog and digital circuits.

**Analog circuits :** The wave forms are continuous and all values of signals (voltage or current) are possible as shown in Fig 4.1.

Ex : amplifier, oscillator circuits.

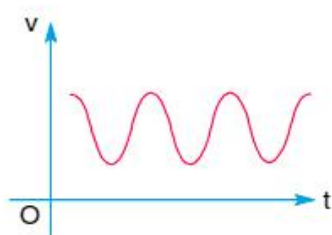


Fig 4.1

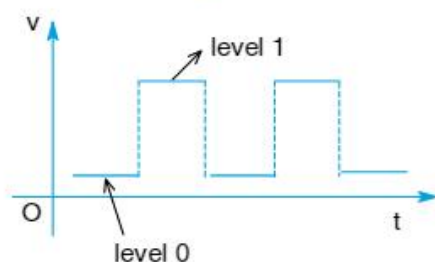


Fig 4.2

**Digital circuits :** The waveforms are pulsed and only discrete values of signals (voltage or current) are possible, as shown in Fig 4.2.

Ex: logic gates.

We shall restrict our study to some basic building blocks of digital electronics (called logic gates) which process the digital signal in a specified manner. Logic gates are used in calculators, digital watches, computers and telecommunication etc.

## 4.2 BOOLEAN ALGEBRA

An English mathematician George Boole developed an Algebra of logic which is called Boolean algebra in his honour. It is binary or two valued logic i.e. it permits only two values or states for its variables. These two states are 'true' and 'false' in logic but are represented by 'on' and 'off' states in electronic circuits.

The two variables of the Boolean algebra are usually represented by 0 and 1 (called as bits).

There are no negative or fractional numbers. Logically, we may write, if  $X = 0$  then  $X \neq 1$ , and if  $X = 1$  then  $X \neq 0$ .

Boolean algebra differs from both ordinary algebra and the binary number system. In Boolean algebra  $1 + 1 = 1$ , while ordinary algebra  $1 + 1 = 2$  and in binary number  $1 + 1 = 10$  (one zero). It should be emphasized, however, that although Boolean Algebra uses two (1 and 0) numbers as mathematical symbols, it is an Algebra of words or ideas, not of numbers. Boolean algebra uses only three operations on its variables. These operations are

- (i) OR addition represented by a + (plus) sign.
- (ii) AND multiplication represented by a  $\times$  (cross), or a  $\bullet$  (dot) sign.
- (iii) NOT operation represented by a bar over a variable.

The Boolean algebra tells us that for binary variables (0 and 1) the following holds.



Table-1

OR	AND	NOT
$0 + 0 = 0$	$0.0 = 0$	$\bar{0} = 1$
$0 + 1 = 1$	$0.1 = 0$	$\bar{1} = 0$
$1 + 0 = 1$	$1.0 = 0$	
$1 + 1 = 1$	$1.1 = 1$	

There are some more postulates and theorems in Boolean algebra. These theorems are utilized to simplify digital logic networks in the same way as the mathematical logic is used to manipulate ordinary algebraic expressions. But the Boolean algebra has a major advantage over the ordinary algebra that its variables assume only two values (0 and 1) to carry out the computations. Thus it is more simple, speedy and accurate.

#### 4.3 POSTULATES AND THEOREMS OF BOOLEAN ALGEBRA

As already stated, Boolean algebra has its own set of fundamental laws which are given below.

##### 1. OR Laws

OR laws in general form may be expressed as

- (i)  $A + 0 = A$  (ii)  $A + 1 = 1$   
 (iii)  $A + A = A$  (iv)  $A + \bar{A} = 1$

##### 2. AND Laws

- (i)  $A.0 = 0$  (ii)  $A.1 = A$   
 (iii)  $A.A = A$  (iv)  $A. \bar{A} = 0$

##### 3. Complementation (or NOT) Laws

- (i)  $\bar{\bar{0}} = 1$  (ii)  $\bar{\bar{1}} = 0$   
 (iii) If  $A = 0$ , then  $\bar{A} = 1$   
 (iv) If  $A = 1$ , then  $\bar{A} = 0$  (v)  $\bar{\bar{A}} = A$

Here  $\bar{\bar{A}}$  refers to double complement operation.

##### 4. Commutative Law

- (i)  $A + B = B + A$  (ii)  $A \bullet B = B \bullet A$

Thus order in which a combination of terms is performed does not matter.

##### 5. Associative Laws

- (i)  $A + (B + C) = (A + B) + C$   
 (ii)  $(A + B) + (C + D) = A + B + C + D$   
 (iii)  $A \bullet (B \bullet C) = (A \bullet B) \bullet C$

Thus removal of brackets from logical expressions and regrouping of variables is allowed.

##### 6. Distributive Laws

- (i)  $A \bullet (B + C) = A \bullet B + A \bullet C$   
 (ii)  $A + B \bullet C = (A + B) \bullet (A + C)$   
 (iii)  $A + \bar{A} \bullet B = A + B$

Thus factoring or multiplying out of expressions is permitted.

#### 4.4 DE MORGAN'S THEOREM

DeMorgan's theorems (or rules) are very useful in simplifying complicated logical expressions and can be stated as under :

**Theorem 1 :** The complement of the sum of two (or more) variables is equal to the product of complements of the variables i.e.,  $\overline{A + B} = \bar{A} \bullet \bar{B}$

**Theorem 2 :** The complement of the product of two (or more) variables is equal to the sum of complements of the variables i.e.,  $\overline{A \bullet B} = \bar{A} + \bar{B}$ .

#### 4.5 DIGITAL LOGIC GATES

A logic gate can be defined as an electronic circuit which make logic decisions. It has one, two or more inputs and one output. The output waveforms of a logic gate depends upon the input waveforms and the input-output characteristic of the circuit described in terms of mathematical logic based upon Boolean algebra. We will discuss some important logic gates.

##### 4.5.1 THE OR GATE

The OR circuit has two or more inputs and would give an output if a pulse is applied to any one of the inputs. If the  $n$  inputs to the OR logic circuit be designated by  $A, B \dots N$ , and the output by  $Y$ , then the OR operation may be defined as "Y equals A or B or ..... or N". The Boolean expression for OR operation is written as,



$$Y = A + B + \dots + N$$

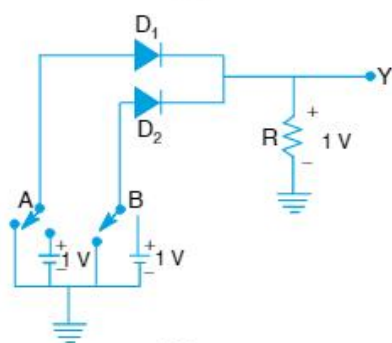
where the + symbol indicates the OR concept. It is to be noted that each of the symbols A, B....N may assume one or two possible values, either 0 or 1. Fig. 4.3(a) gives the symbolic representation of the OR gate. Fig 4.3(b) shows a two input OR gate using two ideal diodes  $D_1$  and  $D_2$ . Here A and B represent the two inputs and Y the output. R represents the output load resistor. There are, four possibilities in which the input voltages may appear.

- (i) When both  $A = 0\text{ V}$  and  $B = 0\text{ V}$ , i.e., there is no voltage either at A or B, none of the diode conducts and output  $Y = 0\text{ V}$ .
- (ii) When  $A = 0\text{ V}$  and  $B = 1\text{ V}$ , diode  $D_2$  is forward biased and hence conducts. The circuit current flows via R dropping 1V across it. In this way output Y achieves a potential of 1 volt. Thus  $Y = 1\text{ V}$ .



Circuit symbol for OR

(a)



(b)

Fig 4.3

- iii) When  $A = 1\text{ V}$  and  $B = 0\text{ V}$ ,  $D_1$  is forward biased and hence conducts causing output  $Y = 1\text{ V}$ .
- iv) When both  $A = 1\text{ V}$  and  $B = 1\text{ V}$ , both diodes are forward biased and conduct but the drop across R is 1V i.e. output  $Y = 1\text{ V}$  because voltage of A and B are in parallel.

All the possible conditions in a two input OR circuit can be represented in a tabular form known as truth - table. It represents all possible inputs and their corresponding outputs. The truth table for two inputs OR operation is given below.

Table-2

Input		Output
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

In logic algebra,  $A + B = Y$  means if A is true or B is true then Y will be true, it does not mean that sum of A and B equals Y. There exists a parallelism between the logic OR gate and the connection of electrical switches. Fig 4.4 shows an equivalent OR switch. There exists a circuit between terminals 1 and 2 if switch A or switch B or both are closed.

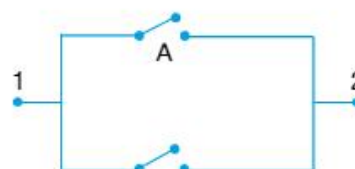


Fig 4.4

Thus OR gate is equivalent to a parallel circuit in its logic function. It is also called inclusive OR gate because it includes the case when both inputs are true.

#### 4.5.2 TRANSISTOR OR GATE

Fig 4.5 shows a transistor OR gate. It consists of three transistors  $Q_1$ ,  $Q_2$  and  $Q_3$  supplied from a common supply  $V_{CC} = 5\text{ V}$ .

- (i) If  $A = 5\text{ V}$  i.e., + 5V is applied to A,  $Q_1$  is forward biased and hence conducts. When  $Q_1$  is saturated, entire  $V_{CC} = 5\text{ V}$  drops across  $R_1$  and hence C goes to ground i.e., its potential = 0 V. Consequently  $Q_3$  is cut off and D goes to  $V_{CC} = 5\text{ V}$ . Hence the output between D and ground is 5V.



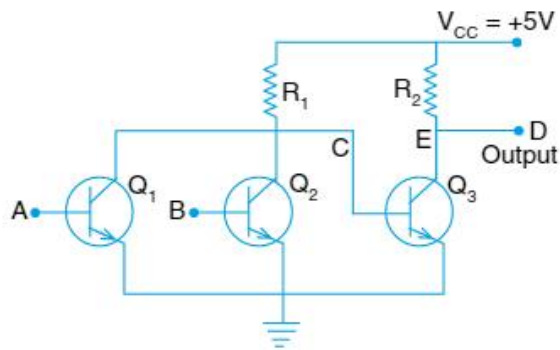


Fig 4.5

(ii) If  $B = 5V$ ,  $Q_2$  is forward biased and hence conducts. It causes C to go to ground i.e.,  $C = 0V$ . Thus there is no forward bias on the base of  $Q_3$ . Hence  $Q_3$  is cut off and D again goes to  $V_{CC} = 5V$ .

(iii) If  $A = 0V$ ,  $B = 0V$  i.e. both A and B are ground. Then  $Q_1$  and  $Q_2$  are both cut-off. Consequently,  $Q_3$  becomes forward biased and conducts. As a result, entire  $V_{CC}$  drops across  $R_2$ . It drives E and hence D to ground i.e., output = 0 volt.

#### 4.6.1 THE AND GATE

The AND gate, is also called a coincidence circuit. The AND circuit has two or more inputs, and would give an output if a pulse of common polarity is applied at each input simultaneously. For n inputs A, B, ...N, the AND operation for the output Y is defined as, "Y equals A and B and .. and N". The Boolean expression for the AND operation is written as,  $Y = AB \dots N = A \cdot B \dots N = A \times B \times \dots \times N$

Thus a dot ( $\bullet$ ) or a cross ( $\times$ ) is placed between symbols to represent AND operation.

The AND gate works on the Boolean algebra.  $A \times B = Y$  or  $A \bullet B = Y$  or  $AB = Y$  Thus the output Y of the AND gate is 1 only when both the inputs A and B are 1, i.e., AND gate gives an output only when all the inputs are present. Thus it is an all or nothing gate whose output occurs only when all its inputs are present.

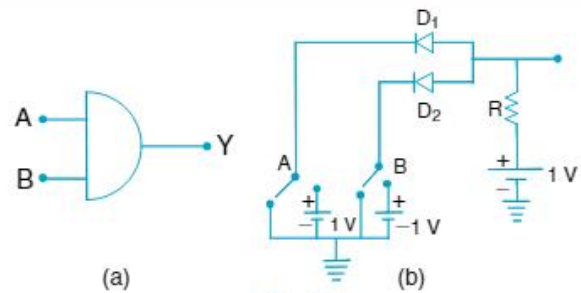


Fig 4.6

Fig 4.6(b) shows a two - input AND gate using two ideal diodes  $D_1$  and  $D_2$  while Fig 4.6(a) gives its symbolic representation. Here A and B represent the two inputs and Y the output. R represents the output load resistor. The two input voltages are assumed to be either 0 or 1V for the sake of simplicity. The logical operation of AND gate is

(i) When both  $A = 0V$  and  $B = 0V$ , the inputs are short circuited to ground but the 1V battery on the output side biases the diodes  $D_1$  and  $D_2$  in the forward direction. Consequently both diodes conduct and the output is also shorted to ground through the diodes. Thus the output  $Y = 0V$ .

(ii) When  $A = 0V$  and  $B = 1V$ , diode  $D_1$  conducts and the output is short circuited to ground through this diode. Therefore the output  $Y = 0V$

(iii) When  $A = 1V$  and  $B = 0V$ , diode  $D_2$  conducts and the output is short circuited to ground through this diode. Therefore, output  $Y = 0V$ .

(iv) When both  $A = 1V$  and  $B = 1V$ , neither  $D_1$  and  $D_2$  conducts. No current, therefore, flows through R and the output  $Y = 1V$ .

All the conditions in a two - input AND gate may be represented in a truth table as follows.

Table-3

Input		Output
A	B	$Y = A \times B$
0	0	0
0	1	0
1	0	0
1	1	1



The equivalent AND operation switching circuit is shown in Fig 4.7. Evidently, when both switches A and B are closed, there is a path between 1 and 2. Thus AND gate is equivalent to series switching circuit. The AND gate symbolizes logic multiplication according to Boolean algebra.



Fig 4.7

#### 4.6.2 TRANSISTOR AND GATE

Fig 4.8 shows a transistor AND circuit, consisting of three transistors  $Q_1$ ,  $Q_2$  and  $Q_3$  supplied from a common supply  $V_{CC} = 5V$ .

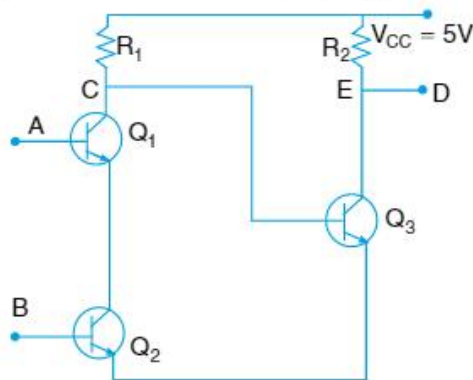


Fig 4.8

When  $A = B = +5V$ , then both transistors,  $Q_1$  and  $Q_2$  conduct. Consequently, the supply voltage of  $+5V$  drops across  $R_1$ . It drives point C to ground and hence base of transistor  $Q_3$  is cut off and D goes to supply voltage  $+5V$ . Thus there is an output at C only when there is an input at A and B. If either  $A = 0V$  or  $B = 0$  volt, then either  $Q_1$  or  $Q_2$  will be cut off and there will be no drop across  $R_1$ . Then point C will be at  $+5V$ . As a result  $Q_3$  will conduct dropping entire  $V_{CC}$  across  $R_2$ . It drives E and hence D to ground i.e., 0 volt.

#### 4.7 THE NOT GATE OR INVERTER CIRCUIT

Another example of the basic digital circuits is the NOT gate. A NOT circuit has one input and one output. It inverts the polarity of a pulse applied

to it. Thus a NOT circuit serves to negate the input function. If A is the input, then “output Y equals NOT A” Thus its output is NOT the same as its input. The Boolean expression for inverter is written as  $Y = \bar{A}$ , where the bar over represents NOT. Hence if the letter A represent DOWN level (0),  $\bar{A}$  represents UP (1) and if  $A = 1$ ,  $\bar{A} = 0$  The truth table for NOT operation is given below.

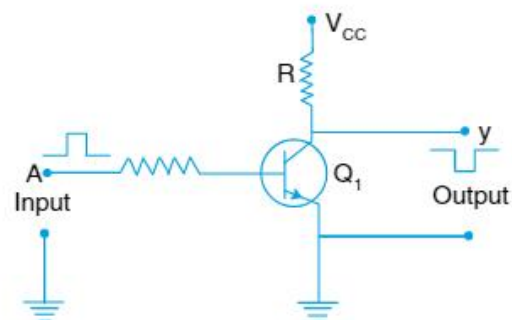
Fig 4.9(a) shows the circuit symbol of NOT gate. Fig 4.9(b) shows a NOT circuit. In the grounded emitter configuration, the output is taken from the collector. When no signal is applied at the input i.e  $A = 0V$ , the transistor will be cut OFF and the output Y will go to  $V_{CC}$ . Thus when input is low, output is high. Similarly when signal is applied at the input i.e.,  $A = 1V$ , the transistor will be ON and the output Y will be 0.

Table-4

Input	Output
A	$Y = \bar{A}$
0	1
1	0



(a) Circuit Symbol of NOT Logic



(b)



(c) Input Output waveform of an inverter

Fig 4.9



Thus when input is high, the output is held at a low value. Thus in a NOT circuit the output is not present when an input signal is applied. Thus the output is the inverse of input. The NOT circuit inverts the waveform as shown in Fig 4.9(c), but keeps the variable operating between the same two limits  $E_1$  and  $E_2$ .

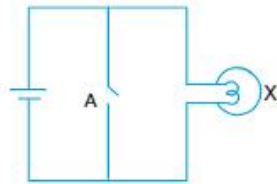


Fig 4.10

The equivalent NOT operation of an electrical circuit is as shown in Fig 4.10. Switch A is connected parallel to the bulb (X) :

When A is open ( $A=0$ ), the bulb lights up ( $X = 1$ )

When A is closed ( $A=1$ ), the bulb goes off ( $X=0$ )

#### 4.8 THE EXCLUSIVE OR GATE

The EXCLUSIVE OR (abbreviated as XOR) operation obeys the definition, that a two input circuit provides an output when one input or the other is present but not when both inputs are present. The OR gate, described earlier, is called an INCLUSIVE OR gate, since it also provides an output when both inputs are available.

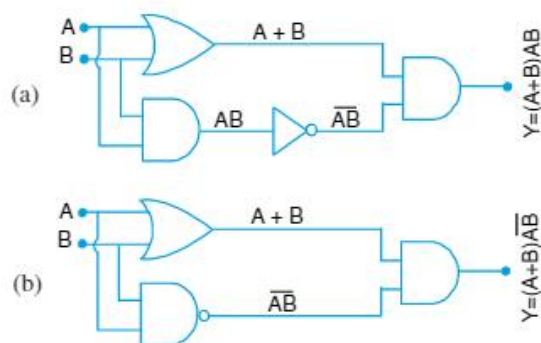


Fig 4.11

The above definition of EXCLUSIVE OR (XOR) operation is equivalent to statement. "If  $A = 1$  or  $B = 1$ , but not simultaneously, then  $Y = 1$ ". In terms of Boolean expression this may be written as,  $Y = (A + B)(\overline{AB})$ . This function is illustrated in the logic diagram in Fig 4.11(a). Fig 4.11(b) gives the alternative diagram in which inverters are shown by circles.

The XOR operation may also be stated as, if  $A = 1$  and  $B = 0$  or if  $B = 1$  and  $A = 0$ , then  $Y = 1$ . The corresponding Boolean expression is,  $Y = A\overline{B} + \overline{A}B$ . The block diagram according to this logic is given in Fig 4.12.

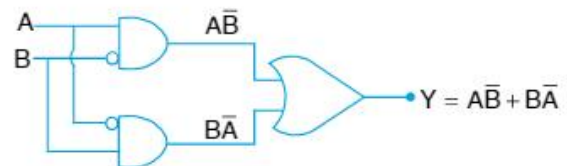


Fig 4.12

The truth for  $X_{OR}$  is

Table-5

Input		Output
A	B	$Y = A\overline{B} + \overline{A}B$
0	0	0
0	1	1
1	0	1
1	1	0

The logic symbol for the XOR gate is shown in Fig 4.13. It may be visualised as a combination of AND, OR and NOT gates.



Fig 4.13

Symbolically, we write XOR operation as  $Y = A \oplus B$

#### 4.9 THE NAND GATE

A negated AND is called a NOT-AND or NAND gate. If at the output of AND gate the NOT



gate is connected, a NAND gate will be formed, as shown in Fig 4.15(a). Thus NAND is a logic system in which a NOT circuit follows an AND gate. In Fig 4.14 a NAND gate is achieved by putting a transistor NOT gate at the output of a diode AND gate. Such gates using diodes and transistors are called diode - transistor logic (DTL) gates.

The capacitor C across  $R_1$  in Fig 4.14 is added to improve the transient response of the inverter (NOT) circuit. It helps in bringing the transistor out of saturation condition by removing the minority carrier saturation charge stored in the base of the transistor when the input signal changes abruptly between two logic states.

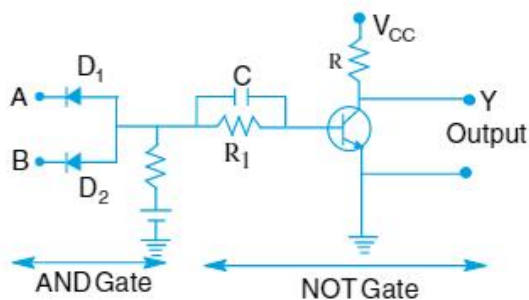


Fig 4.14

Fig 4.15(a) gives the logic symbol for two input NAND gate (external inverter form) while yet another form (internal inverter form) is shown in Fig 4.15(b).

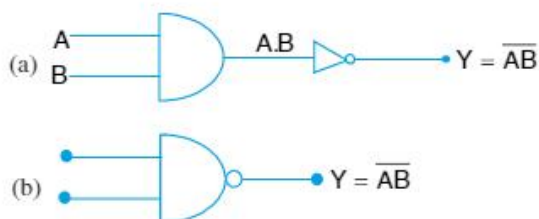


Fig 4.15

Evidently, the output of the AND gate is inverted by the NOT gate yielding the NAND operation. Its output is given by the Boolean equation  $Y = \overline{AB}$ . The truth table of NAND gate is given below.

Table-6

Input		Output
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Thus this gate gives an output 1 if either A or B or both are 0.

#### 4.10 NAND GATE IS A UNIVERSAL GATE

A NAND gate is known as a universal gate because it can be used to realize all the three basic logic functions, i.e., of an OR gate, AND gate and NOT gate (or inverter) as shown below.

**1. As NOT Gate :** As shown in Fig 4.16, if the two inputs of a NAND gate are connected together, then we get a NOT gate. In such a case, the logic symbol of is NAND employed.

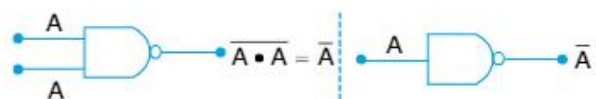


Fig 4.16

**2. As AND Gate :** An AND gate can be produced by using two NAND gates as shown in Fig 4.17.

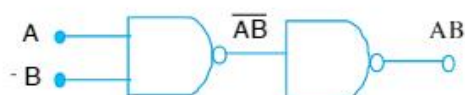


Fig 4.17

**3. As OR Gate :** OR gate can be made out of three NAND gates as shown in Fig 4.18.

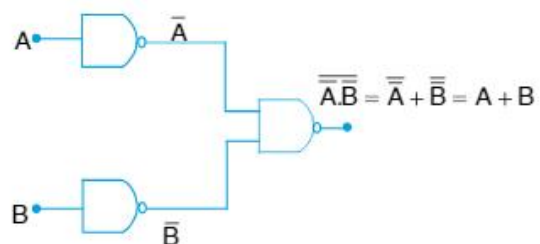


Fig 4.18



## PHYSICS-IIID

### 4.11 THE NOR GATE

A NOR gate. It is the circuit combination in which a NOT circuit follows an OR gate is represented symbolically in Fig 4.19 in which a NOT gate follows an OR gate.

The Boolean expression for the NOR gate is  $Y = \overline{A + B}$ .

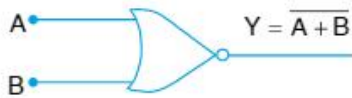


Fig 4.19

The output of the OR gate is inverted by the NOT gate and thus yields NOR operation. The truth table for NOR gate is given below :

Table-7

Input		Output
A	B	$Y = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

Obviously, a NOR gate will have an output of 1 only when all its input are 0. Alternatively, in a NOR gate, output is true when all inputs are false. A NOR gate can be implemented by employing only resistors and transistors as shown in Fig 4.20.

It is known as a resistor-transistor logic (RTL) NOR gate. The operation of the circuit is very simple. When both inputs A and B are 0, no base current flows in two transistors and the transistors are cutoff so that the output voltage Y is almost equal to  $V_{CC}$ .

Therefore, when  $A = 0$  and  $B = 0$ , we have  $Y = 1$ . If either A or B = 1, one transistor saturates forcing point Y to go to ground i.e., then  $Y = 0$ .

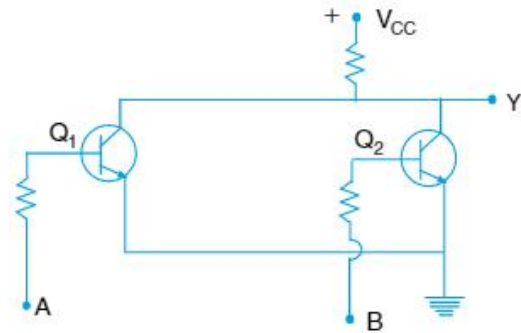


Fig 4.20

### 4.12 NOR GATE IS A UNIVERSAL GATE

NOR gate is also called universal gate because it can also perform all the three functions of an OR gate, AND gate and NOT gate. It is as explained below.

**1. As OR gate :** As shown in Fig 4.21 an OR gate can be realized by connecting the output of a NOR gate to an inverter. The output of NOR gate is  $\overline{A + B}$  which is inverted by inverter to give  $Y = A + B$ , the logic function of a normal OR gate.

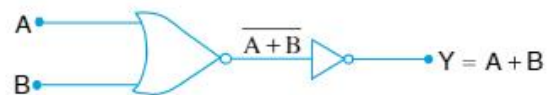


Fig 4.21

**2. As AND gate :** The use of two inverters and a NOR gate has been shown in Fig 4.22 to get an AND gate.

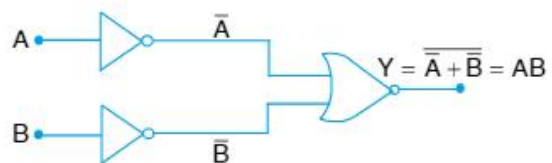


Fig 4.22

Here two inverters have been used, one for each input. The inverted inputs  $\bar{A}$  and  $\bar{B}$  have been applied to the NOR gate. The output of NOR gate :

$$\overline{\bar{A} + \bar{B}} = AB$$



**3. As NOT gate :** If the two inputs of NOR gate are tied together, as shown in Fig 4.23 the output is  $\overline{A + A}$ . By De Morgan's theorem  $\overline{A + A} = \overline{A}$

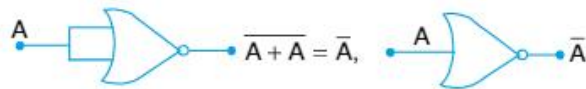


Fig 4.23

### 4.13 INTEGRATED CIRCUITS

In making circuits, the conventional method is components like resistors, inductors, capacitors, diodes, transistors will be chosen and then in desired manner those may be connected by soldering wires. Due to the semiconductor devices, though miniaturisation is introduced, such circuits are still bulky. The other troubles with such circuits are they were less reliable and less shock proof. A large circuit can be fabricated on a small single block of a semiconductor which is known as integrated circuit (IC). It consists of many passive components like R, C and active devices like diode and transistor. The most widely used technology in preparing IC is Monolithic Integrated Circuit. Monolithic is a Greek word - mono means single and lithos means stone. It means the entire circuit is formed on a single silicon crystal known as chip.

The dimension of a chip are as small as 1 mm × 1 mm or even smaller than them. The chip will be enclosed in a protective plastic case with connections coming out in the form of pins. There are two types of ICs. The linear or analogue IC processes analogue signals which change smoothly and continuously over a range of values between a maximum and a minimum. The output almost varies linearly with the input. Linear IC is used as operational amplifier. The second type of IC is digital IC. Digital IC processes signals that have only two values. They contain circuits like logic gates. Depending upon the number of logic gates they are called with different names. For logic gates ≤ 10, it is known as Small Scale Integration (SSI), for logic gates ≤ 100, it is Medium Scale Integration

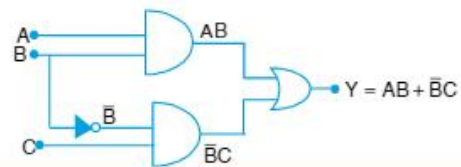
(MSI), for logic gates ≤ 1000, it is Large Scale Integration (LSI), for logic gates ≥ 1000, it is Very Large Scale Integration (VLSI).

#### Example-4.1

Draw the logic circuit corresponding to the Boolean expression.  $Y = AB + \overline{B}C$ .

**Solution :**

It is an expression showing sum of two products. Thus we require two AND gates and an OR gate. To generate  $\overline{B}$  we also require a NOT gate. Their circuit can be drawn as follows.



#### Example-4.2

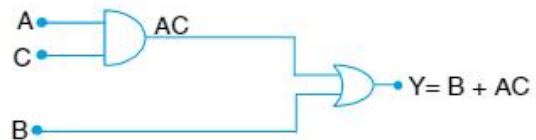
Simplify  $Y = AB + ABC + \overline{A}B + \overline{A}BC$  using Boolean Algebra. Draw the resultant simplified logic circuit.

**Solution :**

Given  $Y = AB + ABC + \overline{A}B + \overline{A}BC$

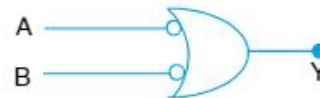
$$Y = (A + \overline{A})B + AC(B + \overline{B}) = B + AC \quad (\because B + \overline{B} = 1)$$

Logic Circuit is shown below.



#### Example-4.3

Write Boolean equation for the output of fig. and solve this equation for all possible input conditions.



**Solution :**

The Boolean equation for the output of fig.

- (i) When  $A = 0$   $B = 0$  then  $Y = \overline{0} + \overline{0} = 1 + 1 = 1$
  - (ii) When  $A = 0$ ,  $B = 1$ , then,  $Y = \overline{0} + \overline{1} = 1 + 0 = 1$
  - (iii) When  $A = 1$ ,  $B = 0$ , then  $Y = \overline{1} + \overline{0} = 0 + 1 = 1$
  - (iv) When  $A = 1$ ,  $B = 1$ , then  $Y = \overline{1} + \overline{1} = 0 + 0 = 0$
- Hence  $Y = \overline{AB}$



## PHYSICS-IIID

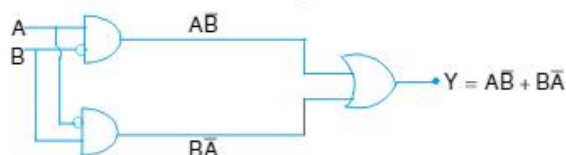
### Example-4.4

Draw logic diagrams for the Boolean expressions given below.

(i)  $A \cdot \bar{B} + \bar{A} \cdot B = Y$  (ii)  $(A + \bar{B}) \cdot (\bar{A} + B) = Y$

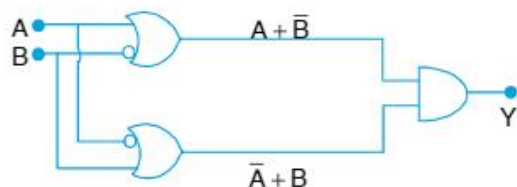
**Solution :**

i) The required logic diagram for the given Boolean expression is given in figure. Here the input B before applying to first AND gate and input A before applying to second AND gate have been inverted. The output of these gates are, therefore,  $A\bar{B}$  and  $\bar{A}B$  respectively. These outputs are fed to OR gate which gives  $Y = A\bar{B} + \bar{A}B$  as shown in figure.



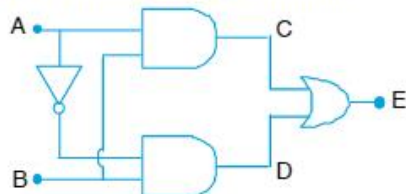
ii) The required logic diagram for the given Boolean expression is shown in figure. The input B to first OR gate and input A to second OR gate have been inverted. The output of these gates are, therefore,  $A + \bar{B}$  and  $\bar{A} + B$  as shown. These inputs when applied to AND gate give the required output.

$$Y = (A + \bar{B}) \cdot (\bar{A} + B)$$



### Example-4.5

Draw the truth table for the given circuit.



**Solution :**

Here  $C = A \cdot B$ ,  $D = \bar{A} \cdot \bar{B}$  and  $E = C + D$ .

So truth table will be as given below.

A	B	$\bar{A}$	$C = A \cdot B$	$D = \bar{A} \cdot \bar{B}$	$E = C + D$
0	0	1	0	0	0
0	1	1	0	1	1
1	0	0	0	0	0
1	1	0	1	0	1

## EXERCISE

### SHORT ANSWER QUESTIONS

- Write four basic rules for adding binary digits?
- Give the Truth Table for binary addition?
- Draw the symbol and Truth Table for: (i) OR and NOR gates. (ii) AND and NAND gates
- Give a brief account of AND and NAND logic gates?
- Explain how OR, AND and NOT gates can be obtained from NOR gate?
- If the output of a 2-input NOR gate is fed as the input to a NOT gate (i) Name the new logic gate obtained (ii) Write down its truth table.
- Describe the working of XOR logic gate?
- Giving the circuit diagram of NAND gate give its truth table?
- Why is the NAND gate called universal building block? Explain?
- Using diodes construct an OR gate and an AND gate?

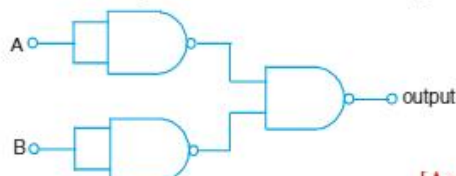
### VERY SHORT ANSWER QUESTIONS

- Name the output function in the following circuit.



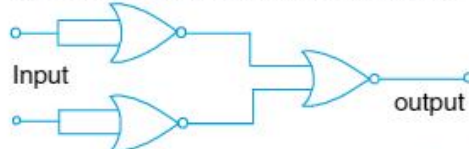
[Ans: AND]

- Name the output function in the following circuit.



[Ans: OR]

- Name the output function in the following circuit.



[Ans: AND]

- $\bar{X}$  and  $\bar{Y}$  are connected to the inputs of an OR gate. The output of the OR gate is connected to the top input of an AND gate. Input Z is connected to the bottom input of the AND gate. The output of the AND gate is labeled C.

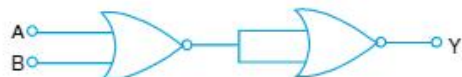
The output C in the above circuit is given by  $C = \dots$

[Ans:  $(\bar{X} + \bar{Y}) \cdot Z$ ]



5. Which logic function has the output “low” only when both inputs are “high”? [Ans: NAND, XOR]

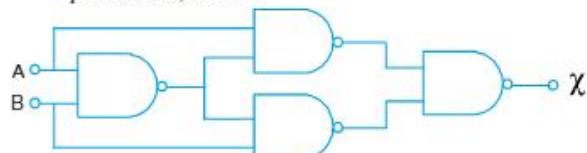
6. Write down the truth table for output Y for all possible inputs A and B in the following circuit:



[Ans: ]

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

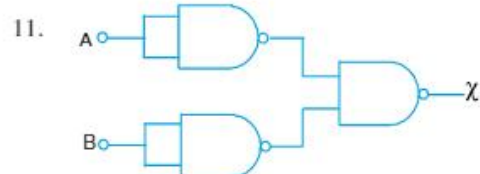
Use the following gate combination to answer questions 7, 8 and 9



7. Evaluate the output Y for the inputs A = 1 and B = 0 [Ans: 1]  
 8. Evaluate the output Y for the inputs A = 1 and B = 1 [Ans: 0]  
 9. Evaluate the output Y for the inputs A = 0 and B = 0 [Ans: 0]  
 10. The truth table shown below corresponds to which gate?

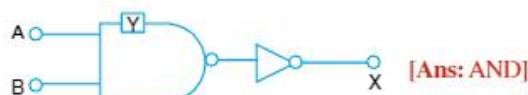
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

[Ans: XNOR]



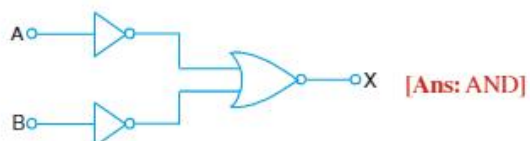
Name the function produced by the combination of gates shown in the figure. [Ans: OR gate]

12. The following diagram represents the logic function of which gate?

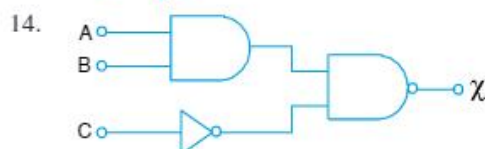


[Ans: AND]

13. Which logic gate is represented by the following combination?



[Ans: AND]



In the given circuit, find the output Y for each of the following inputs.

- a) A = 1, B = 1, C = 0  
 b) A = 1, B = 1, C = 1  
 c) A = 1, B = 0, C = 0  
 d) A = 0, B = 1, C = 1

[Ans: (a) 0; (b) 1; (c) 1; (d) 1]

15.

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

State the Boolean expressions for the given truth table. [Ans:  $Y = \bar{A} + \bar{B}$ ]

16. State two logic functions in which the output is “low” when both inputs are “low” [Ans: OR, XOR]  
 17. Draw the shape of pulse if the logic gate is  
 (i) OR gate (ii) AND gate  
 (iii) NOR gate (iv) NAND gate  
 (v) XOR gate

