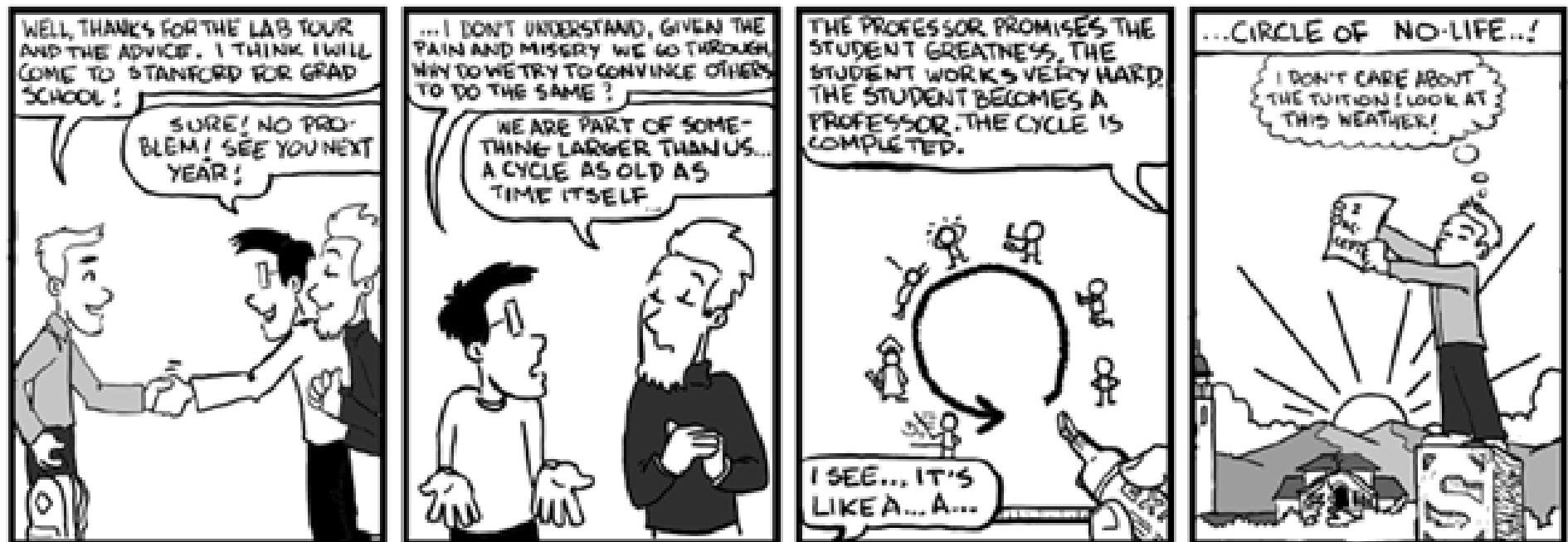


# ECE 322

## The Final Class Finally!!!

(May 2<sup>nd</sup>, 2013)



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# **Plan for Today's Class**

- Announcements
- Peer Factor Handouts
- Bloom's Taxonomy
- Learning Outcomes
- Learning Strategy and Course Review
- Course Feedback to make the course better

# **Announcements**

- Homeworks
  - Total of 9 graded HWs; One lowest score will be dropped
  - Contact Lilian if you have any questions
- Laboratory Grades
  - Matthew is missing some lab reports; Has sent out email to that effect
- Design Projects
  - Provide Feedback and Scores
  - Remember your individual grade will depend on your peer factor handout
- Final Exam
  - Tuesday, May 7<sup>th</sup>, 2013, 12:30PM-2:30PM, DSH 228
  - 3 Cheat Sheets allowed
- Final Grade
  - Will collate all information on HW, Labs, Design Project, Clicker questions, etc and post your grade by Friday, May 10<sup>th</sup>, 2013

# Bloom's Taxonomy of Educational Objectives

## 1. Knowledge

Recalling material you have learned. Remembering facts, principles, steps in a sequence, etc.

## 2. Comprehension

Understanding the material. At this stage you should be able to explain what you know, translate to new forms & symbols and extrapolate.

## 3. Application

At this stage you should be able to use the material in new situations, that is apply concepts, principles, rules, theories and laws to find solutions to new problems - problems you haven't seen before.

## 4. Analysis

At this level you should be able to break things apart so that relationships are understood. For example, you might analyze an amplifier circuit using what you learn about transistors.

## 5. Synthesis

You should be able to put together parts to form a new whole. Engineers do this when they write proposals, design new products, etc.

## 6. Evaluation

Here you should be able to use what you know about a subject area to make critical judgments, rate ideas or objects and to accept or reflect materials based on standards. The key skill is the ability to make judgments.

# Learning Outcomes of the Course

At the end the course, you should be able to:

- Analyze the operation of a field effect transistor and apply the piecewise linear model to determine the DC/AC response of the FET
- Design and analyze the response of various MOSFET and JFET functional circuits such as amplifiers (CS, CG, CD etc), switching circuits, logic gates using AC/DC load line analysis.
- Analyze the operation of a bipolar junction transistor and apply the piecewise linear model to determine the DC/AC response of the BJT
- Design and analyze the response of various BJT functional circuits such as amplifiers (CE, CC, CB, cascade, cascode, Darlington pair, etc), switching circuits, logic gates using AC/DC load line analysis
- Construct Bode plots of the gain magnitude and phase of various amplifier circuits taking into account circuit capacitors and time constants and determine their frequency response.
- Determine the short circuit gain versus frequency of a BJT and the unity gain bandwidth of an FET and determine their Miller capacitances using the expanded hybrid-p model
- Work together in a team and evaluate/assess your individual performance and the performance of your teammates

# **Learning Strategy for Final Exams**

- Review clicker questions
- Review HWs
- Review Mid Terms
- Review TYU, exercise and back of chapter problems from text book
- Review all your class notes (all content from there)

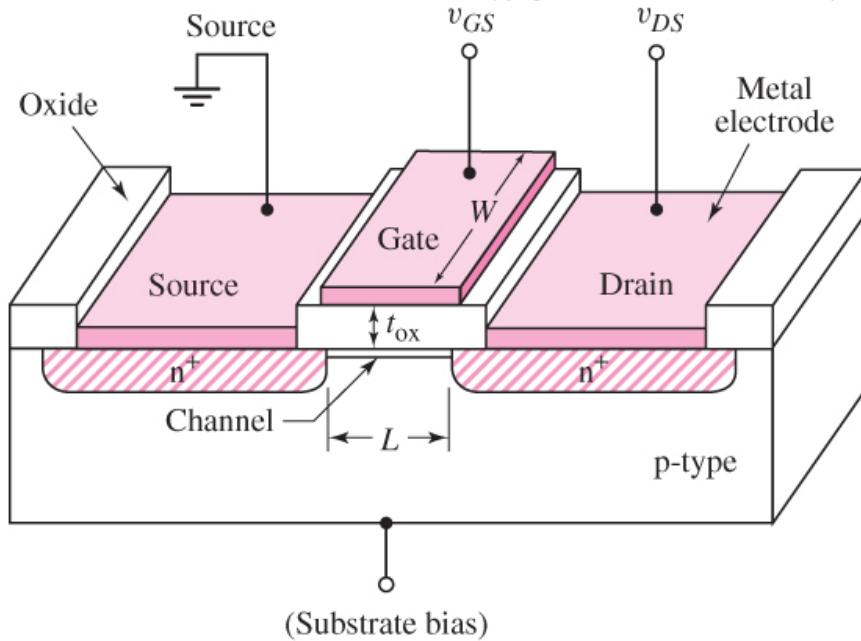
**Course Review: A Flashback....😊**

# **FETs Review**

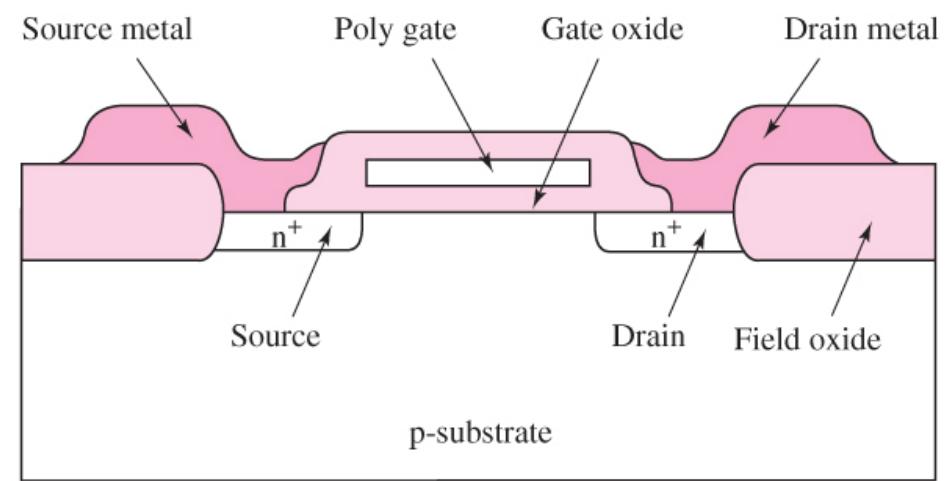
## **(Chapter 3 and 4)**

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(a)



(b)

Fig. 3.10

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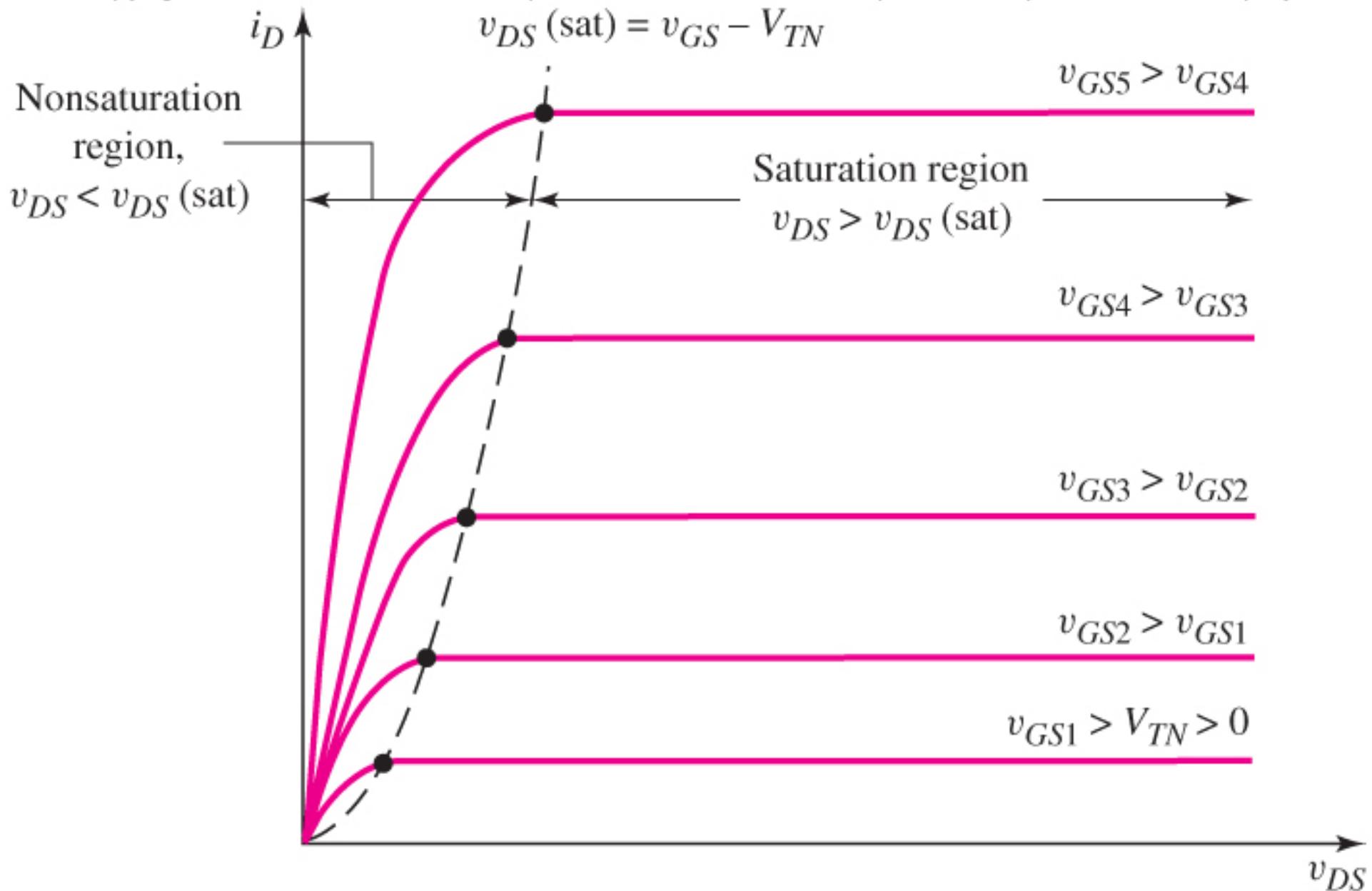


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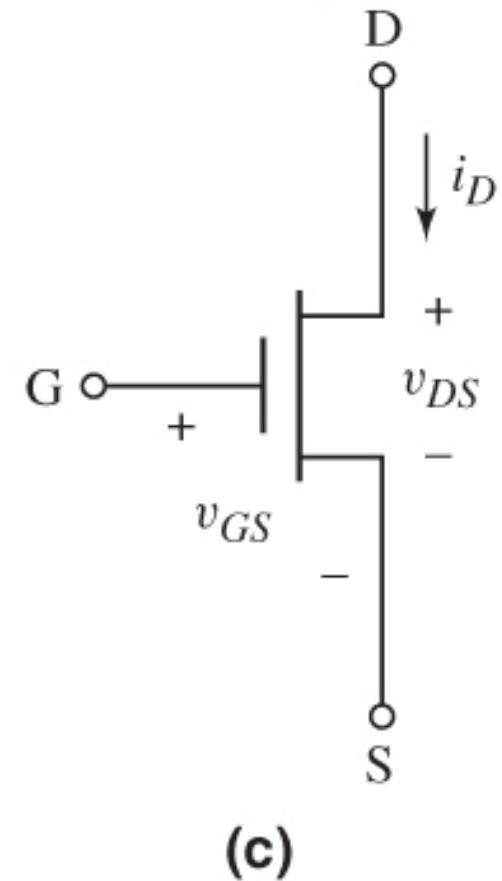
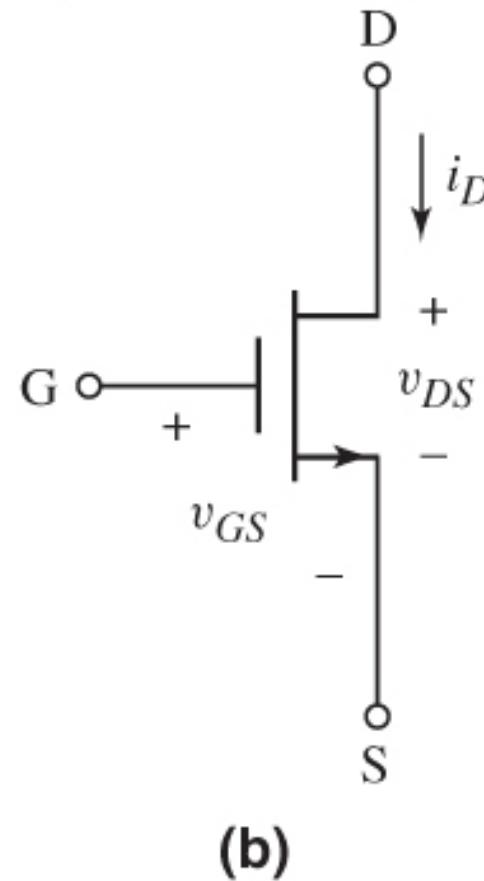
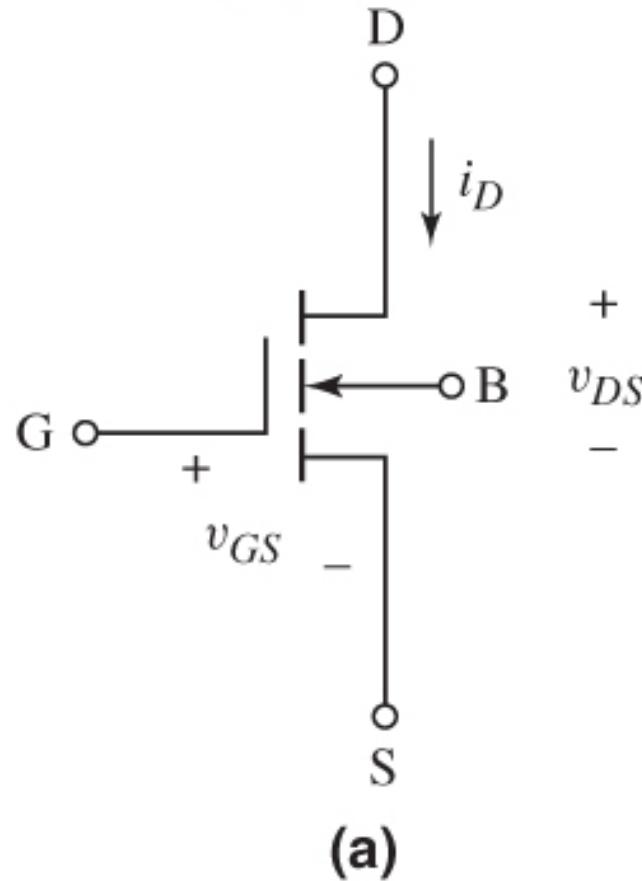
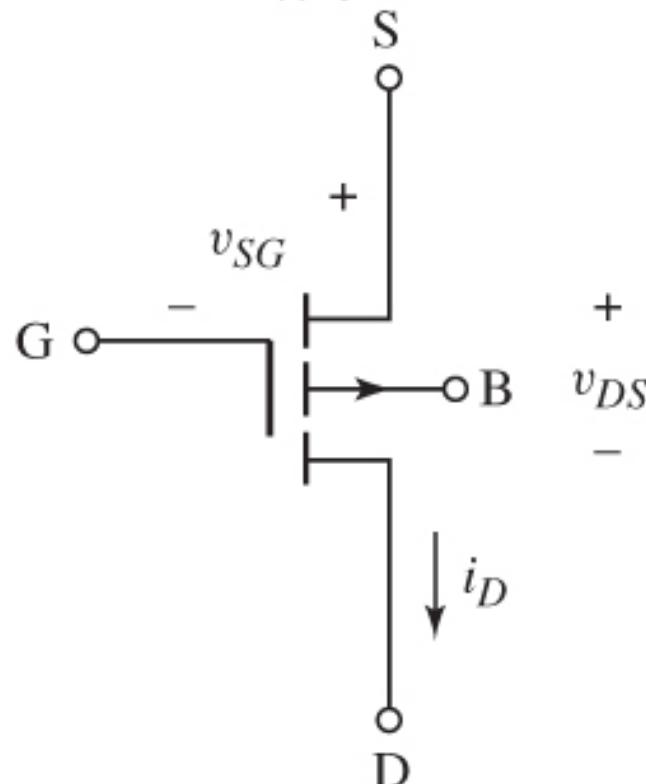
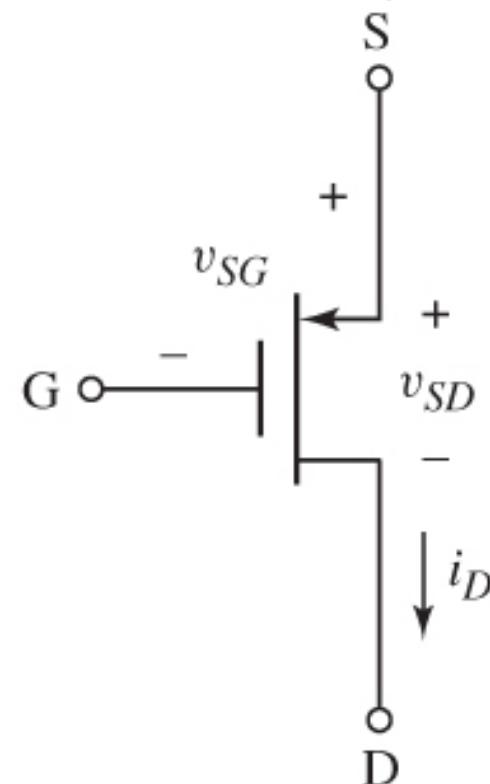


Fig. 3.13

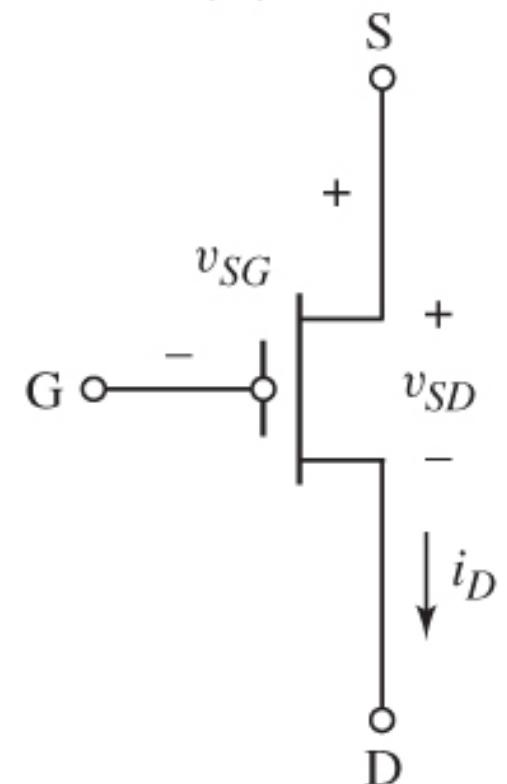
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(a)



(b)



(c)

Fig. 3.14

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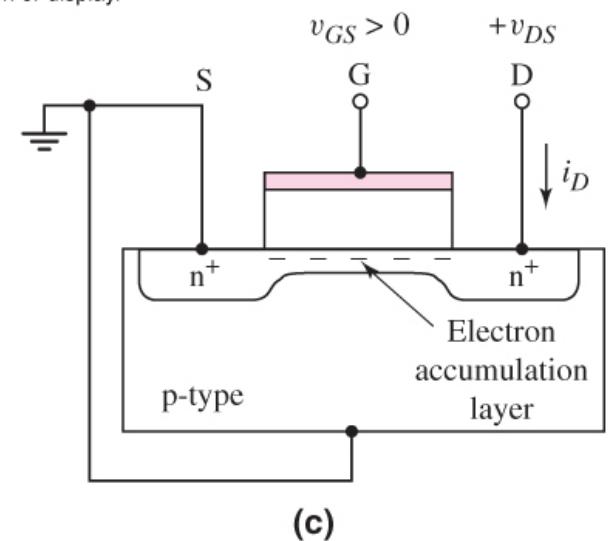
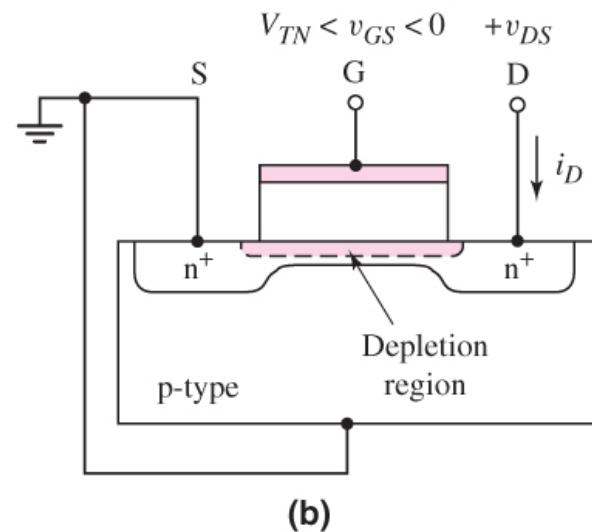
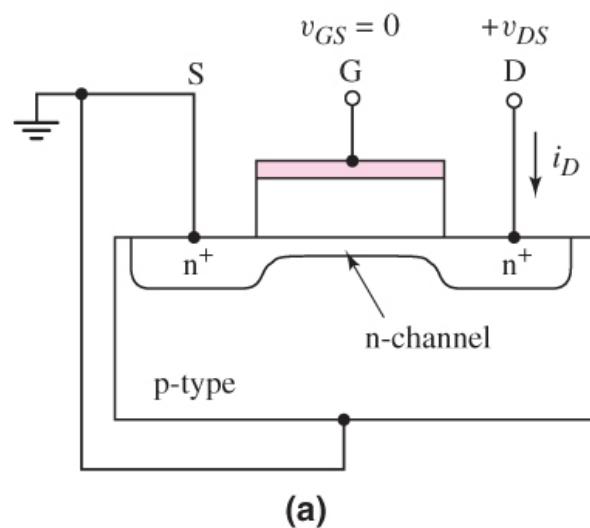
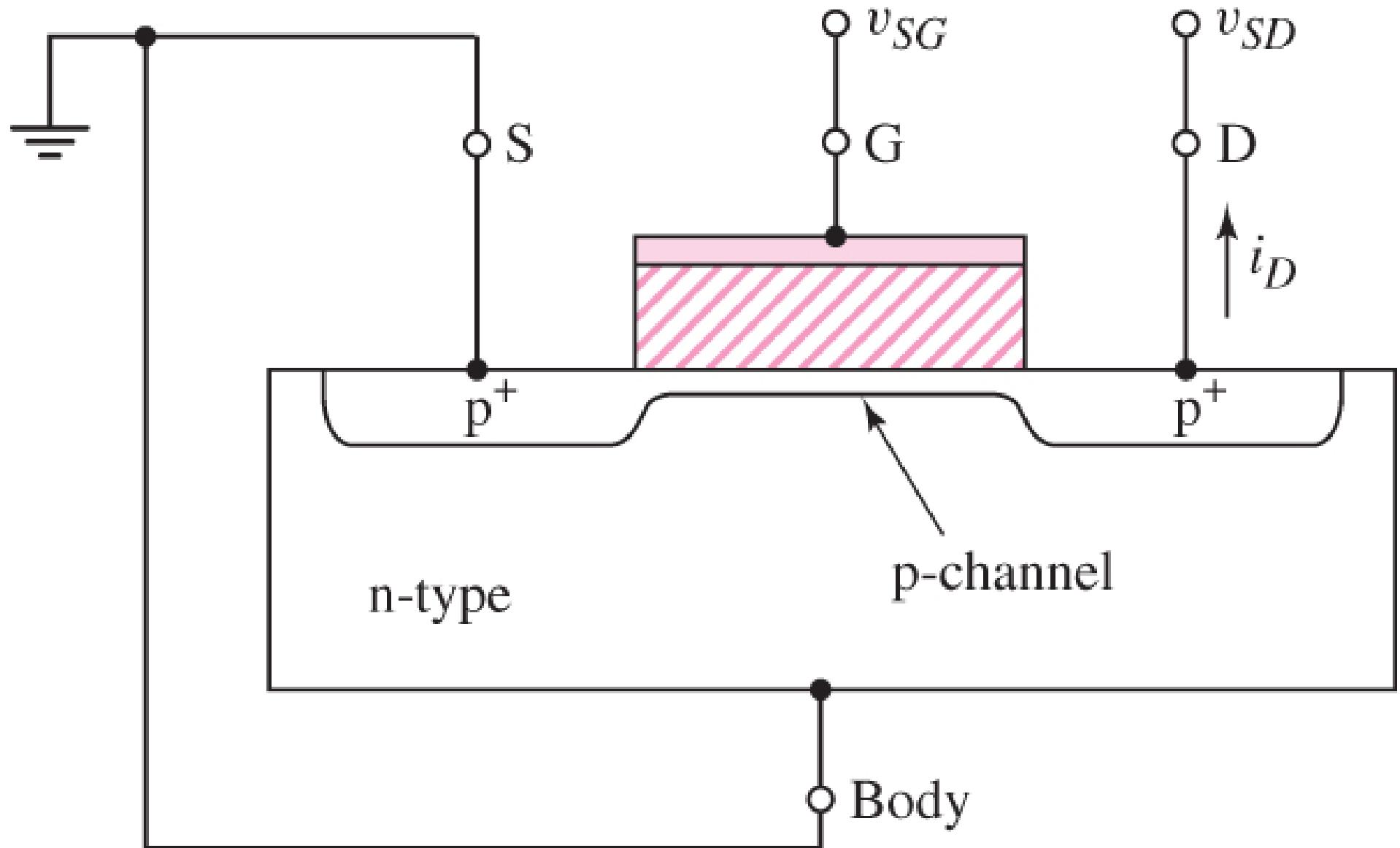


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**Table 3.1 Summary of the MOSFET current–voltage relationships****NMOS**Nonsaturation region ( $v_{DS} < v_{DS}(\text{sat})$ )

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$$

Saturation region ( $v_{DS} > v_{DS}(\text{sat})$ )

$$i_D = K_n(v_{GS} - V_{TN})^2$$

Transition point

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

Enhancement mode

$$V_{TN} > 0$$

Depletion mode

$$V_{TN} < 0$$

**PMOS**Nonsaturation region ( $v_{SD} < v_{SD}(\text{sat})$ )

$$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$$

Saturation region ( $v_{SD} > v_{SD}(\text{sat})$ )

$$i_D = K_p(v_{SG} + V_{TP})^2$$

Transition point

$$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$$

Enhancement mode

$$V_{TP} < 0$$

Depletion mode

$$V_{TP} > 0$$

Fig. 3.20

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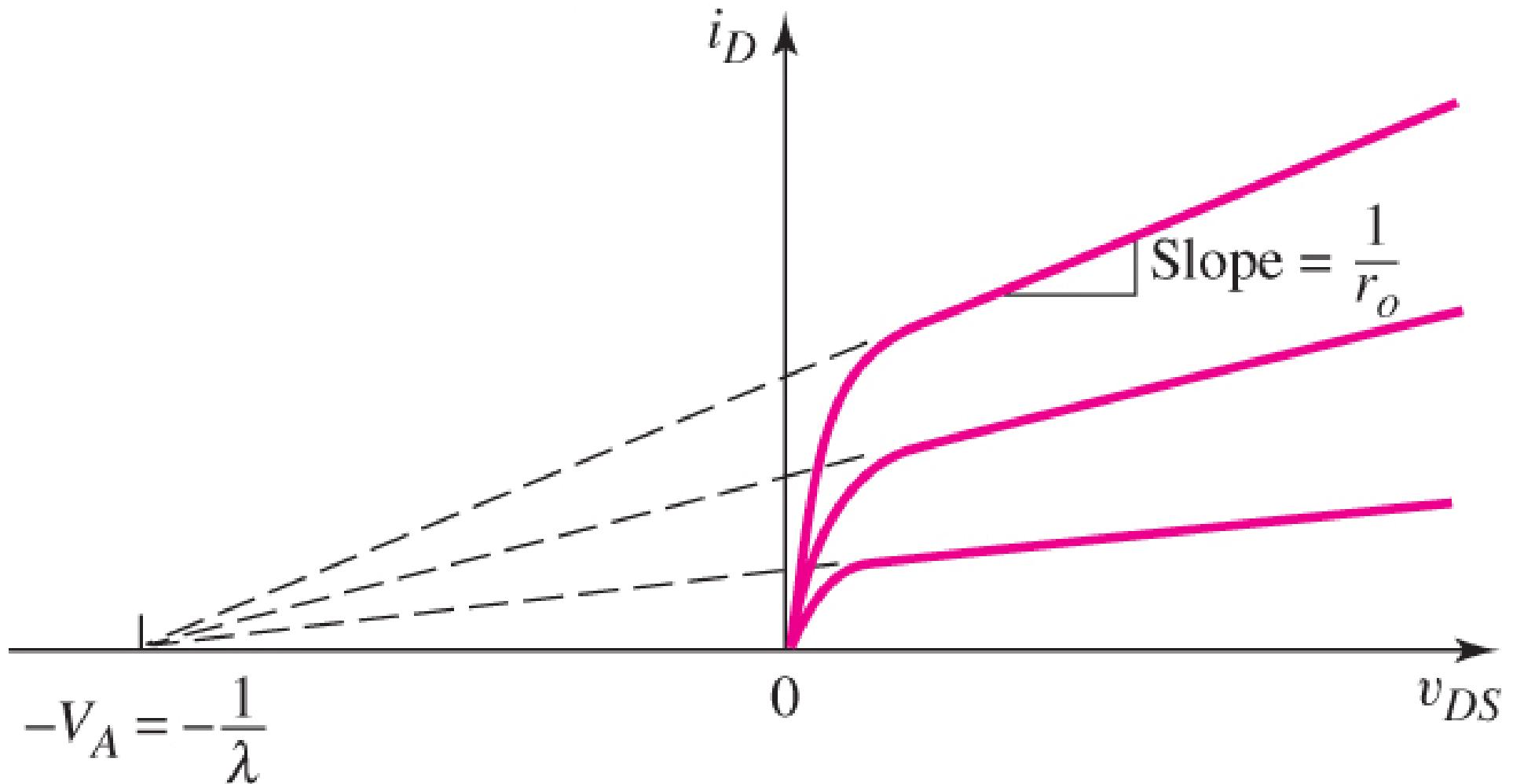


Fig. 3.21

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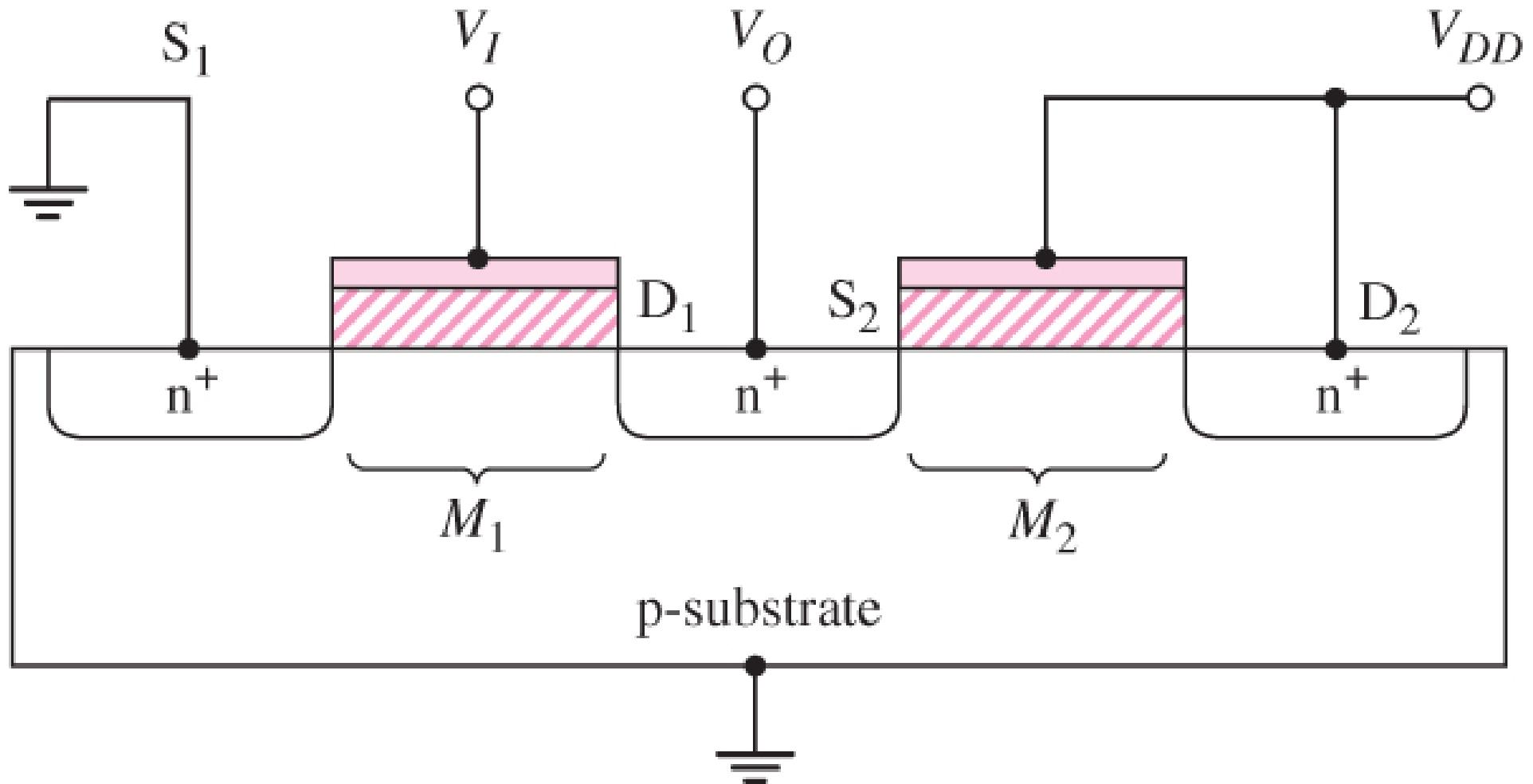


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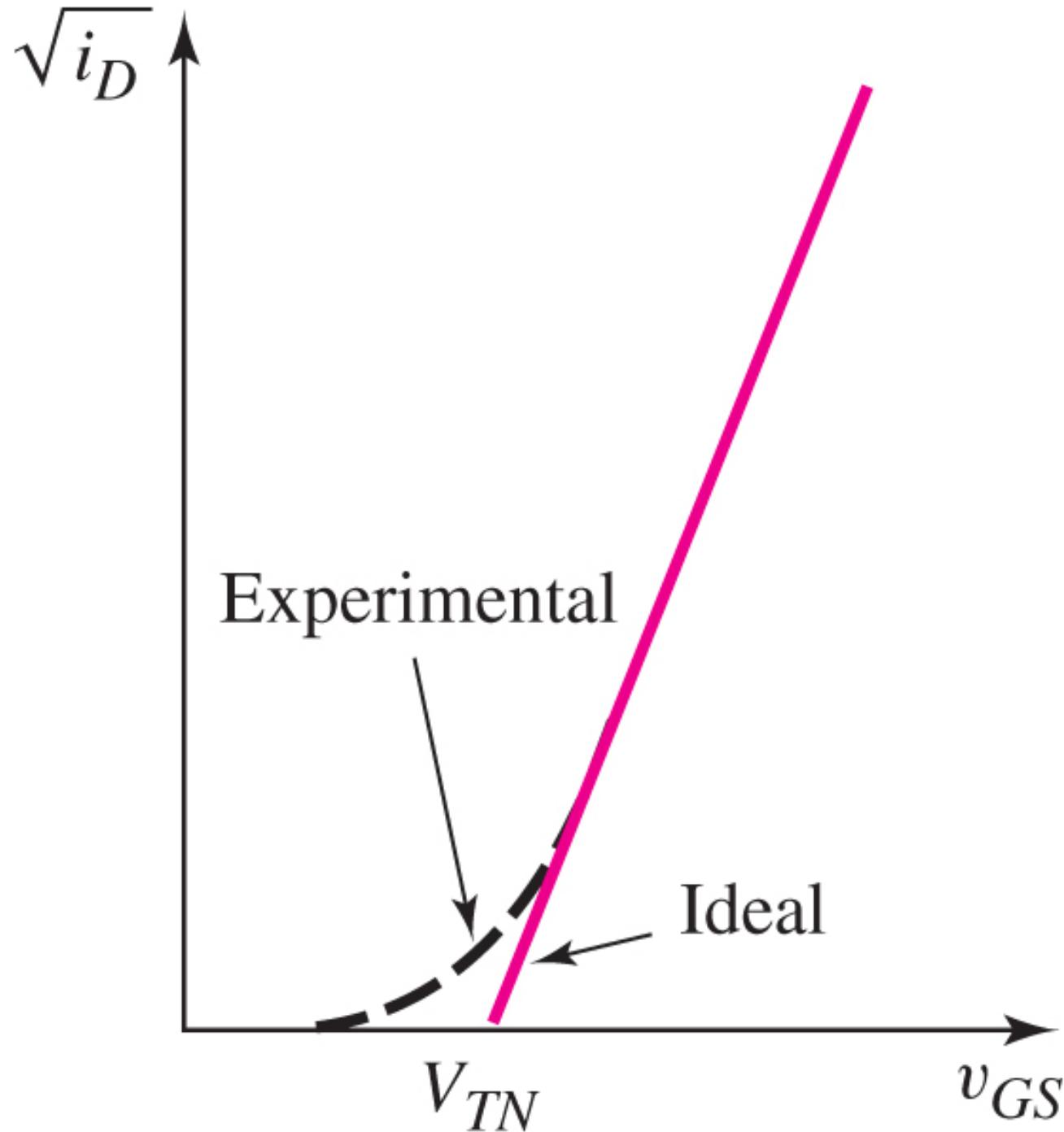


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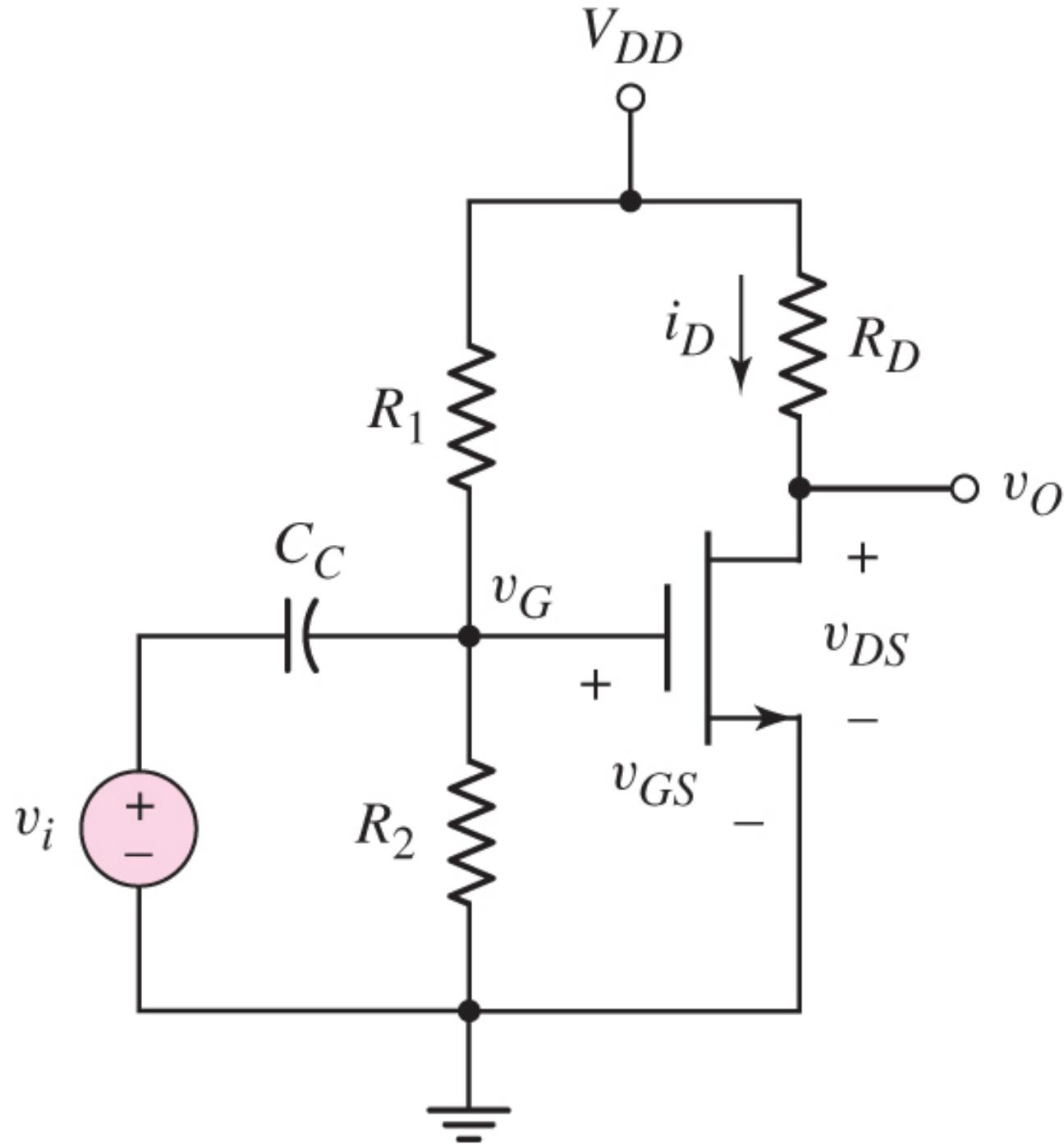
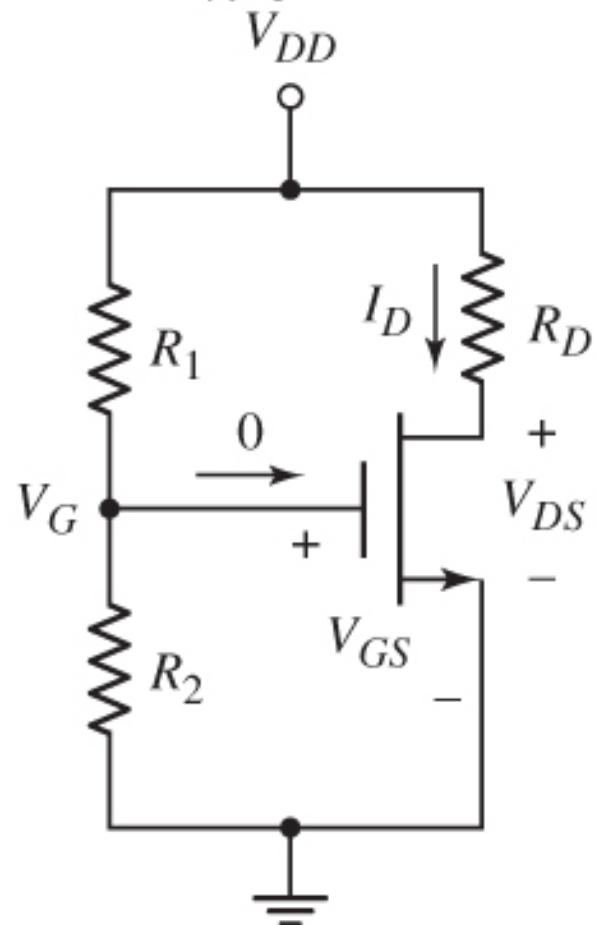
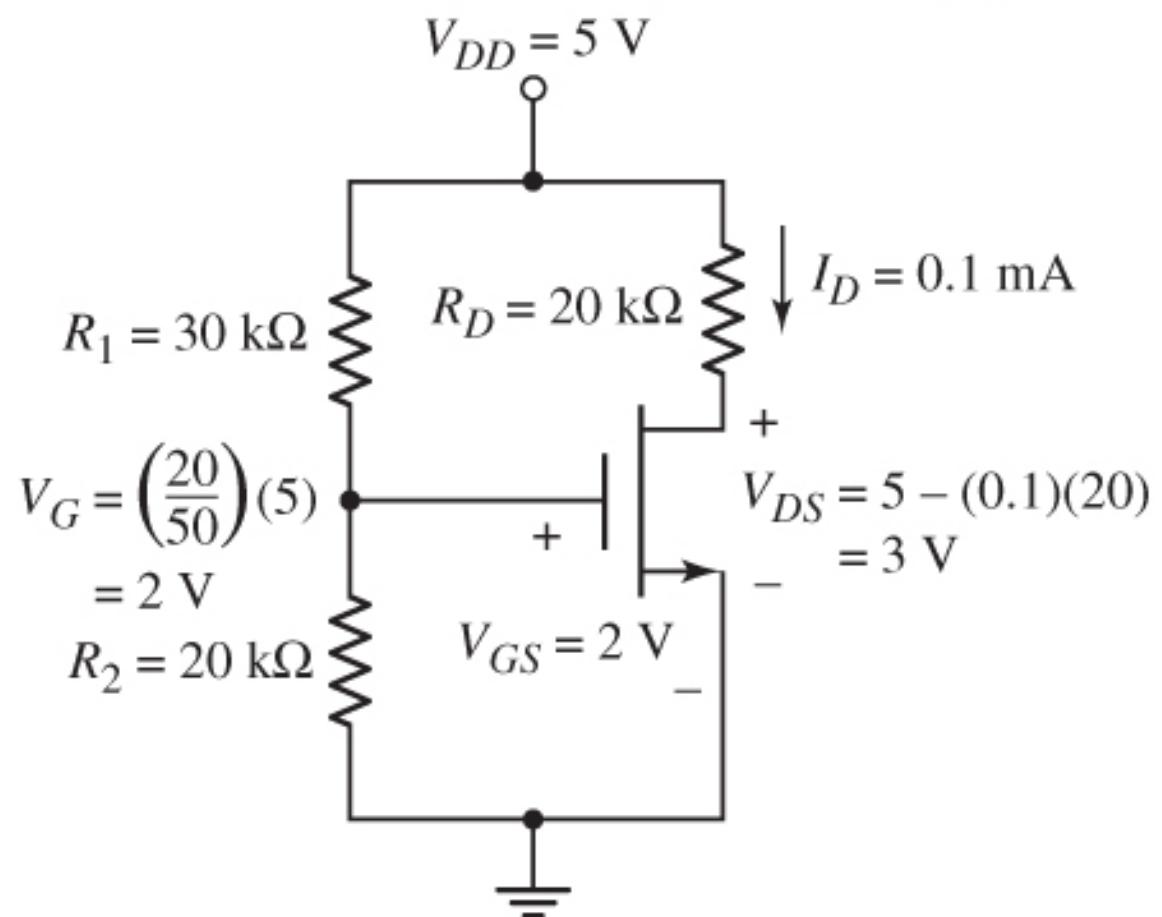


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(a)



(b)

Fig. 3.31

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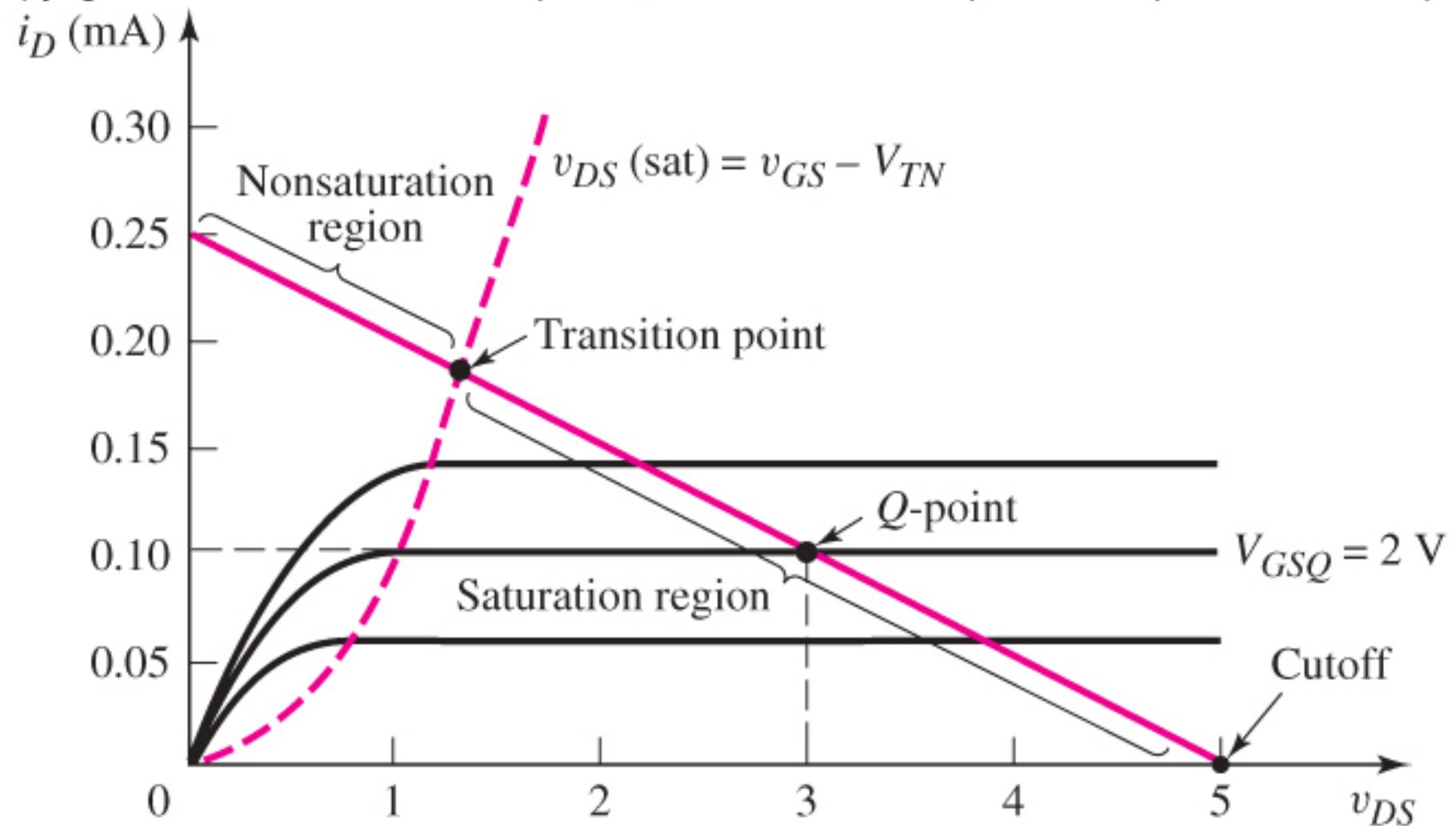


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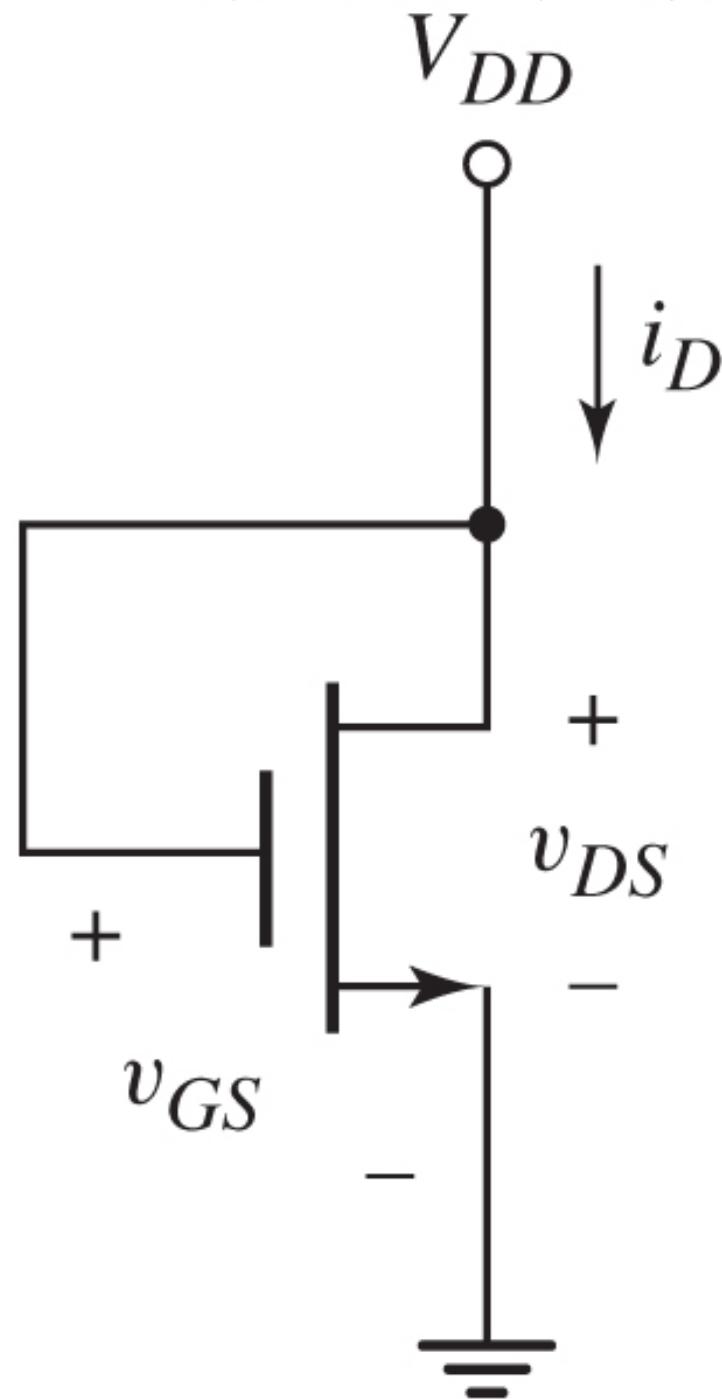


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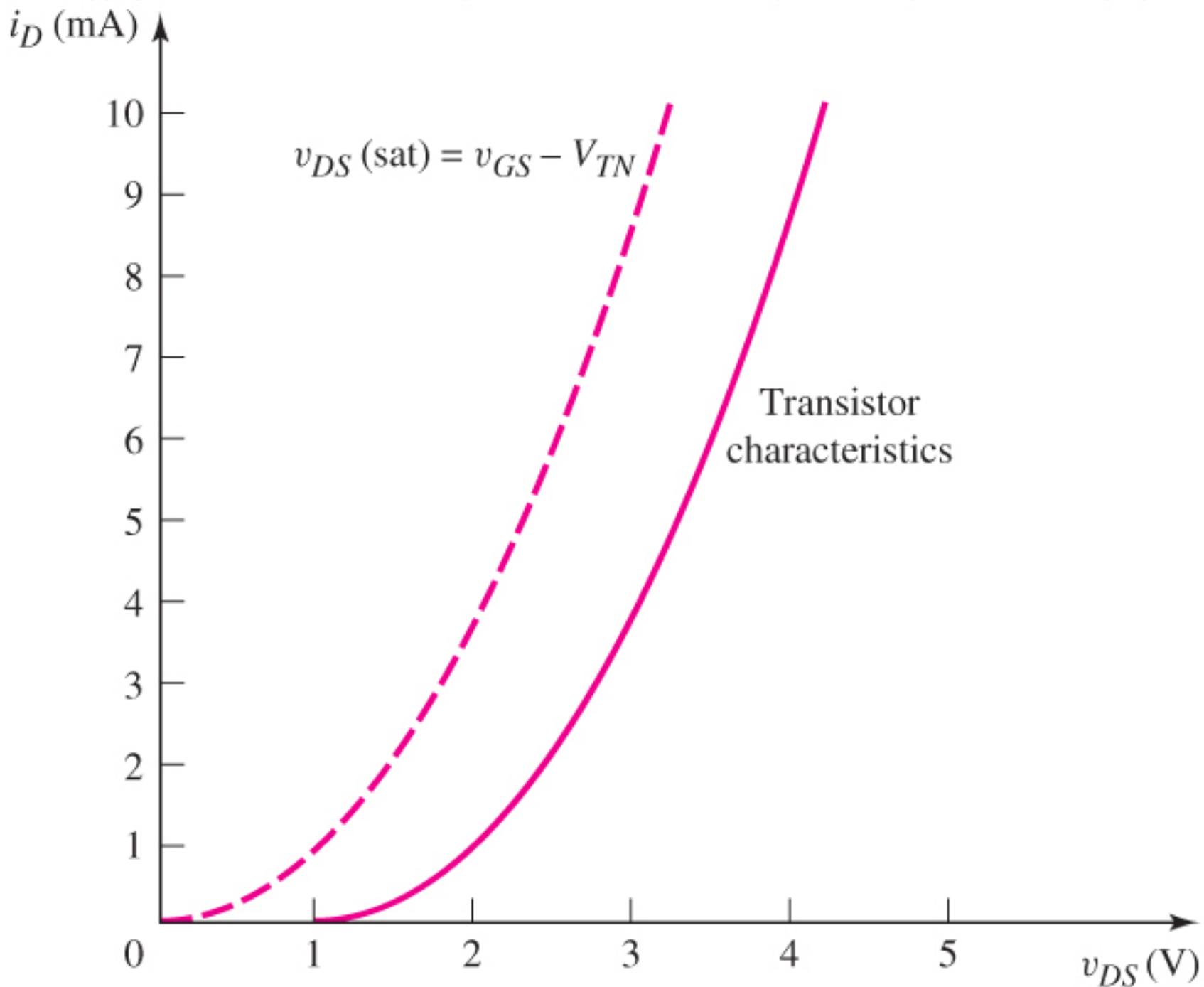


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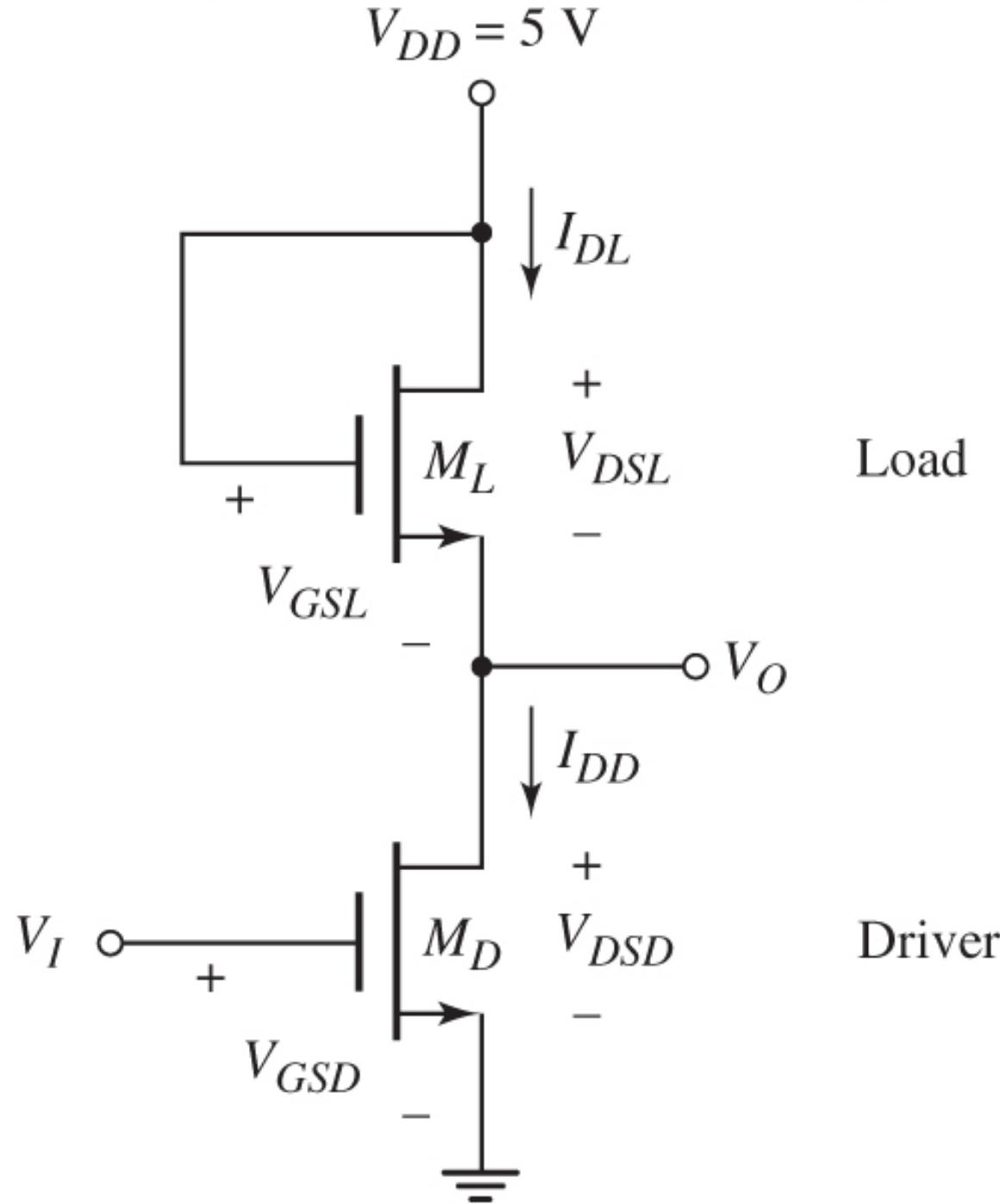


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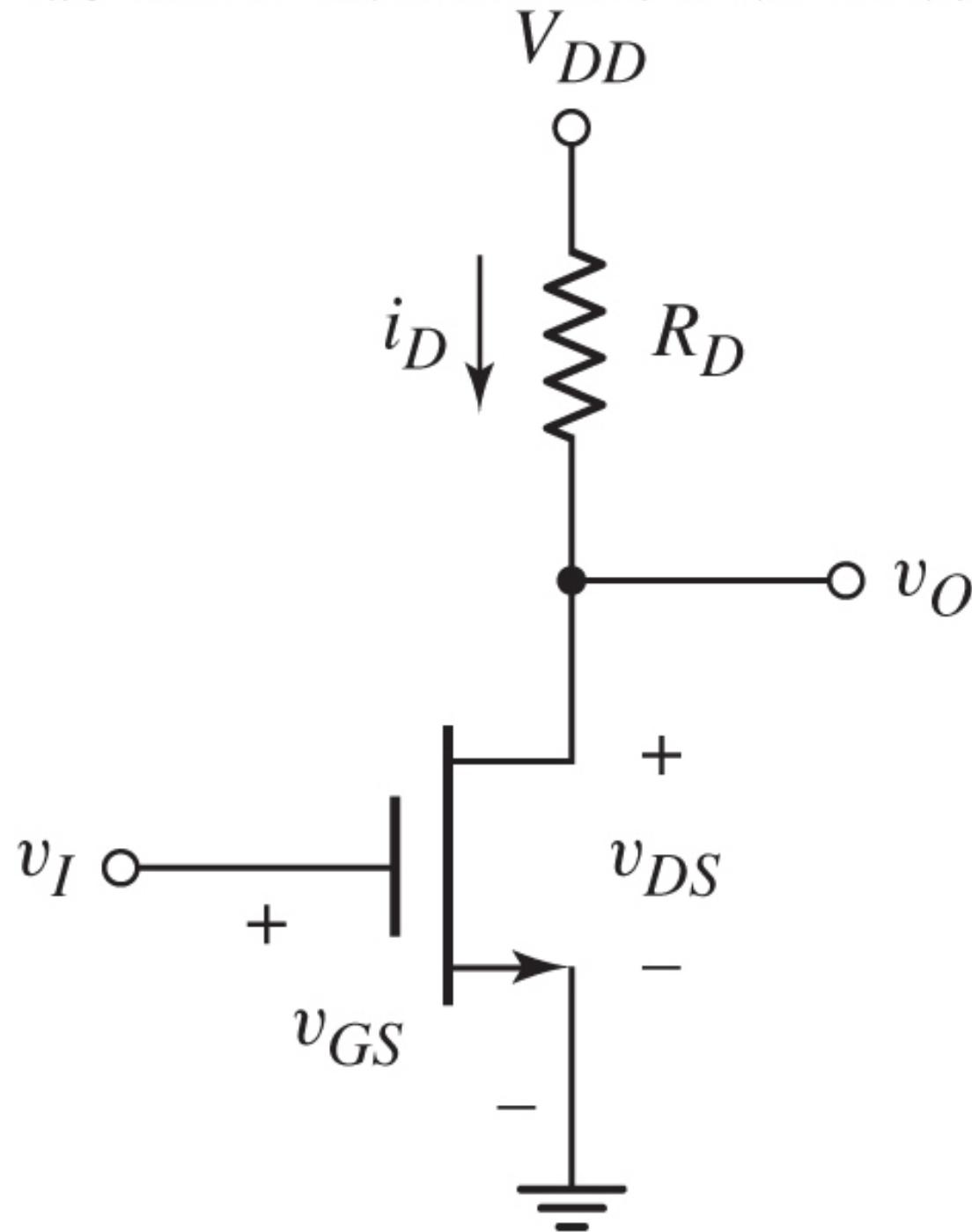


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$$V_{DD} = 5 \text{ V}$$

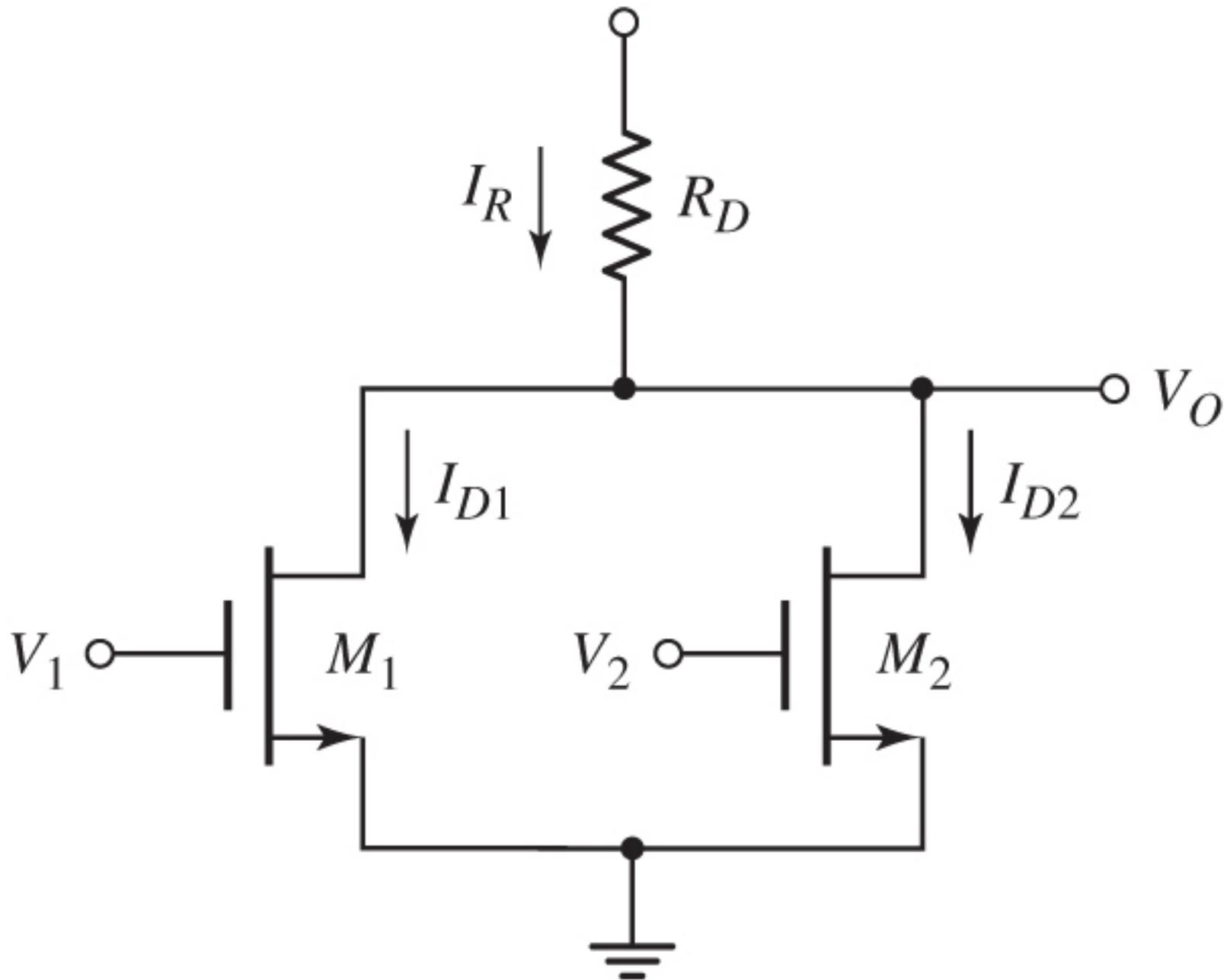


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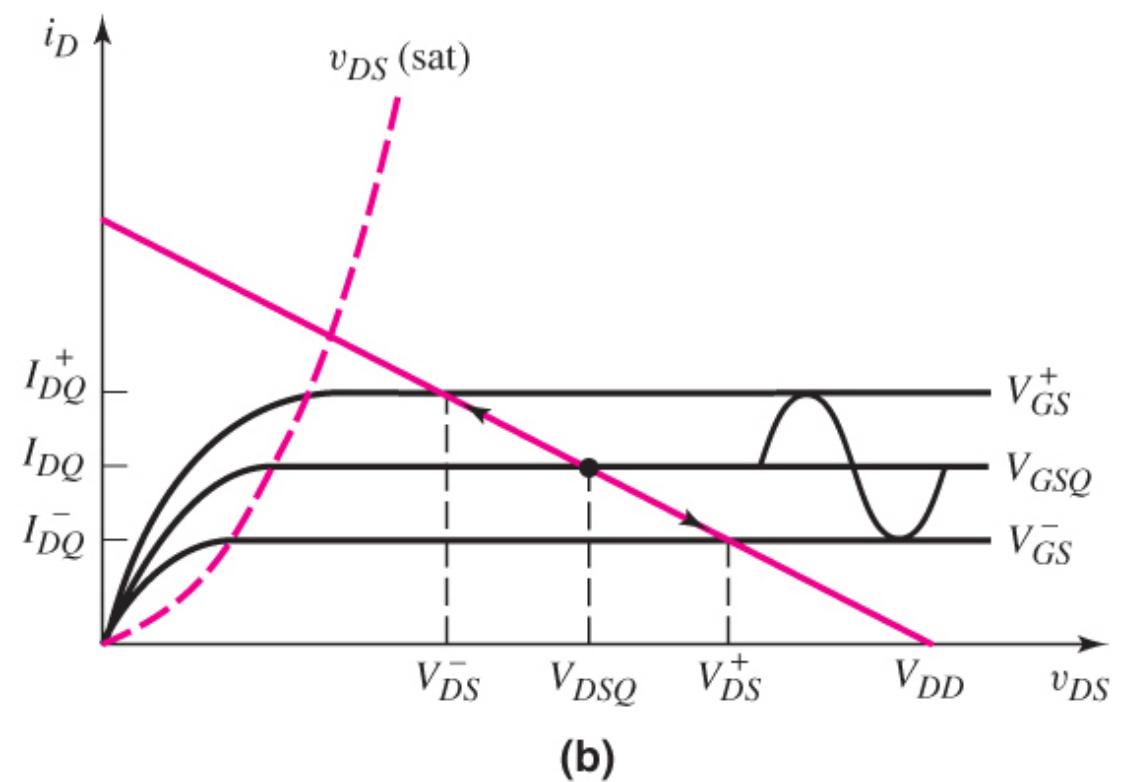
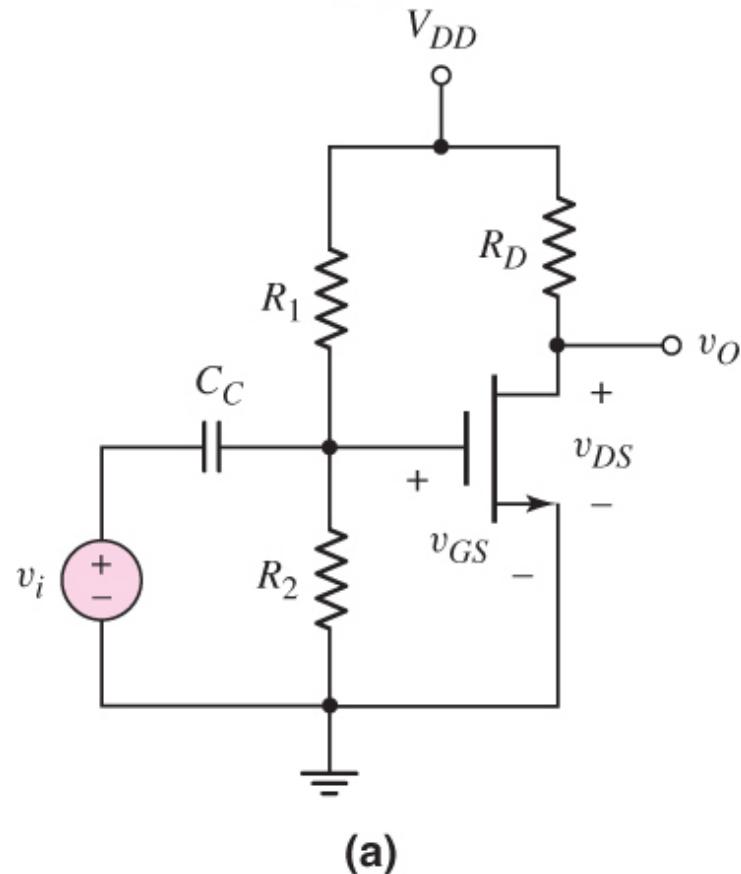


Fig. 3.49

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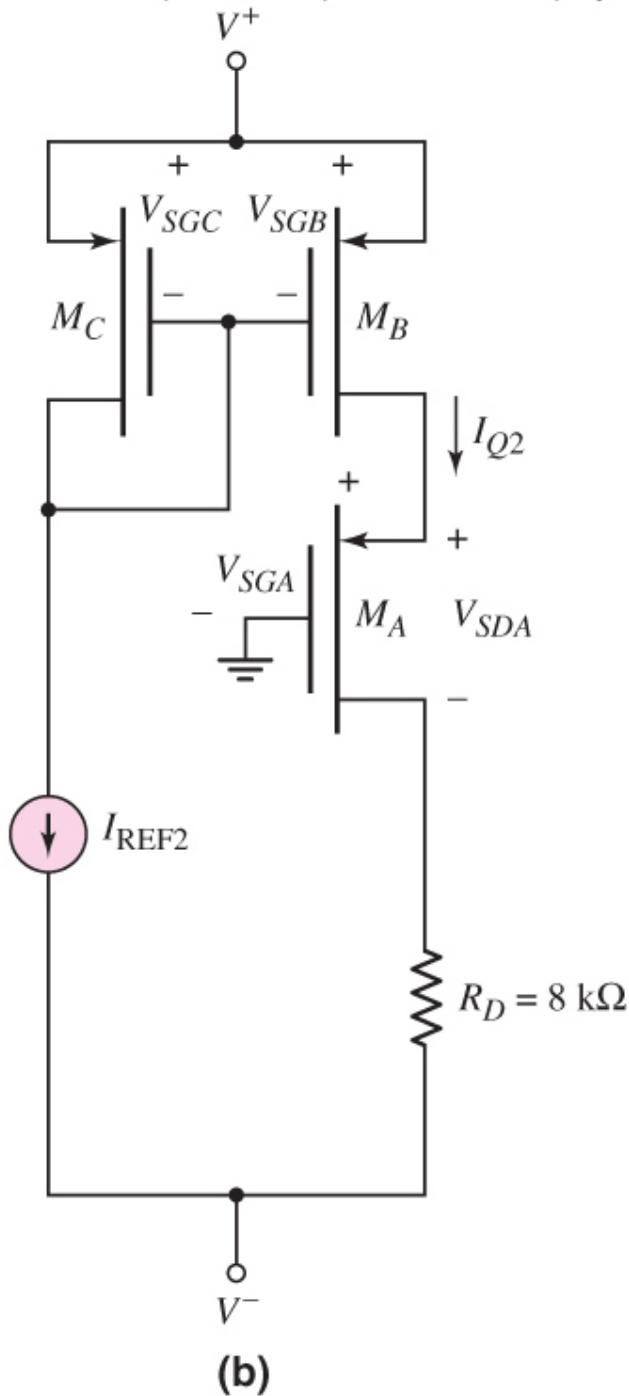
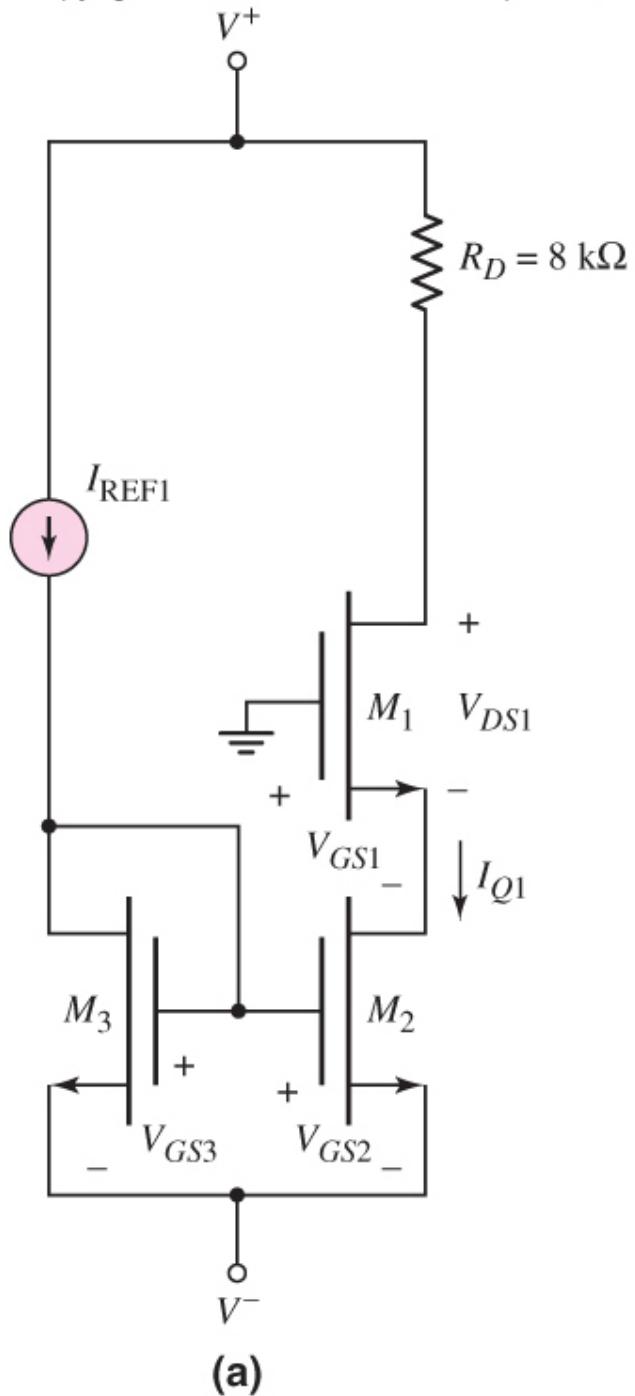


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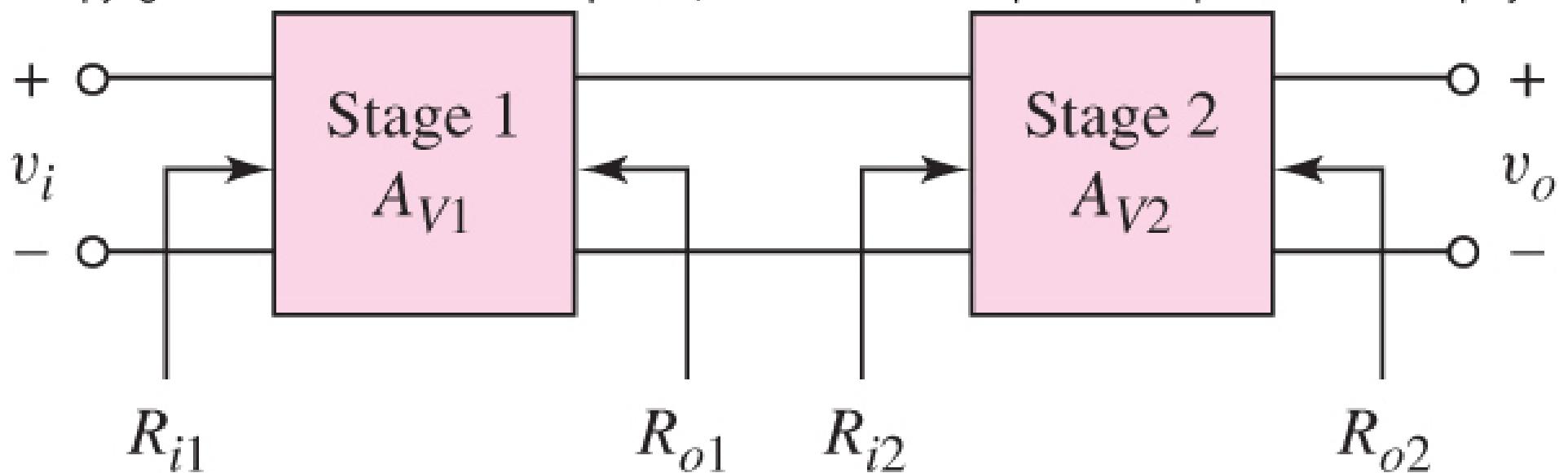


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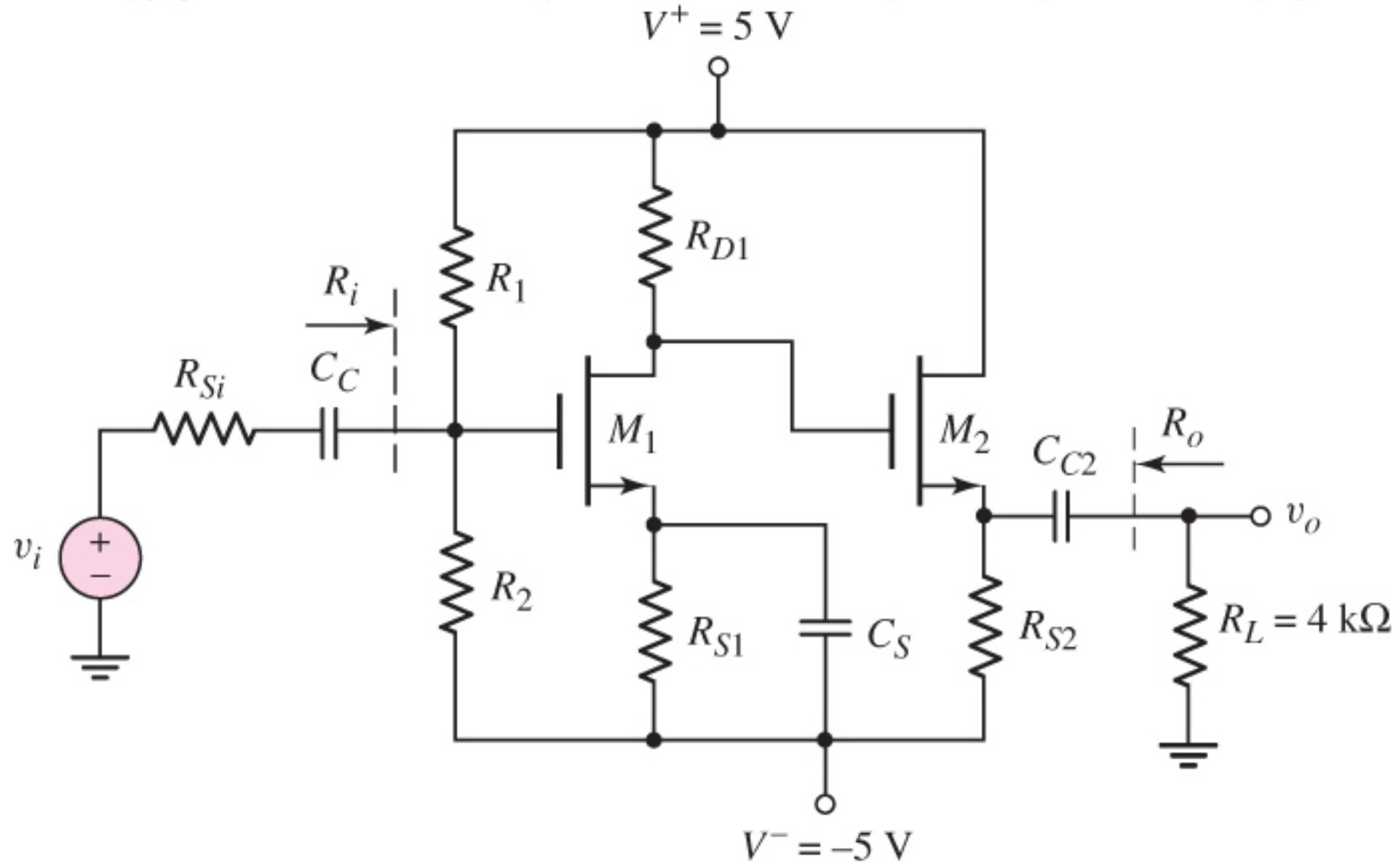


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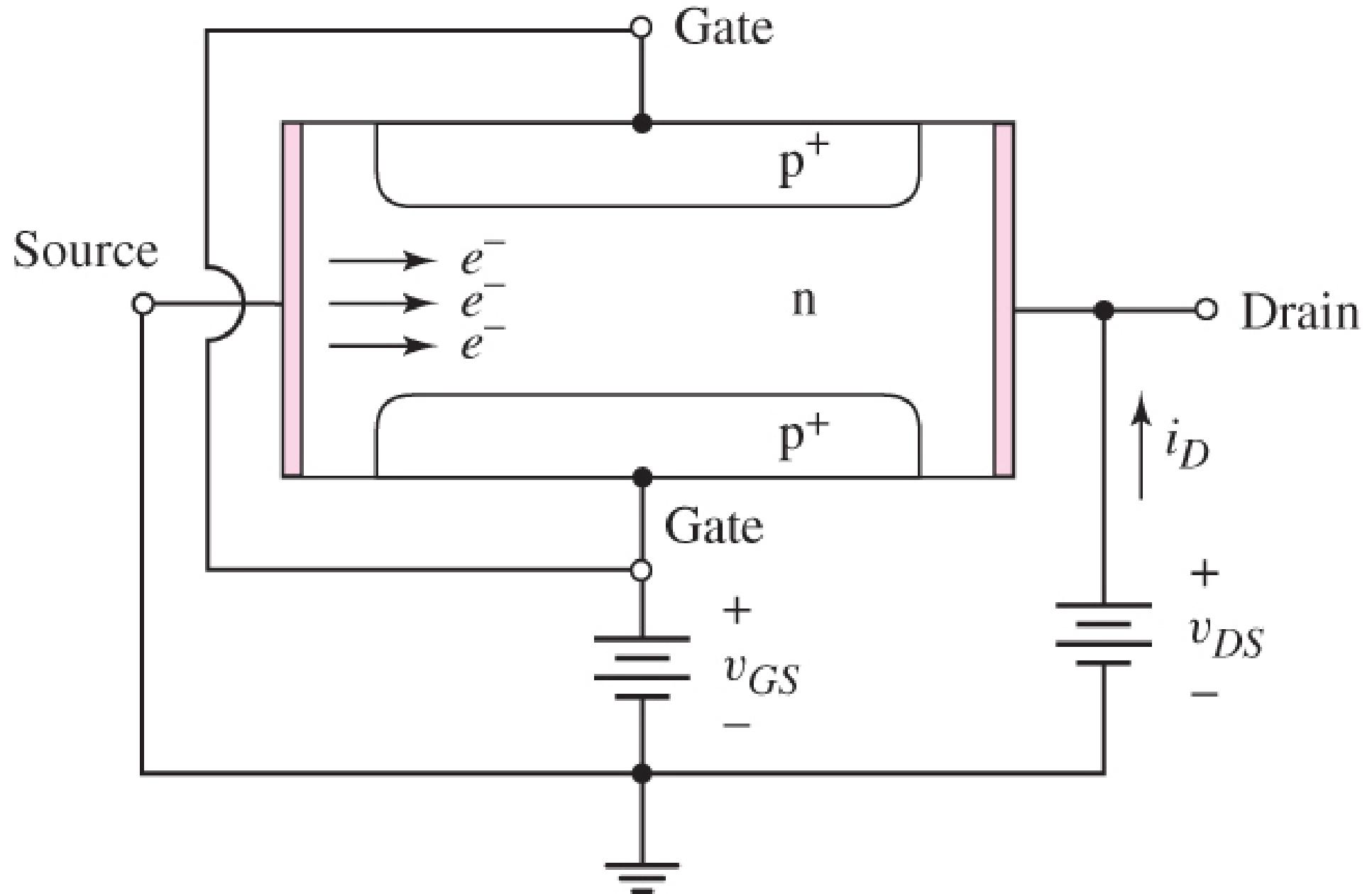


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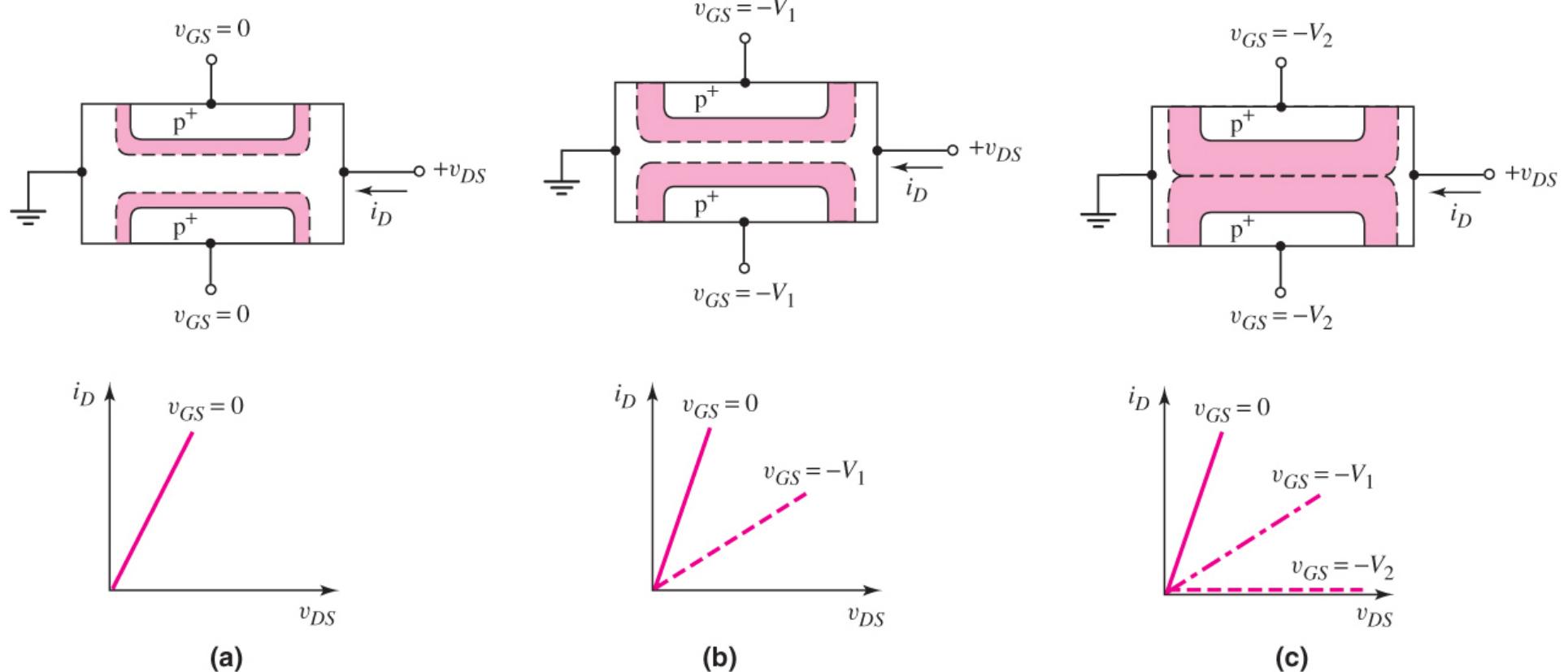


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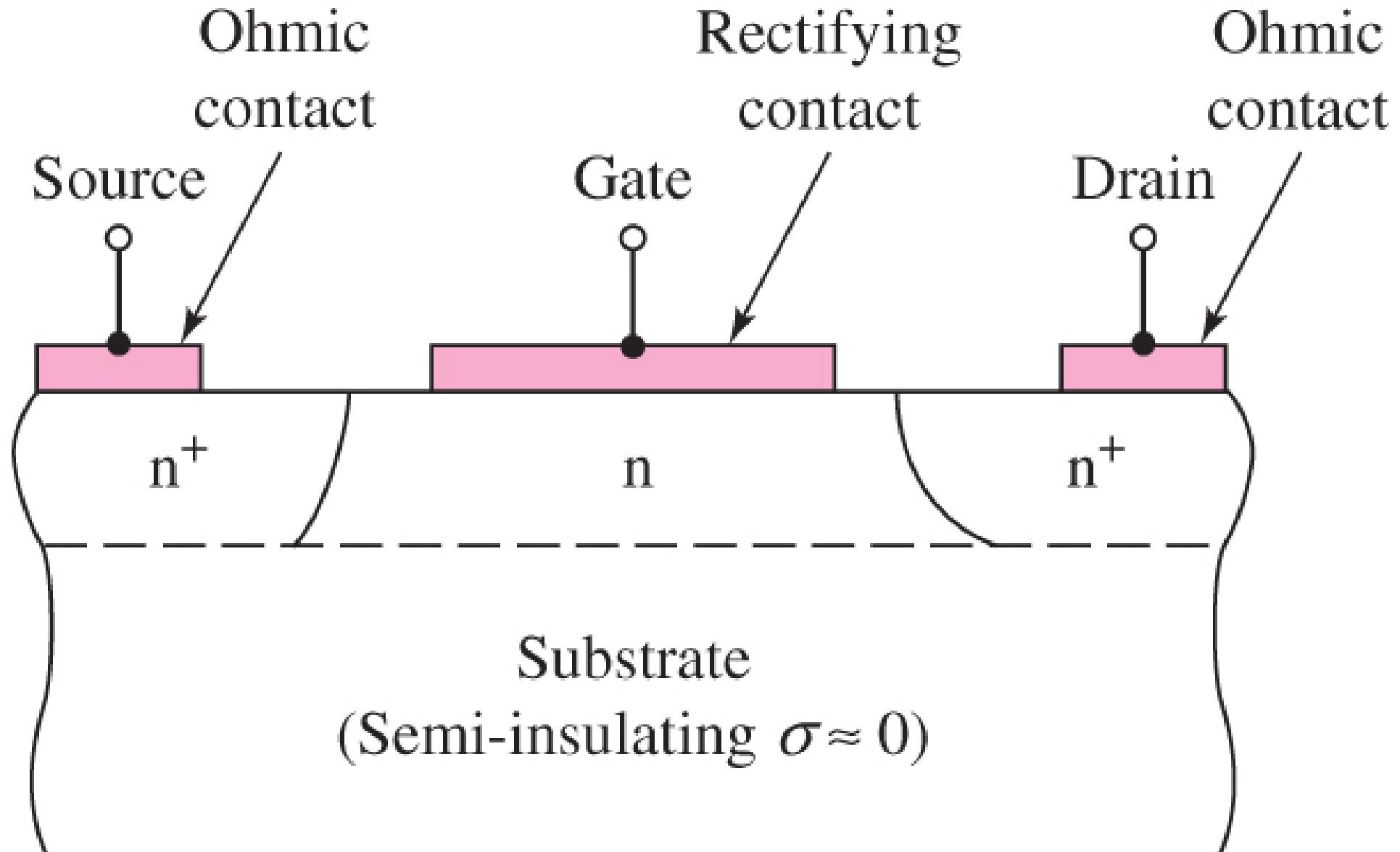
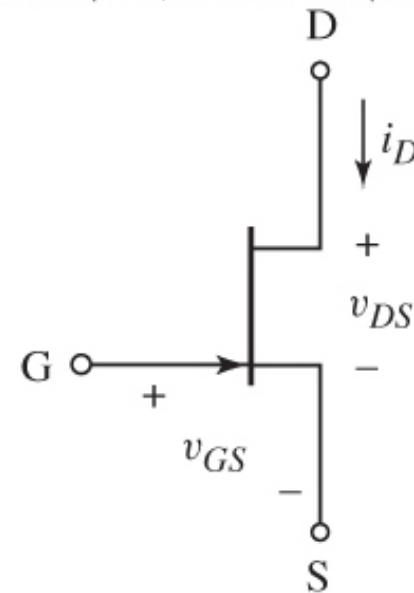
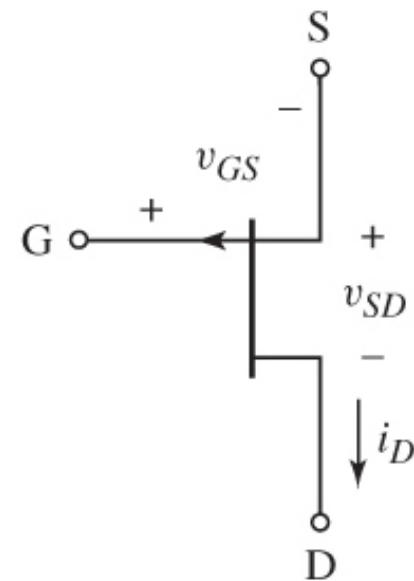


Fig. 3.59



(a)



(b)

Fig. 3.65

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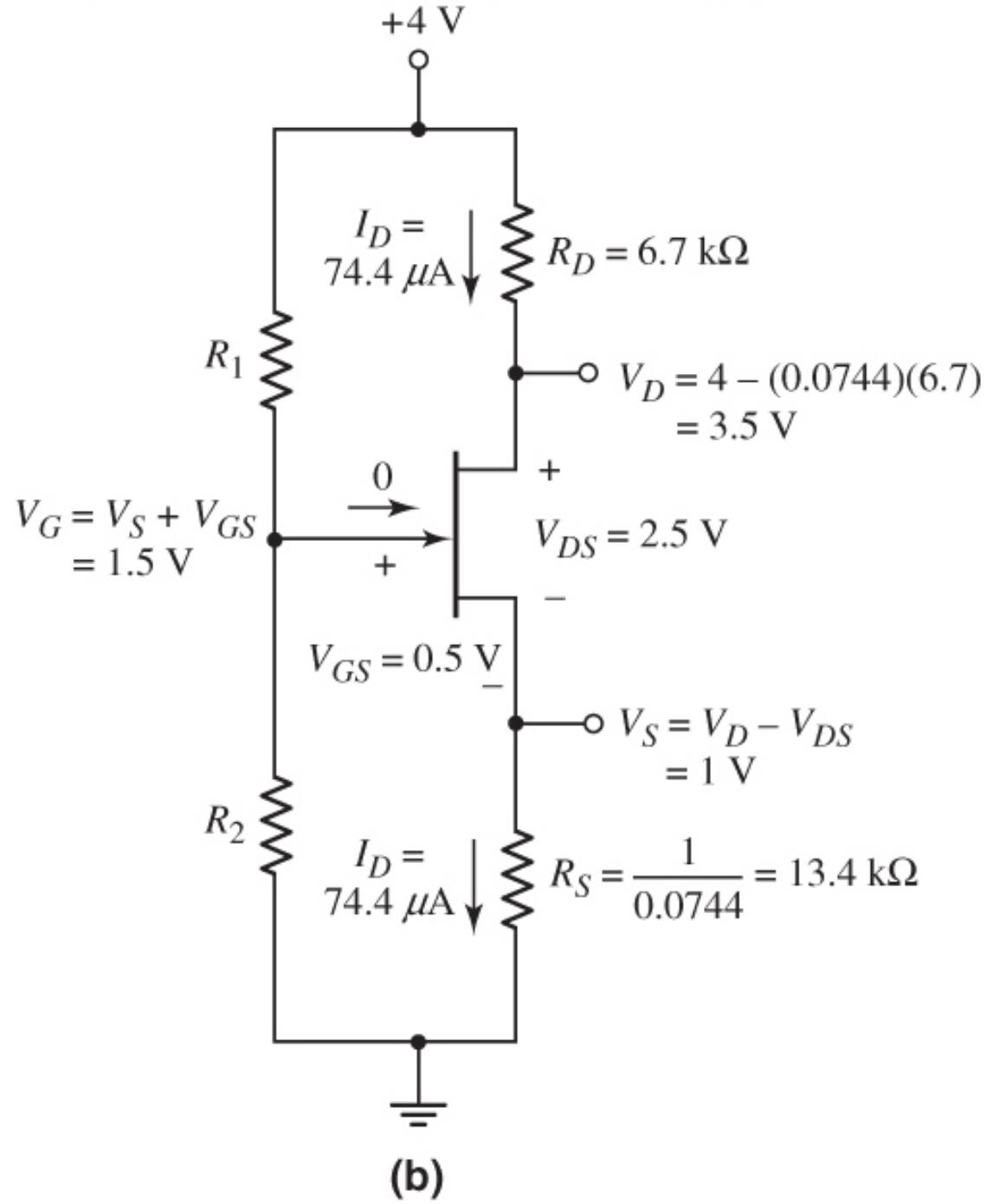
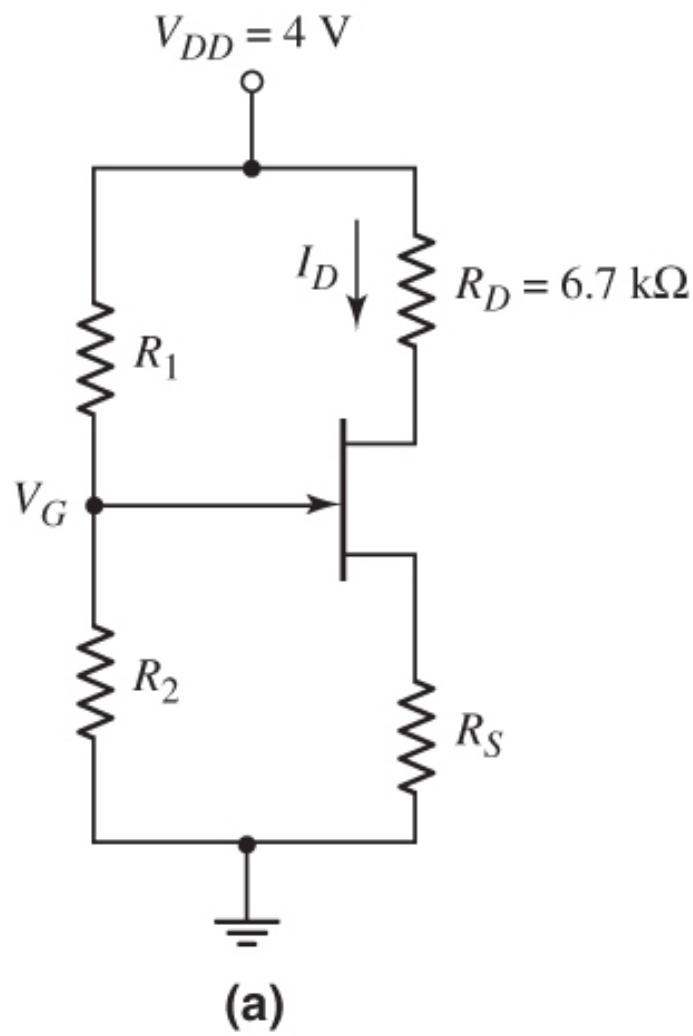


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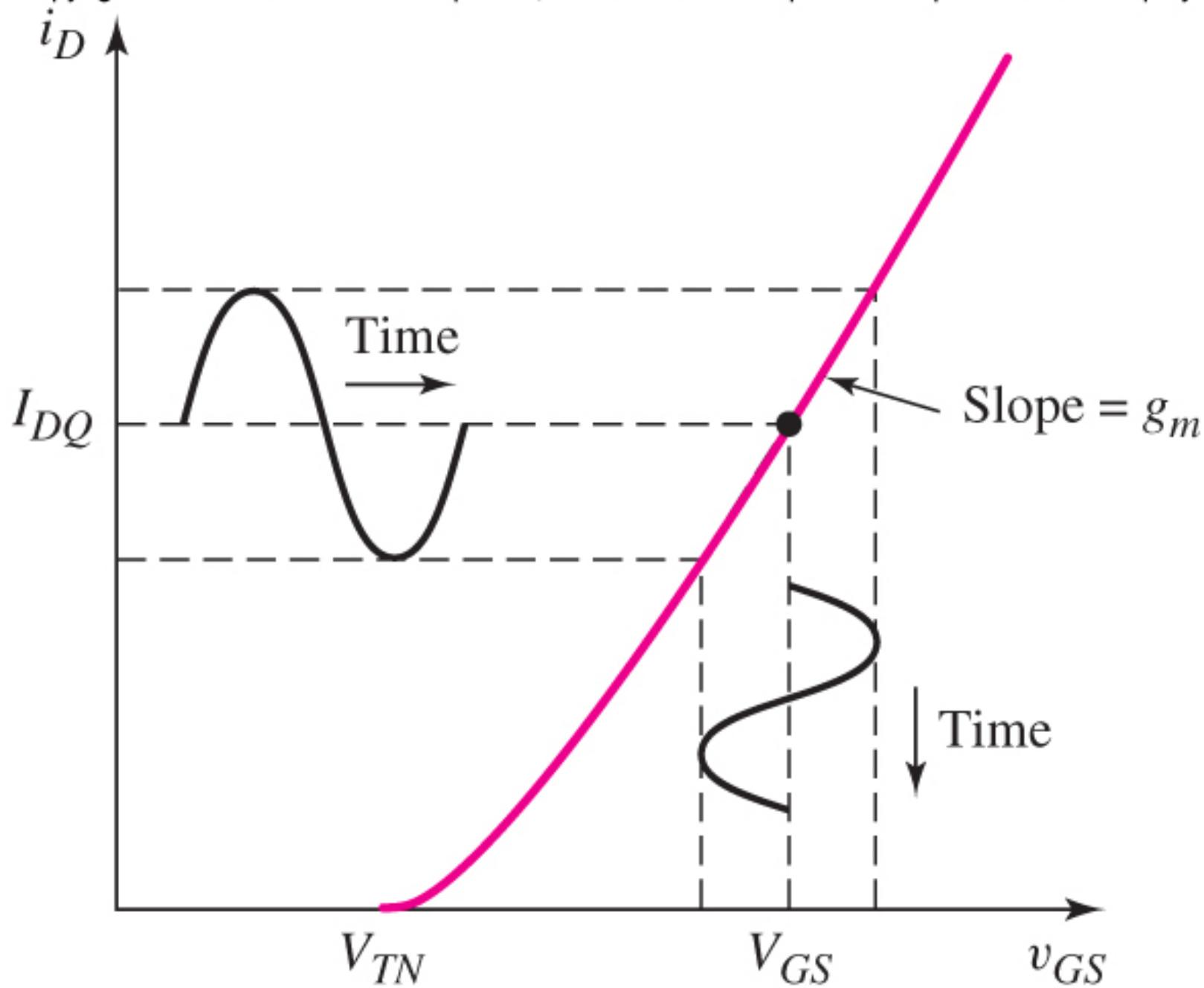


Fig. 4.6

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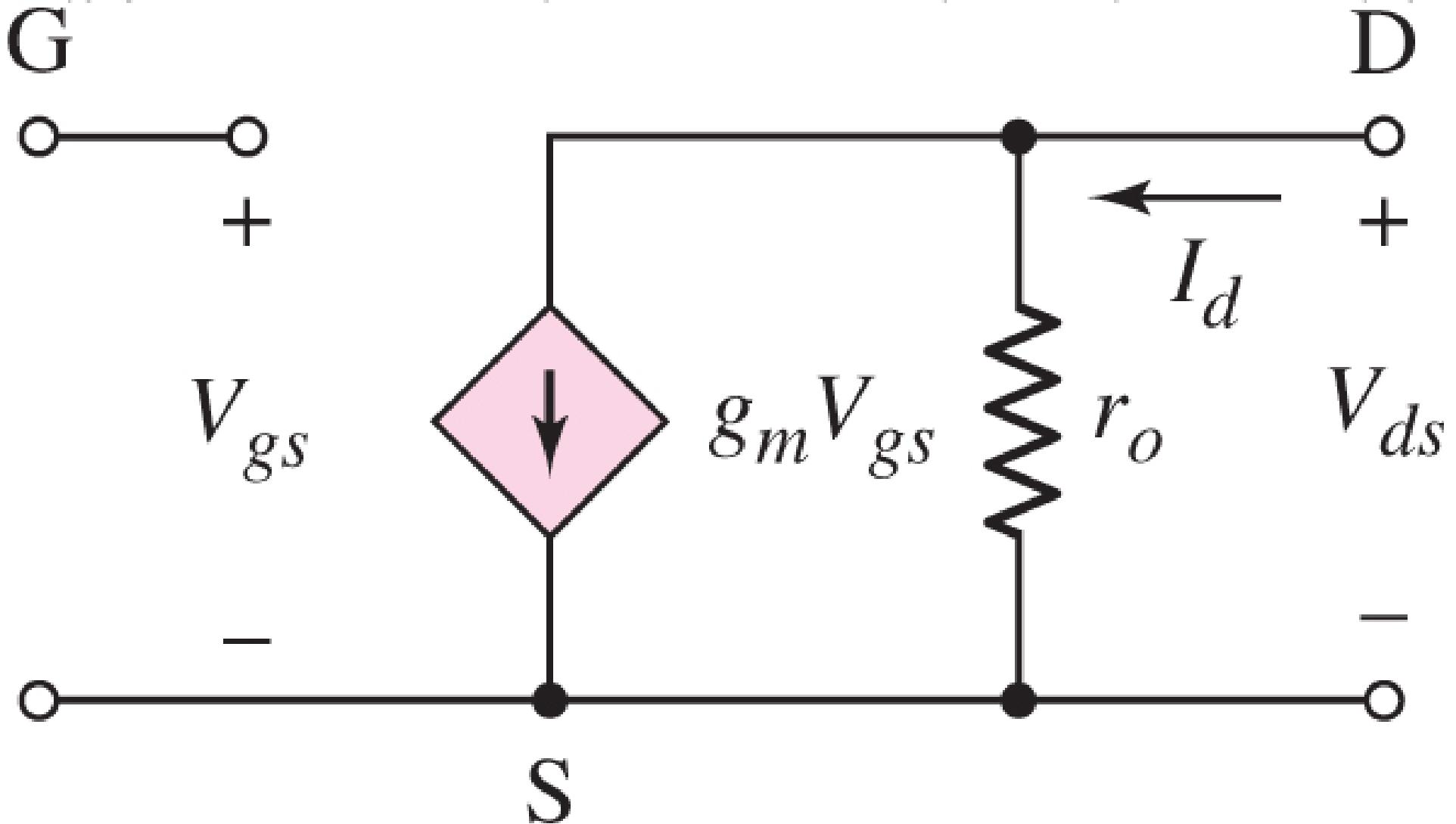


Fig. 4.9

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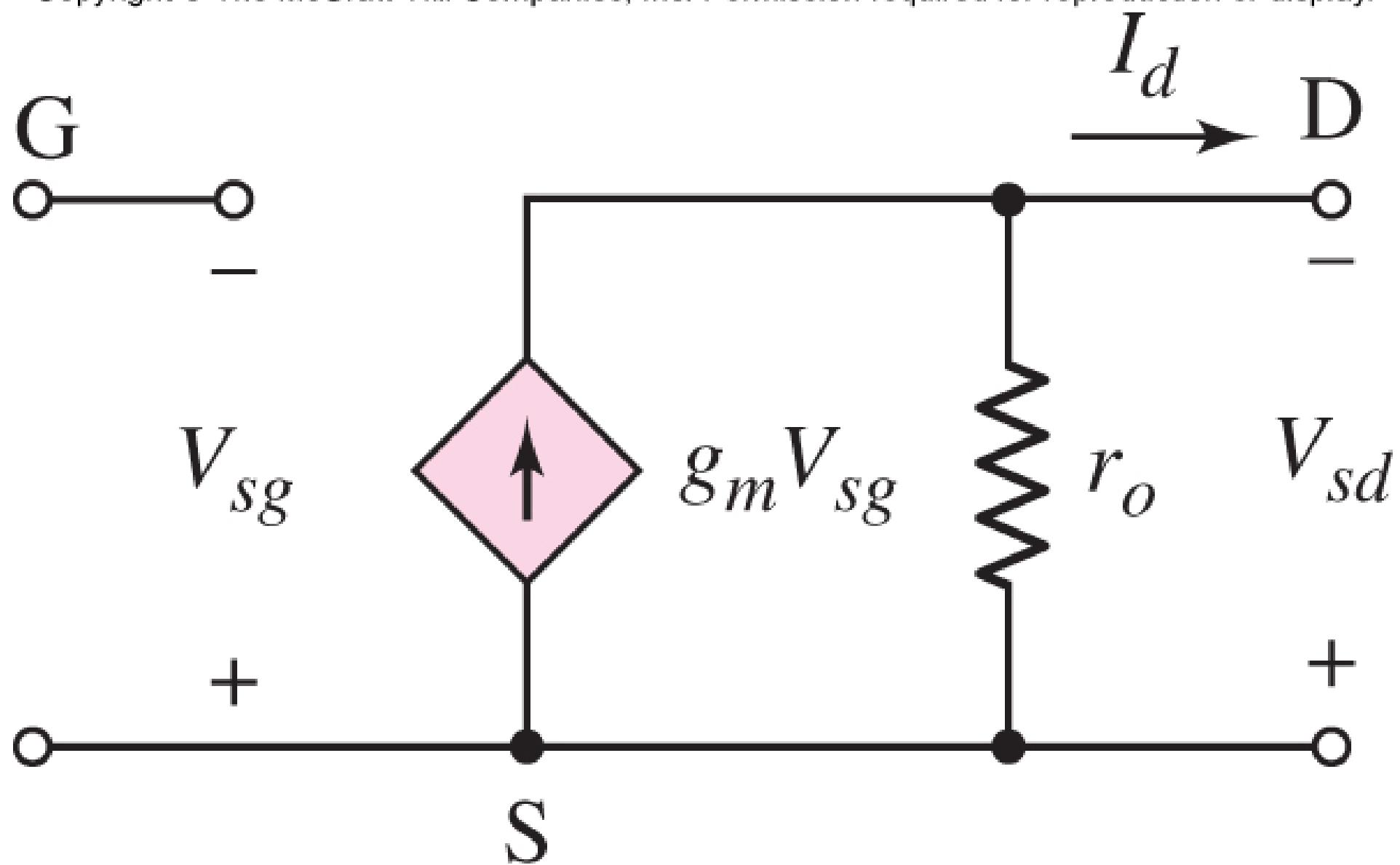


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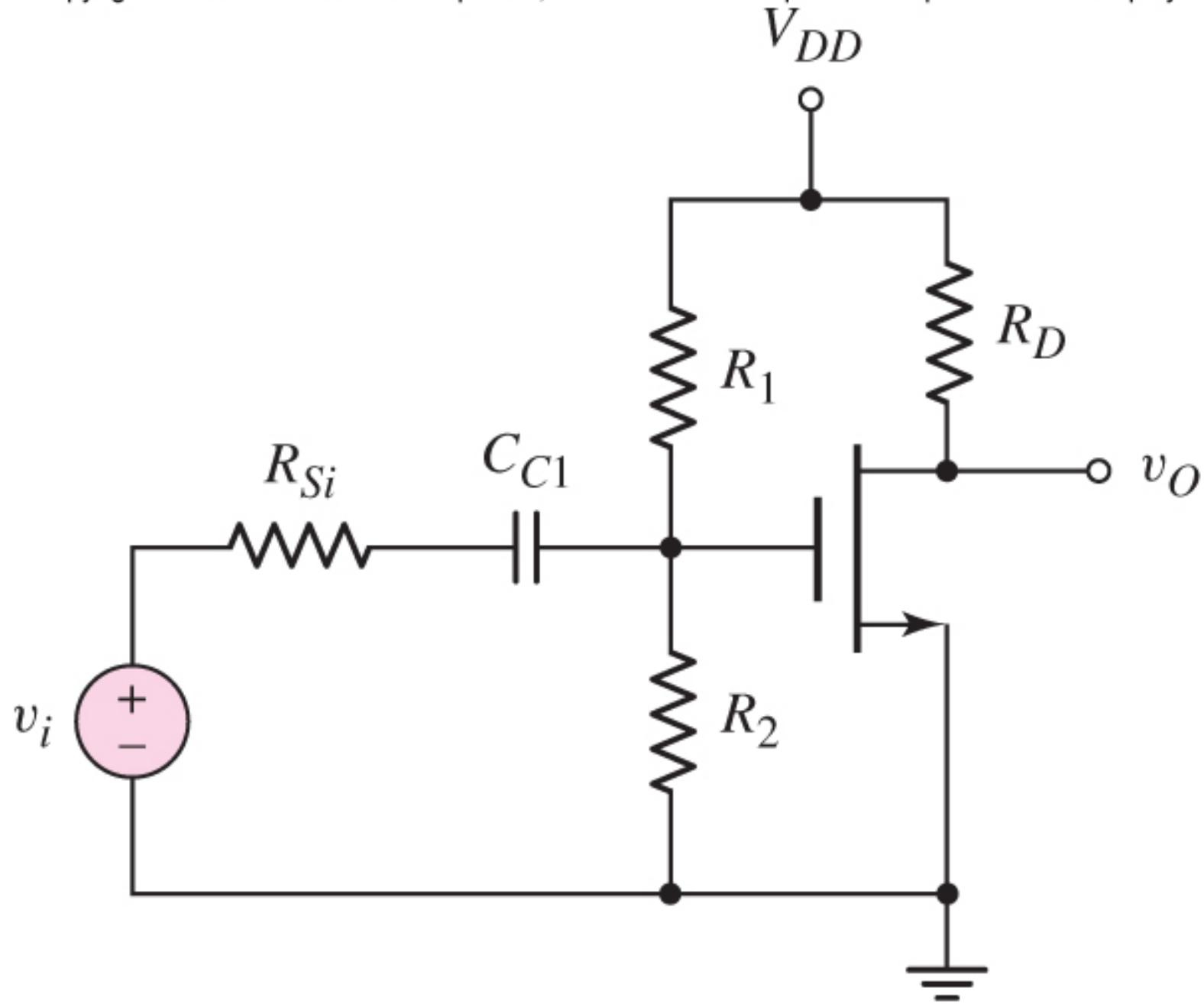


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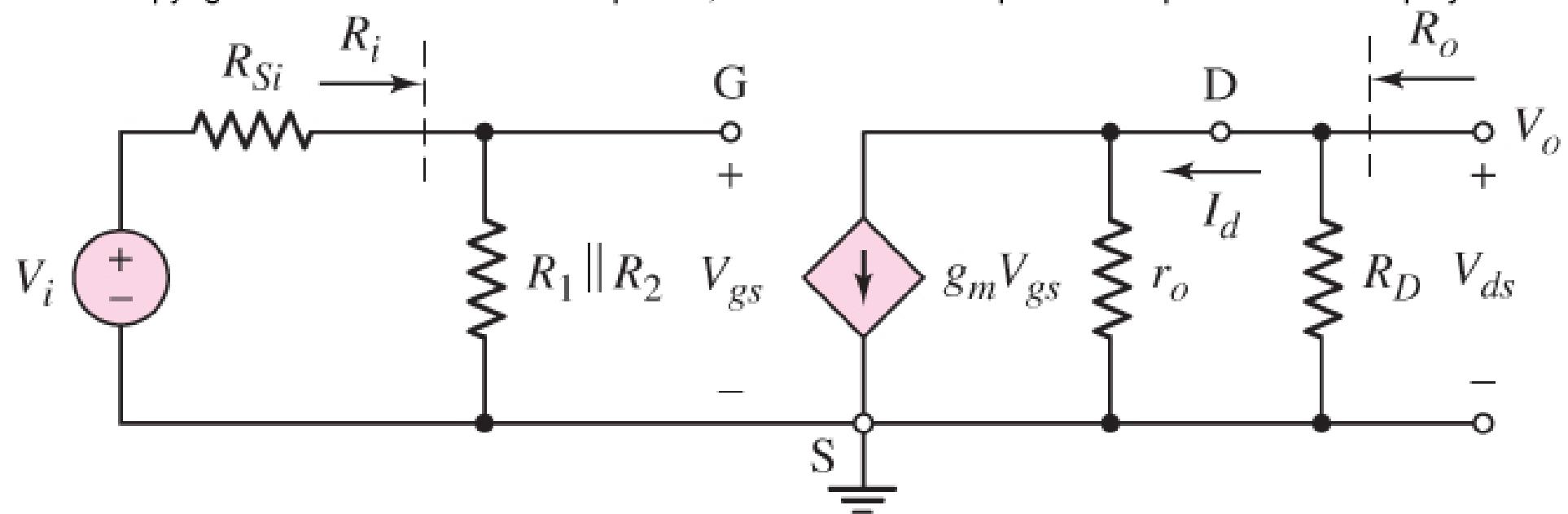


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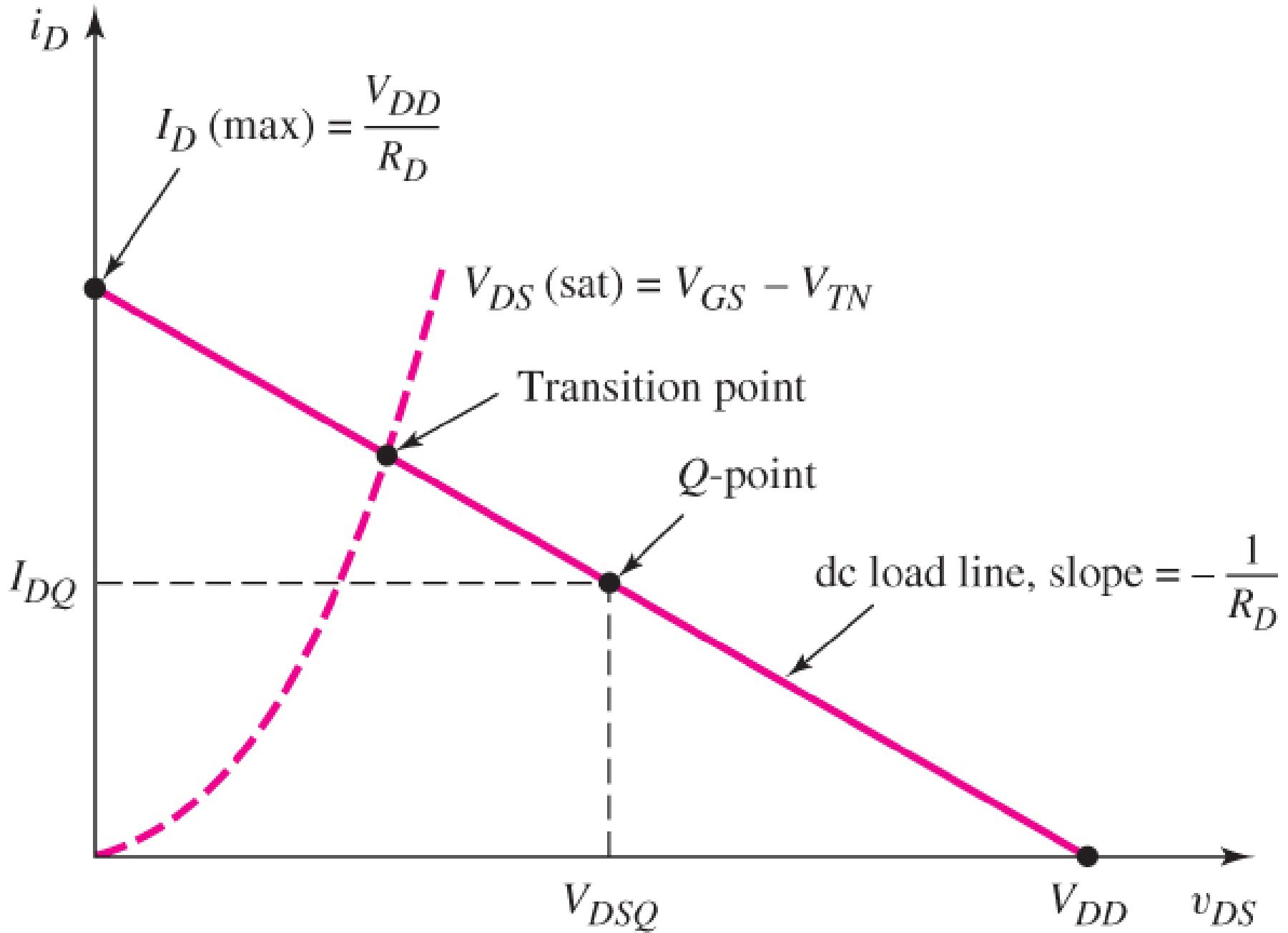


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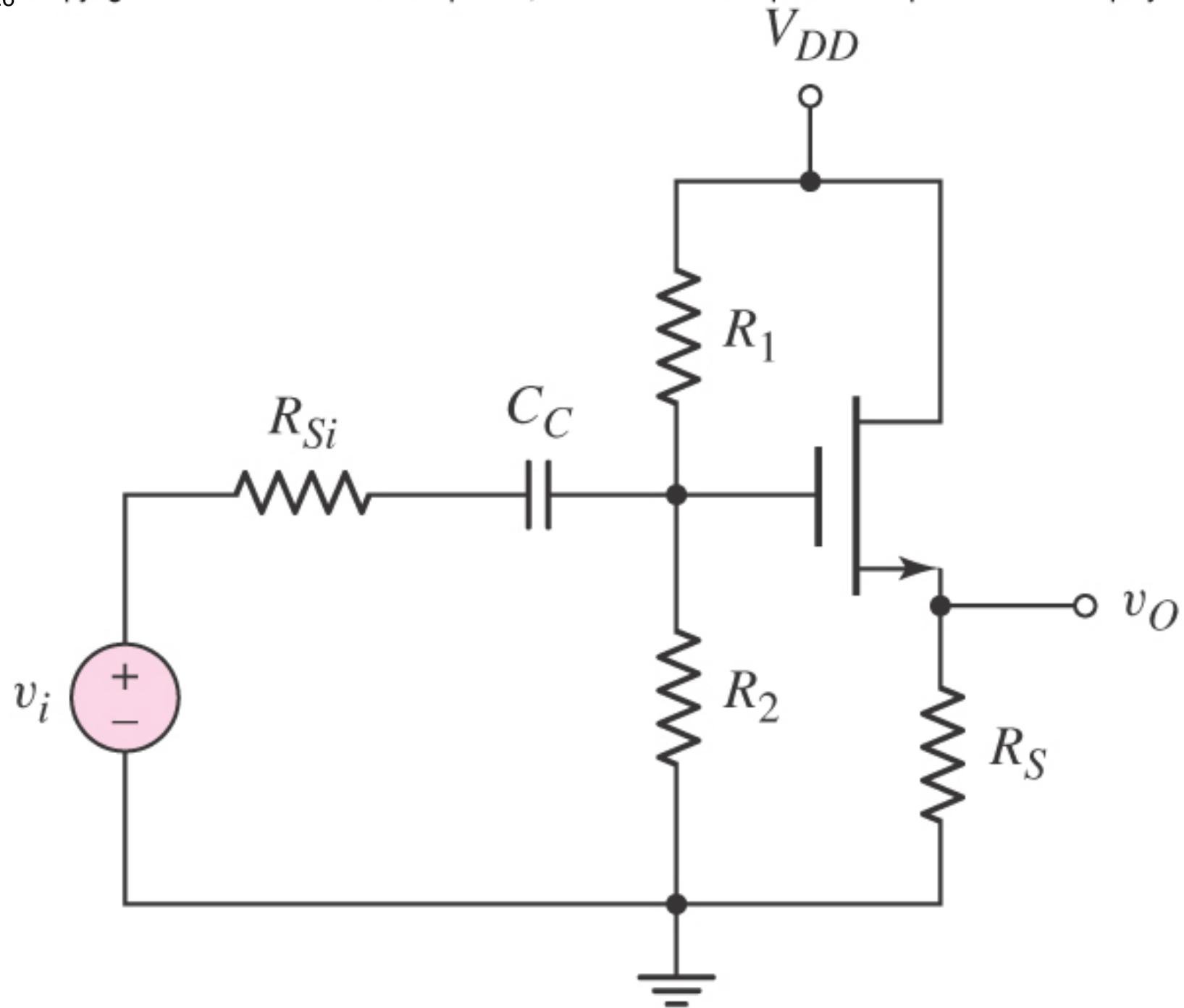
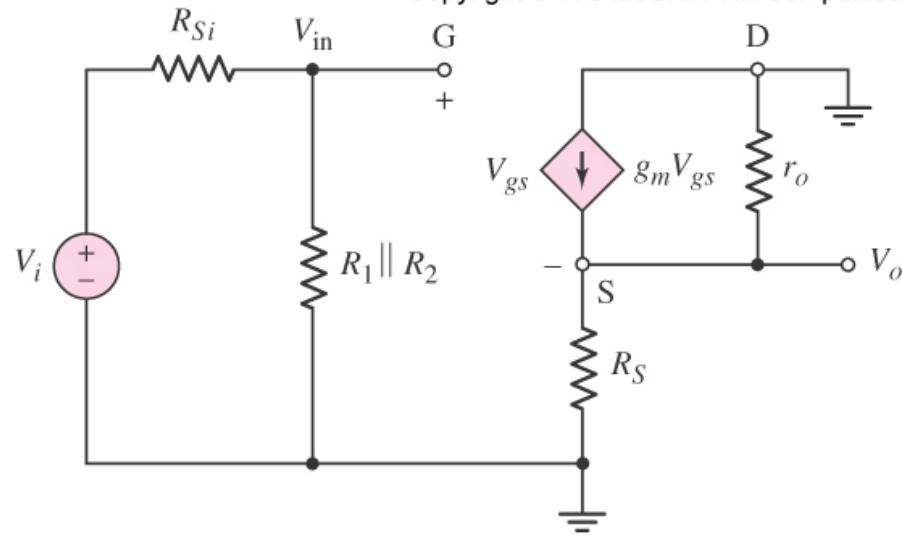
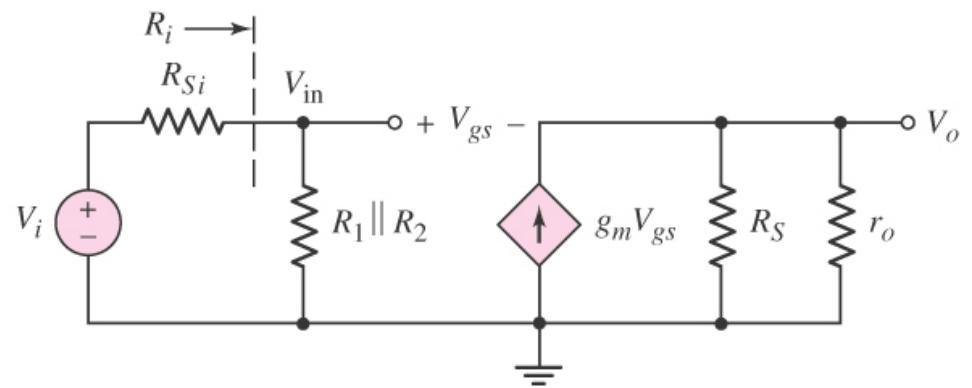


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(a)



(b)

Fig. 4.32

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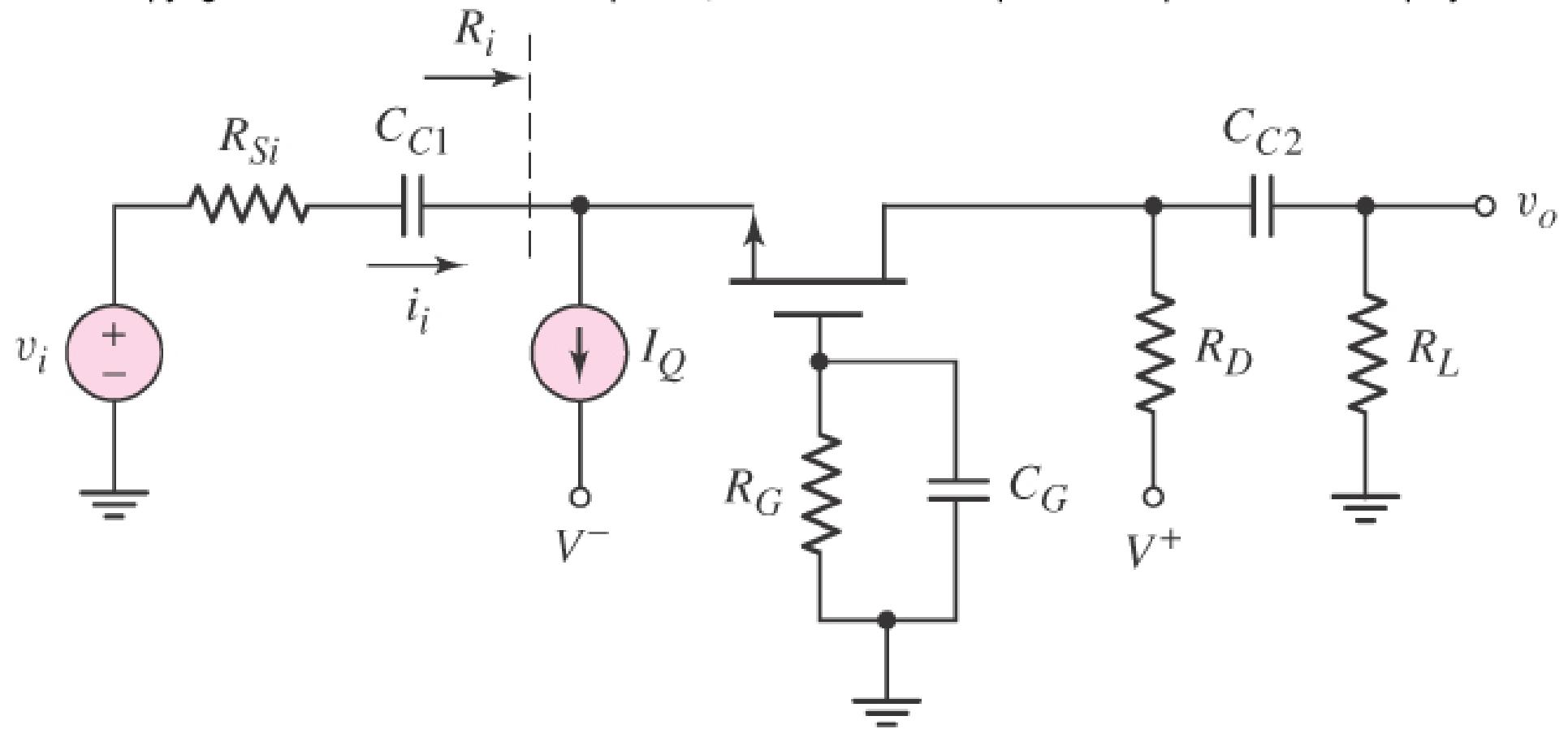


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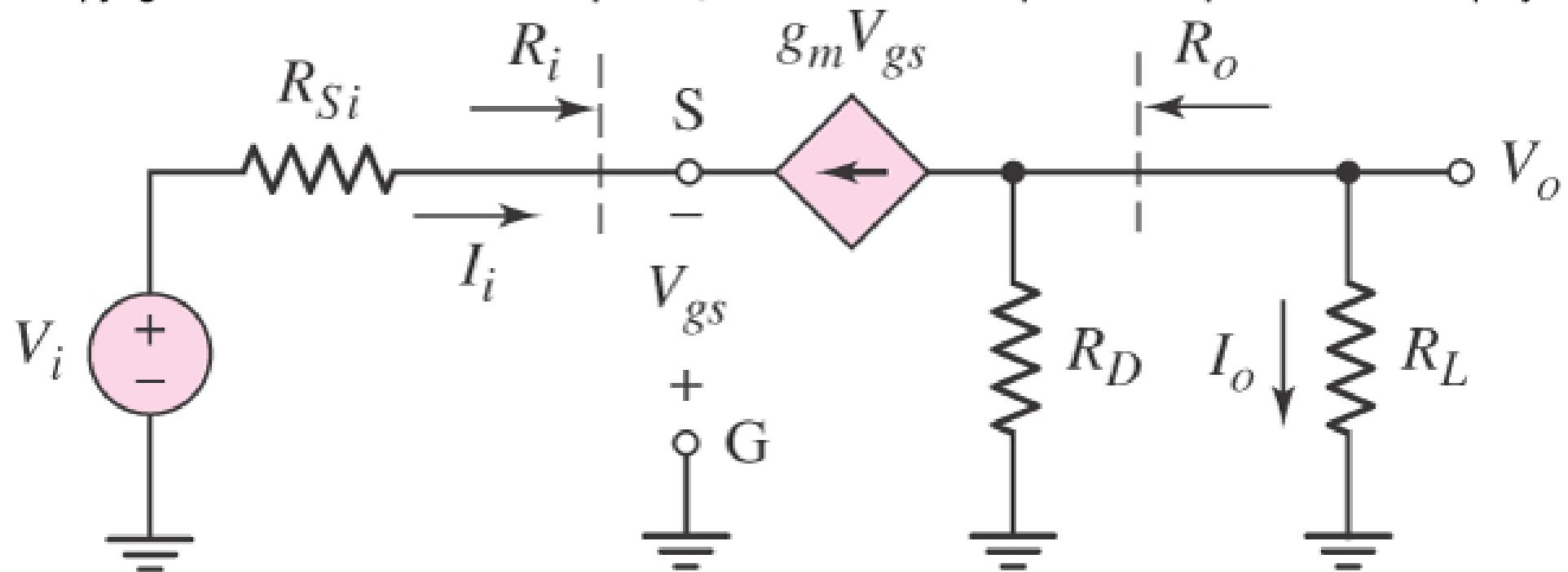


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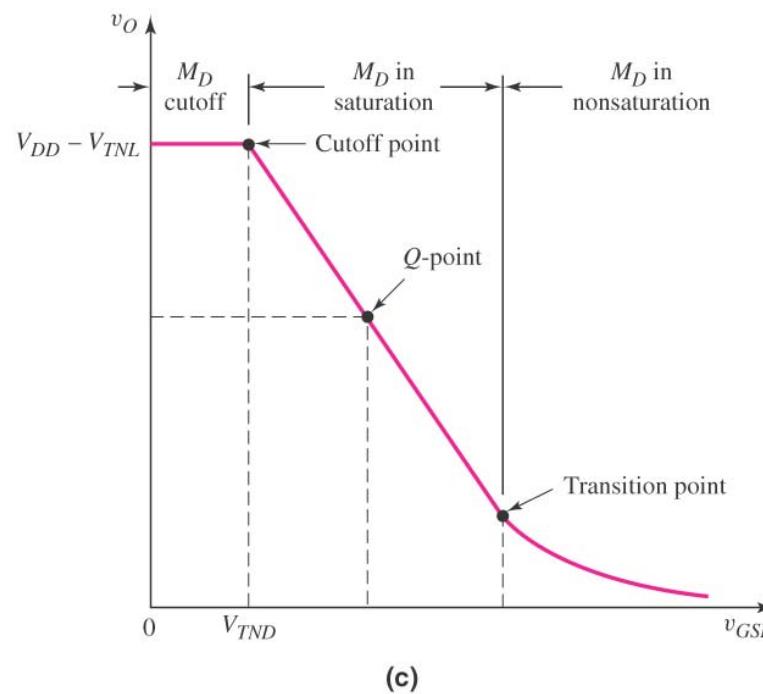
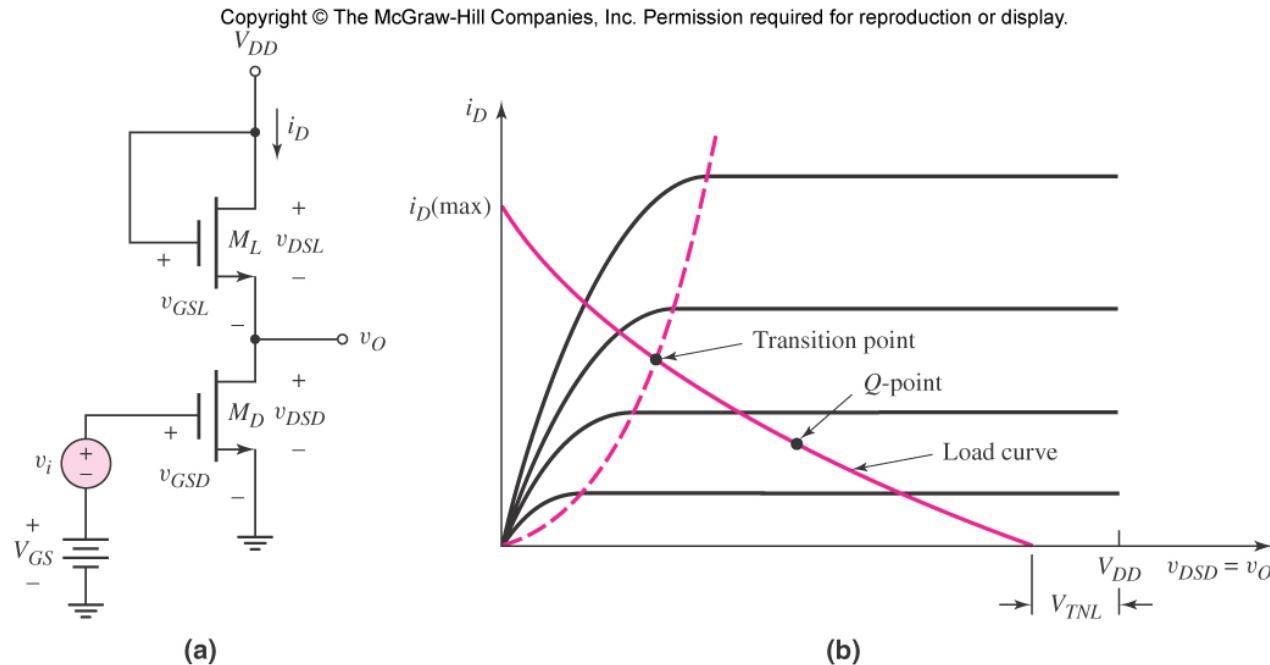


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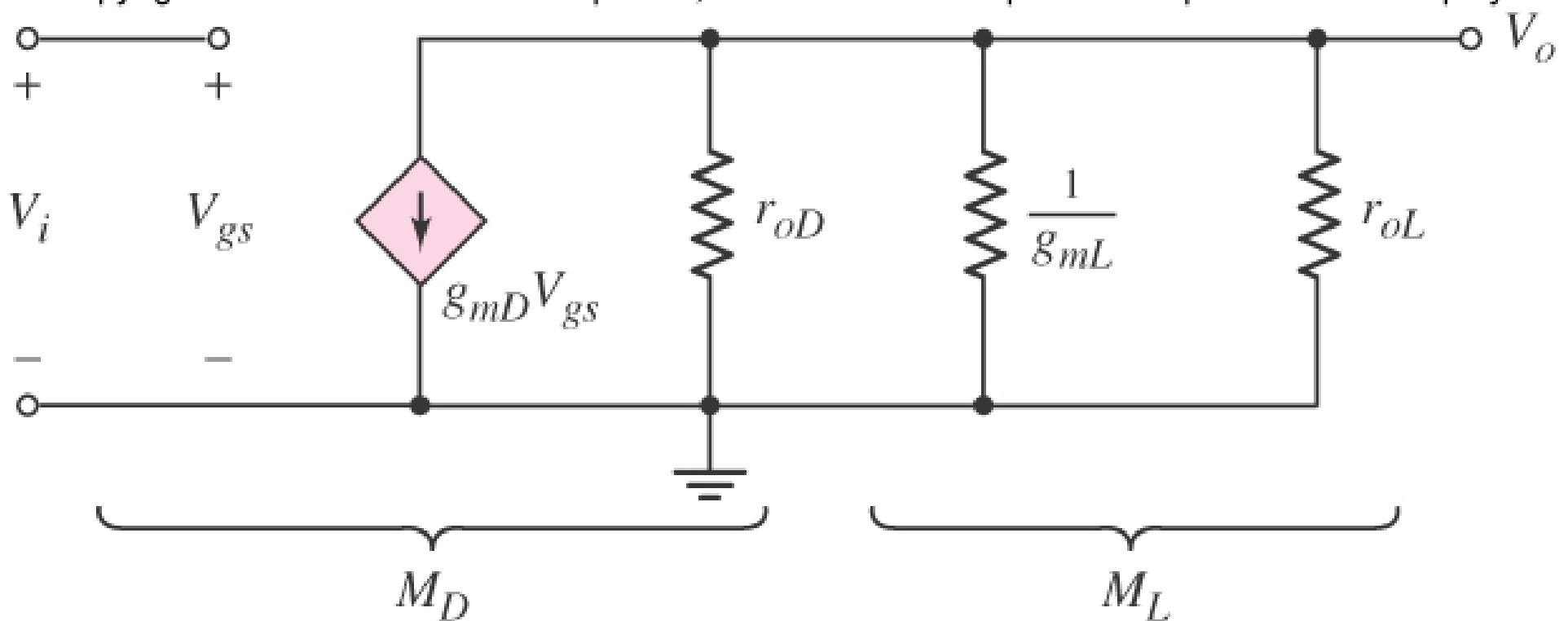


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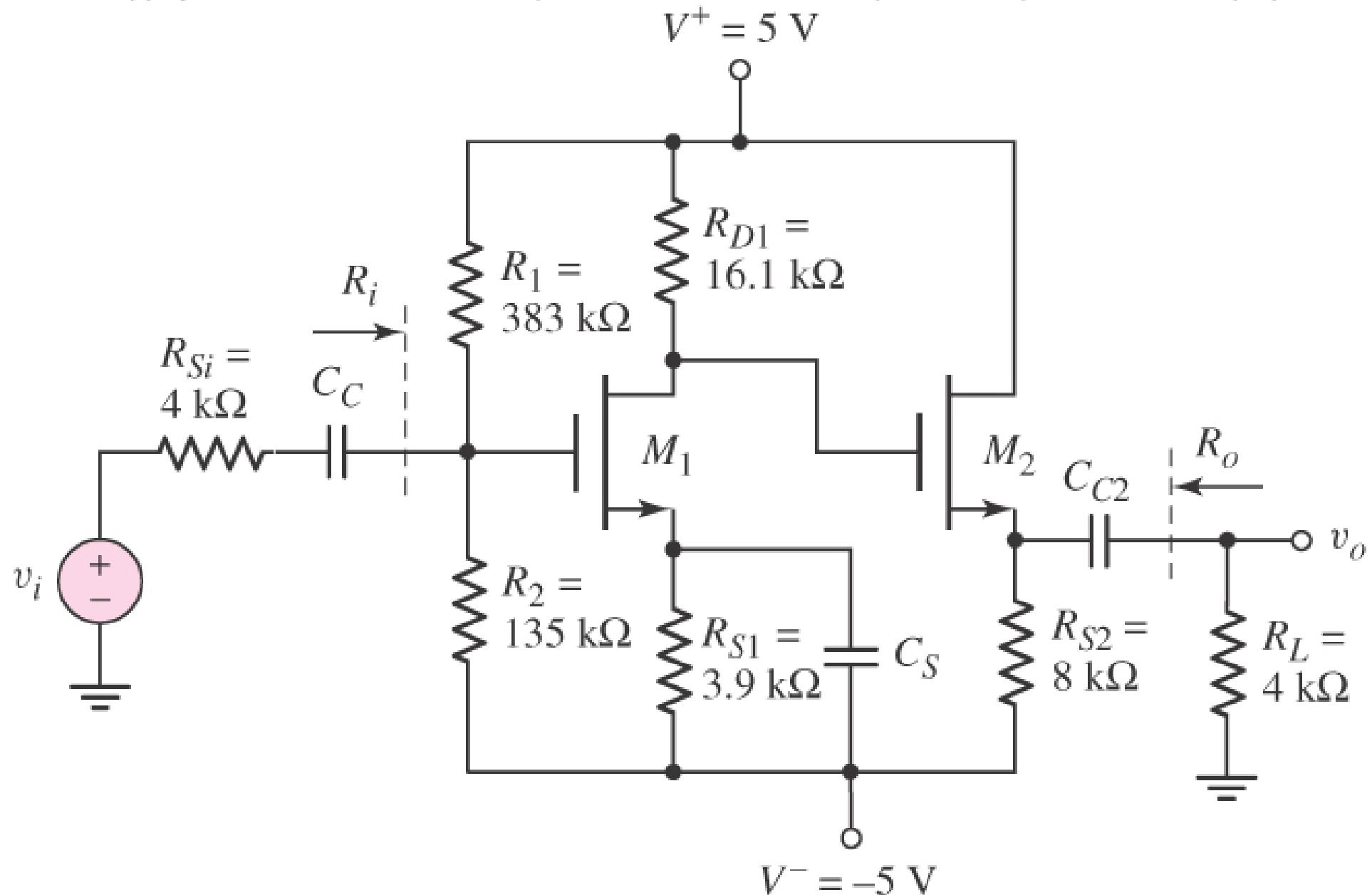


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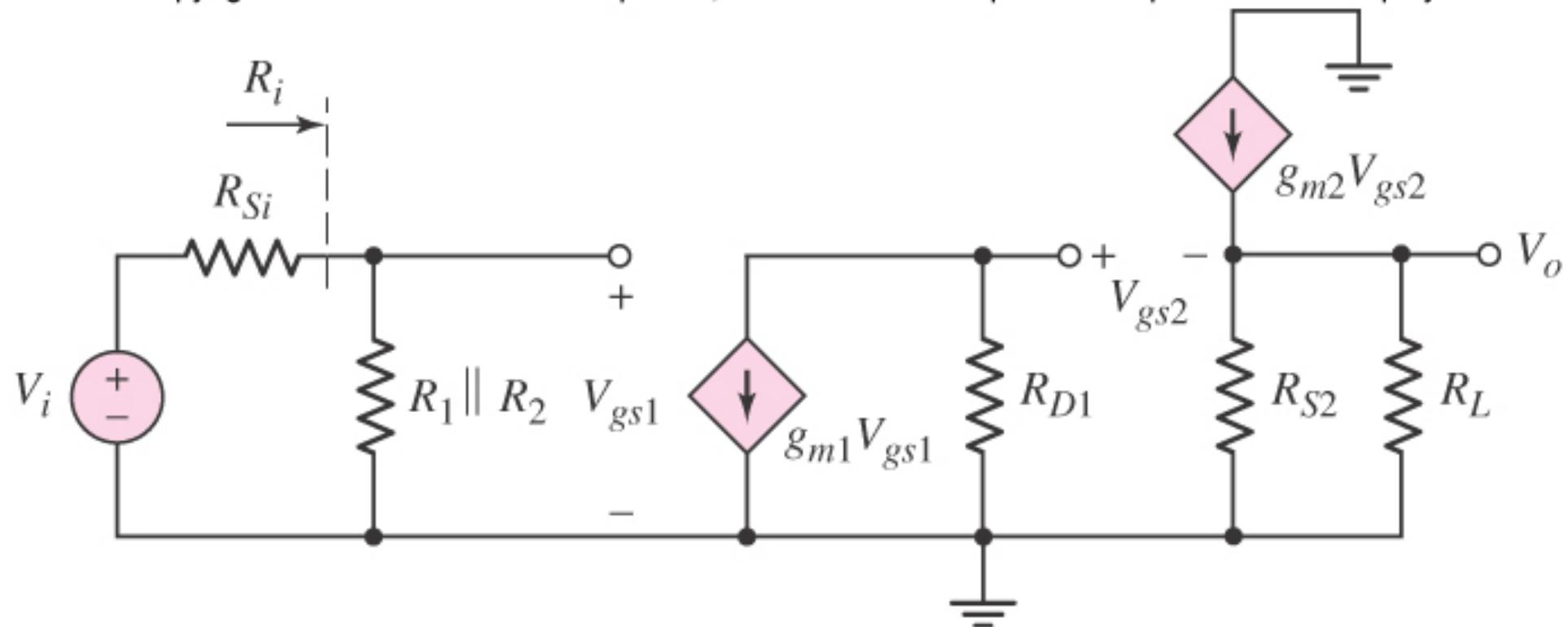


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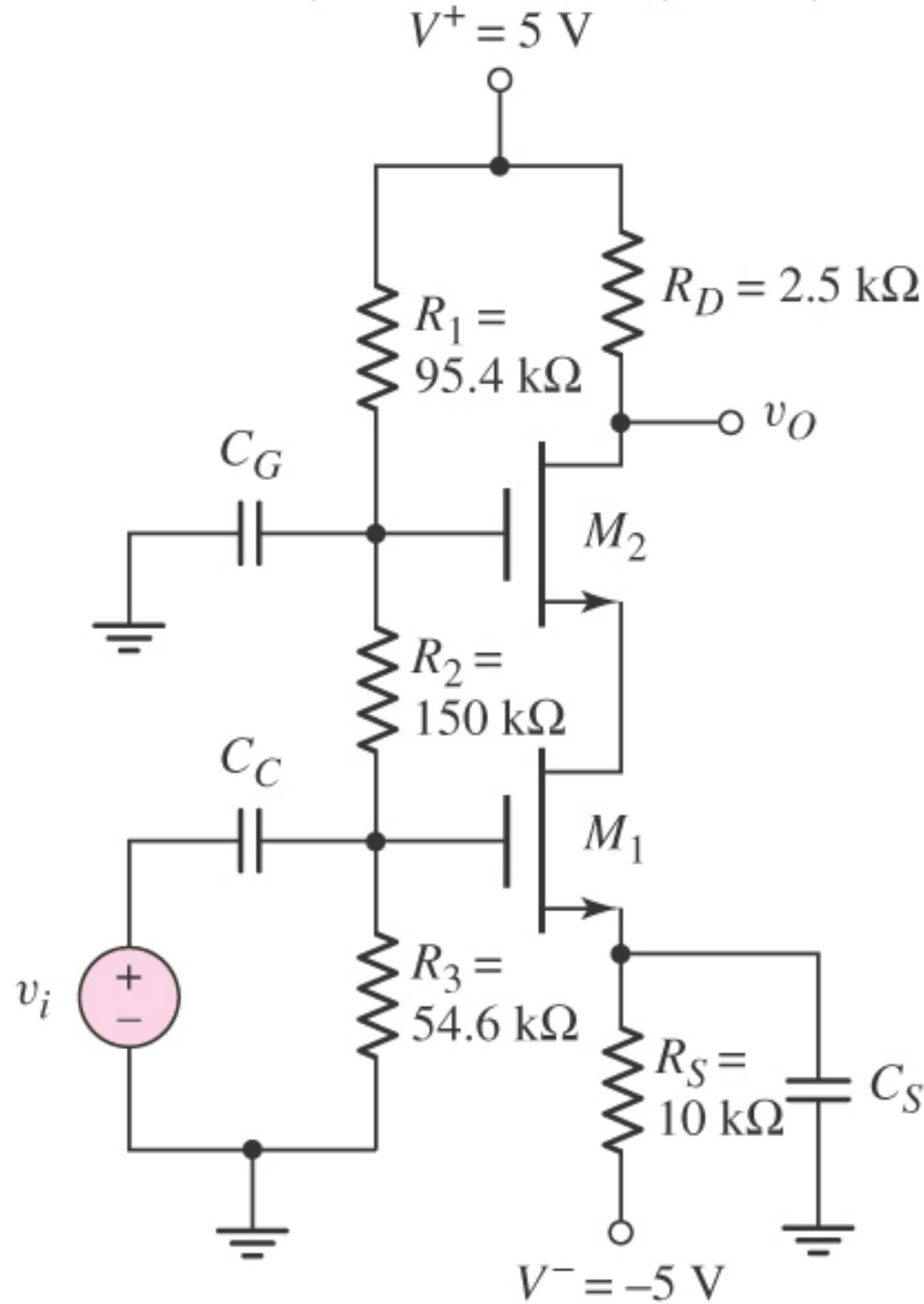
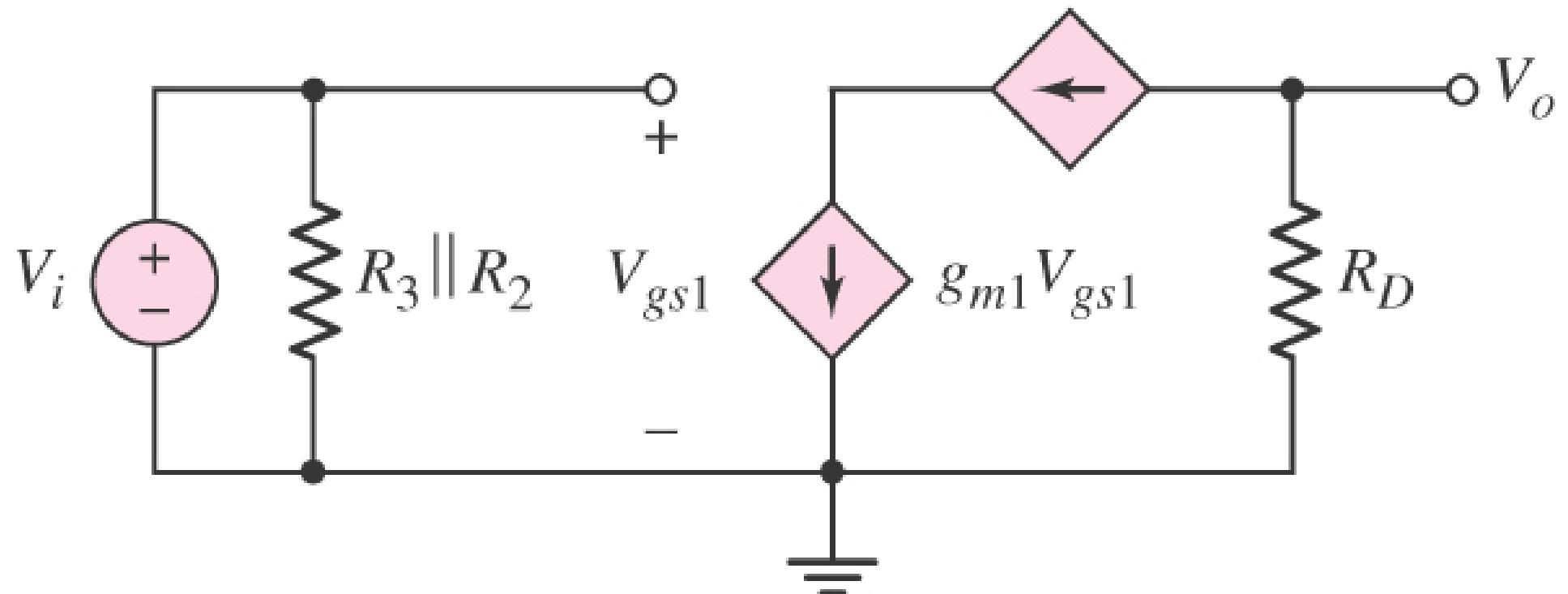


Fig. 4.52

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$$g_{m2}V_{gs2} = g_{m1}V_{gs1}$$

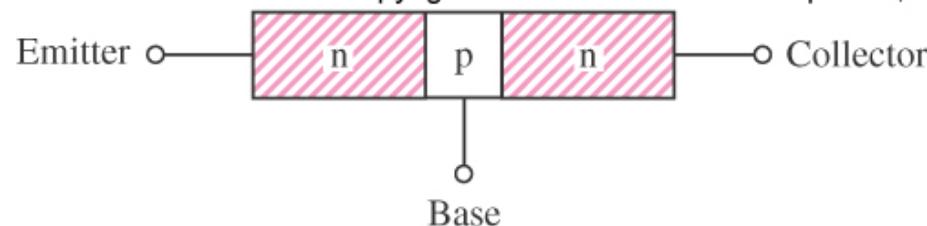


# **BJTs Review**

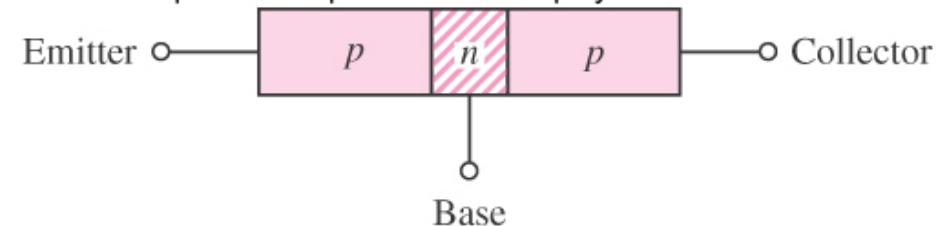
## **(Chapter 5 and 6)**

Fig. 5.1

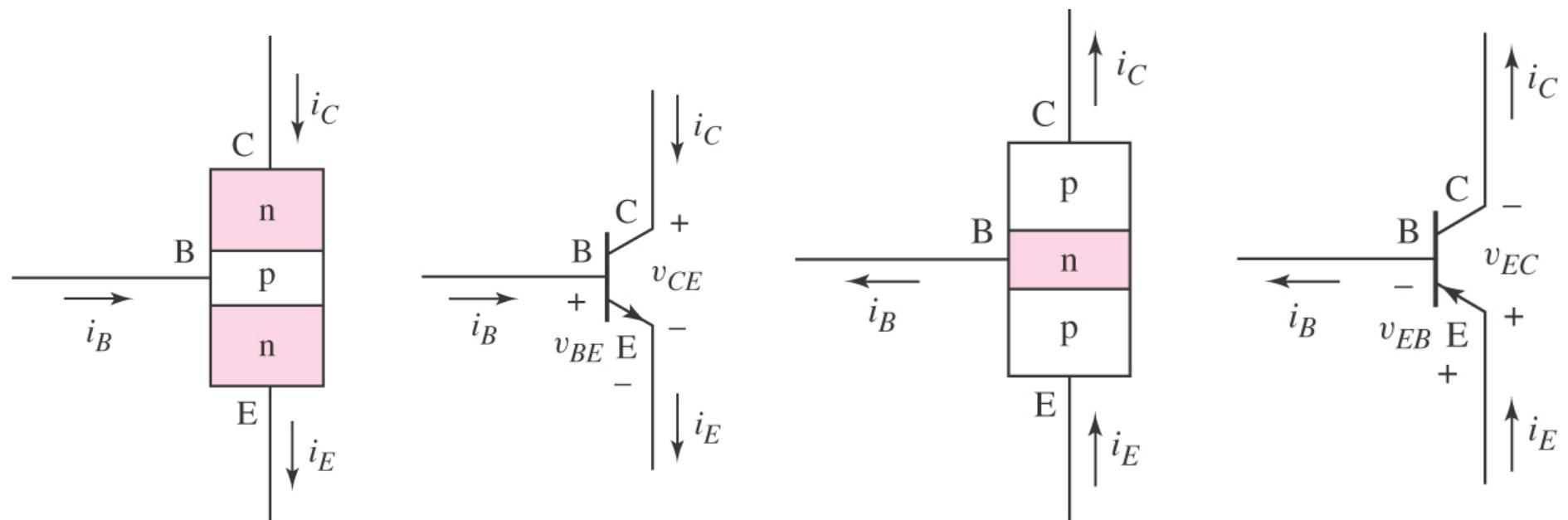
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(a)



(b)



**Table 5.1****Summary of the bipolar current–voltage relationships in the active region****npn**

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \frac{I_S}{\alpha} e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$

**pnp**

$$i_C = I_S e^{v_{EB}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \frac{I_S}{\alpha} e^{v_{EB}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{EB}/V_T}$$

**For both transistors**

$$i_E = i_C + i_B$$

$$i_E = (1 + \beta)i_B$$

$$\alpha = \frac{\beta}{1+\beta}$$

$$i_C = \beta i_B$$

$$i_C = \alpha i_E = \left(\frac{\beta}{1+\beta}\right) i_E$$

$$\beta = \frac{\alpha}{1-\alpha}$$

Fig. 5.12

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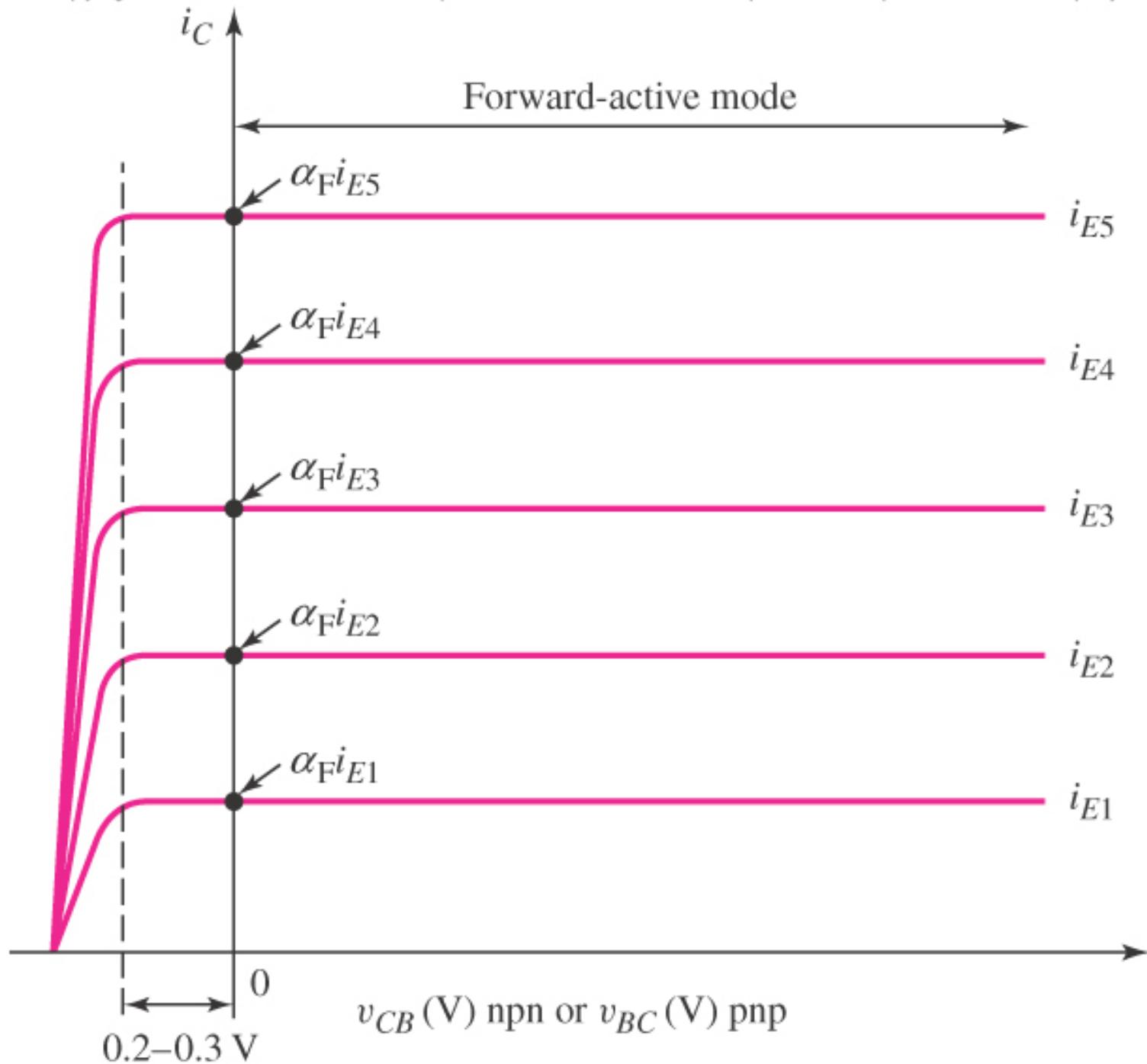


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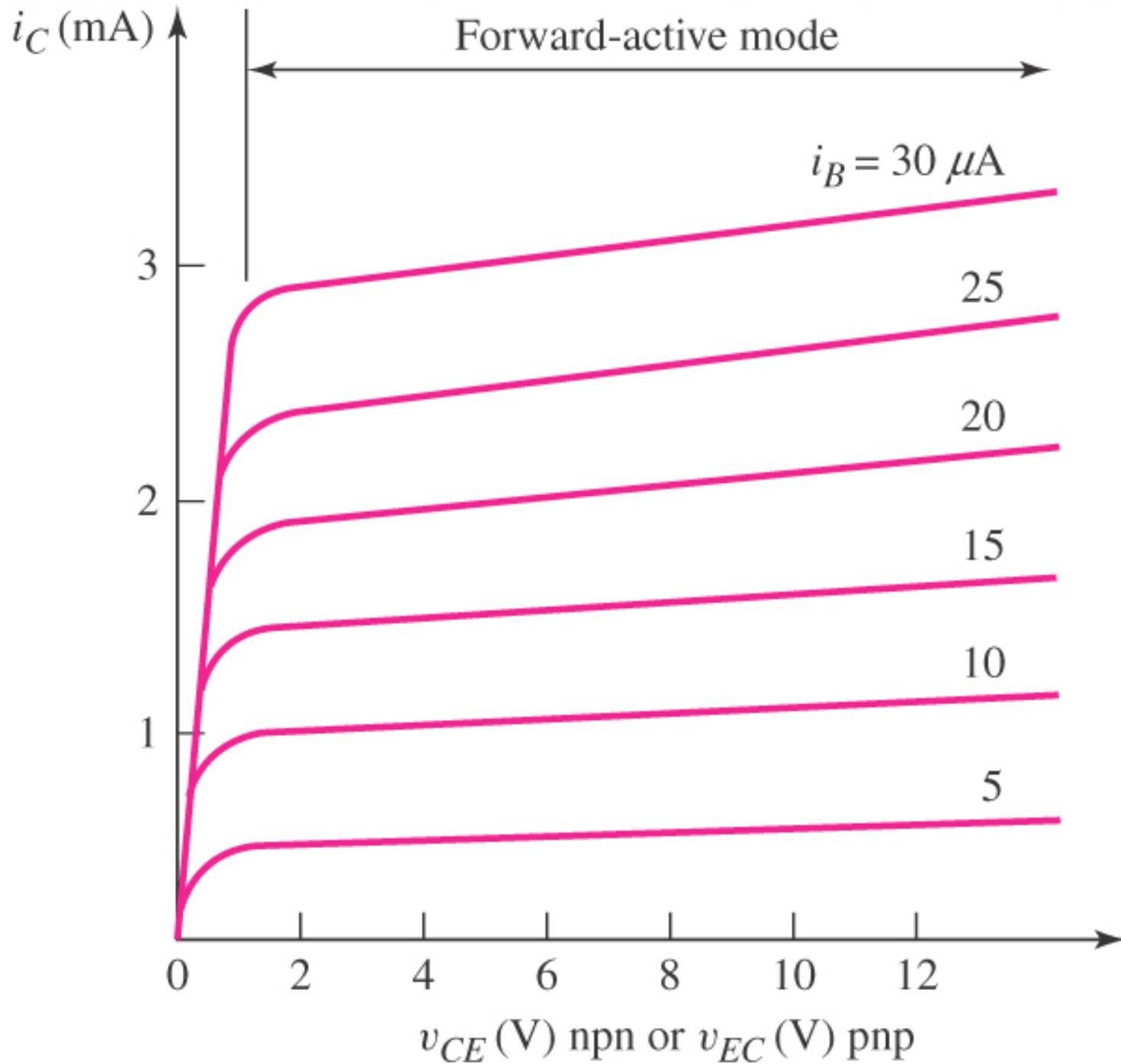


Fig. 5.14

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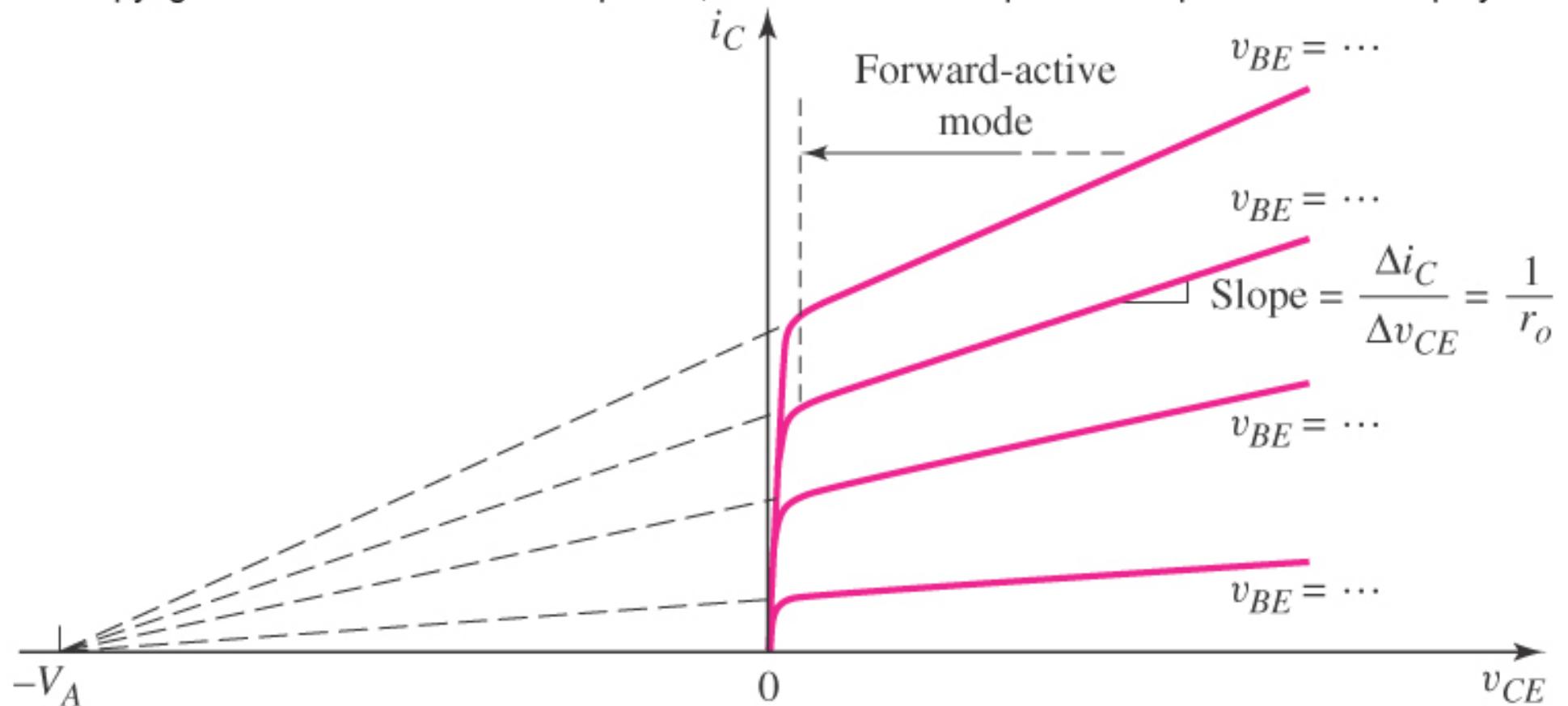


Fig. 5.25

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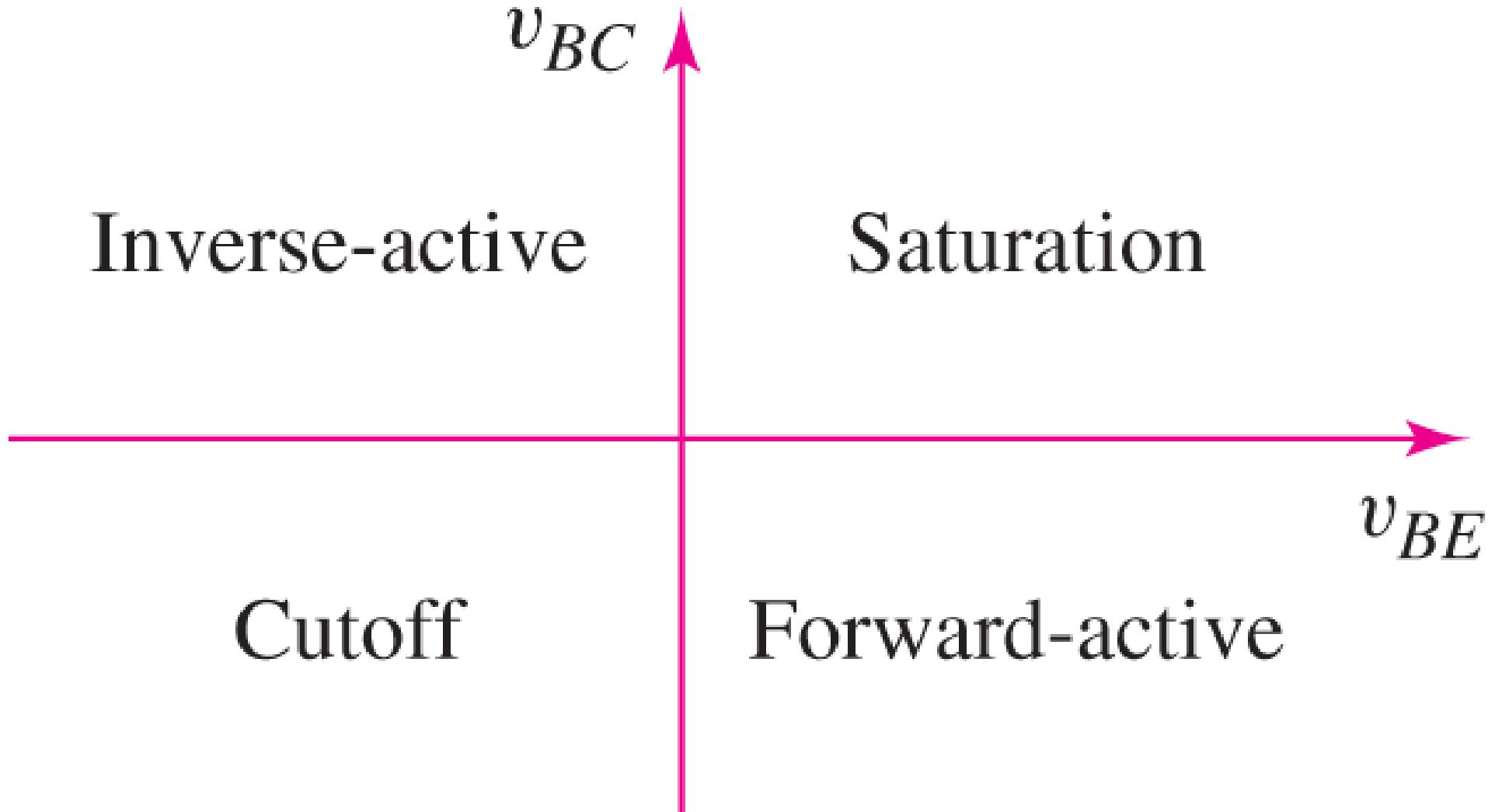
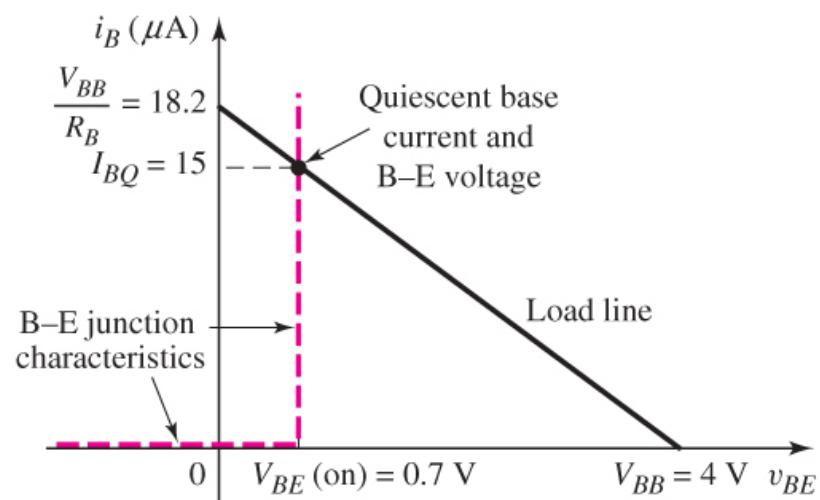
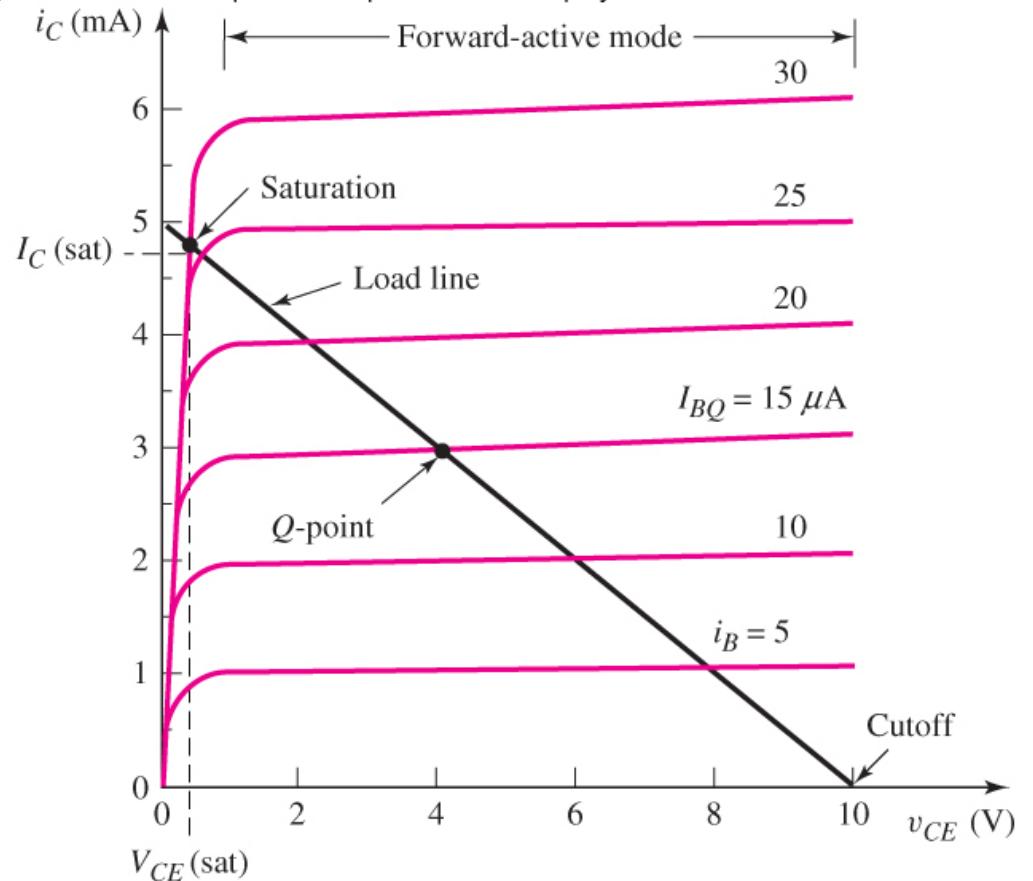


Fig. 5.23

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(a)



(b)

Fig. 5.44

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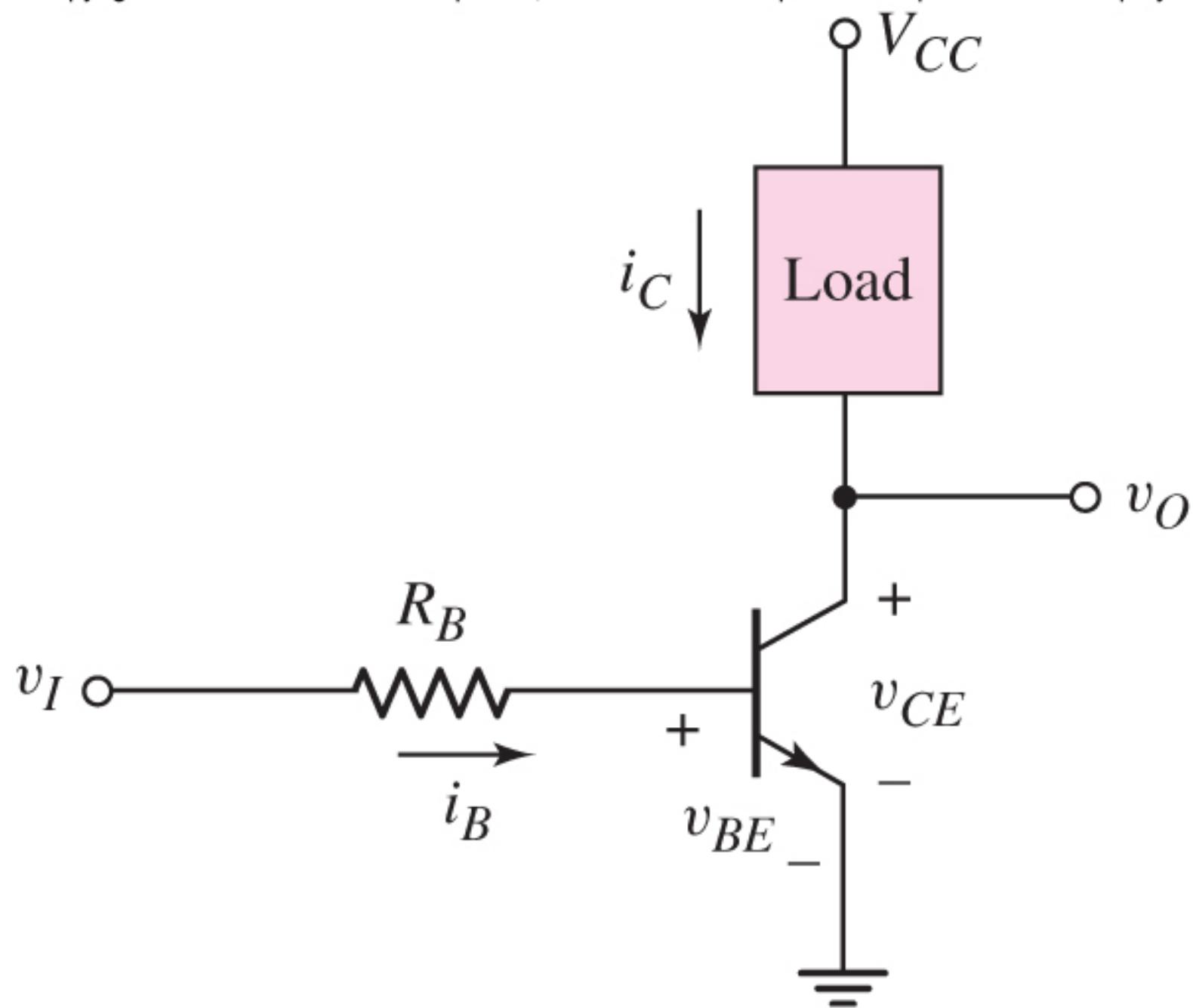


Fig. 5.46

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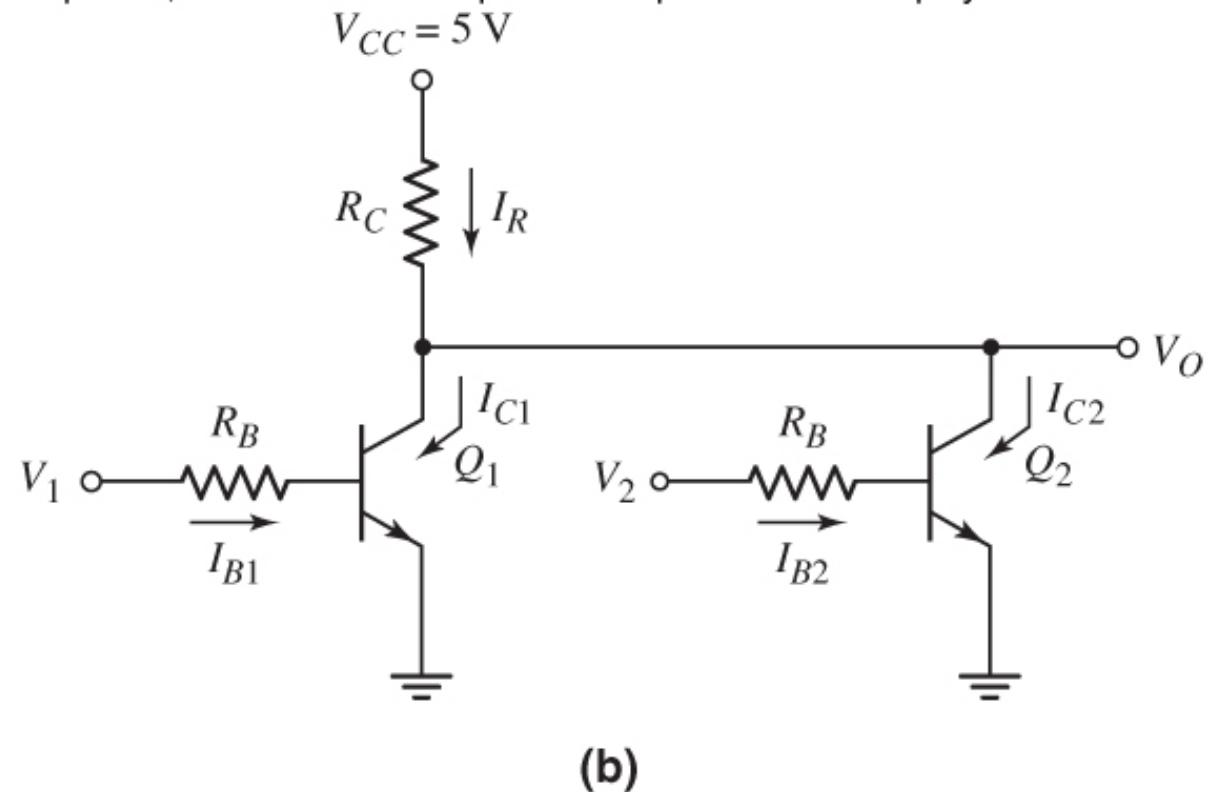
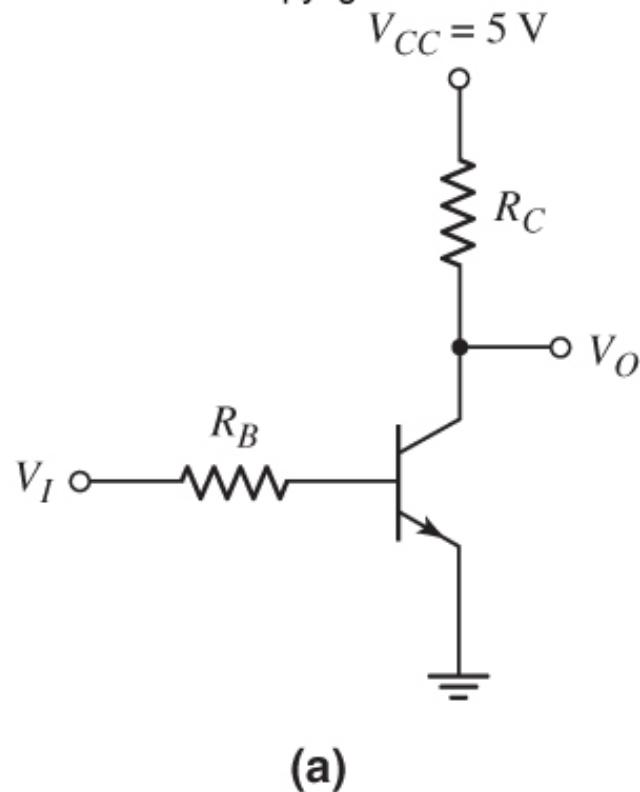
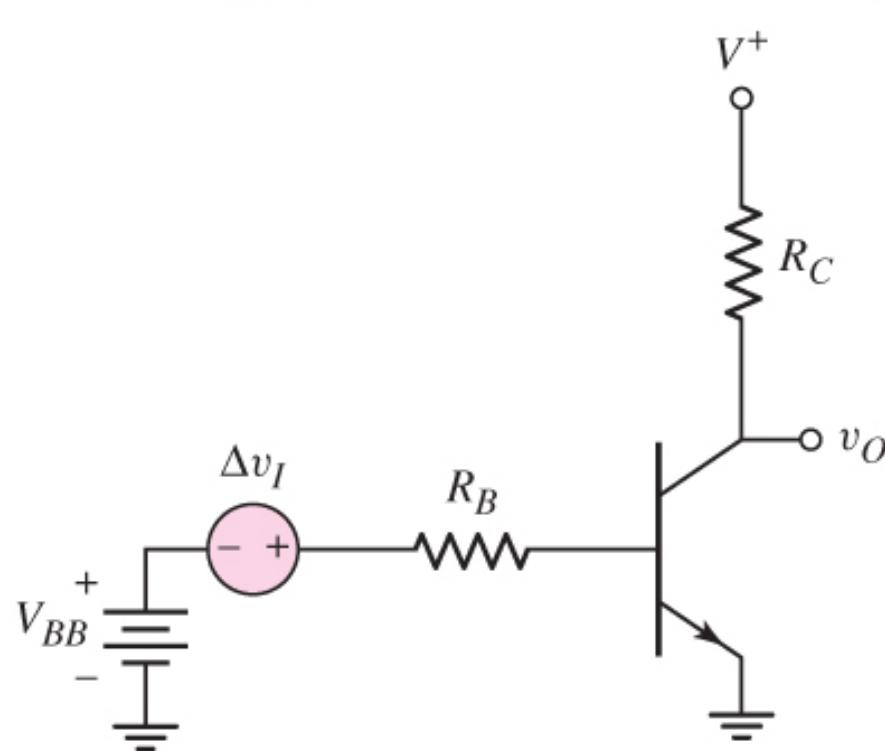
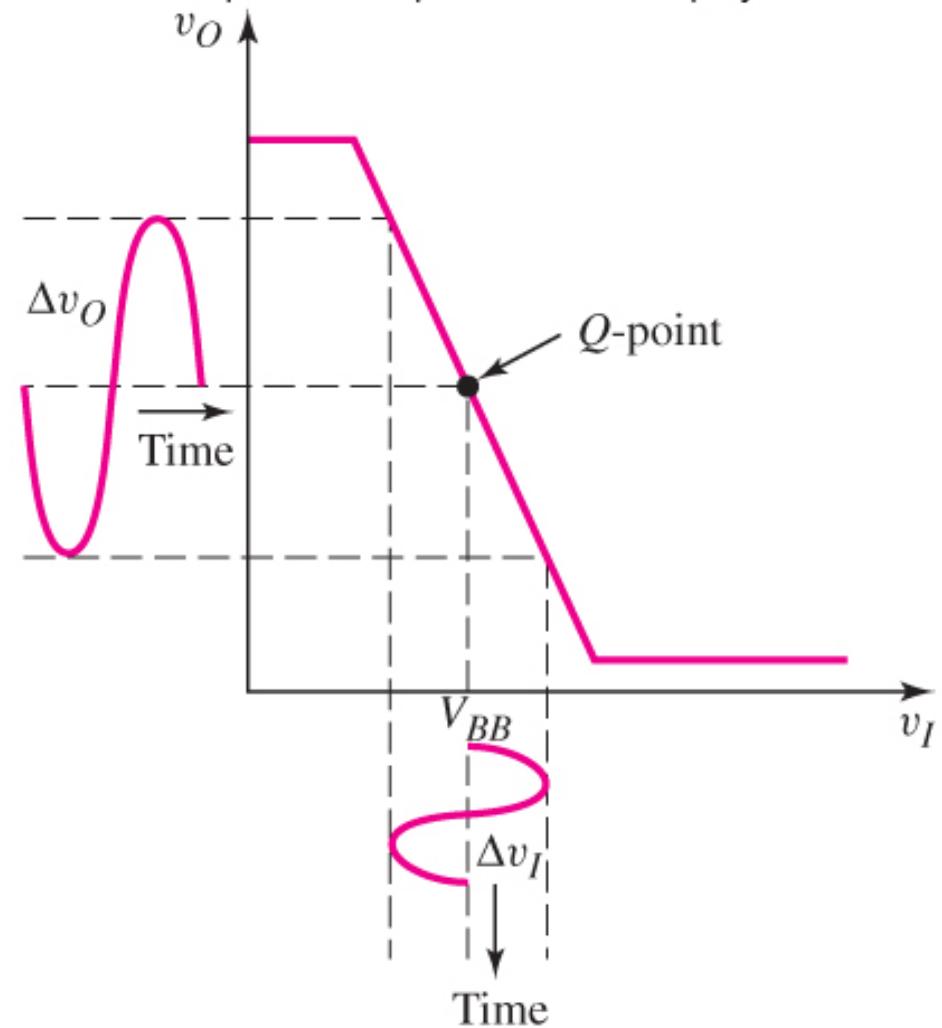


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(a)



(b)

Obtain Voltage Transfer  
Characteristics for a given circuit

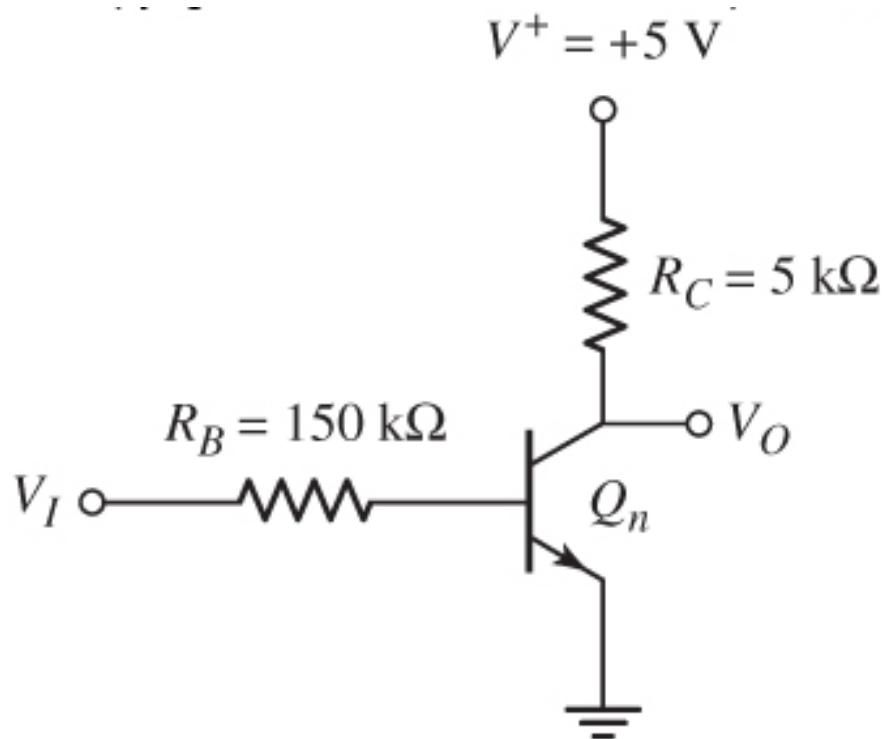


Fig. 5.28

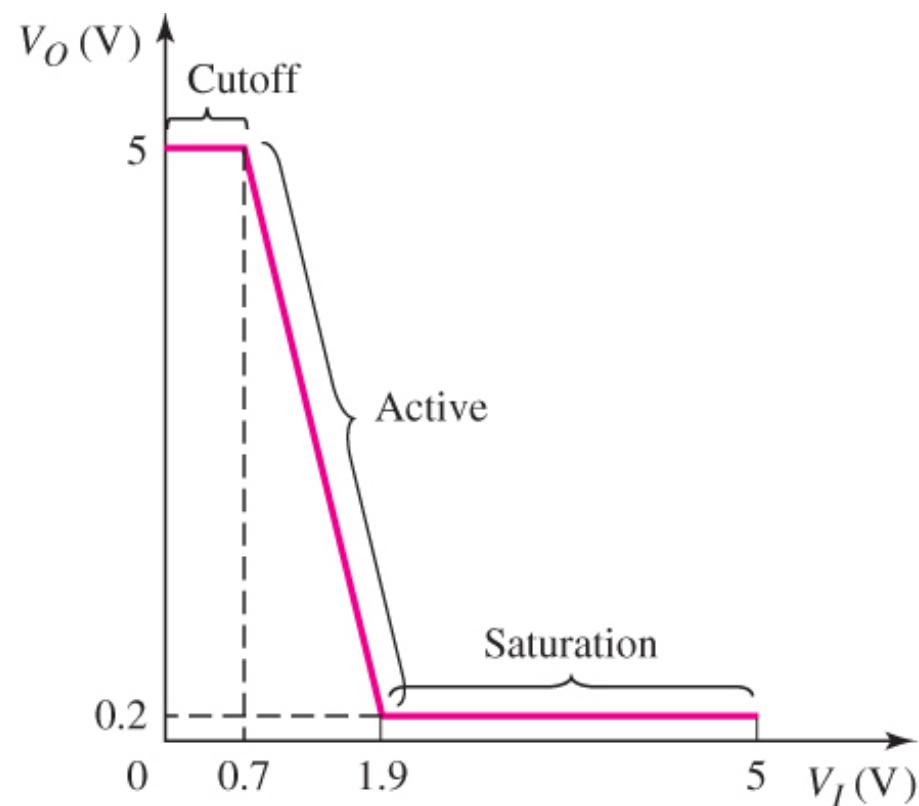
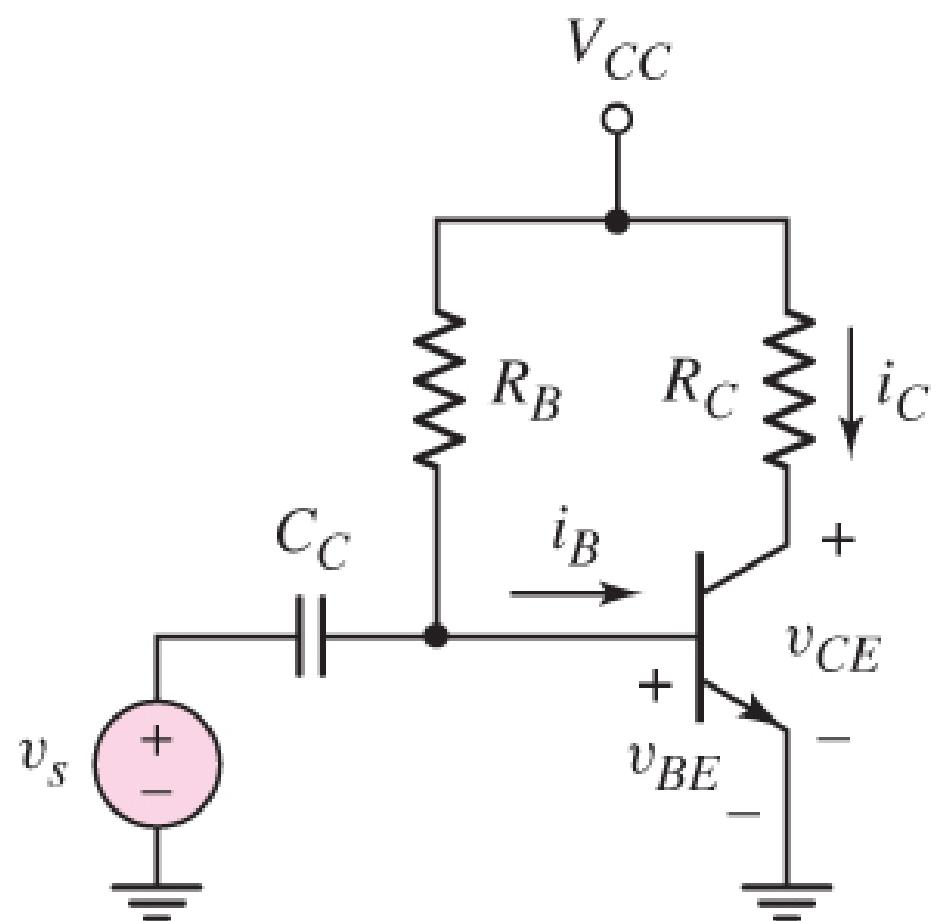
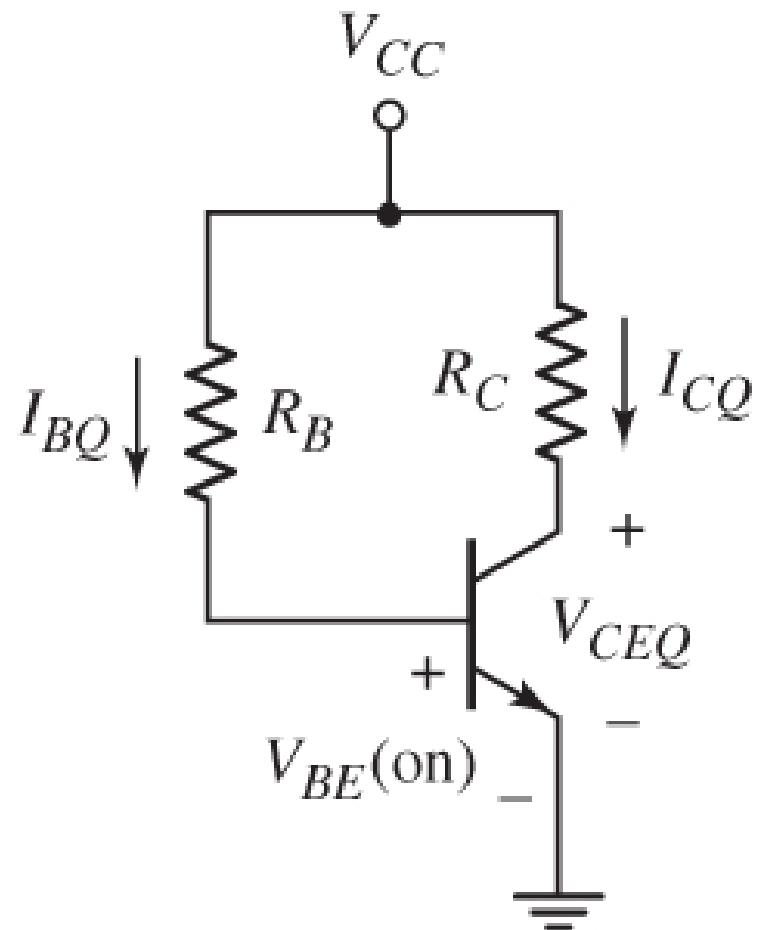


Fig. 5.51

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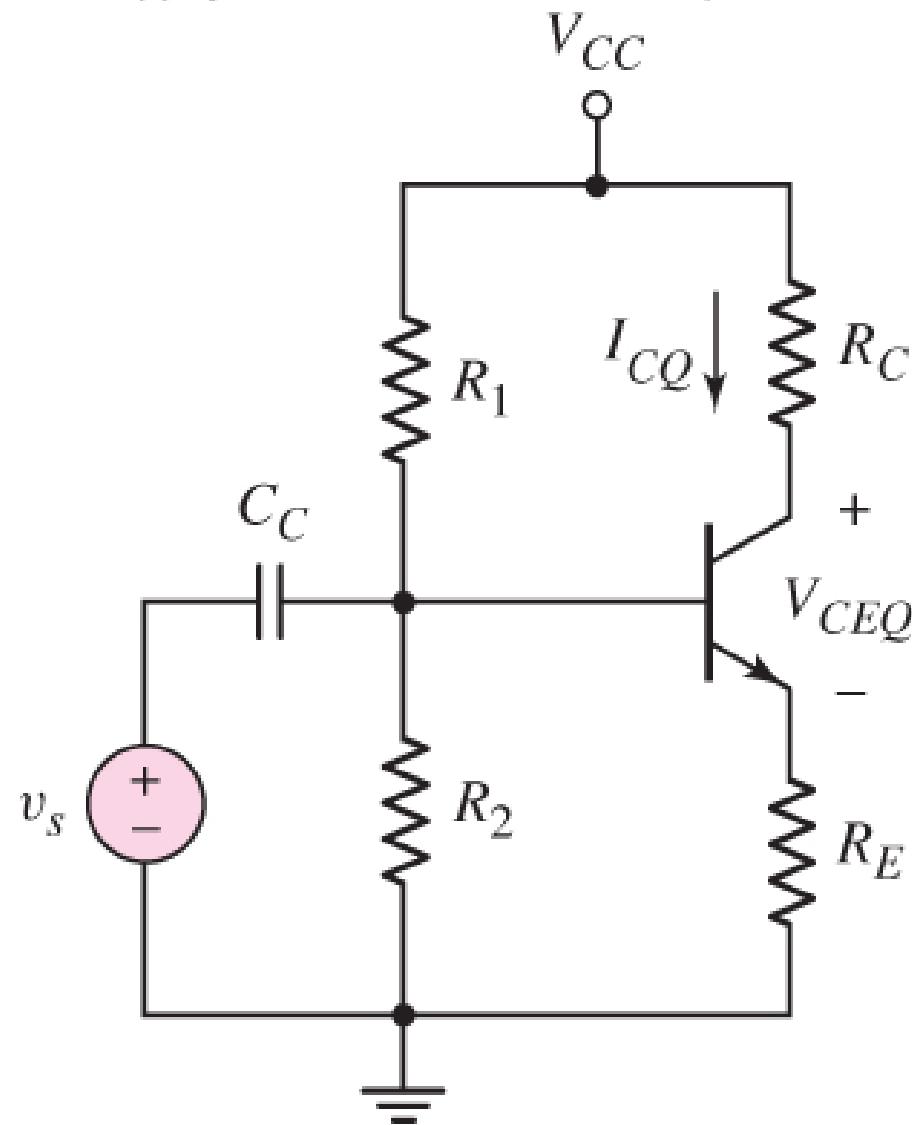
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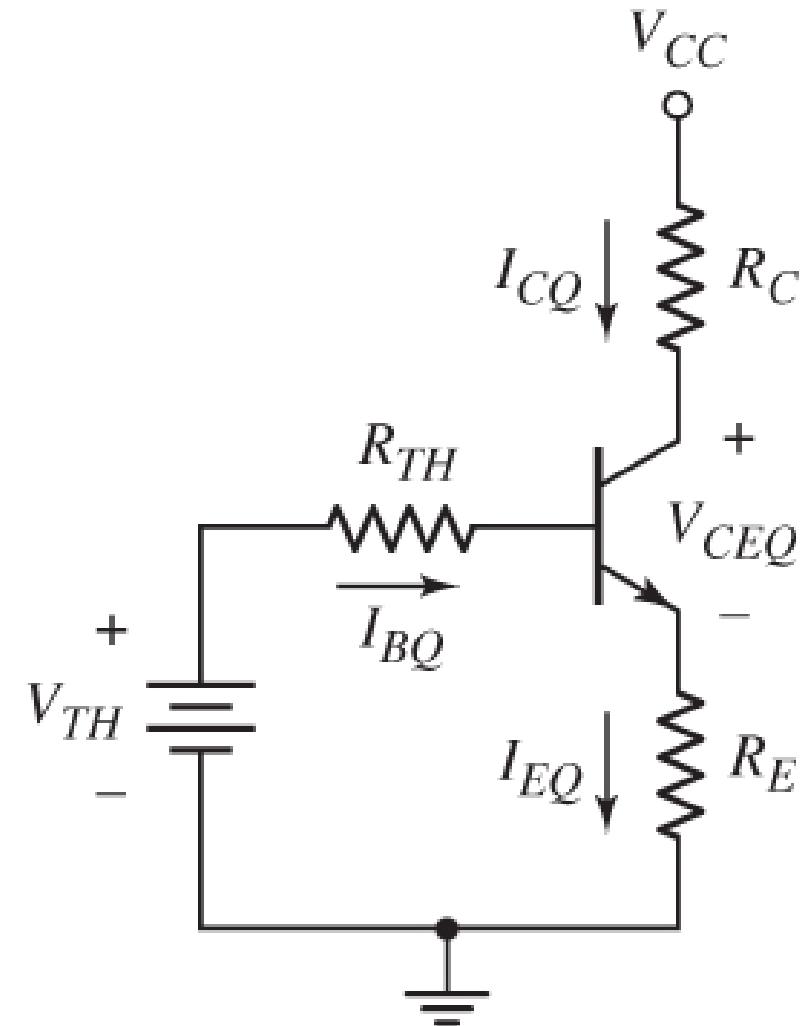
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Fig. 5.54

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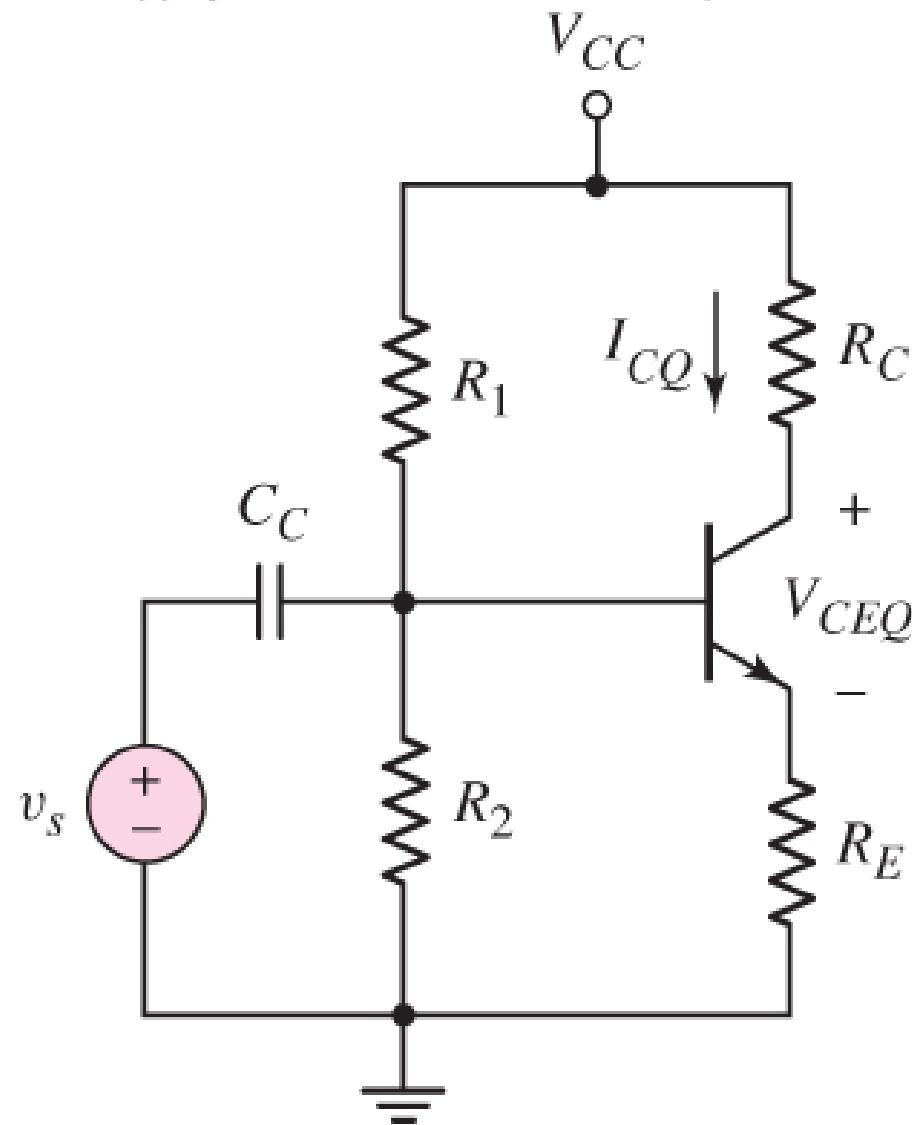
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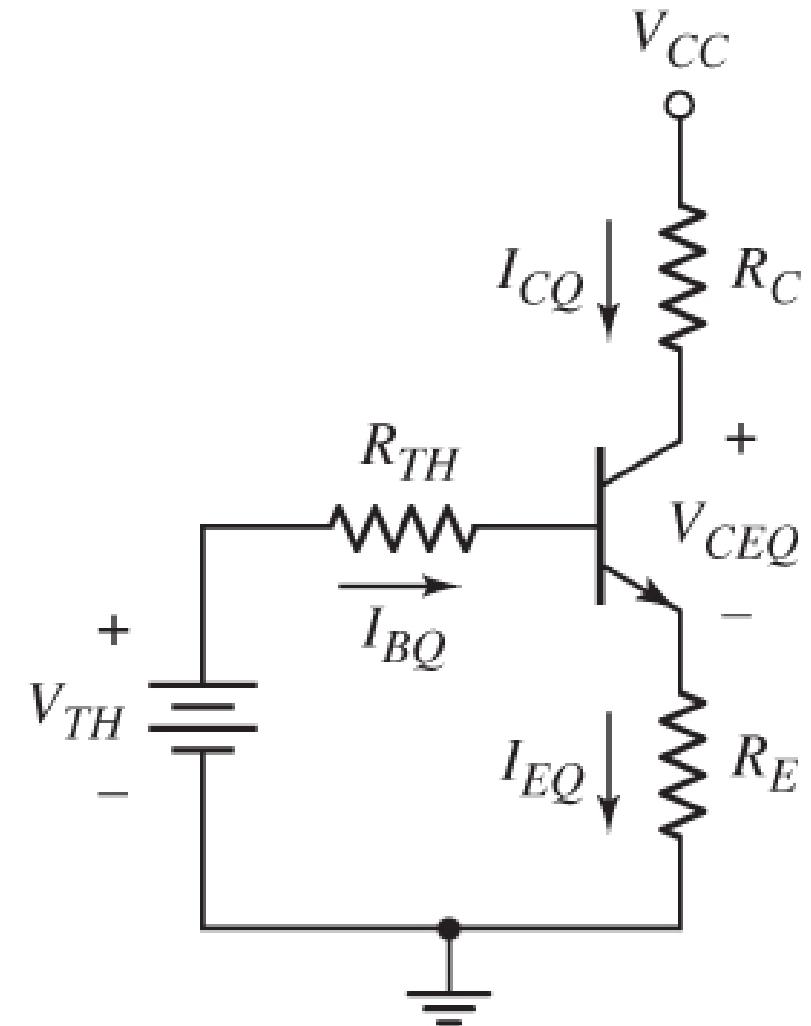
(b)

Fig. 5.54

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(a)



(b)

Fig. 5.60

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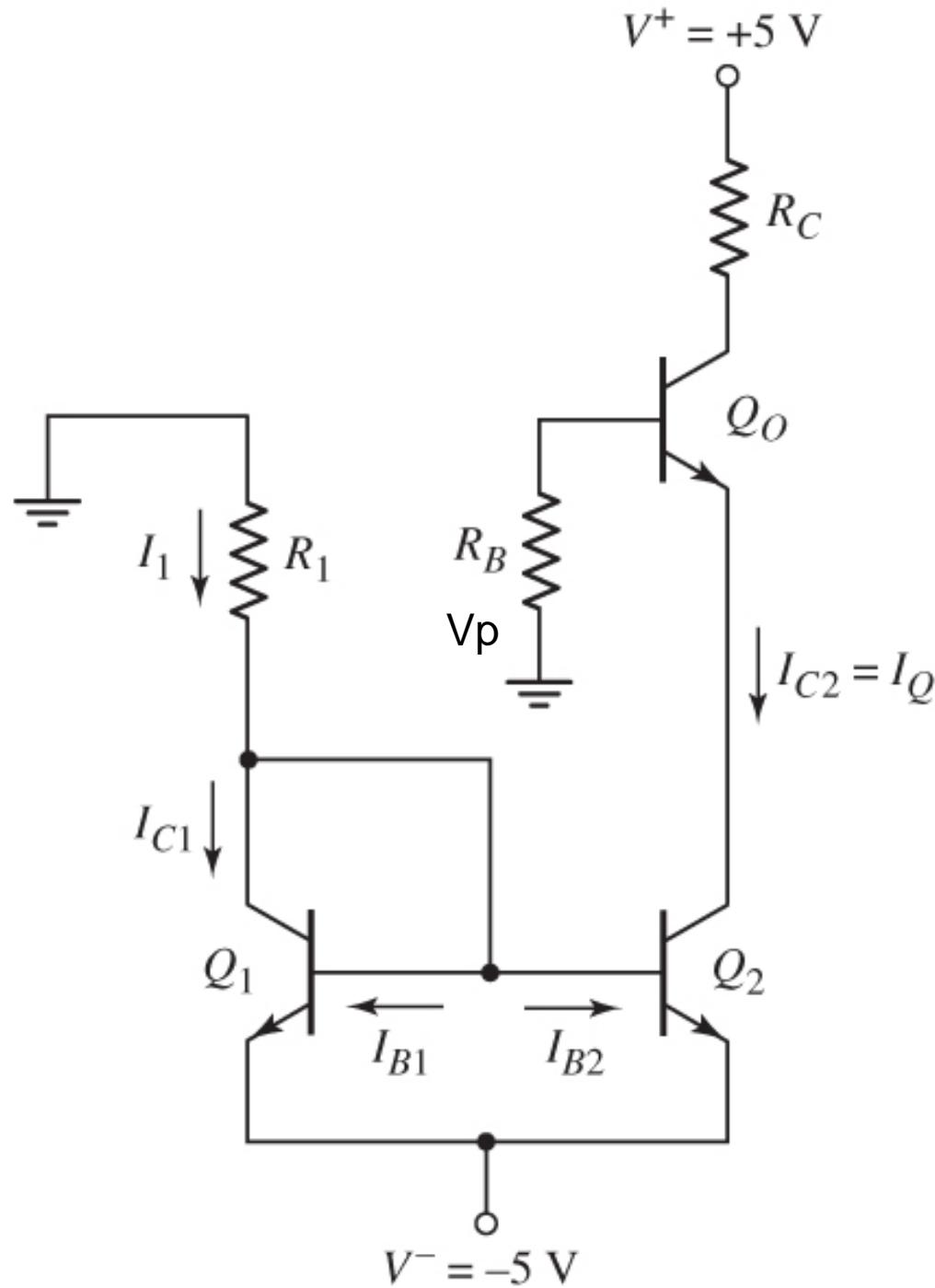


Fig. 5.62

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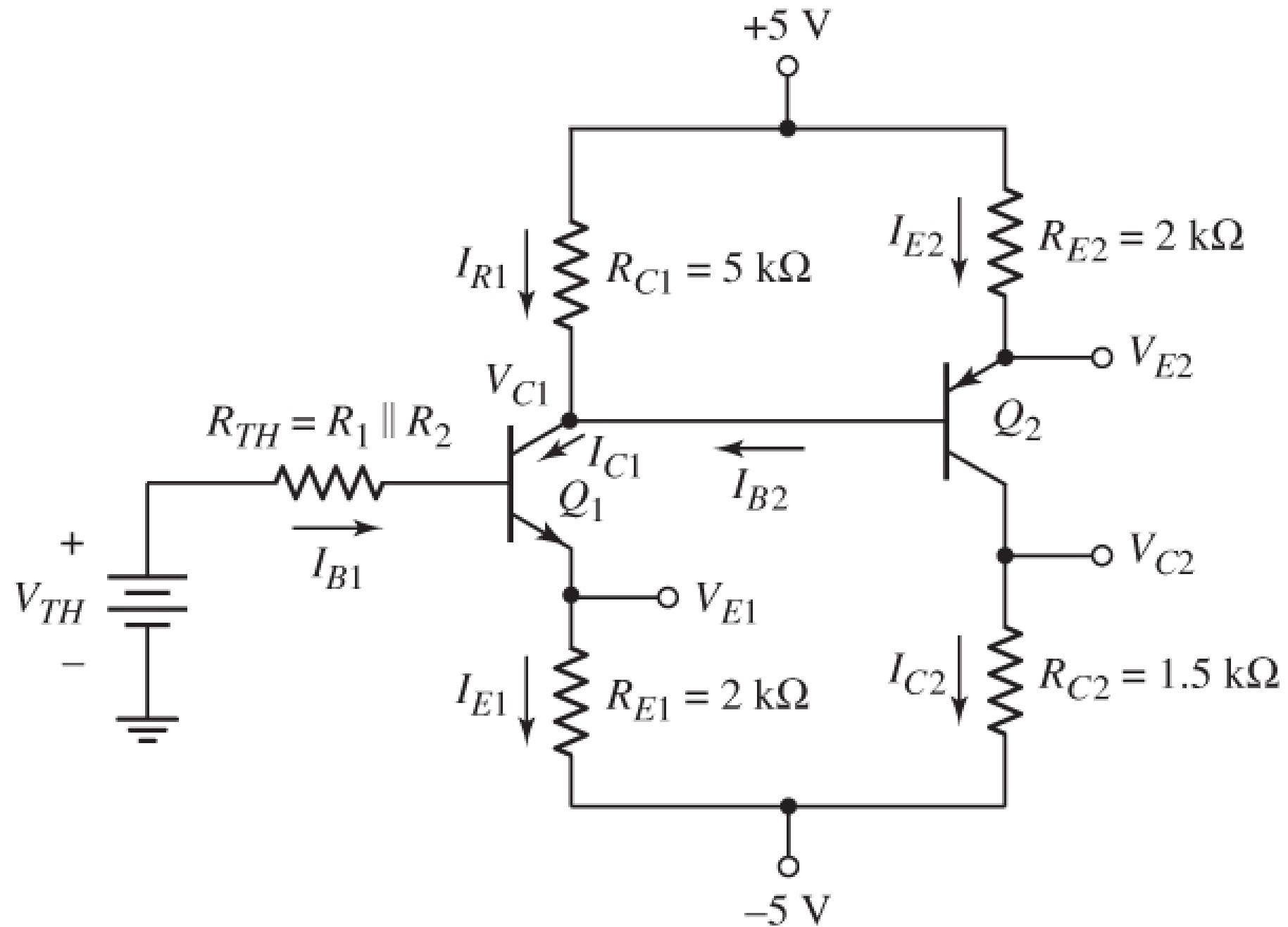
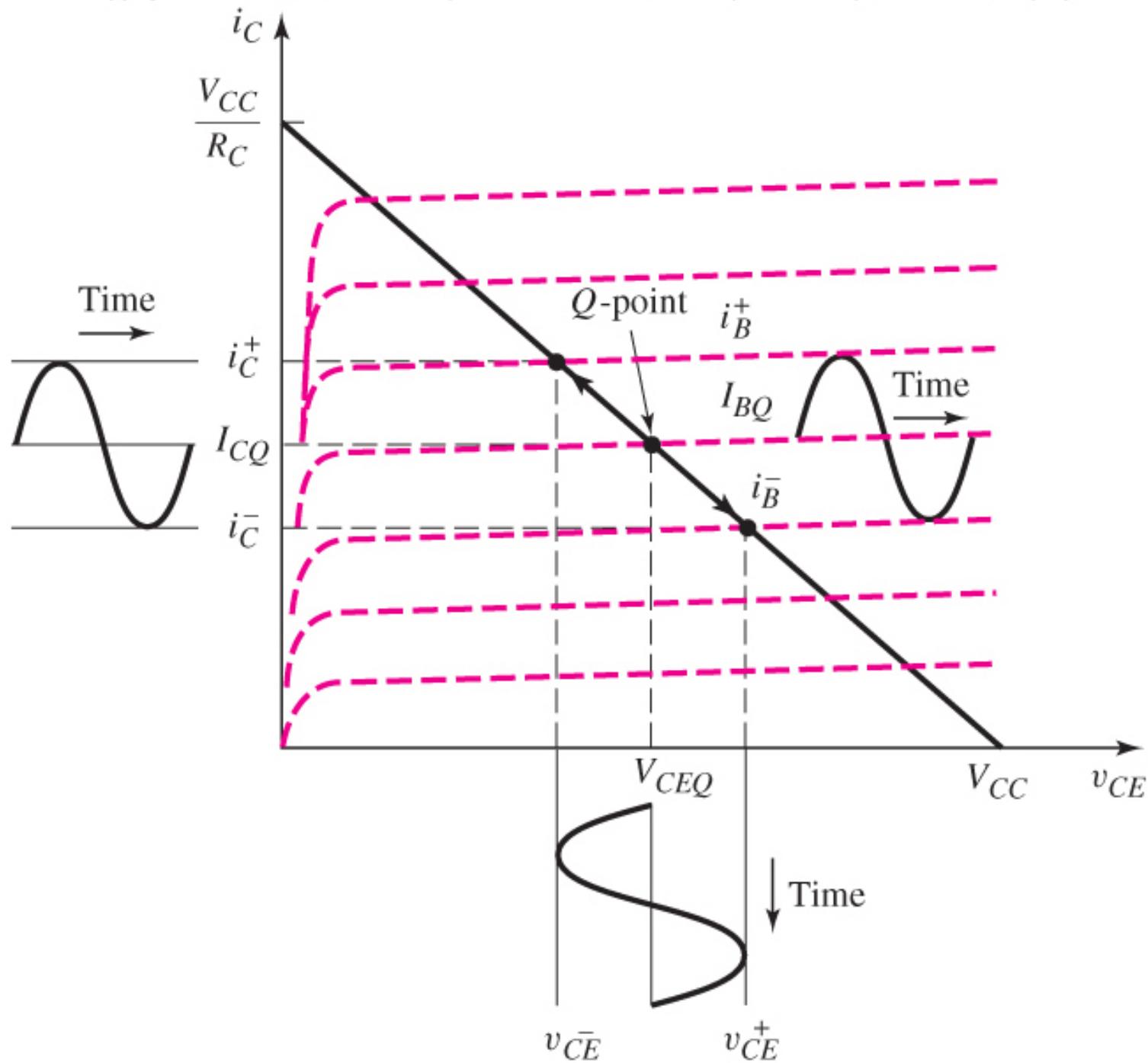


Fig. 6.4

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Tab. 6.3

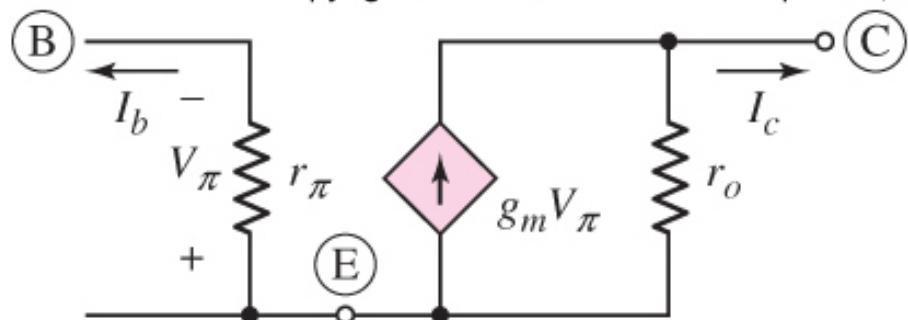
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**Table 6.3** Four equivalent two-port networks

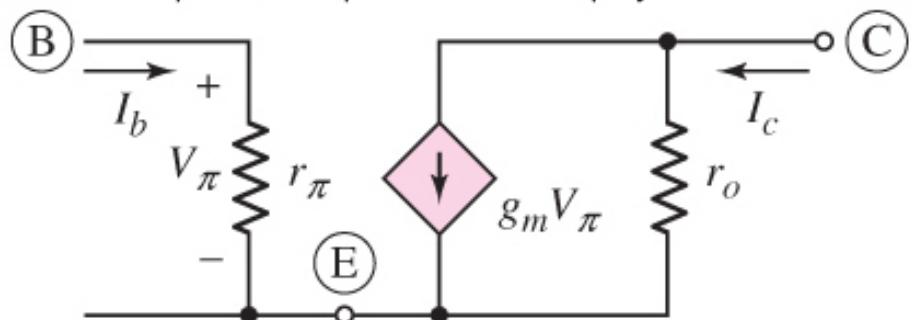
Type	Equivalent circuit	Gain property
Voltage amplifier		Output voltage proportional to input voltage
Current amplifier		Output current proportional to input current
Transconductance amplifier		Output current proportional to input voltage
Transresistance amplifier		Output voltage proportional to input current

# pnp transistor: Polarity of $V_\pi$

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(a)



(b)

Fig. 6.19

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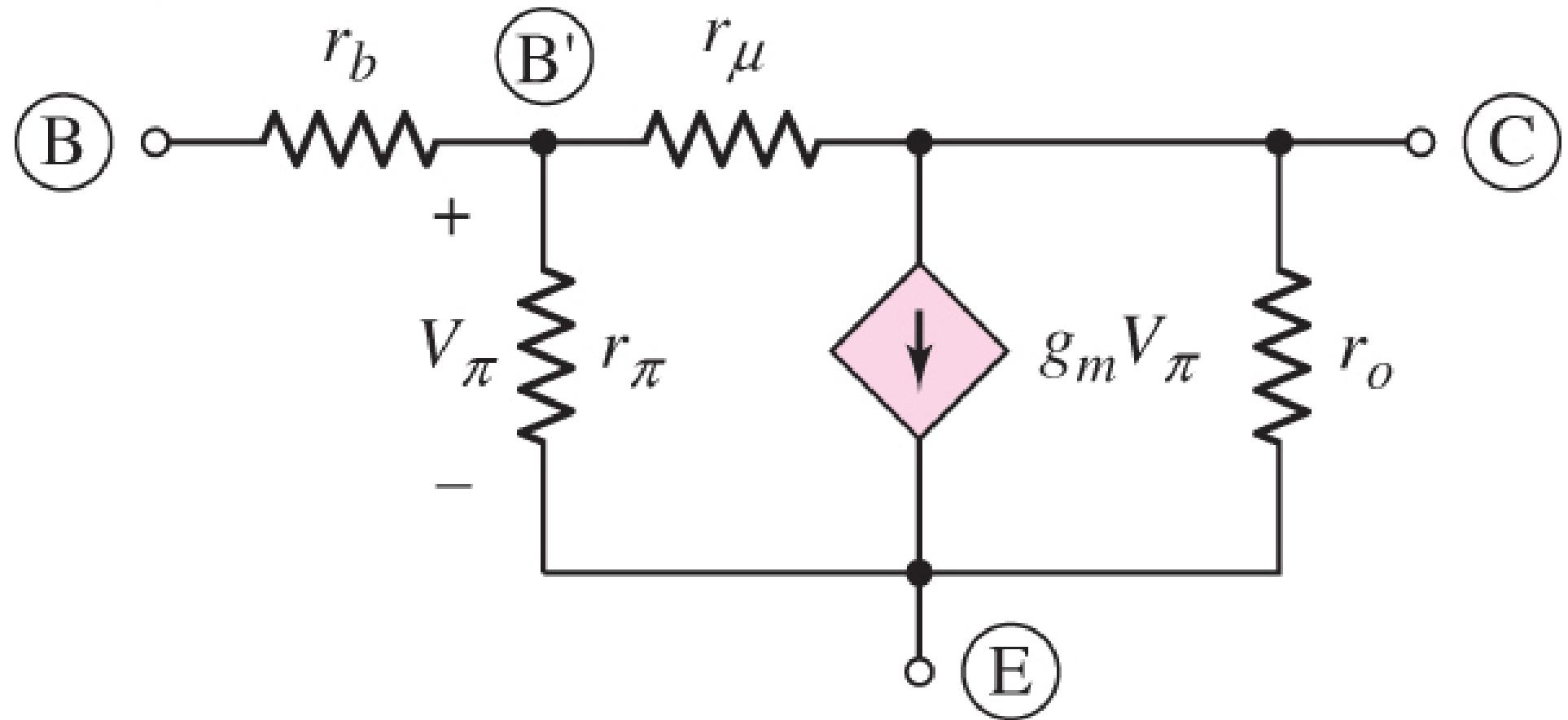
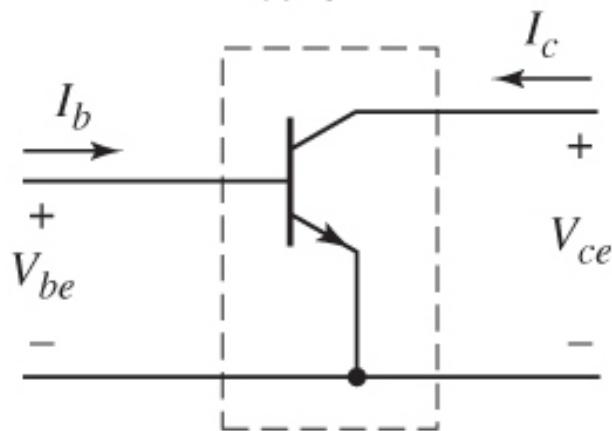
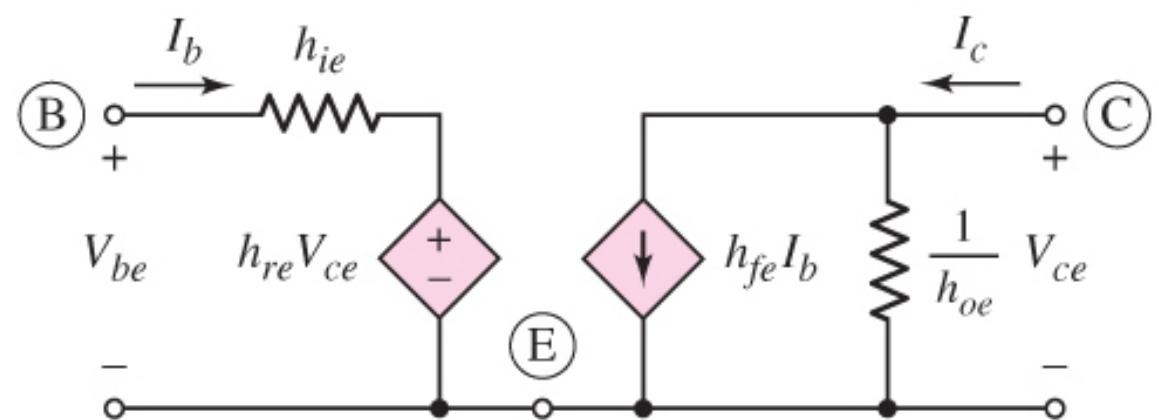


Fig. 6.20

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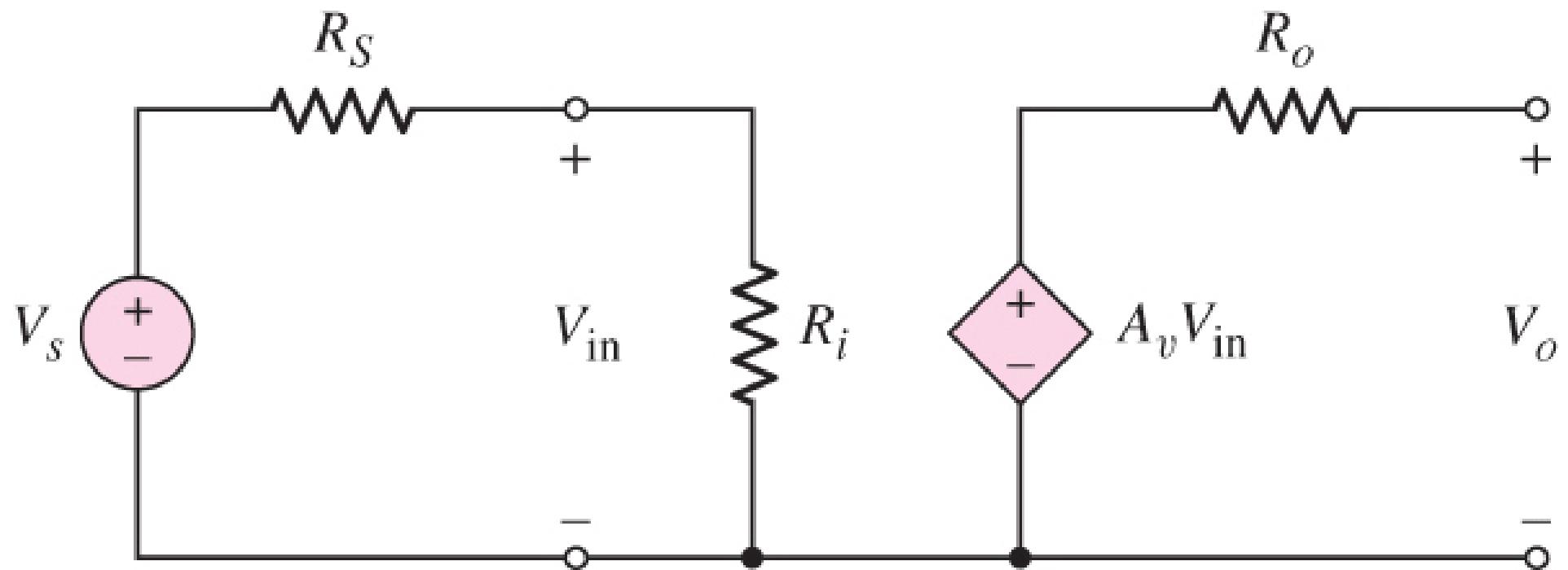
(a)



(b)

Fig. 6.30

## Relationship between $A_v$ , $R_i$ , $R_o$



Tab. 6.4

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**Table 6.4** Characteristics of the three BJT amplifier configurations

Configuration	Voltage gain	Current gain	Input resistance	Output resistance
Common emitter	$A_v > 1$	$A_i > 1$	Moderate	Moderate to high
Emitter follower	$A_v \approx 1$	$A_i > 1$	High	Low
Common base	$A_v > 1$	$A_i \approx 1$	Low	Moderate to high

Fig. 6.29

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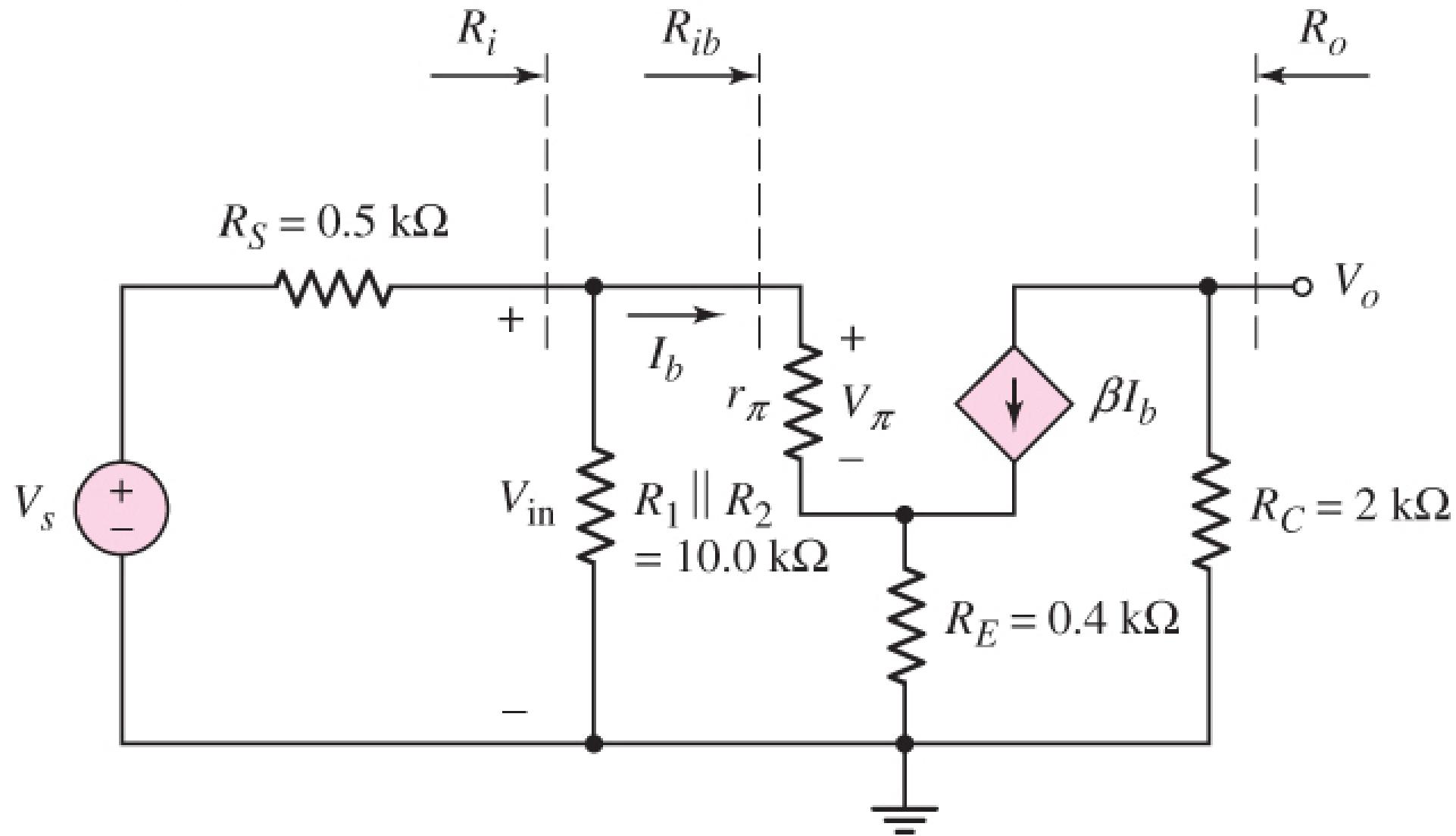
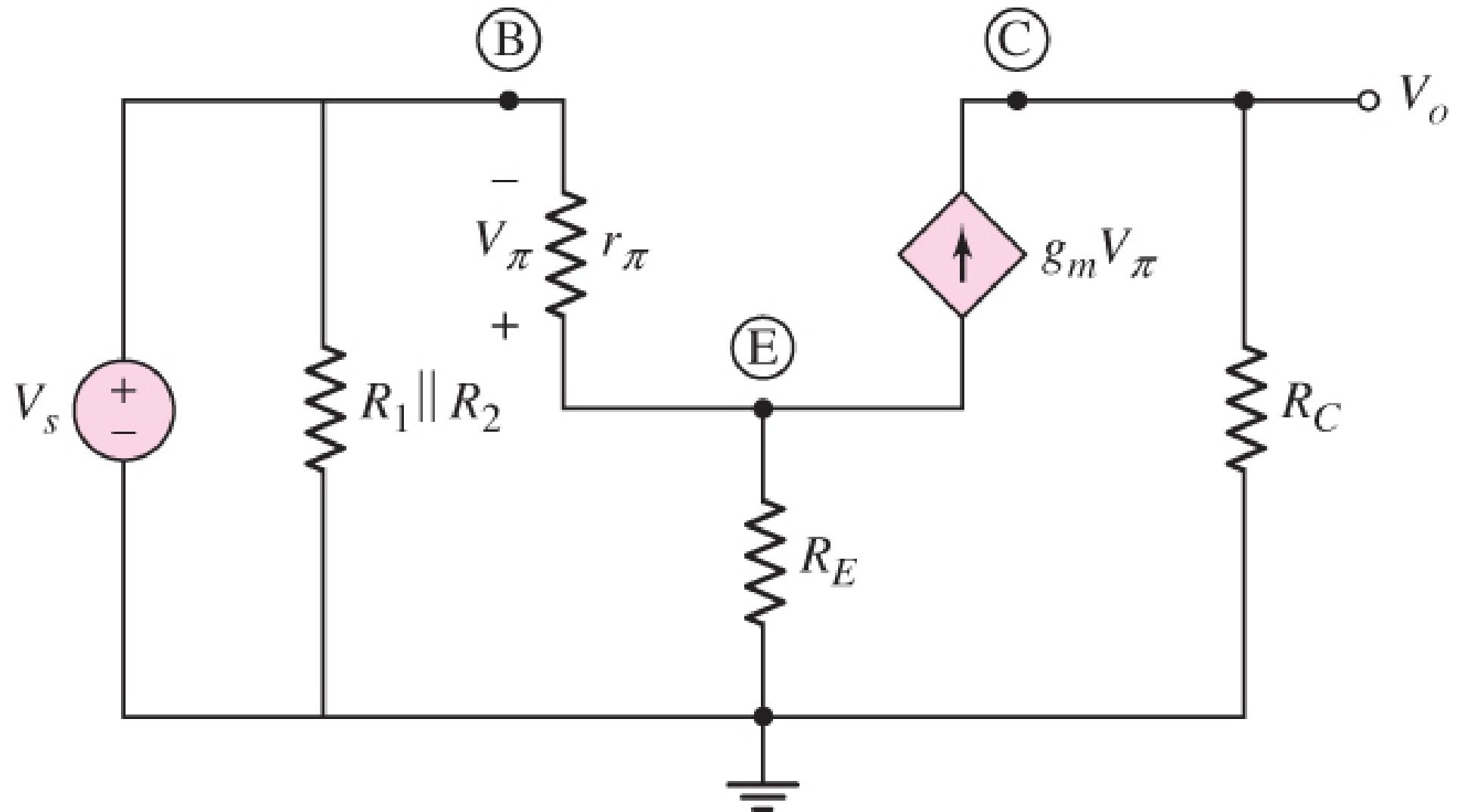


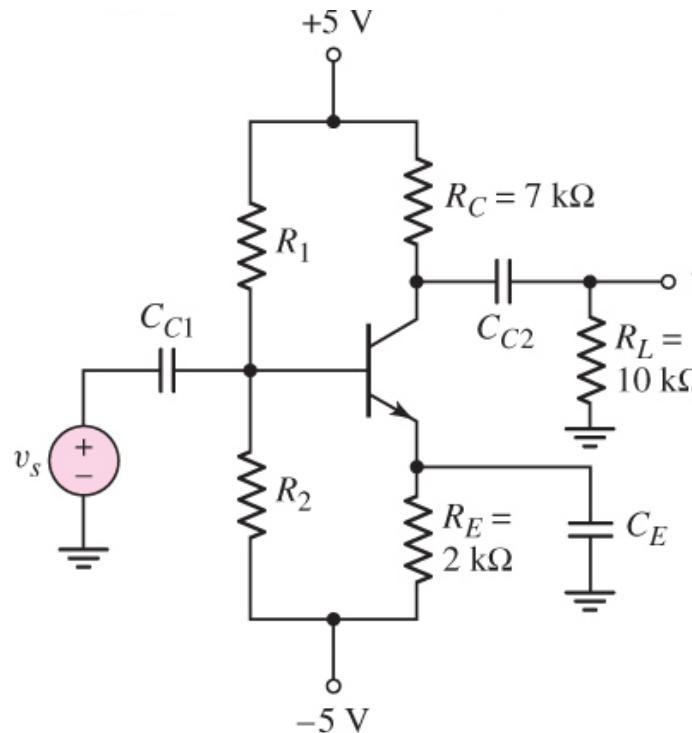
Fig. 6.33

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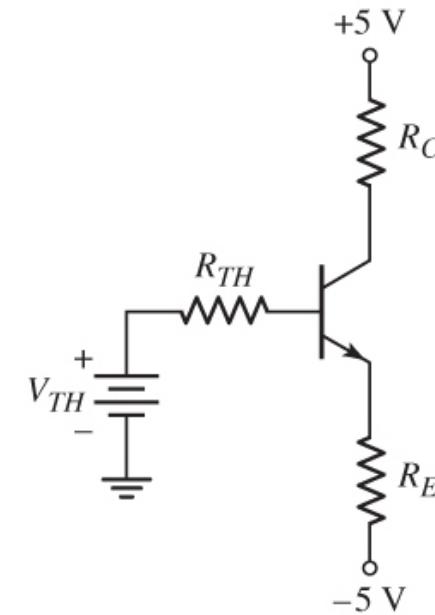


## **AC and DC Load Lines/ Max Symmetrical Swing**

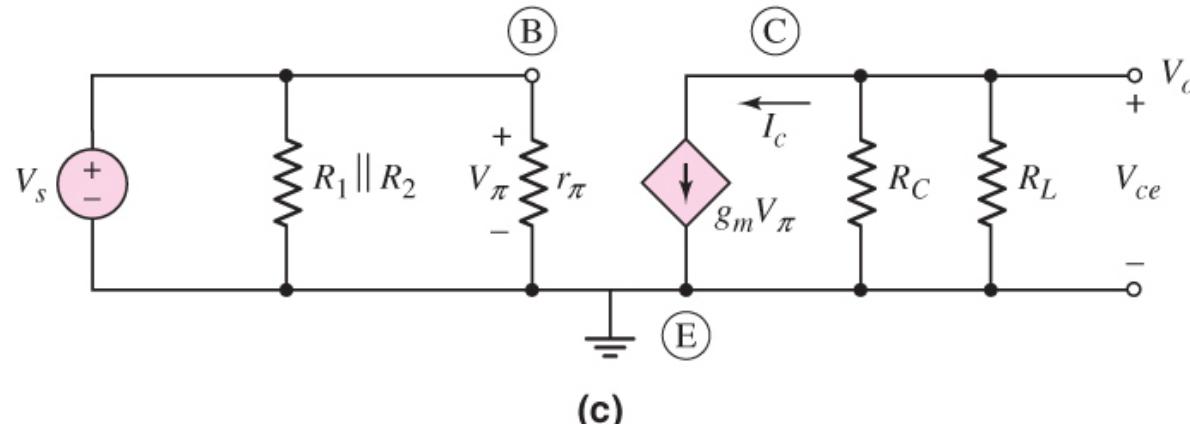
Fig. 6.46



(a)



(b)



(c)

Fig. 6.47

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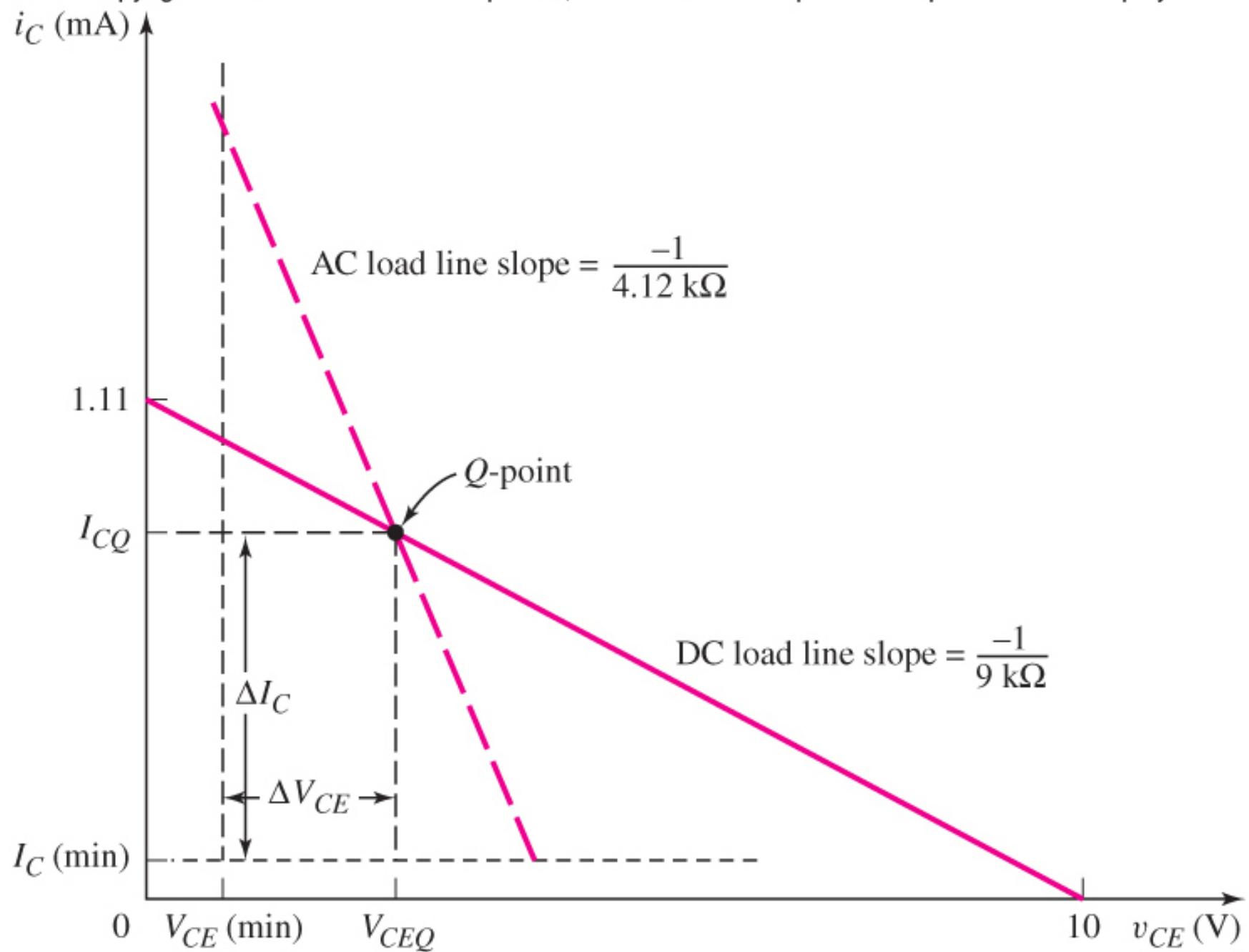


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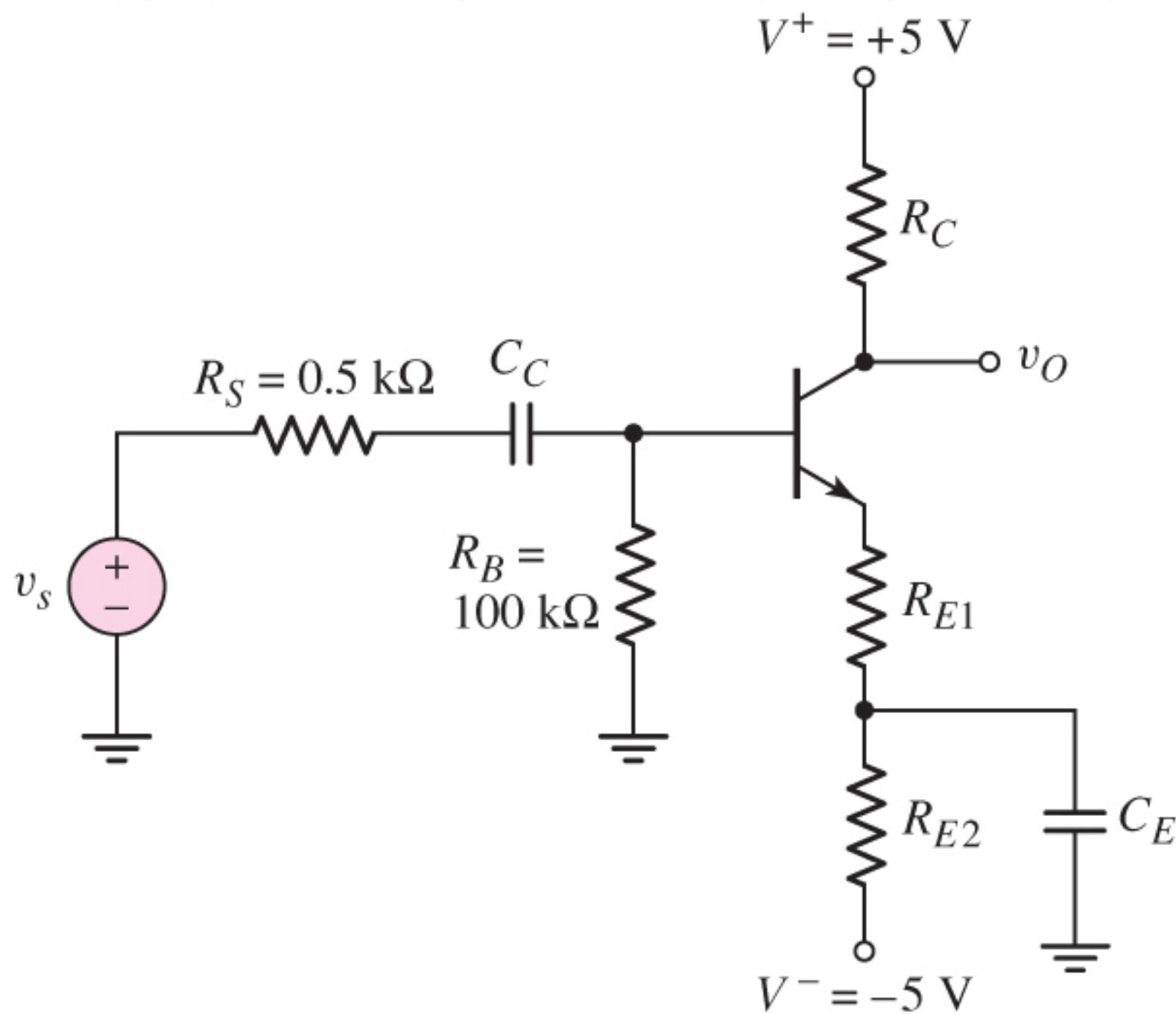


Fig. 6.42

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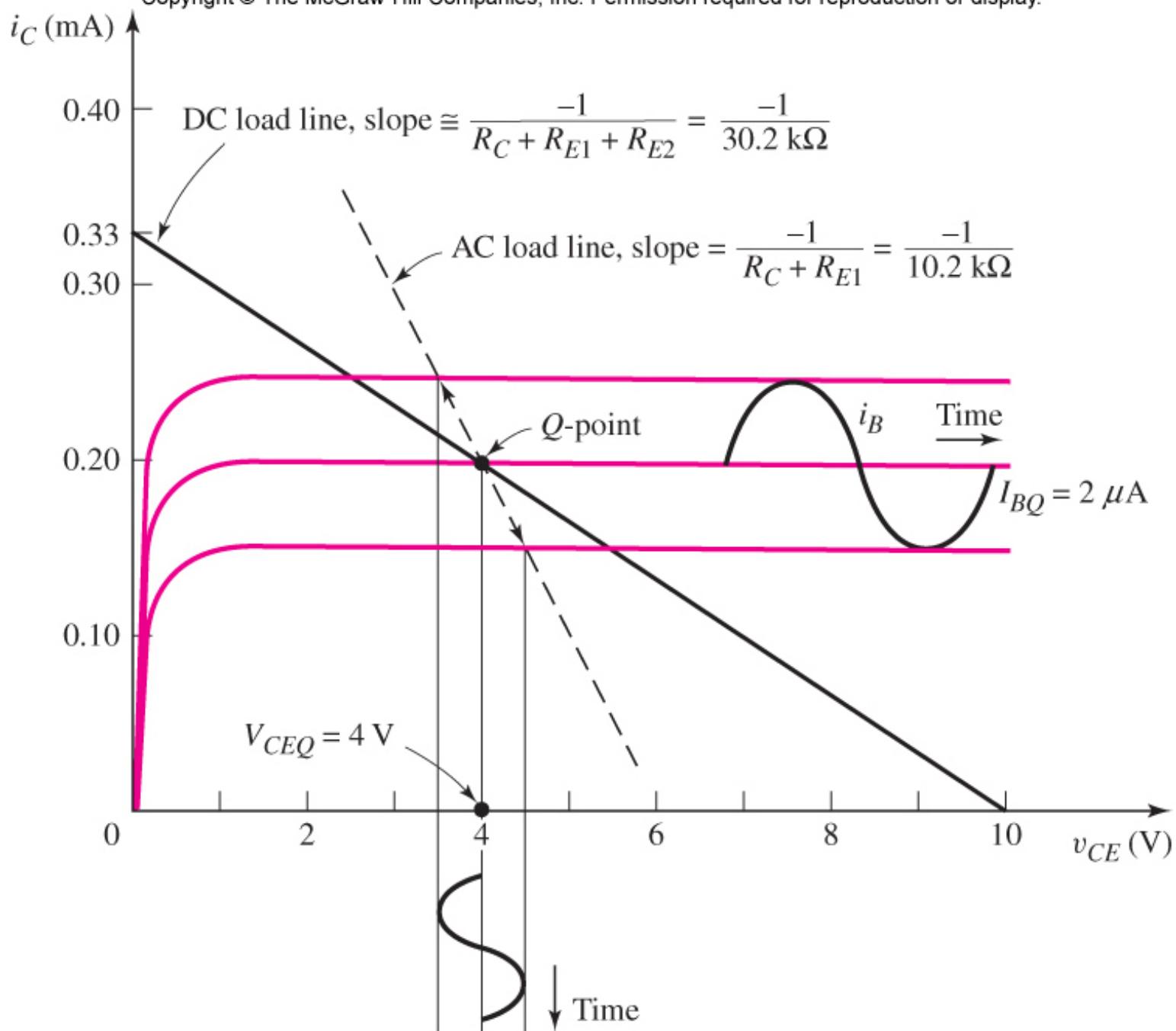


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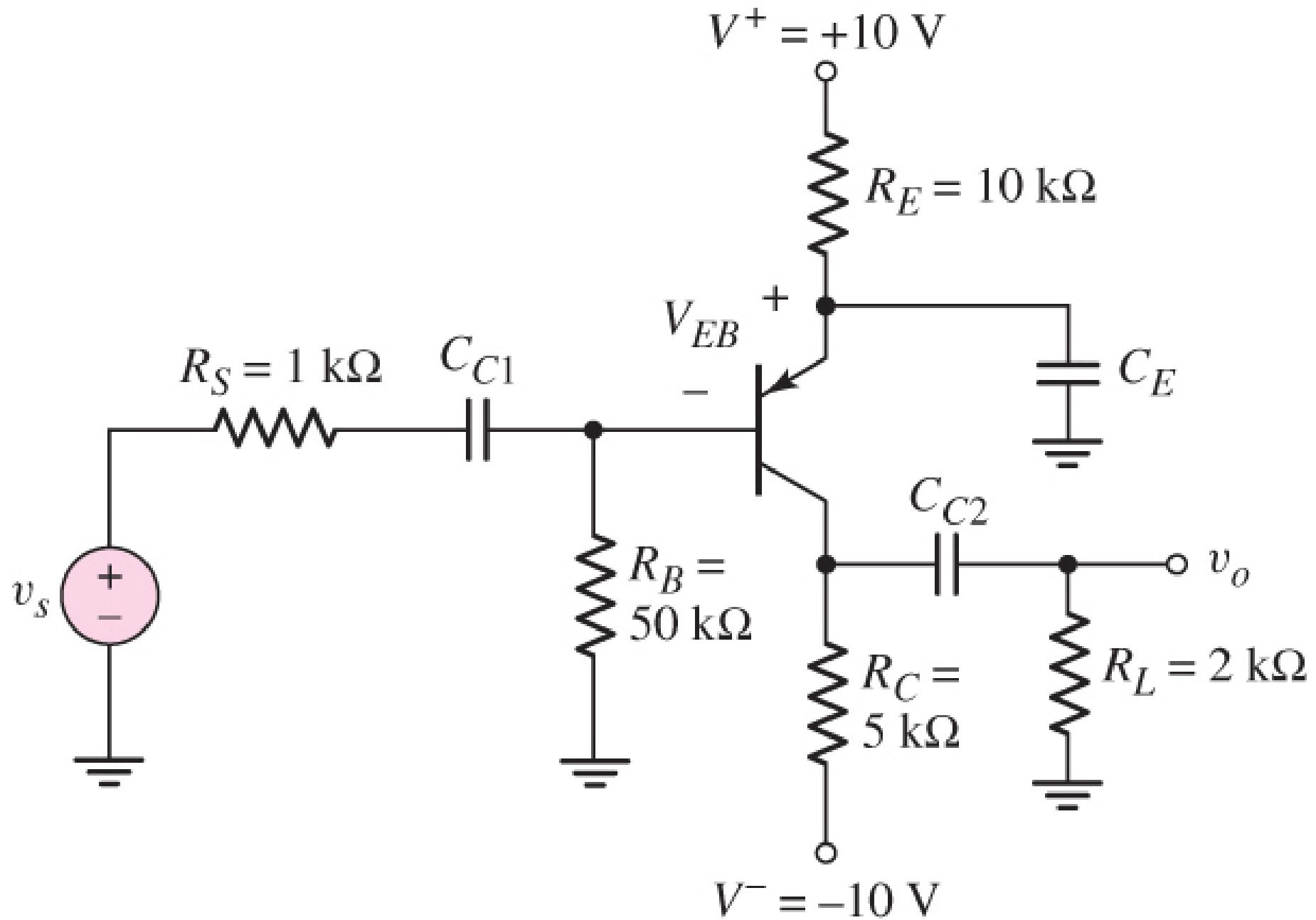


Fig. 6.44

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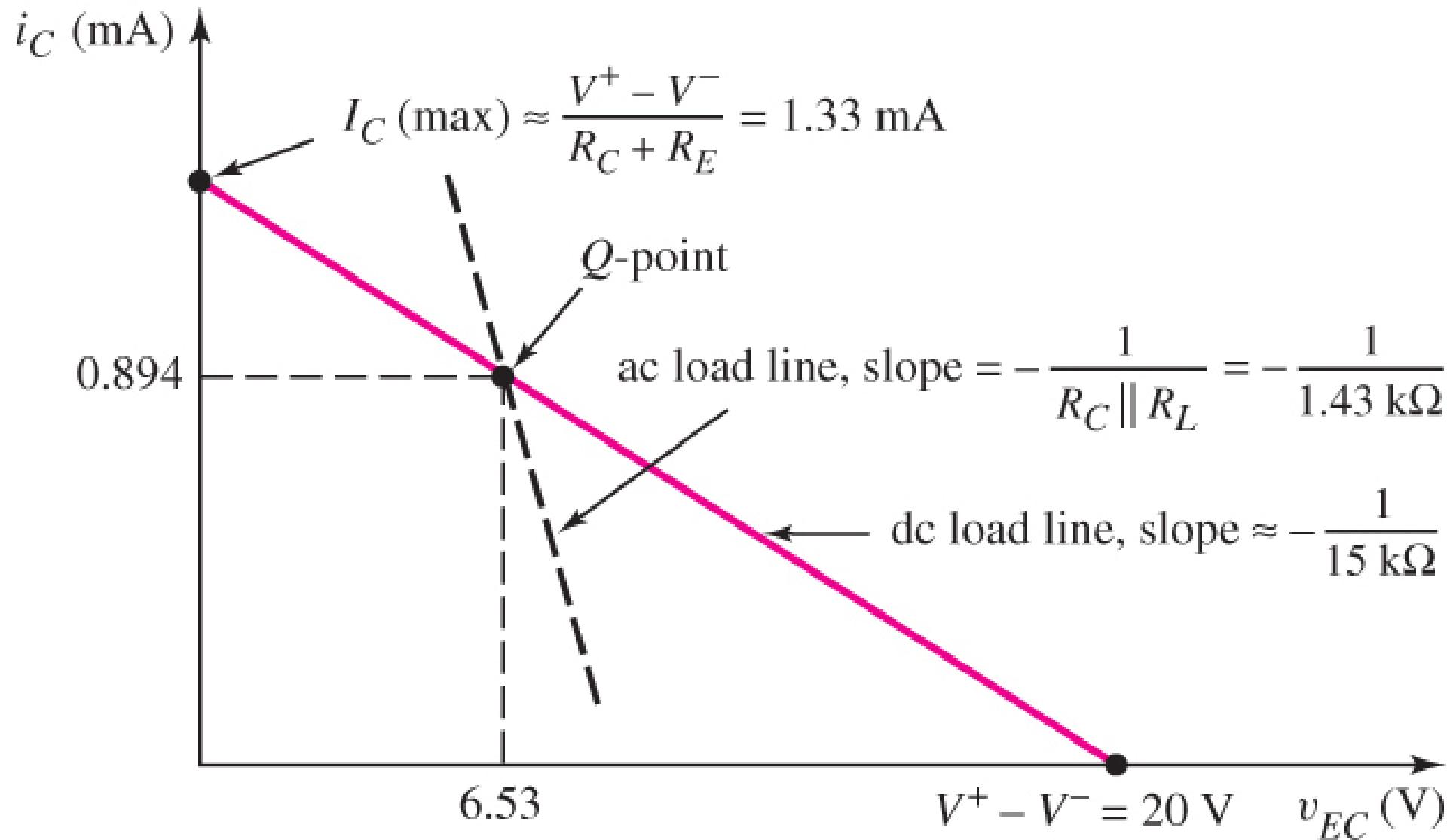


Fig. 6.49

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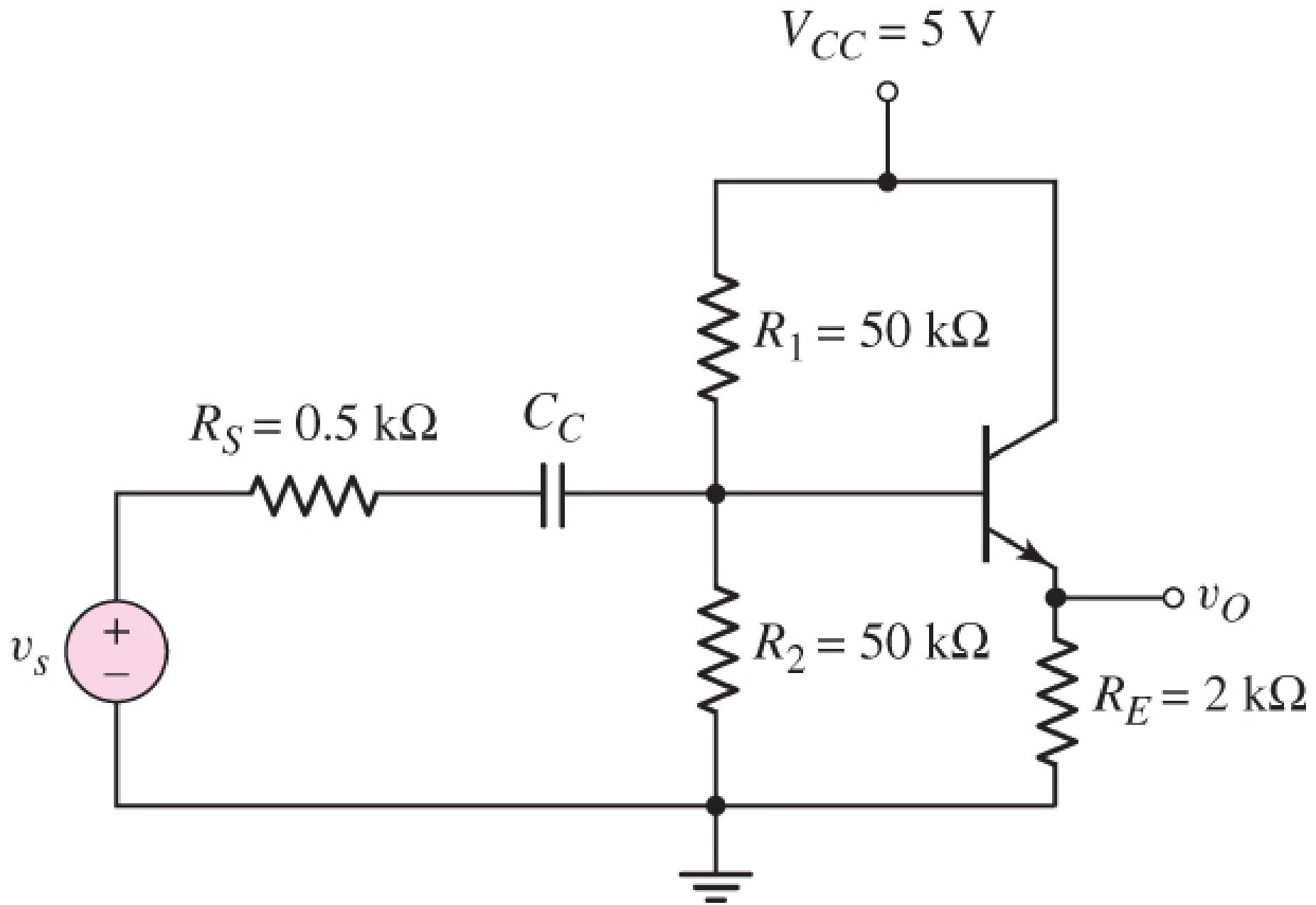


Fig. 6.50

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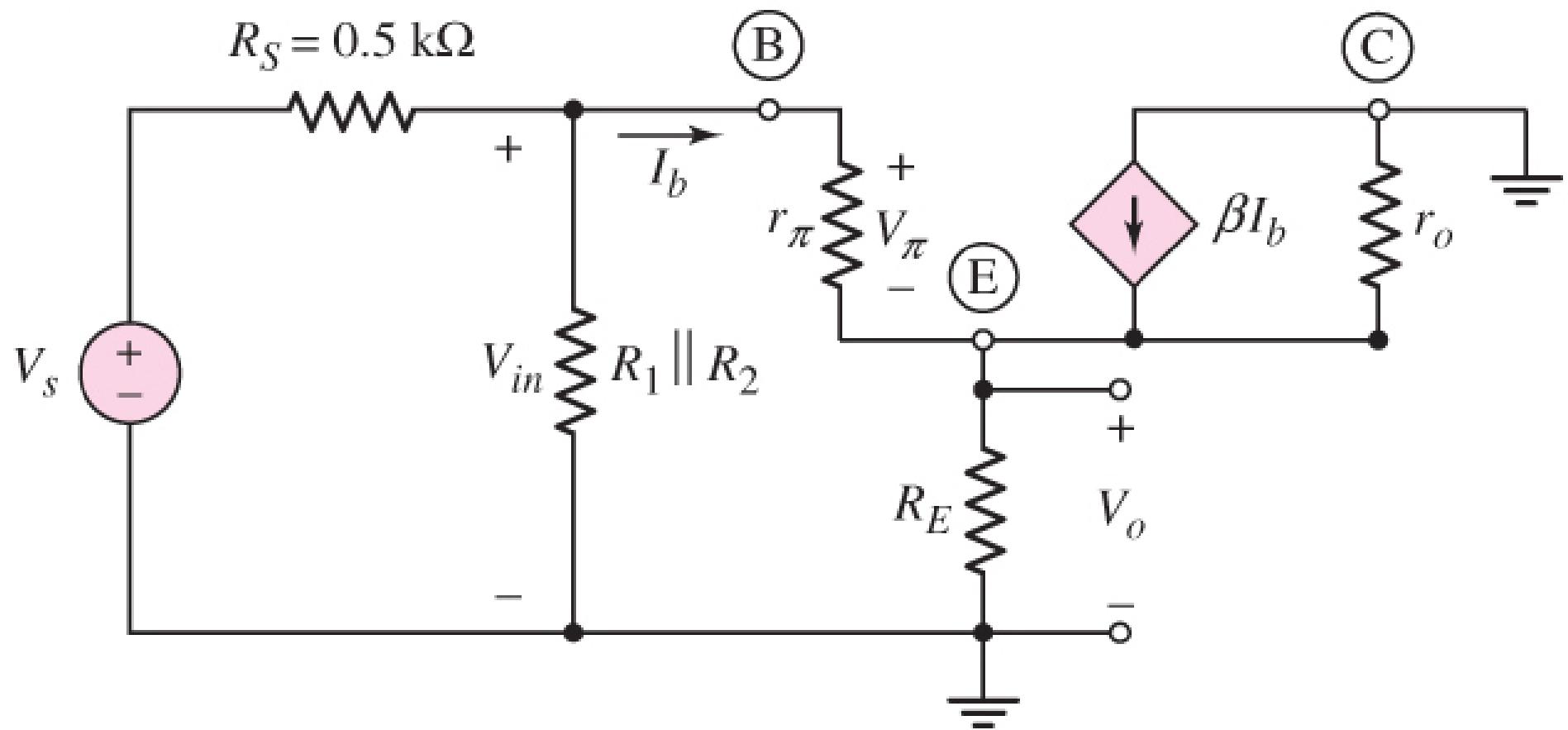


Fig. 6.51

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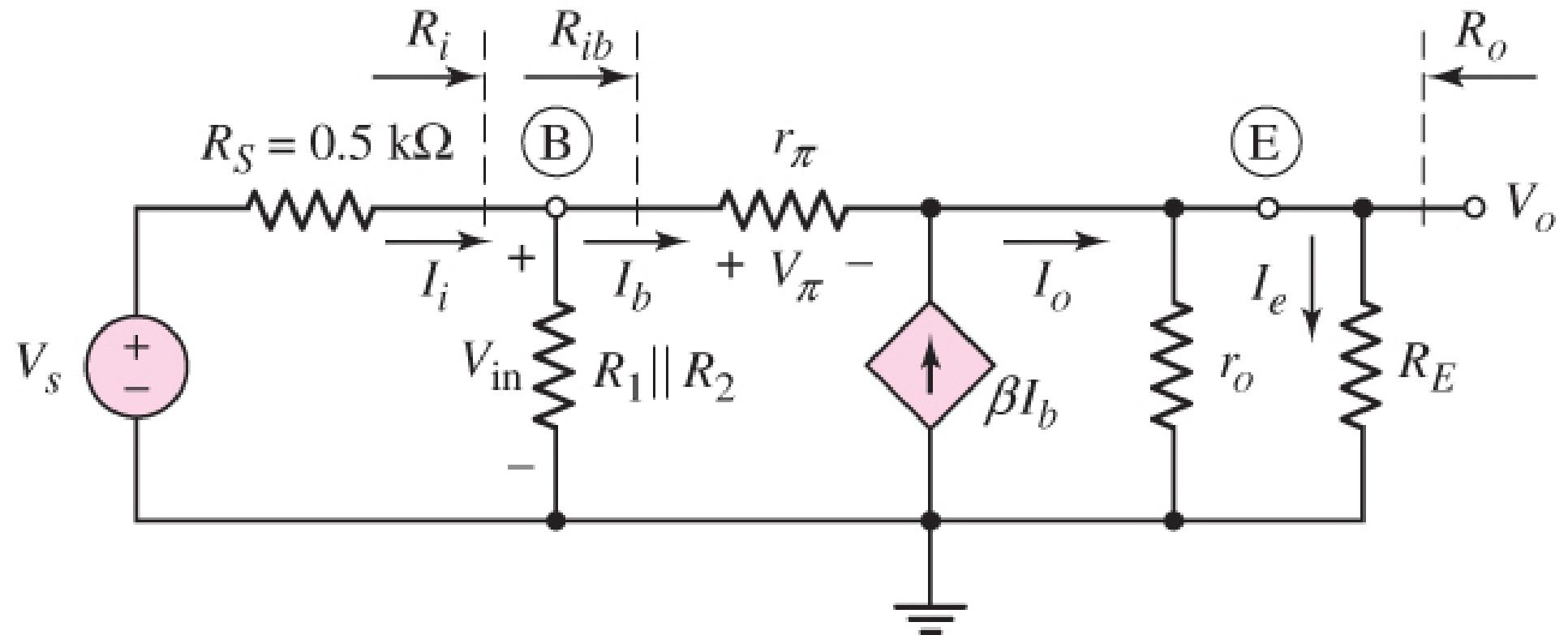


Fig. 6.53

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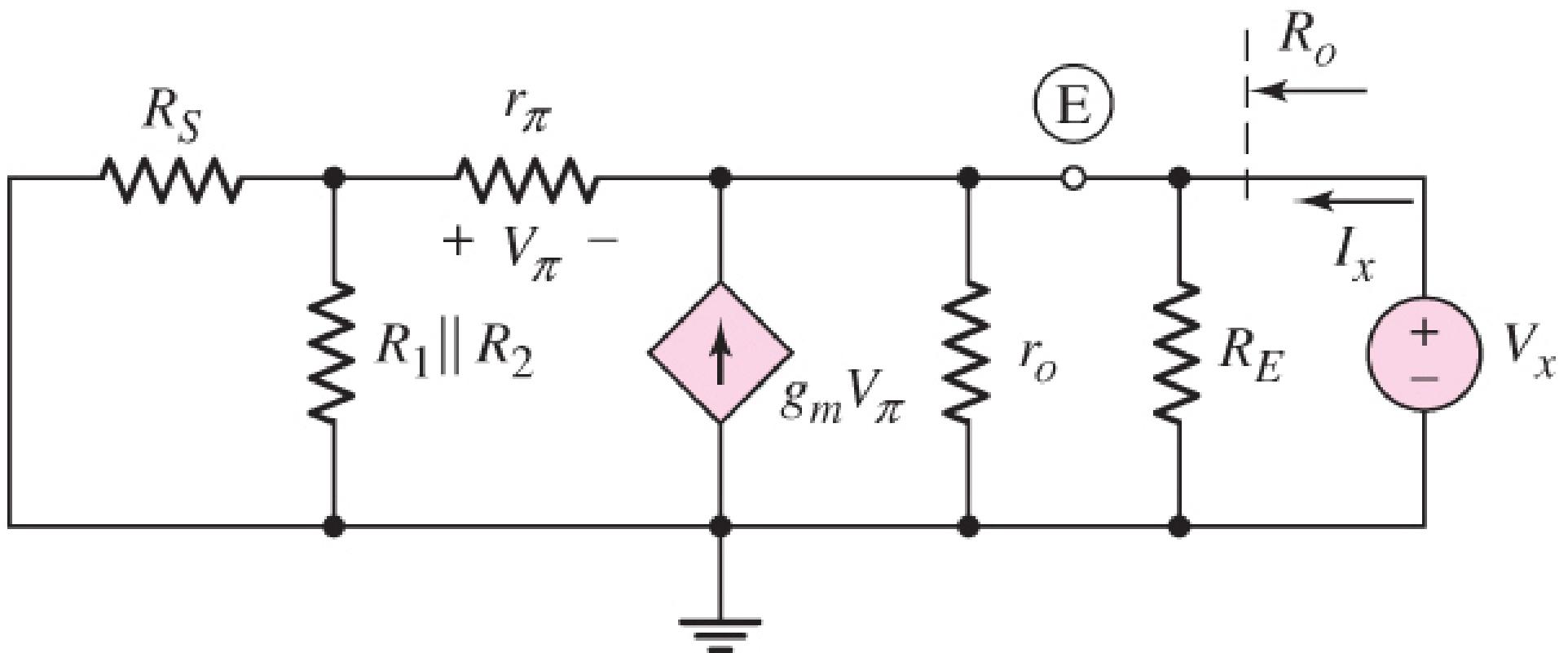


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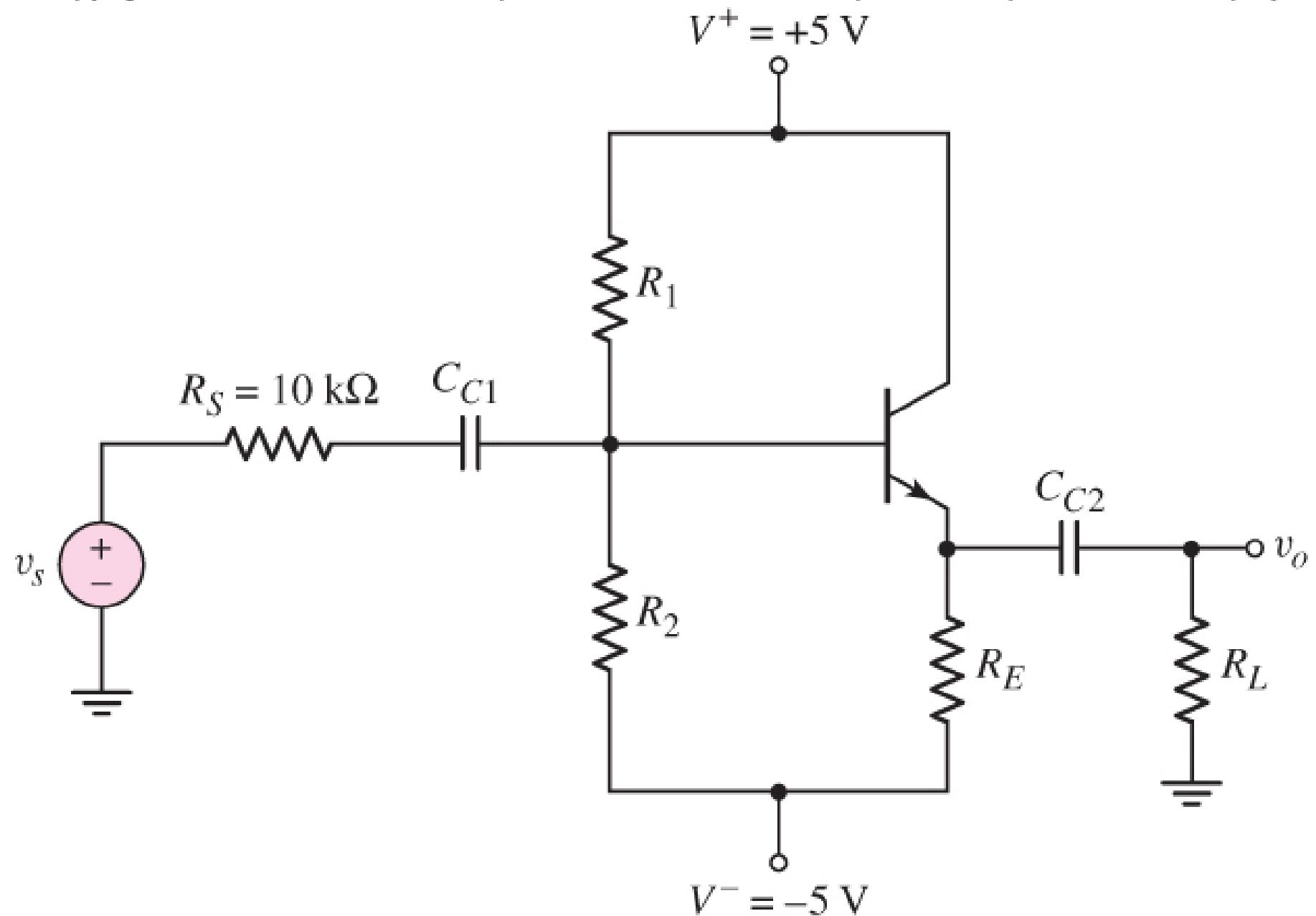


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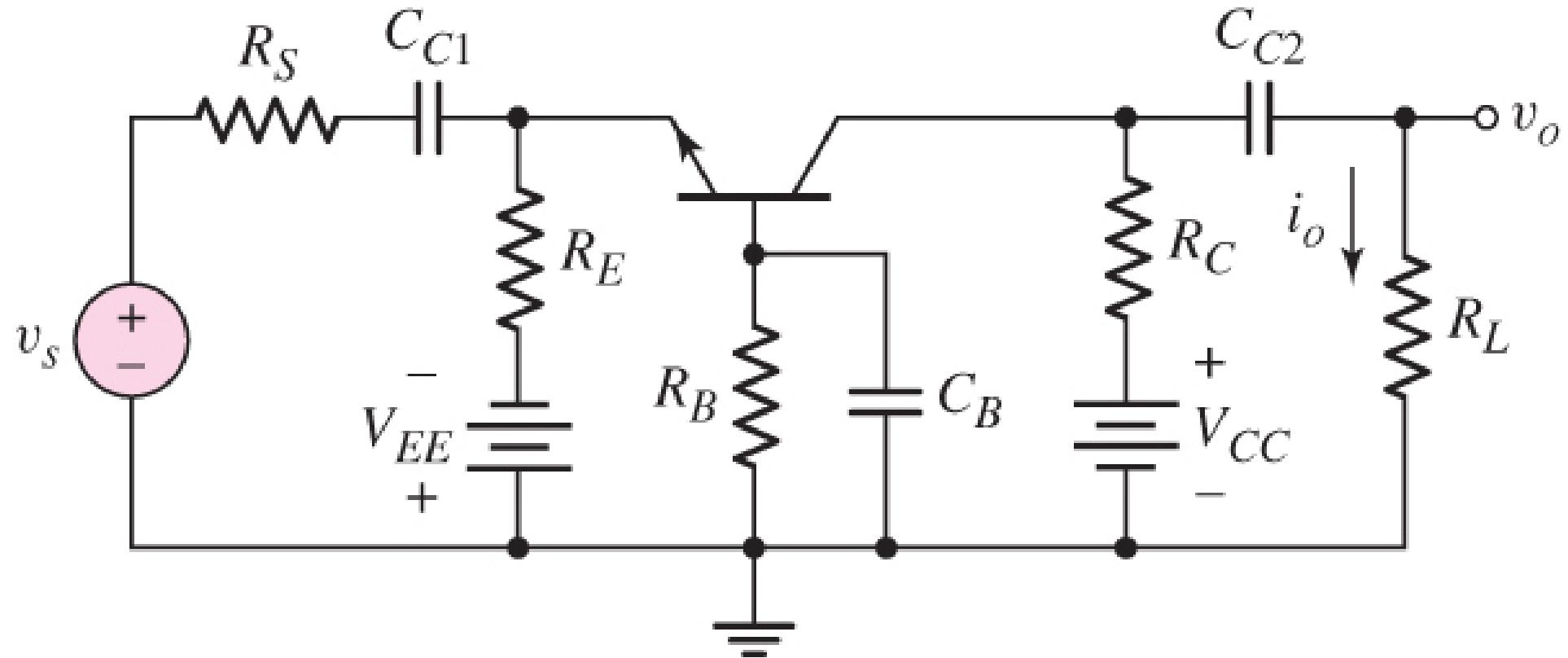
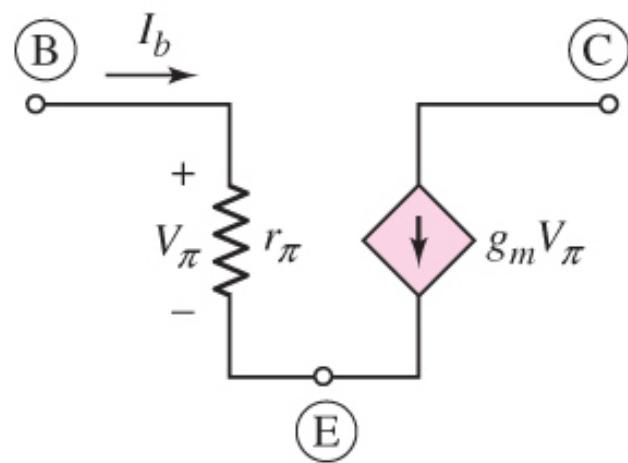
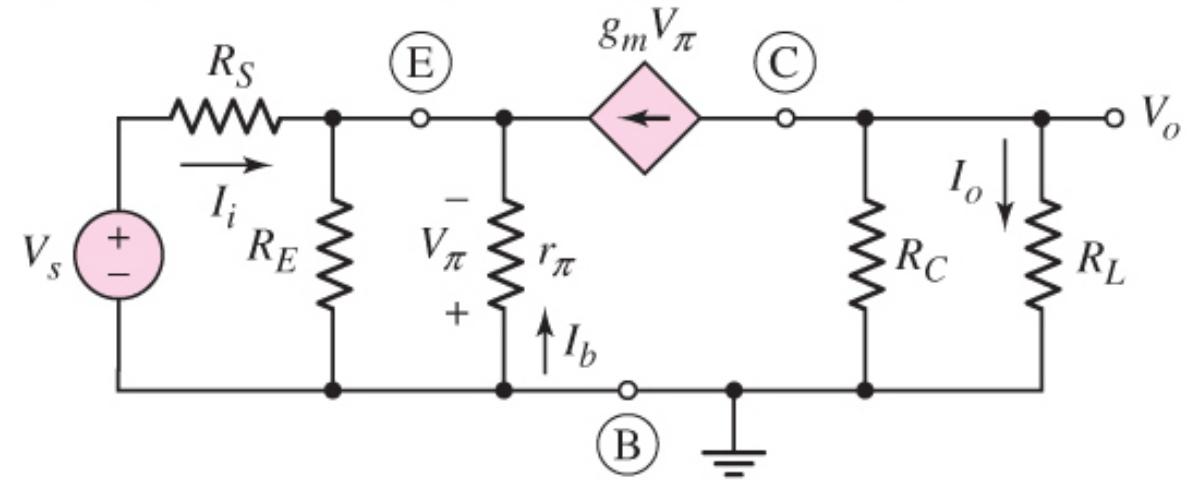


Fig. 6.60

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(a)



(b)

Fig. 6.61

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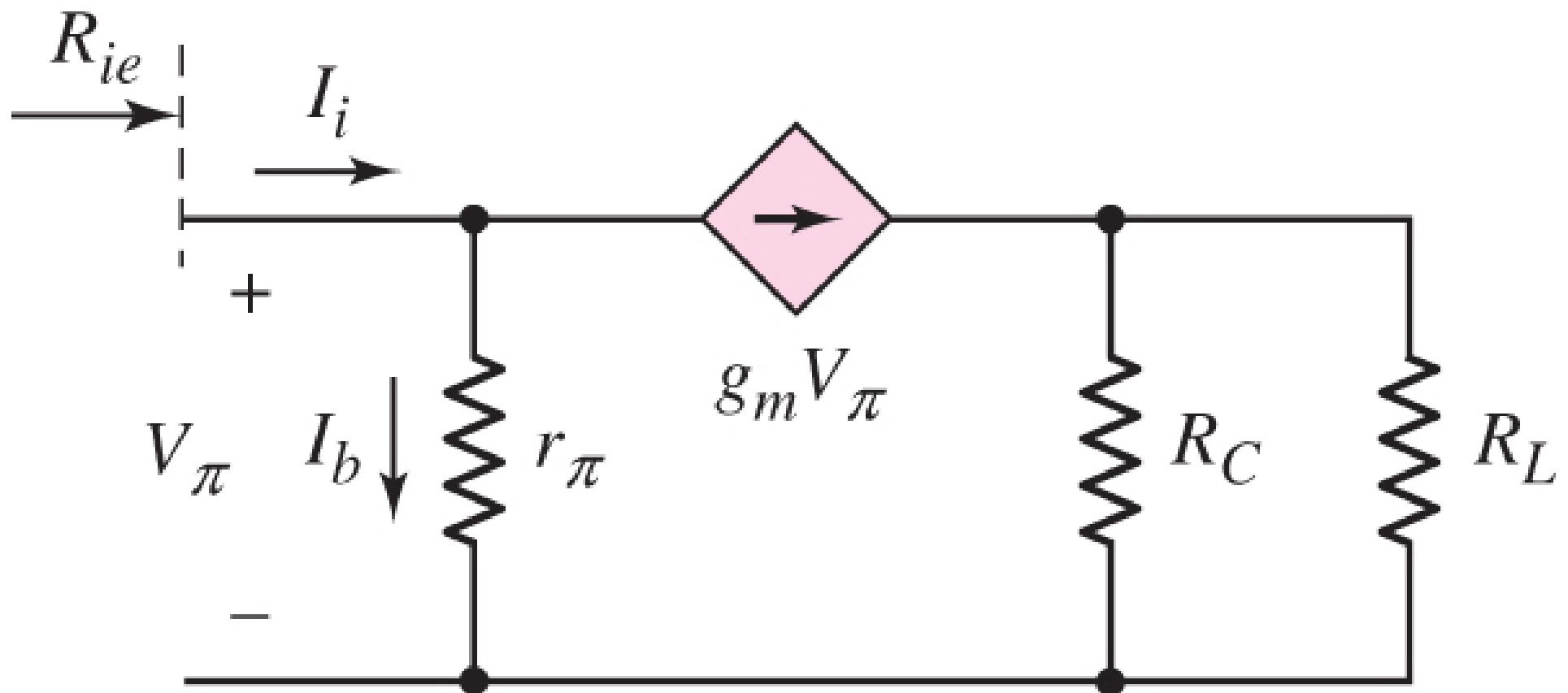


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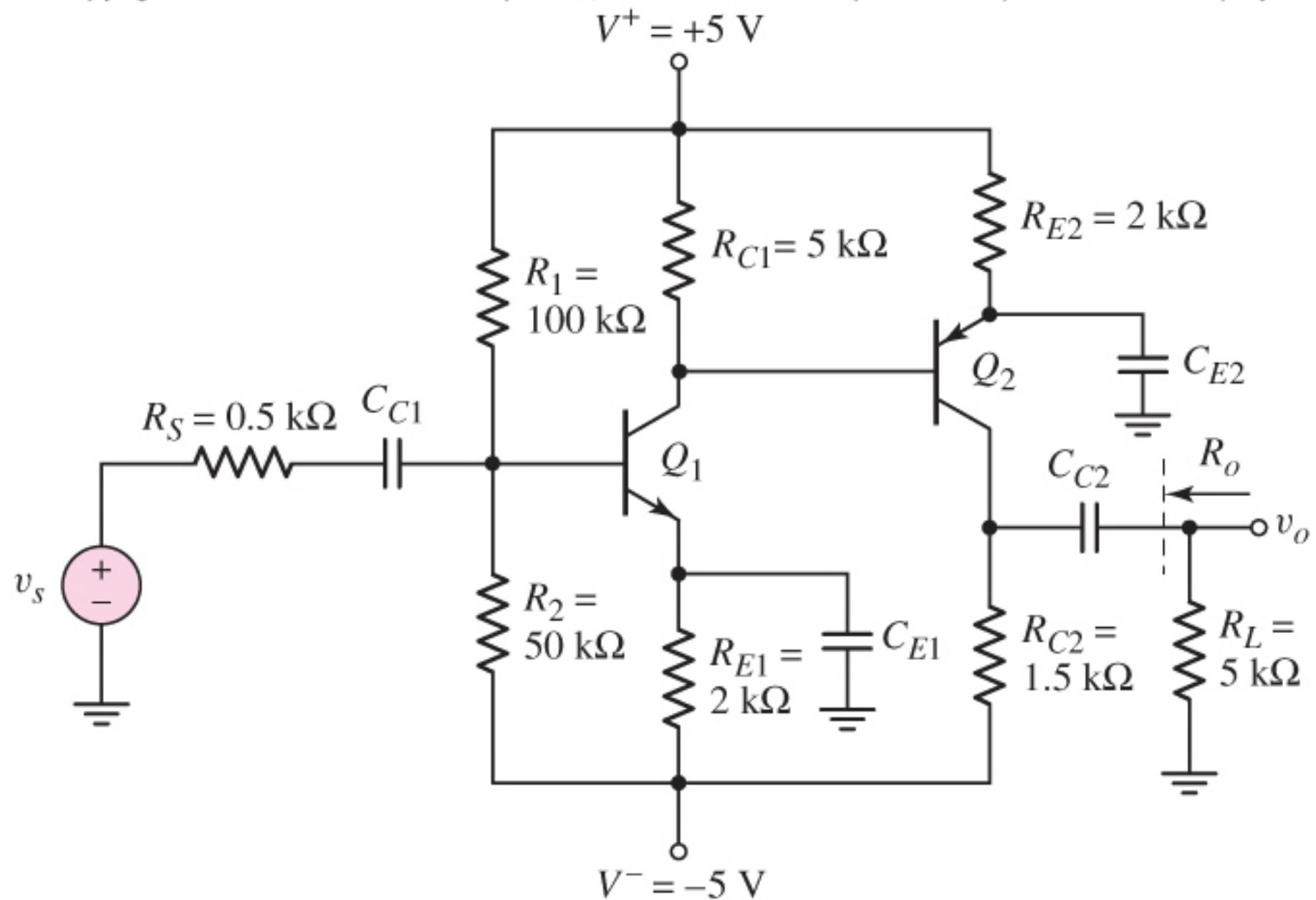
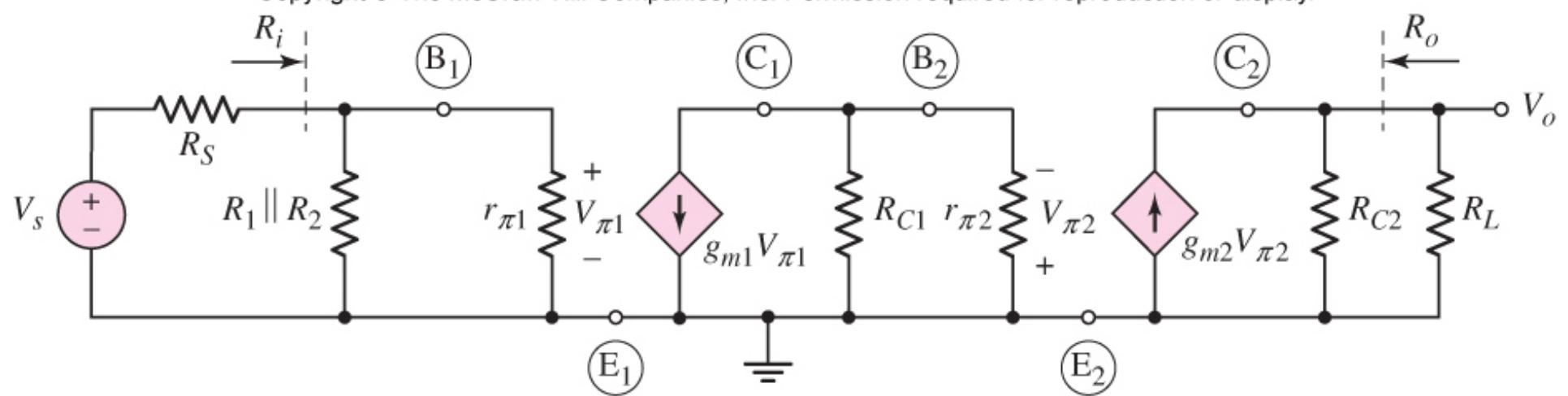


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# **Frequency Response**

## **(Chapter 7)**

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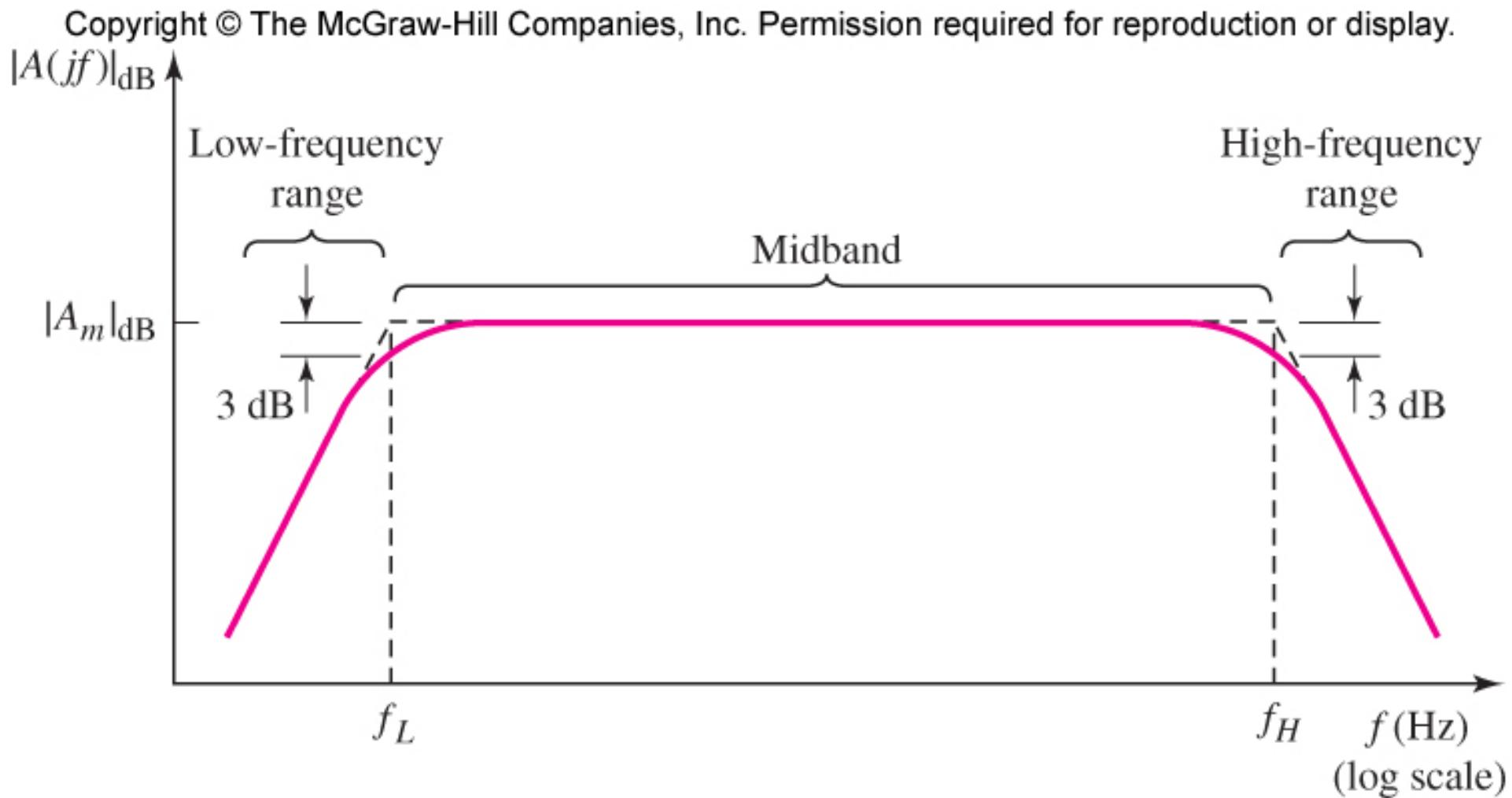


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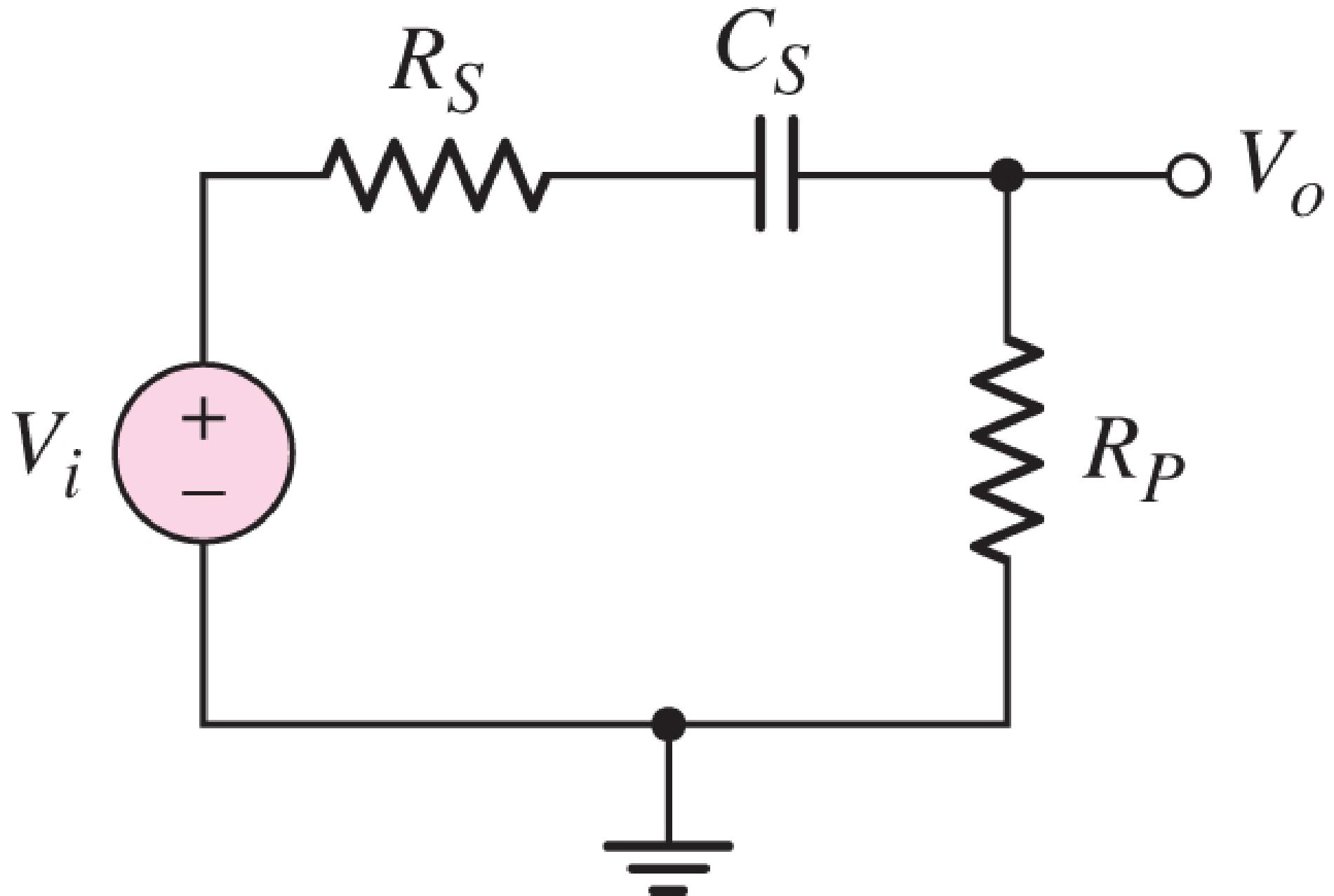


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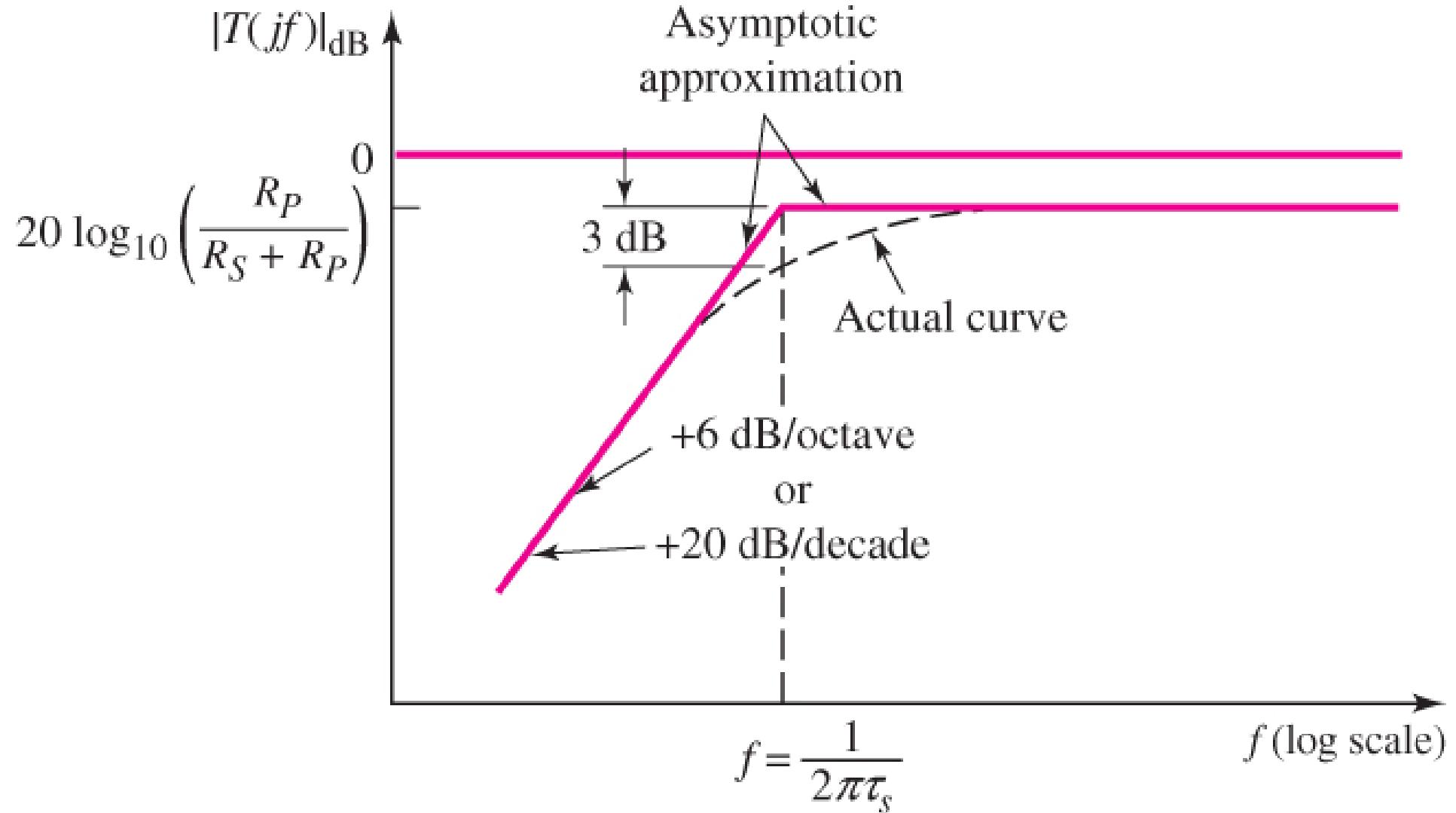


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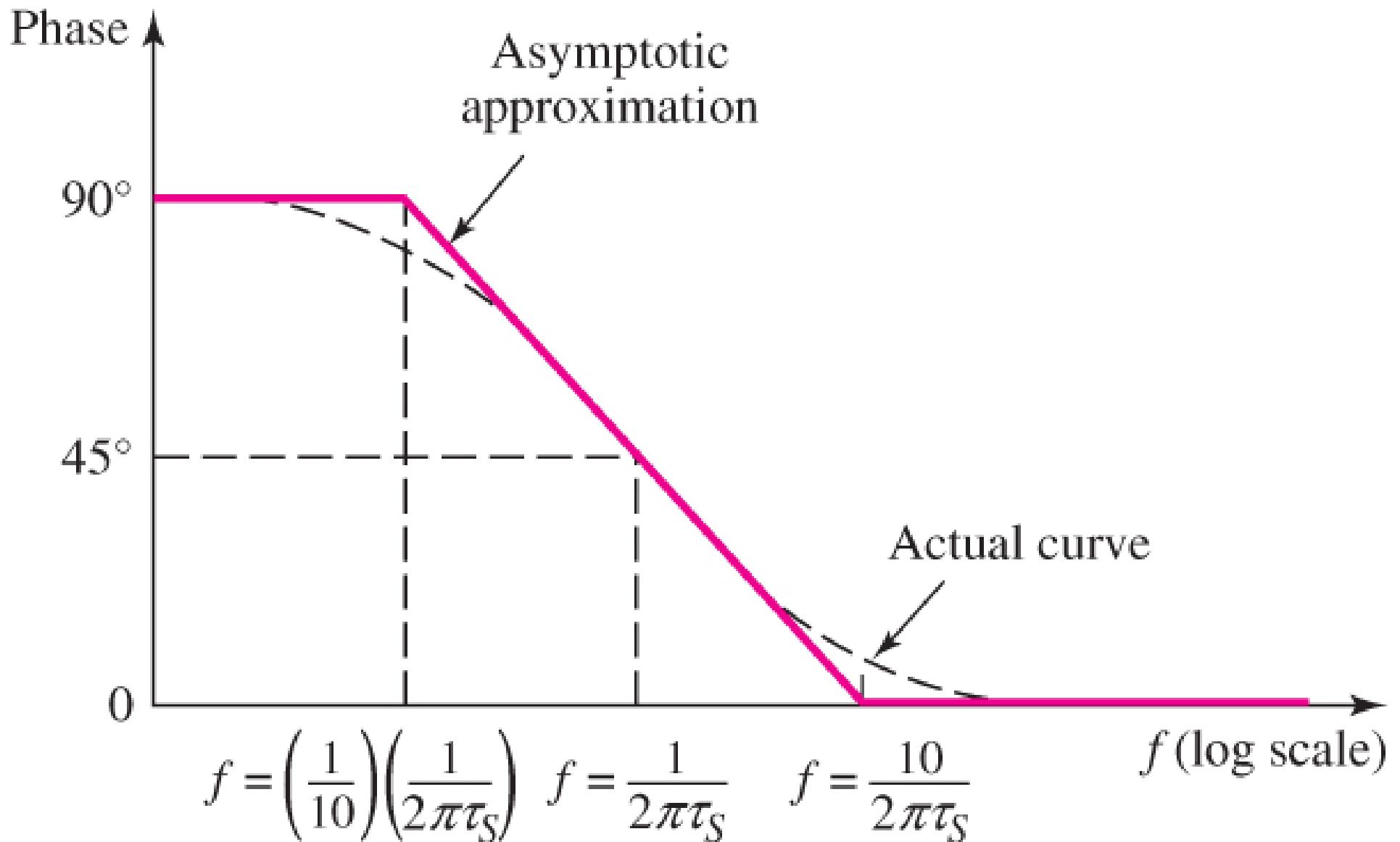


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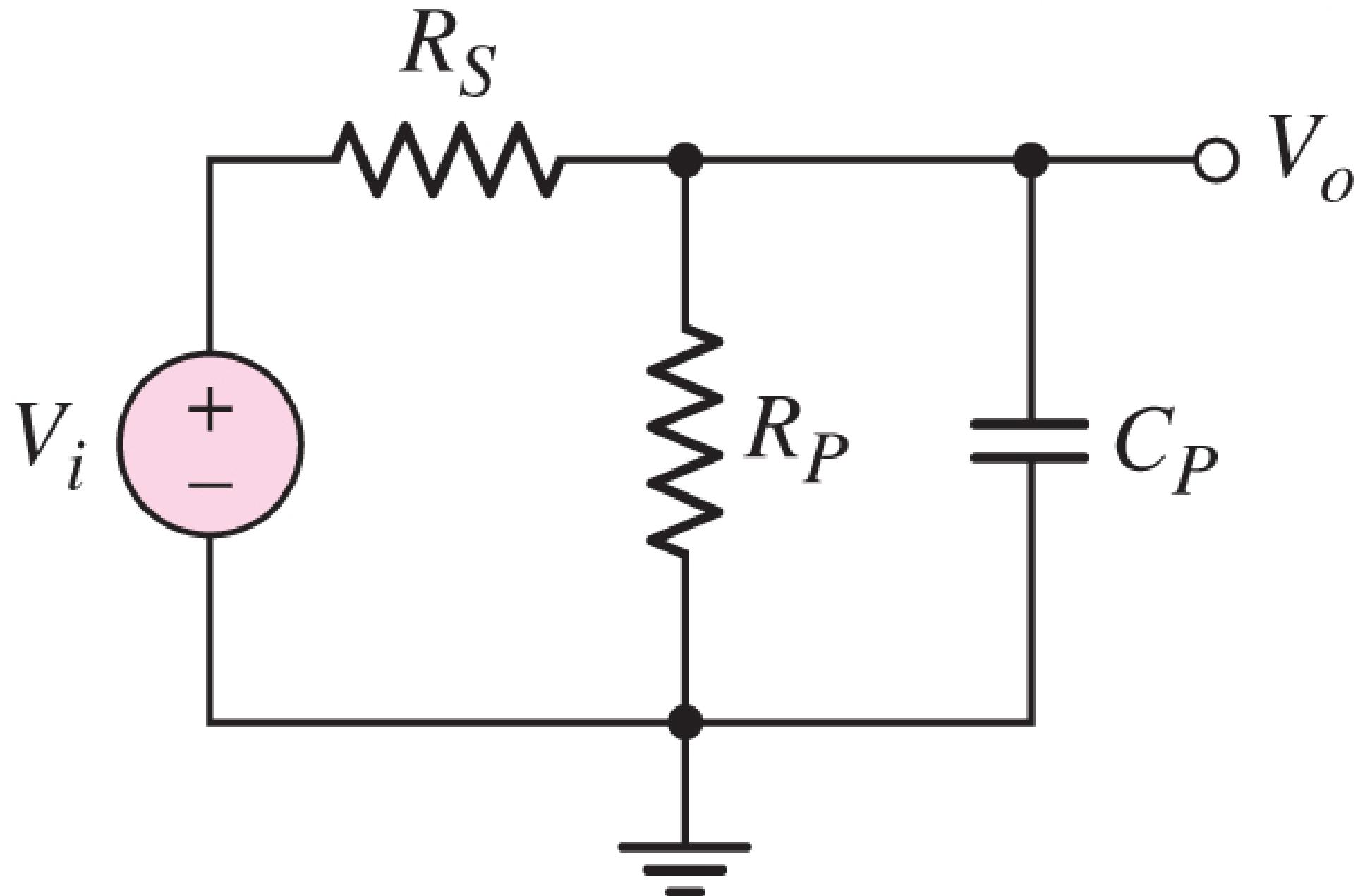


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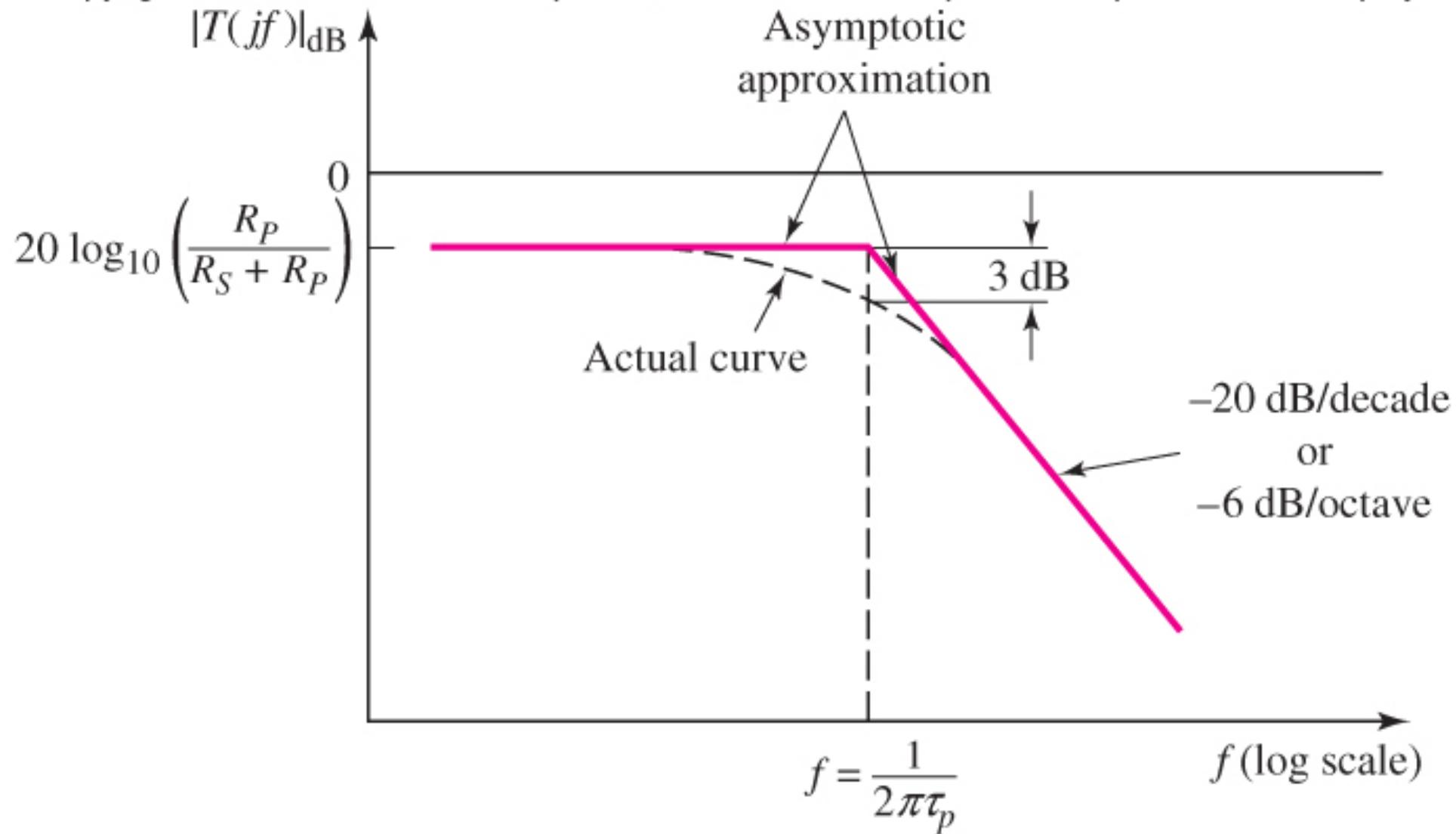


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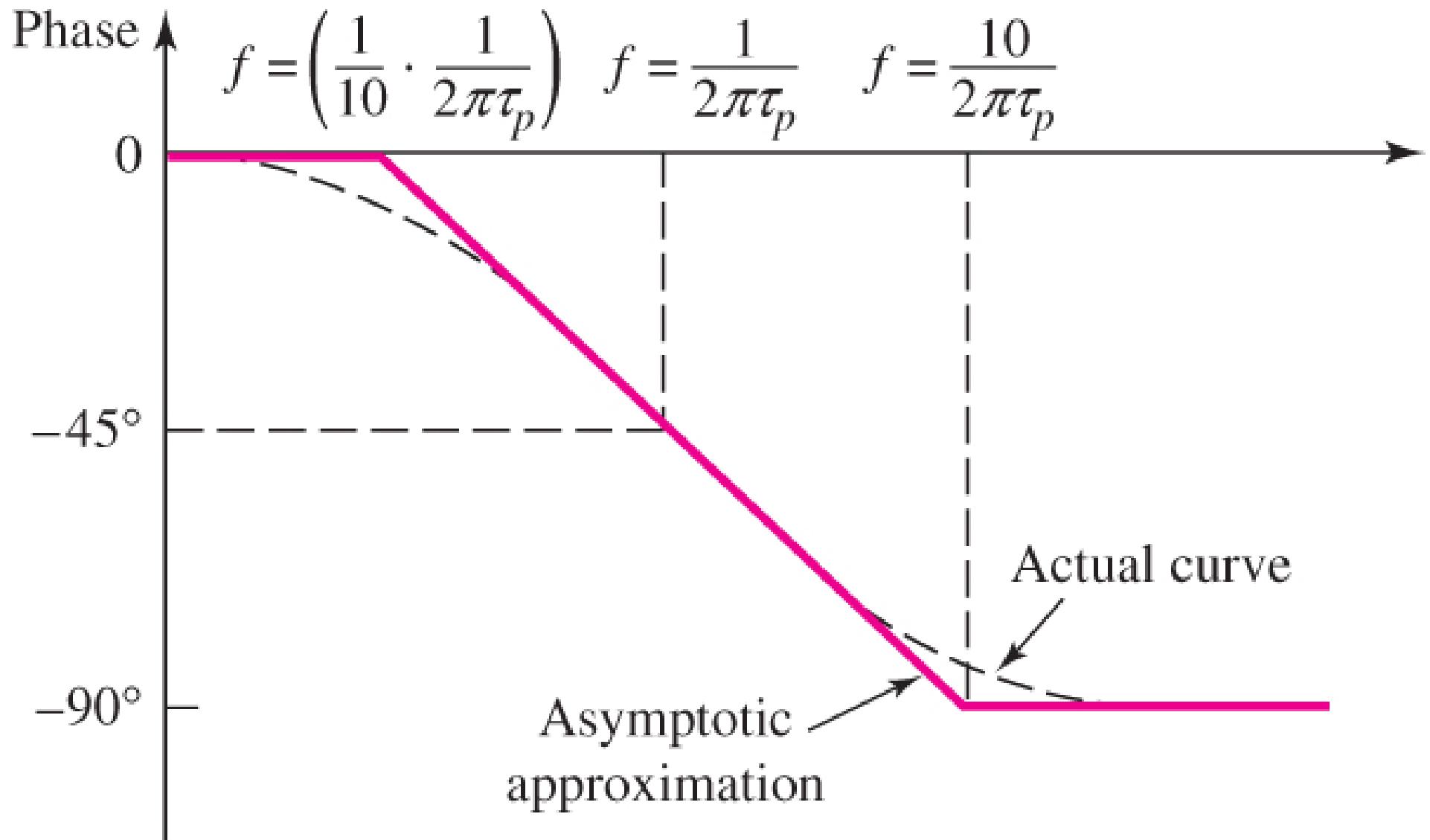


Fig. 7.10

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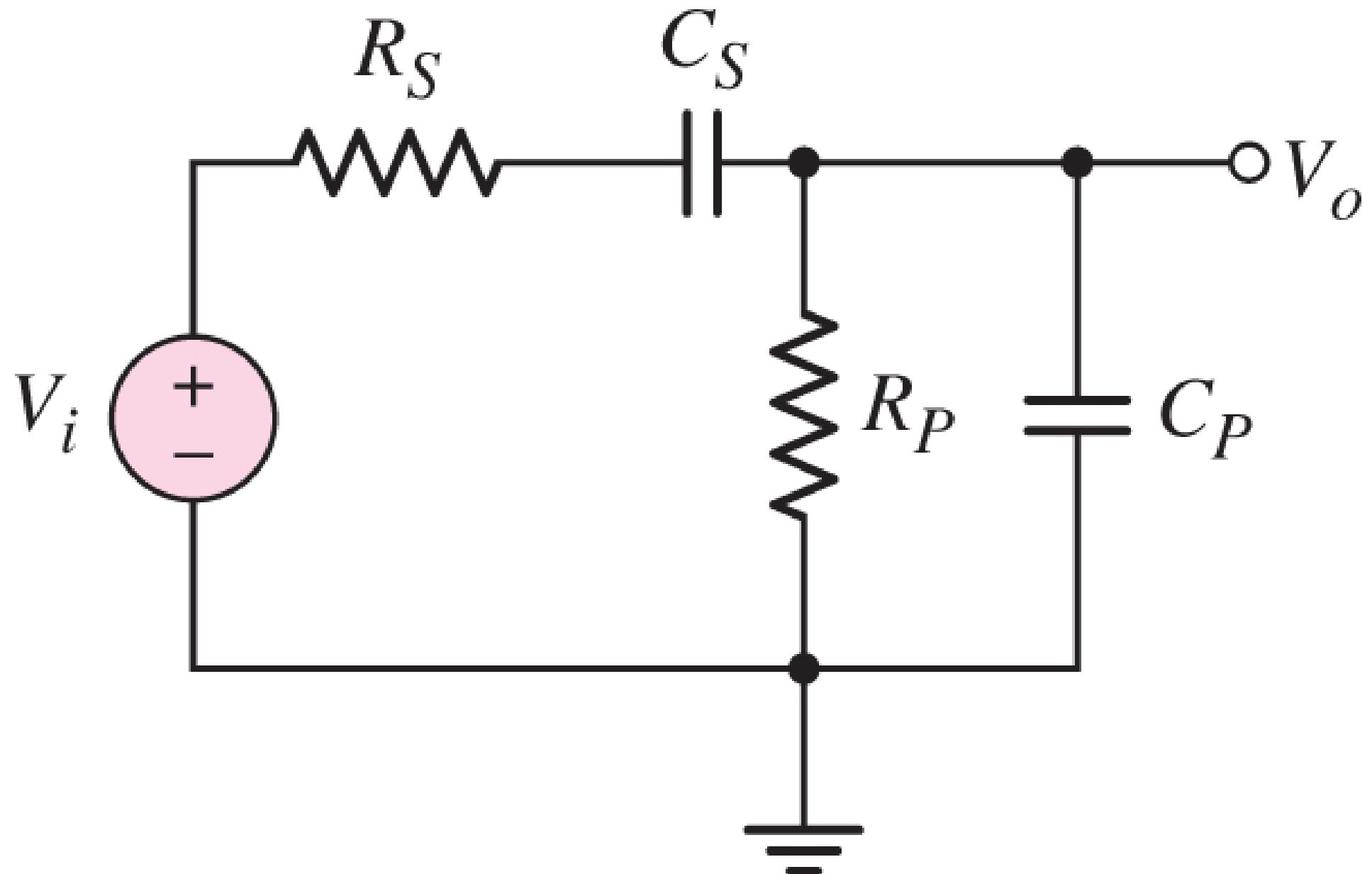


Fig. 7.11

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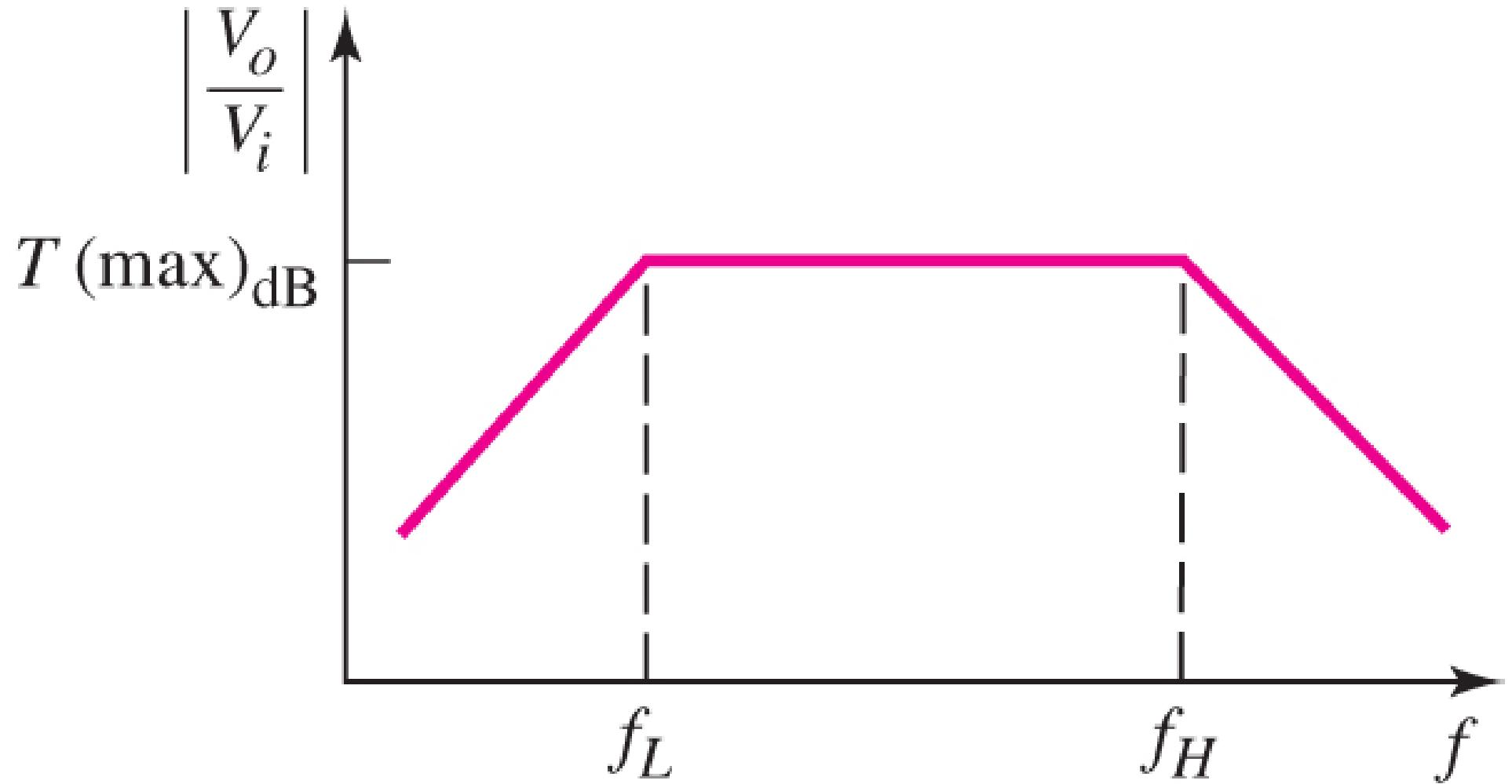
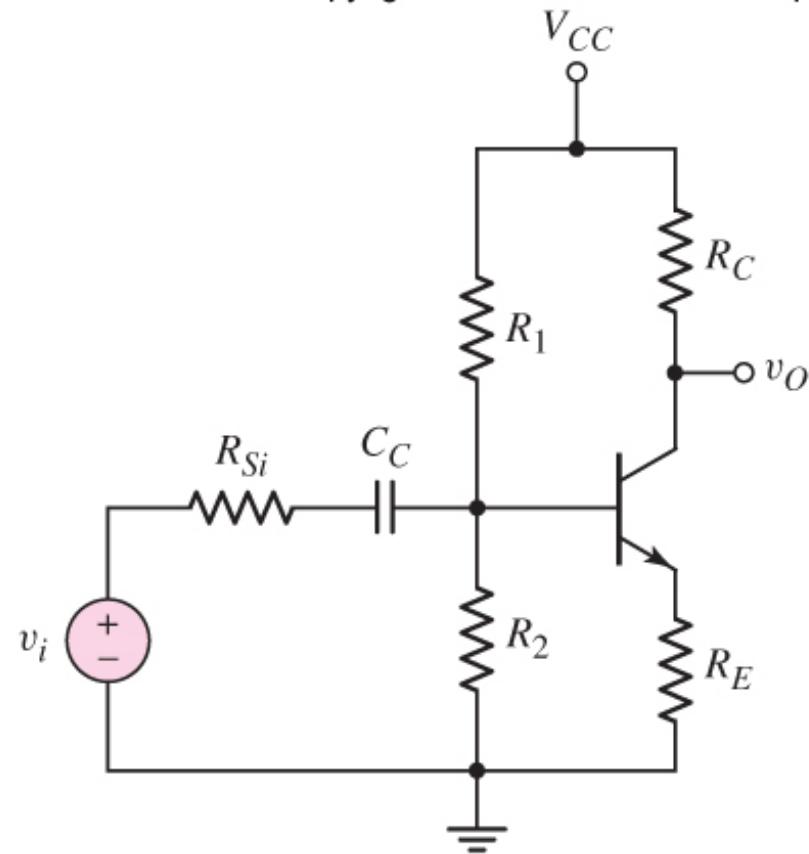
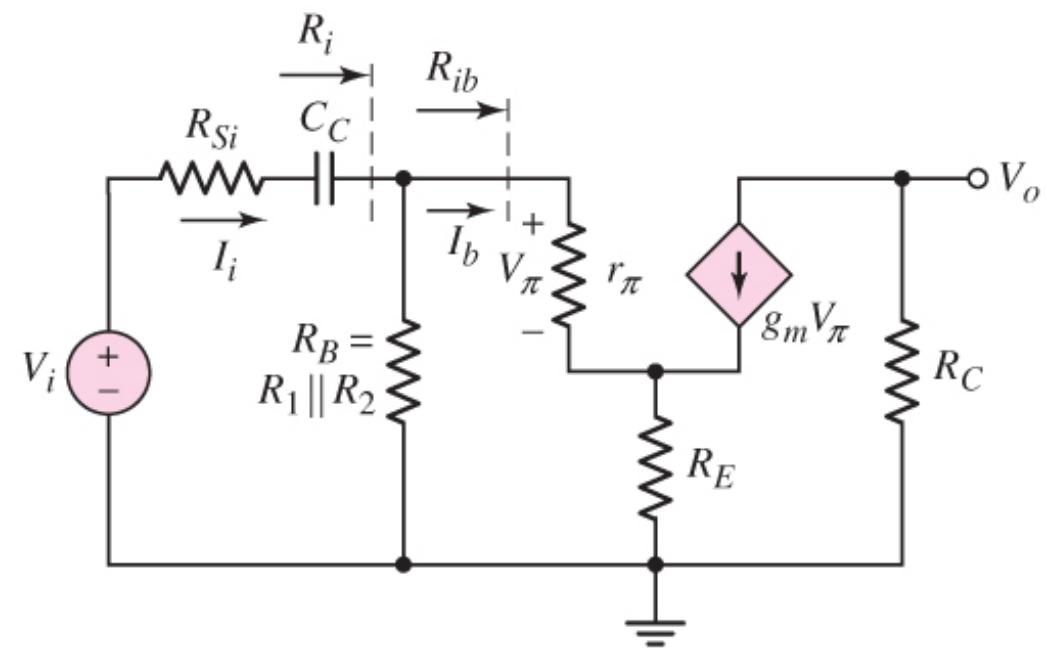


Fig. 7.21

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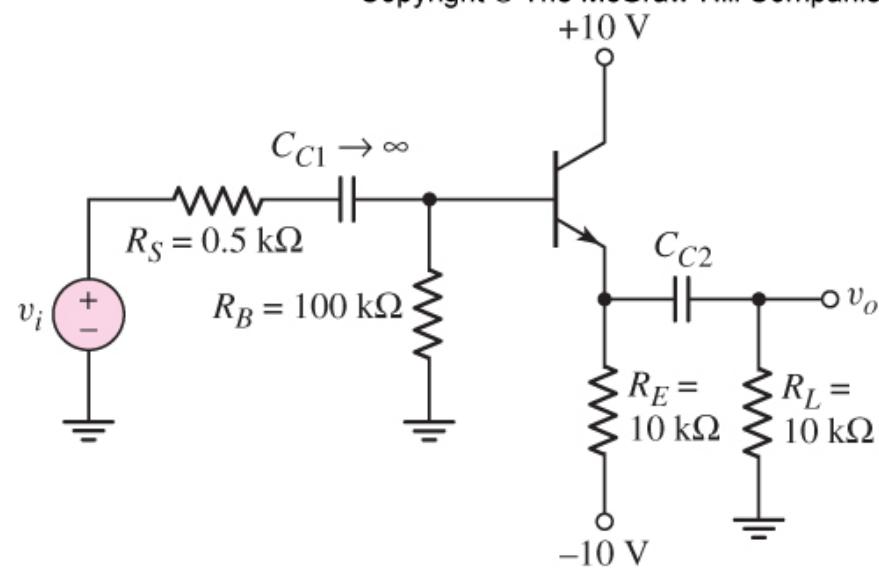
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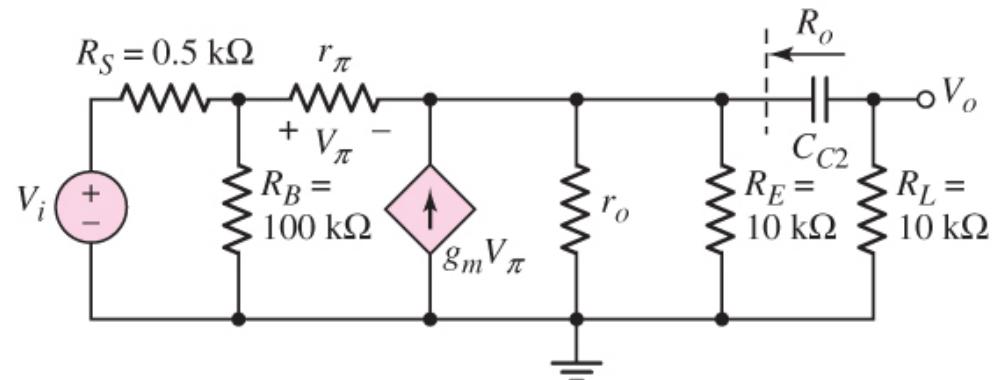
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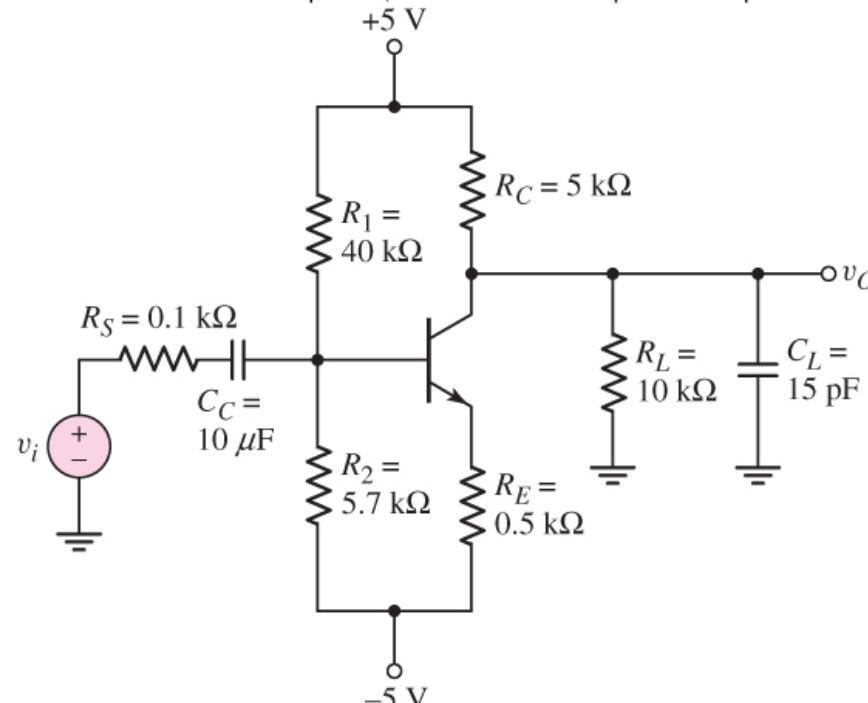
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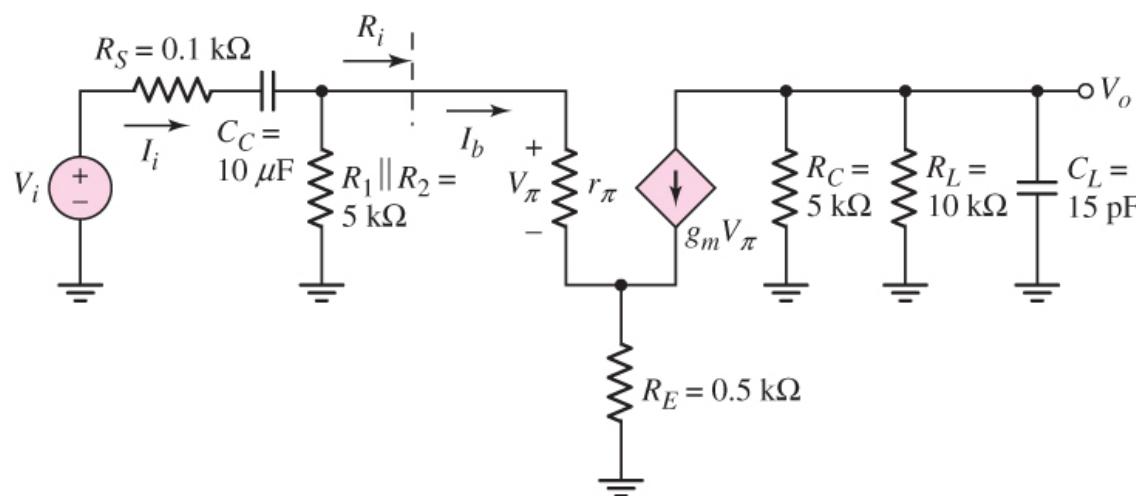
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Fig. 7.26

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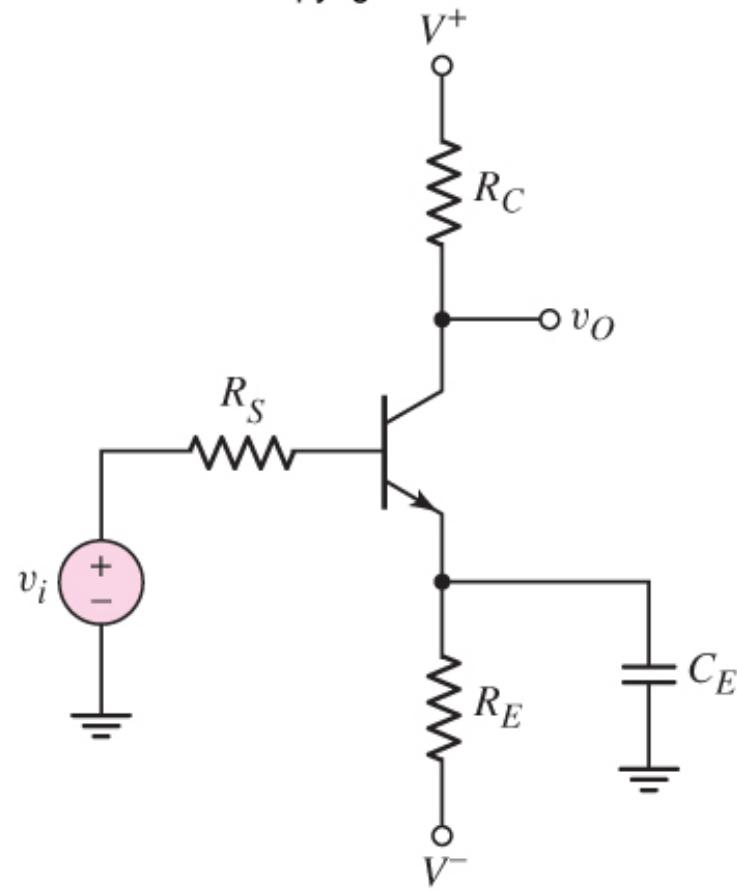
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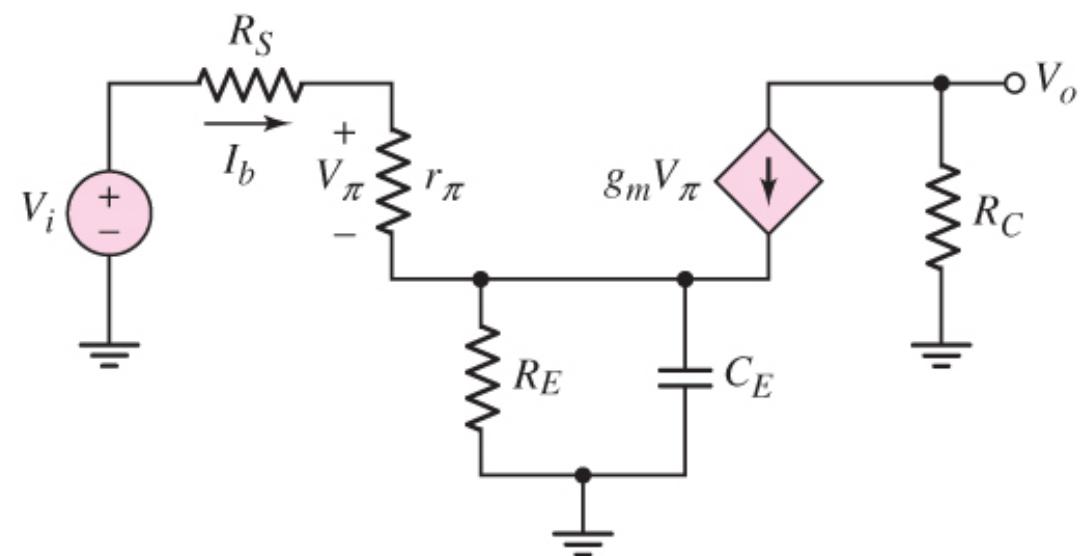
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(a)



(b)

Fig. 7.28

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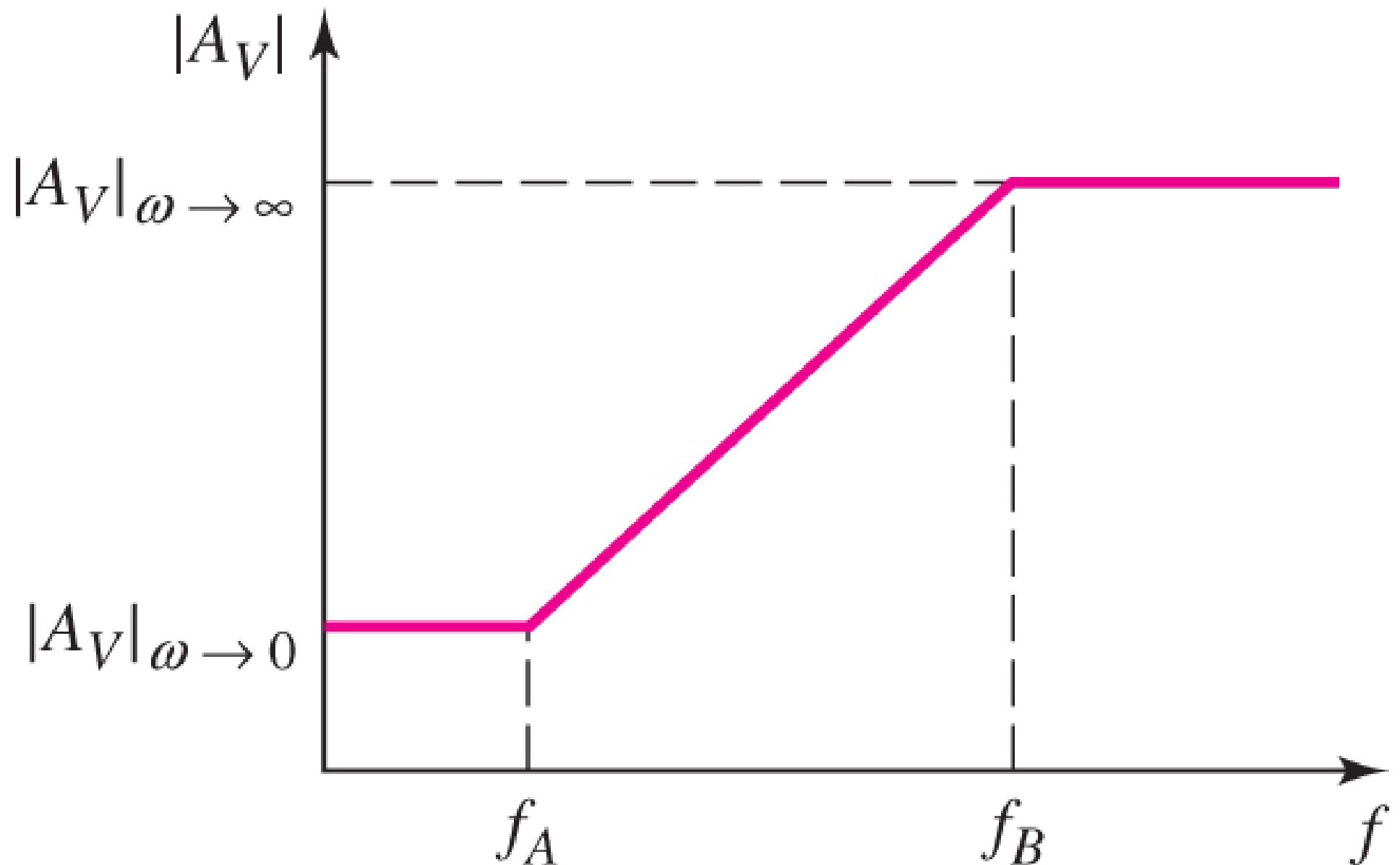


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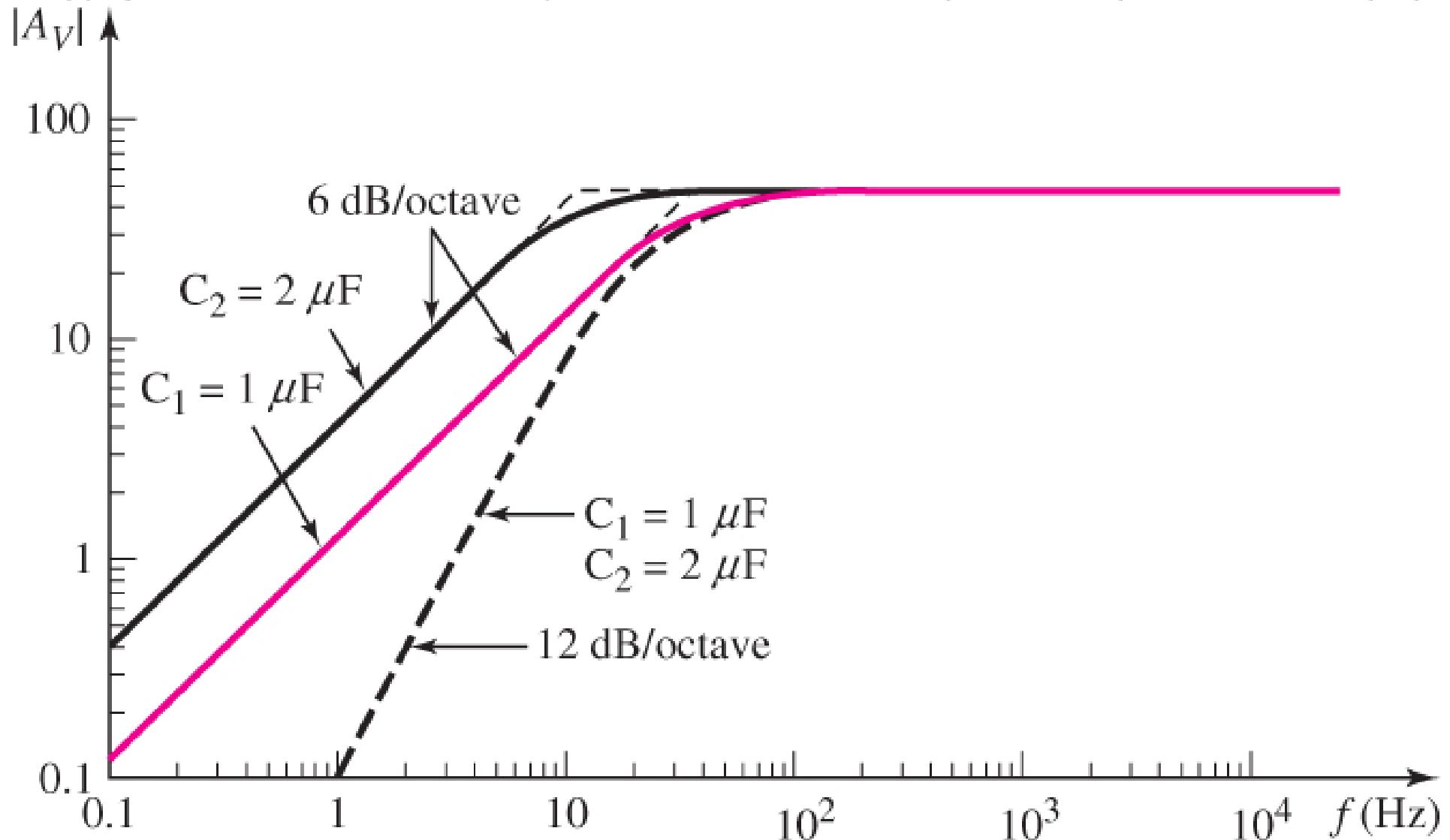
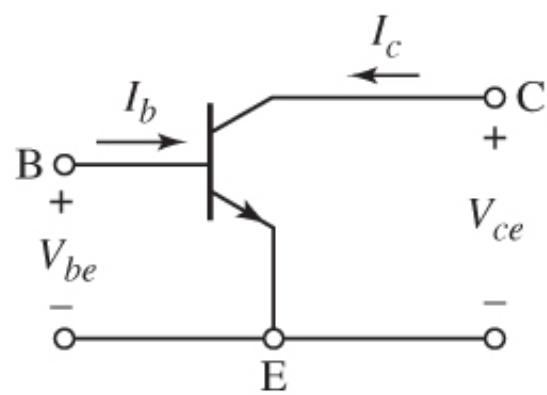
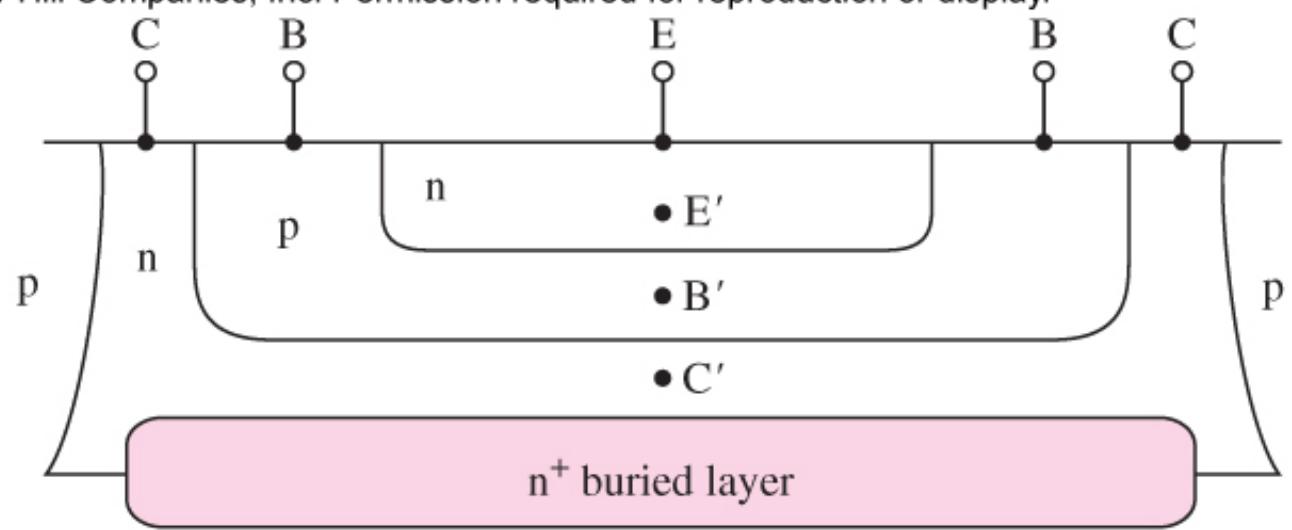


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(a)



(b)

Fig. 7.37

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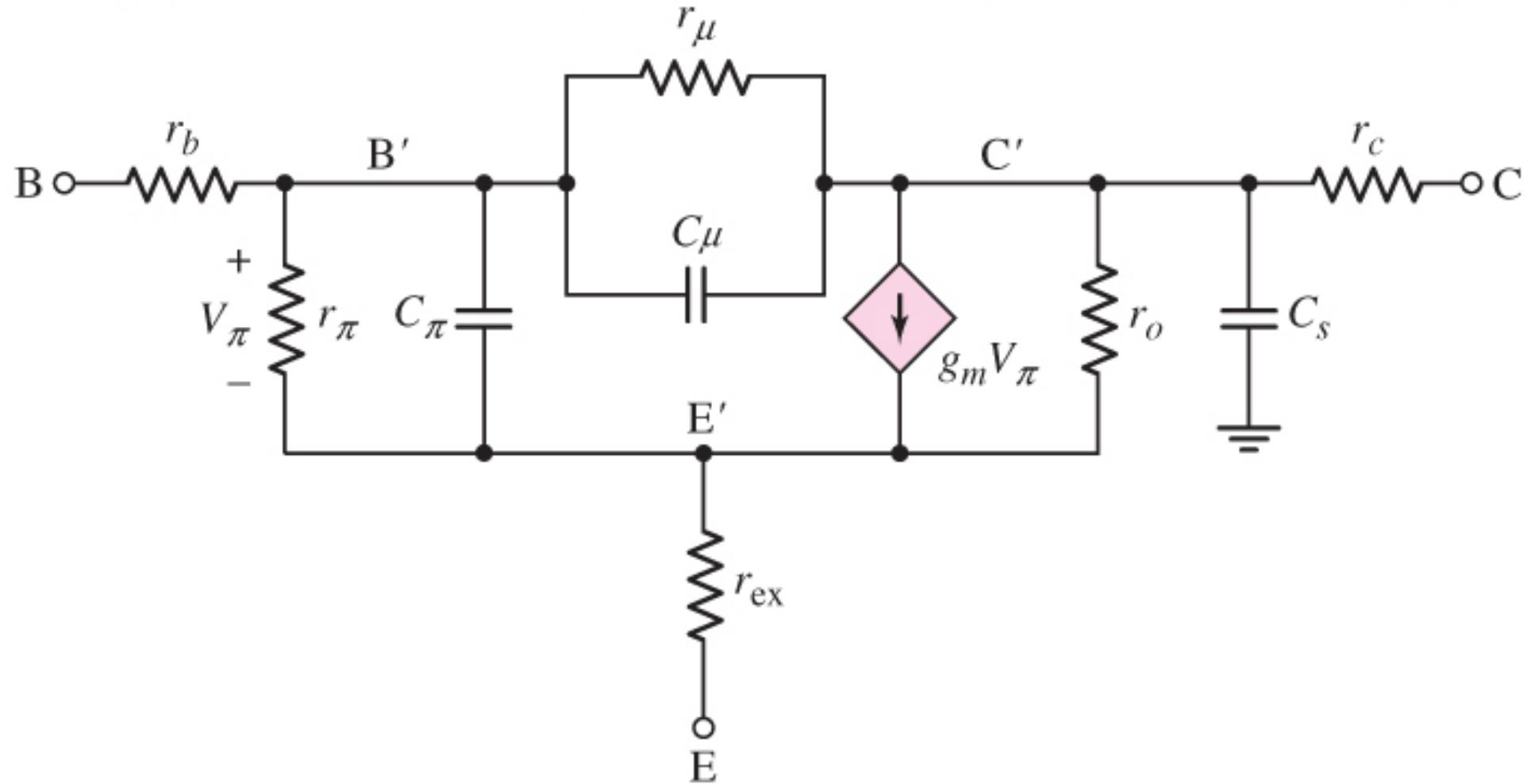


Fig. 7.38

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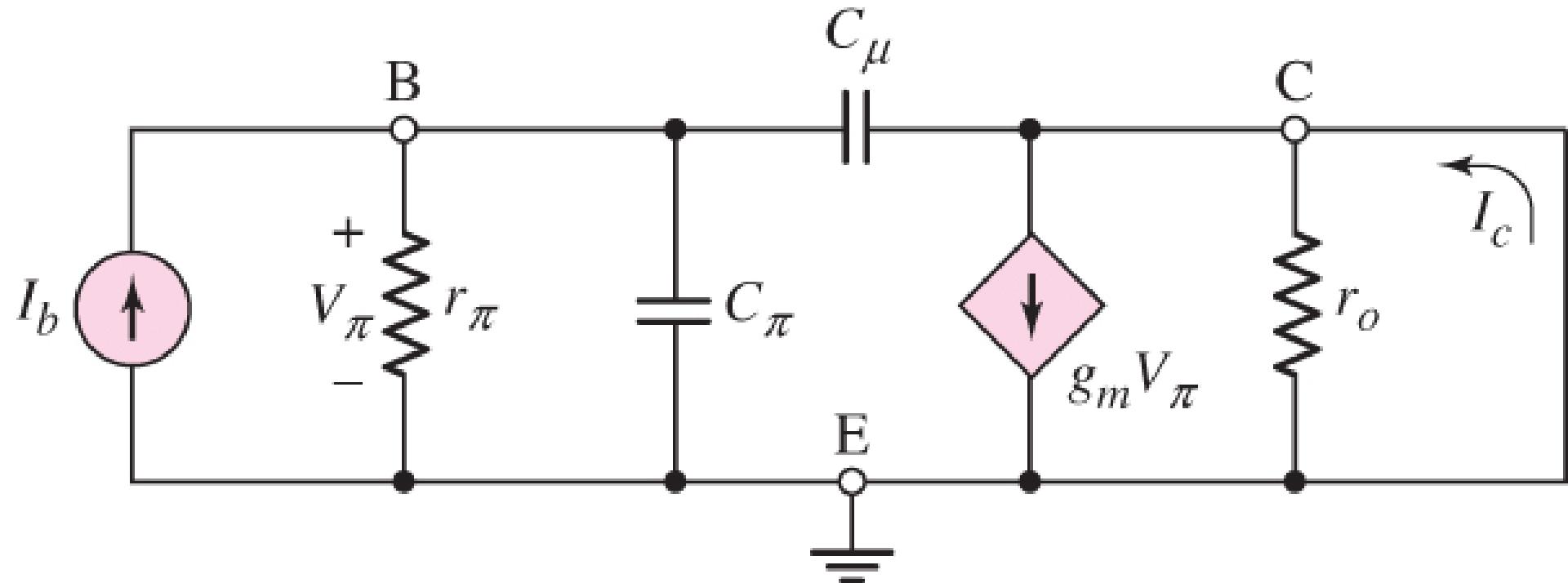
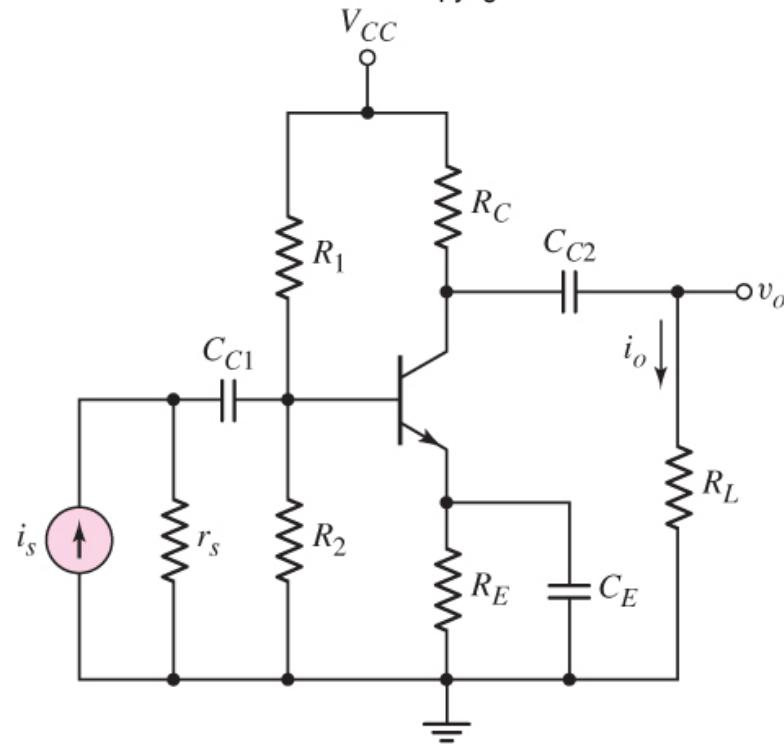
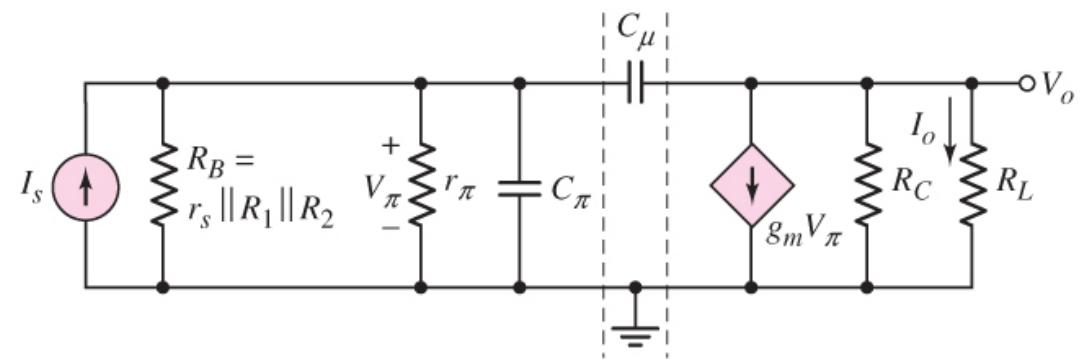


Fig. 7.41

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(a)



(b)

Fig. 7.45

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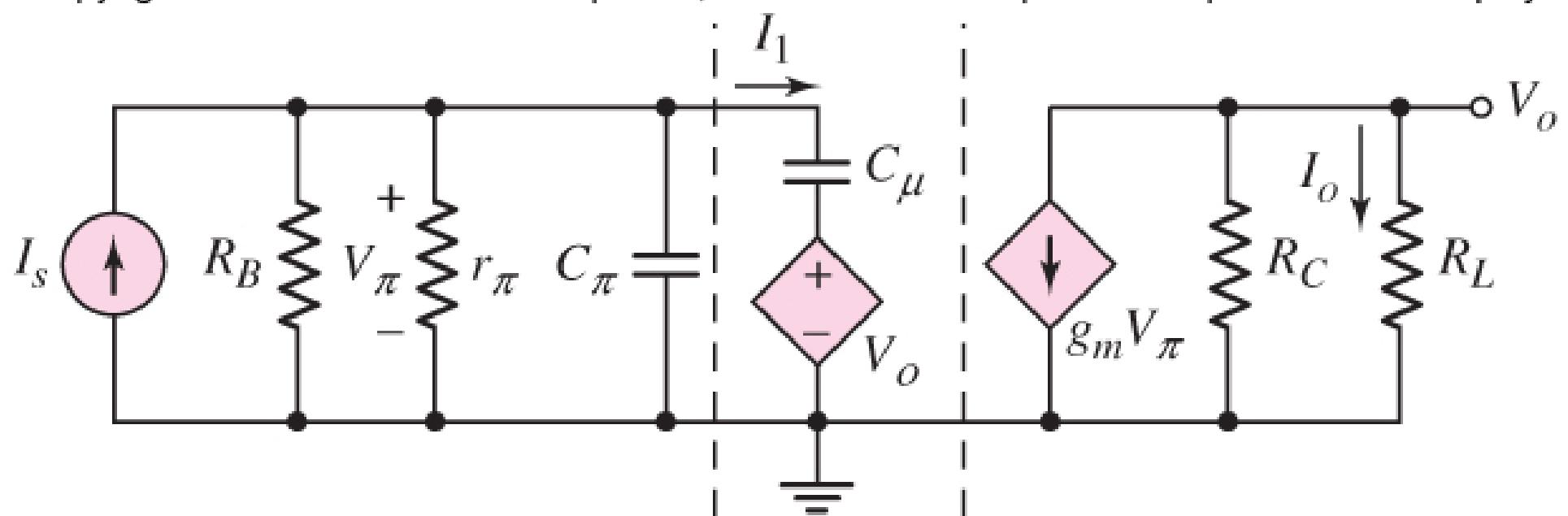


Fig. 7.46

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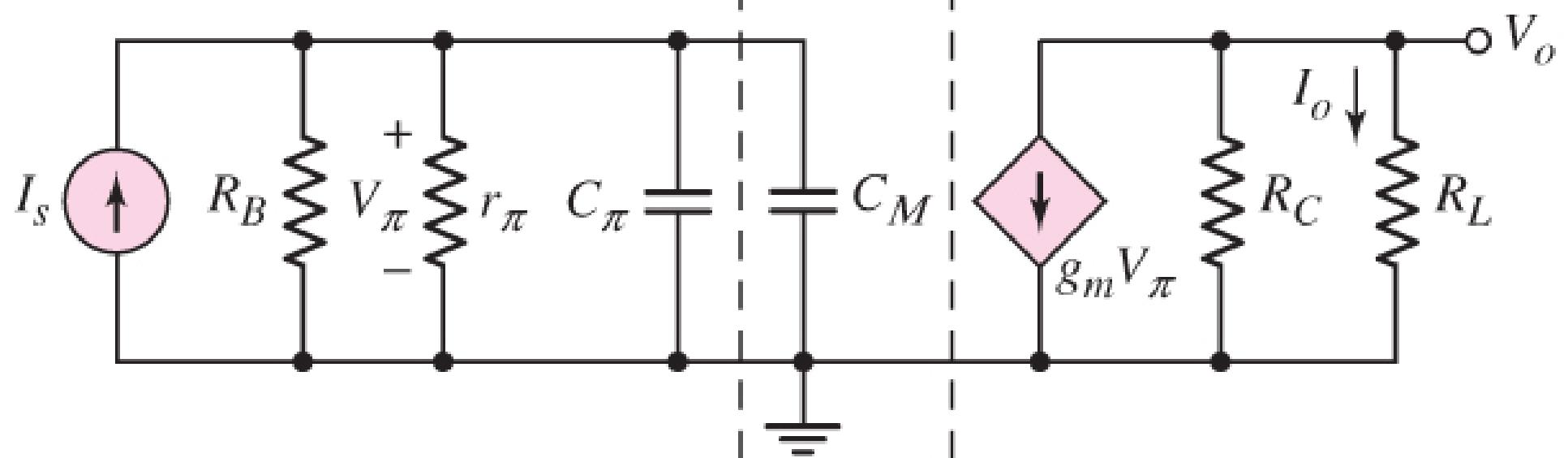


Fig. 7.49

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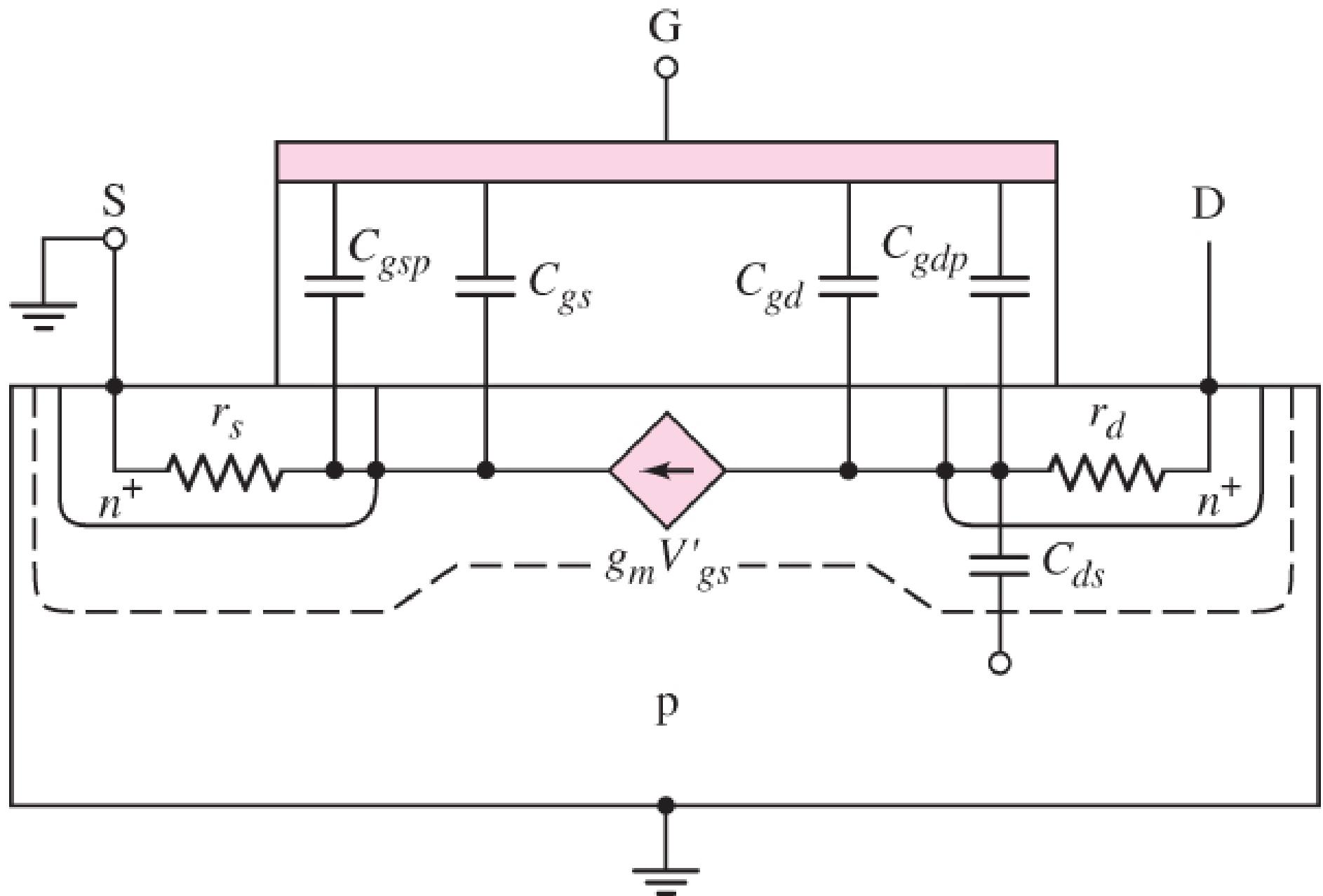


Fig. 7.52

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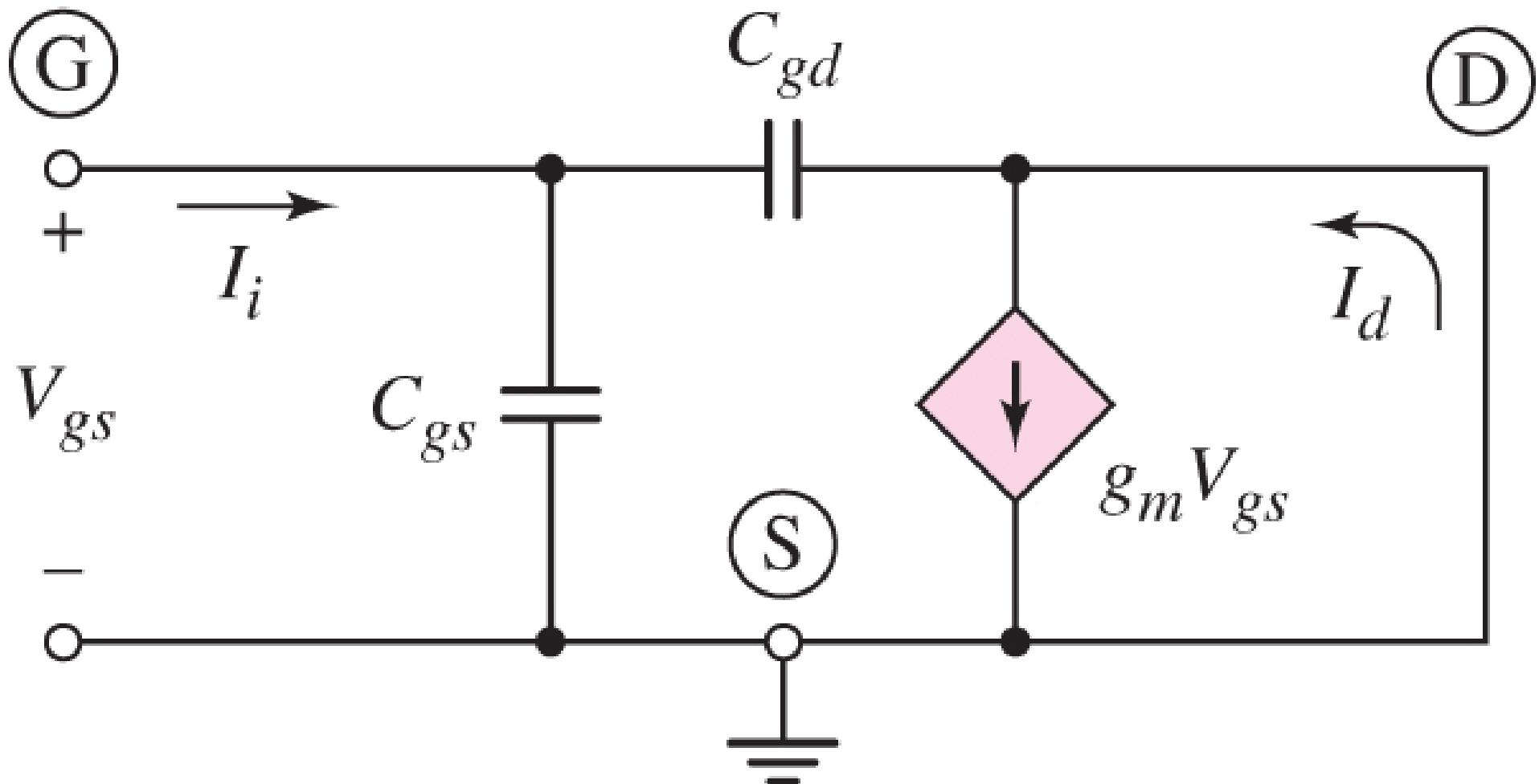


Fig. 7.53

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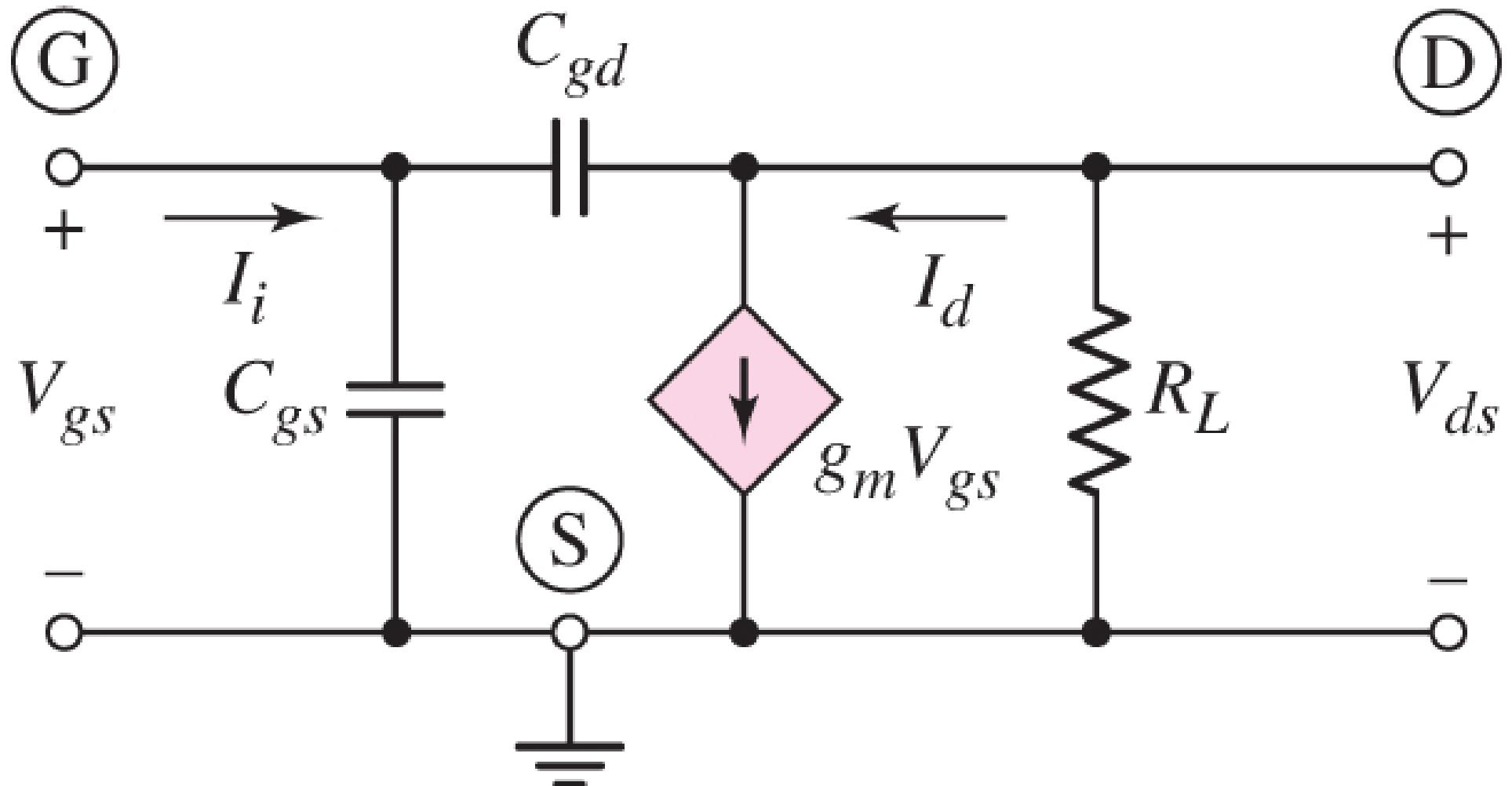
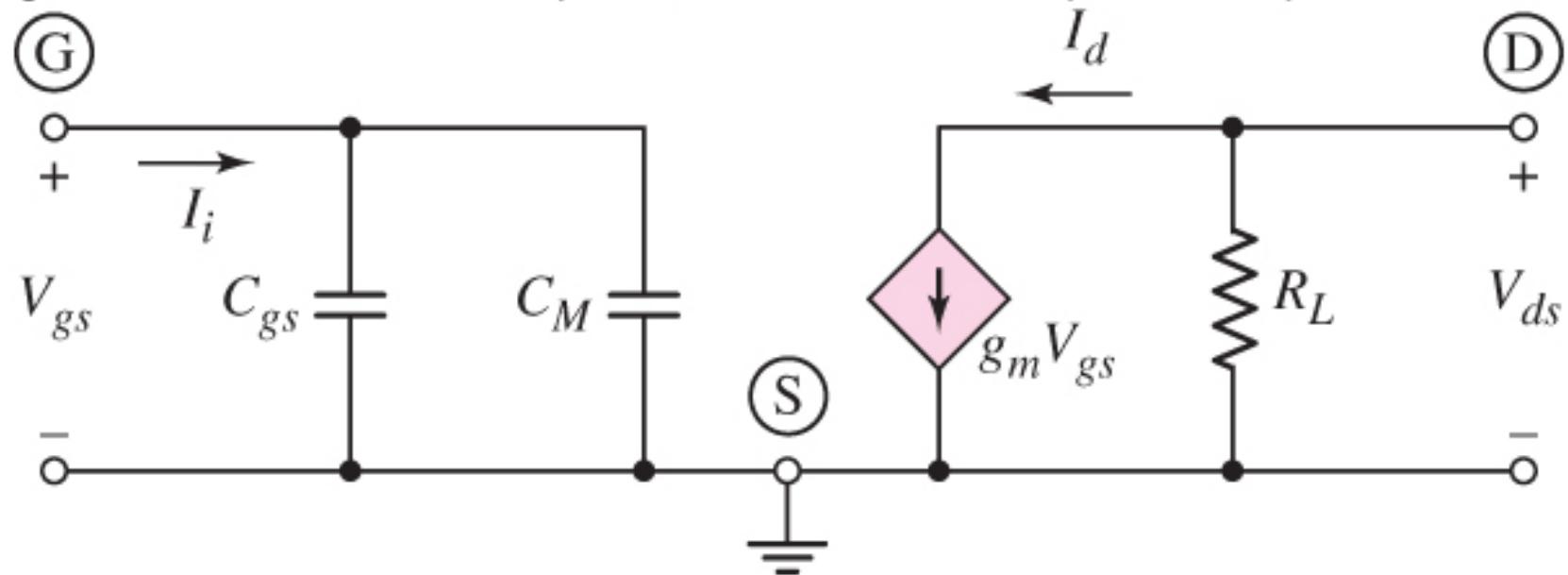


Fig. 7.54

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# Course Feedback

- What did you like about this class?
- What did you not like about this class?
- What did you feel that could be improved for future students
- Some questions to consider
  - Was the course too easy?
  - Would you have liked to see more material covered in the course?
  - What was your feeling about the design project?
  - Did you like the student-centered learning style as opposed to the instructor-centered teaching style?