MXM GRAPHICS MODULE

Specification

MXM Version 2.1A Graphics Module Thermal Electromechanical Specification

November 2007
SP-03493-002_v1.0

Document Change History

Version	Date	Reason for Change
1.0	November 20, 2007	Based on *MXM Version 2.1 Graphics Module Thermal Electromechanical Specification* (SP-03493-001). This document version includes optional support for DisplayPort on DVI_B pins. It also includes the following changes: TV-out changed to optional Reduced GPU zone height to align with current GPUs. Fixed error in Type-III and Type-IV memory zones and thermal mounting locations from MXM v2.1.

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MXM Specification Changes

The following list contains the changes between the *MXM Version 2.0 Graphics Module Thermal Electromechanical Specification* (SP-03026-001_v1.2) and the *MXM Version 2.1A Graphics Module Thermal Electromechanical Specification* (SP-03493-002_v1.0).

- Remove Thermal Transfer Plate (TTP)
- Remove captive screws
- Define mechanicals for system integration holes
- Define mechanicals for thermal attachment holes
- Define module component keep out
- Define system thermal solution keep out
- Assign new pinout for DisplayPort support
- Assign new pinout for HD audio support
- Remove pinout for **IGP_RSVD** support
- Changed TV from required to optional
- Reduced the GPU zone component keep out to align with current products
- Reduced the GPU zone thermal keep out to align with current products

Introduction

The Mobile PCI Express Module (MXM) version 2.1A is a standard graphics interface for PCI Express systems. The specification describes the electromechanical interfaces for the MXM version 2.1A Graphics Module™.

MXM has evolved beyond the notebook space and is now used wherever there is a need for low power, high graphic computation density or the combination of both. As such MXM is now present in blade servers, mobile workstations, living room PCs and small form factor PCs.

An MXM v 2.1A module is identified by its type (I to IV). Each type has a distinct form factor and is aimed at different performance requirements and power consumption.

Applicable Documents

The following documents contain provisions which through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. However, users of this standard are advised to ensure they have the latest versions of referenced standards and documents.

- EIA-364-9 – *Durability Test Procedure for Electrical Connectors and Contacts*
- EIA-364-28D – *Vibration* Test Procedure for Electrical Connectors and Sockets
- EIA-364-27B – *Mechanical* Shock (Specified Pulse) Test Procedure for Electrical Connectors
- EIA-364-23B – *Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets*
- EIA-364-13C – *Mating and Unmating Forces Test Procedure for Electrical Connectors*
- EIA-364-21C – *Insulation Resistance Test Procedure for Electrical Connectors, Sockets and Coaxial Contacts*
- EIA-364-20C – *Withstanding Voltage Test Procedure for Electrical Connectors, Sockets and Coaxial Contacts*
- EIA-364-108 – *Impedance, Reflection Coefficient, Return Loss and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Cable Assemblies or Interconnection Systems*
- EIA-364-101 – *Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems*
- EIA-364-90 – *Crosstalk Ratio Test Procedures for Electrical Connectors, Sockets, Cable Assemblies or Interconnect Systems*
- EIA-364-1000.1 – *Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications*
- ASME Y14.5M – *Dimensioning and Tolerancing Standard*

- SP-03494-001 – *MXM Version 2.1 Graphics Module Software Specification*
- *PCI Express Base Specification* document version 1.1 or earlier
- *SPWG Notebook Panel Specification*, Version 3.0
- *Digital Visual Interface (DVI*), Version 1.0
- HDMI 1.1 or higher – *High-Definition Multimedia Interface (HDMI) Specification*
- *VESA DisplayPort Standard*, Version 1.1
- *Intel High Definition Audio Specification,* Version 1.0

Key Features

- Low cost
- Small size
- Scalable performance
- 16 lane PCI Express support
- LVDS panel support
- Dual DVI support
- DisplayPort support
- VGA support
- TV-out support
- HDMI™ support
- Upgradeable graphics

Configurations

Table 1 lists the dimensions for the four MXM v 2.1A graphics module types.

Table 1. Board Configurations

MXM Type	Width	Length
MXM-I	70 mm	68 mm
MXM-II	73 mm	78 mm
MXM-III	82 mm	100 mm
MXM-IV	82 mm	117 mm

Display Support

Table 2 lists the MXM v 2.1A graphics boards supported displays.

Table 2. MXM V 2.1A Display Support

Display	MXM Display Solutions
VGA	Routed to either VGA or DVI-I connectors on motherboard
Two single-link DVI or One dual-link DVI or two dual-link DVI	DVI routed to connector on motherboard and/or through docking station
TV-out	TV-out routed to connector on motherboard, Supports Composite, S-video and HDTV
Dual-link LVDS	LVDS routed to connector on the motherboard.
HDMI technology	HDMI routed to connector on motherboard and/or through docking station
One DisplayPort	Routed to connector on motherboard and/or through docking station

MXM v 2.1A Display Options

MXM v 2.1A module must support the following interfaces:

- One dual-link LVDS panel display
- One VGA output
- One single-link DVI output

MXM v 2.1A module shall *optionally* support the following interfaces:

- Two single-link DVI outputs
- One dual-link DVI output
- Two dual-link DVI outputs
- HDMI output
- One TV output
- One DisplayPort

All interfaces are routed through the MXM connector to the motherboard. The implementation of display interfaces on the MXM system is left solely to the discretion of the MXM system designer. All display interfaces are optional on the MXM motherboard.

If a system implements any optional interface that is not supported by the installed MXM graphics module, then the display will not be supported by the configured system.

Module Form Factors and Mechanical Keep Outs

Each type of the MXM modules has its own form factor and distinct mechanical keep outs. These keep outs are a combination of z-height restrictions and surface keep outs on the MXM module. The keep outs are necessary for system and thermal solution integration compatibility.

The GPU must be placed at the center of the GPU zone whereas the memories can be placed within the memory zone if a direct contact between the memories and the cooling system is desired. The following keep out definitions include a 0.5 mm clearance from the thermal solution in the x and y direction.

For module types I and II, the four holes surrounding the GPU which are used for thermal attachment will have a 3 mm finished hole with a 6 mm topside grounded pad. For module types III and IV, the four holes will have a 4.5 mm finished hole with a 6 mm topside grounded pad.

The two system integration holes for type I through III and the three integration holes for type IV all have the same size and shall have a 3 mm finished hole with a 6 mm grounded pad on top and bottom.

Figure 1 shows a side view of the general z-height restrictions for all MXM graphics modules unless otherwise specified. In all the following figures which describe the keep out zones, the zones marked with a specified z-height will use the specified restriction and the zones without a marked z-height follow this general z-height restriction: 3.5 mm on the front side and 1.2 mm on the back side.

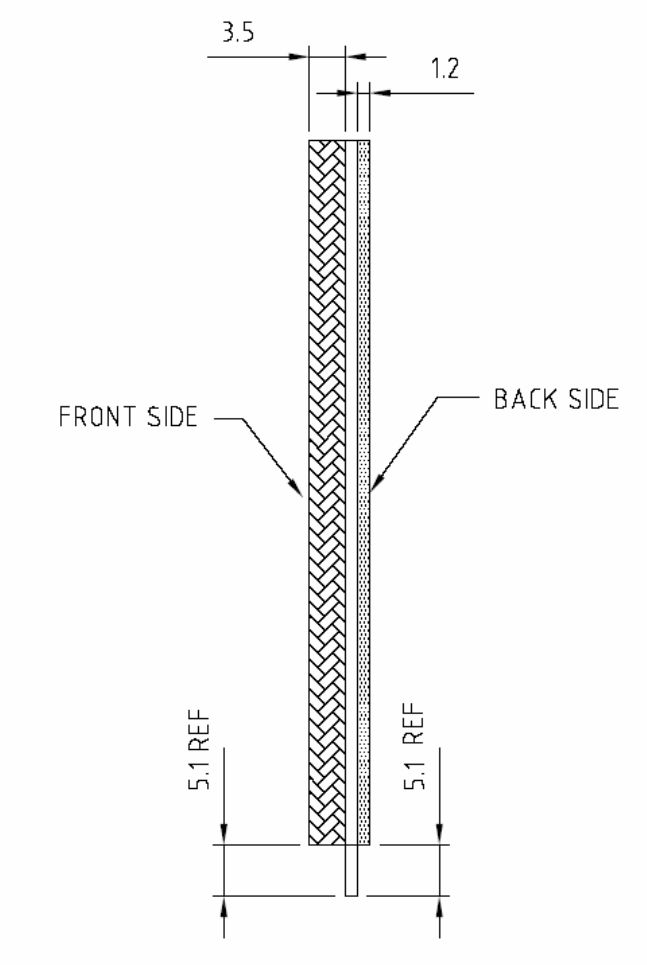

Figure 1. MXM Front Side and Back Side Height Restrictions

MXM-I PCB and Component Keep Outs

Figure 2 through Figure 4 show the MXM-I PCB and component keep outs.

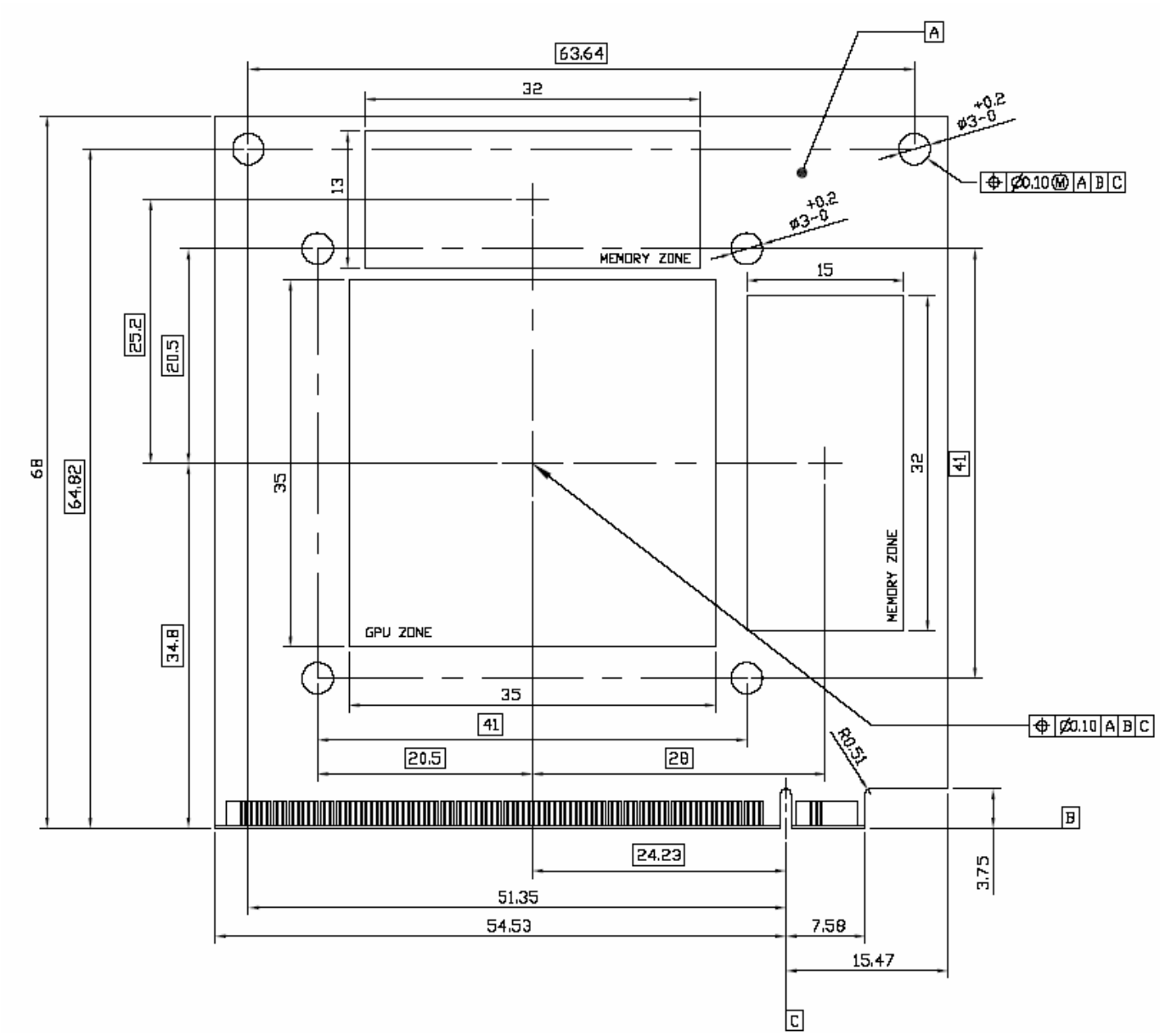

Figure 2. MXM-I PCB Top View

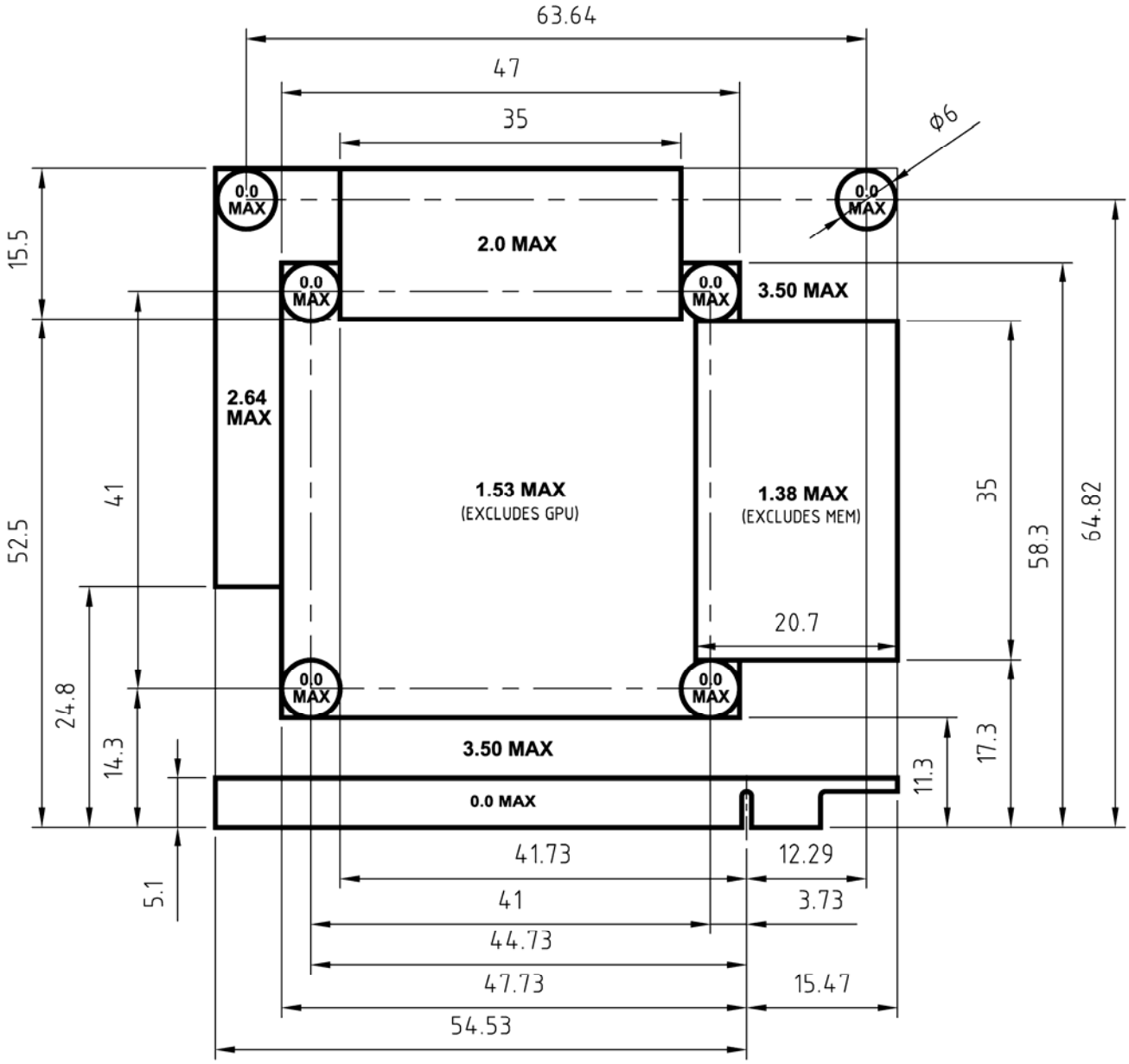

Figure 3. MXM-I Component Keep Outs Top View

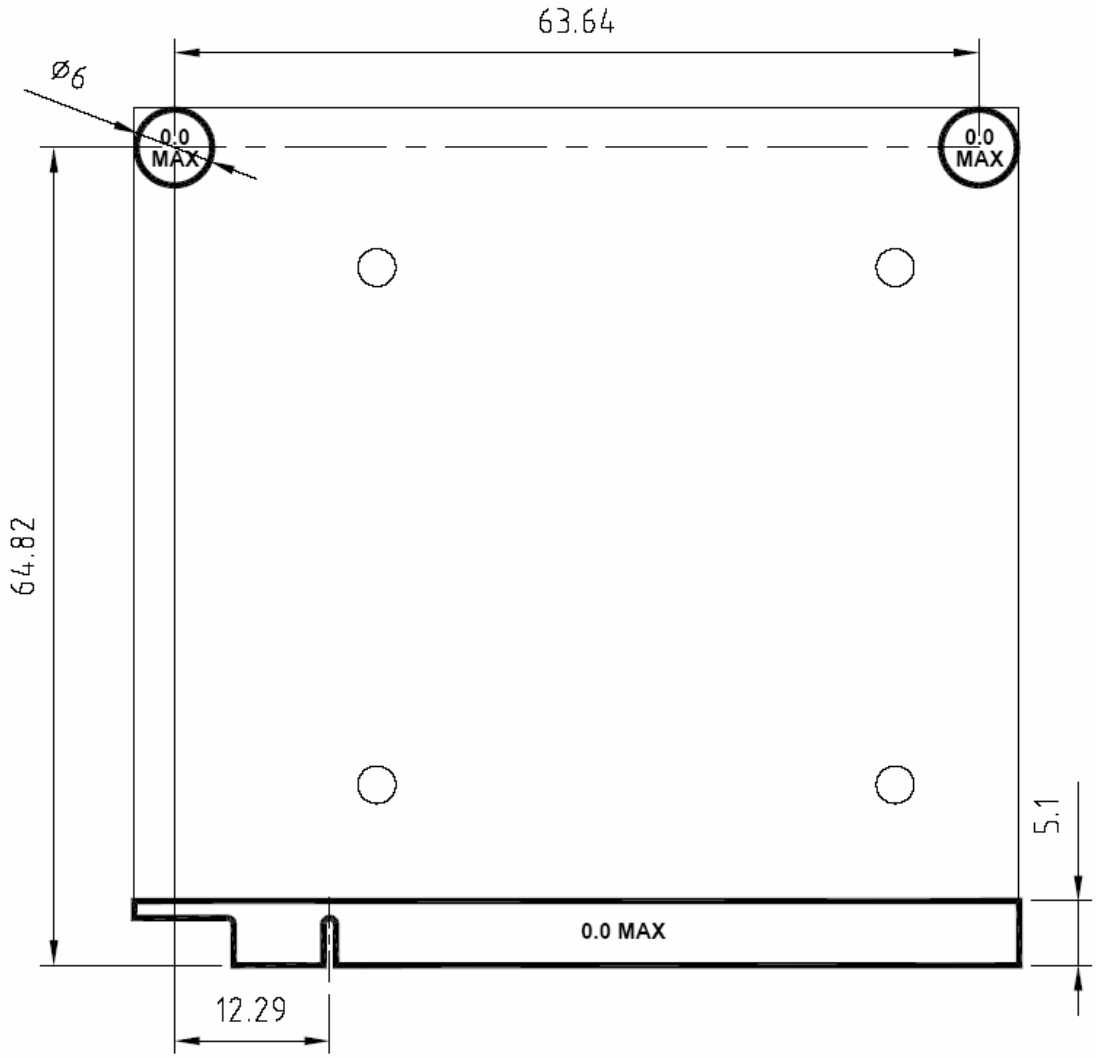

Figure 4. MXM-I Component Keep Outs Bottom View

MXM-II PCB and Component Keep Outs

Figure 5 through Figure 8 show the MXM-II PCB and component keep outs.

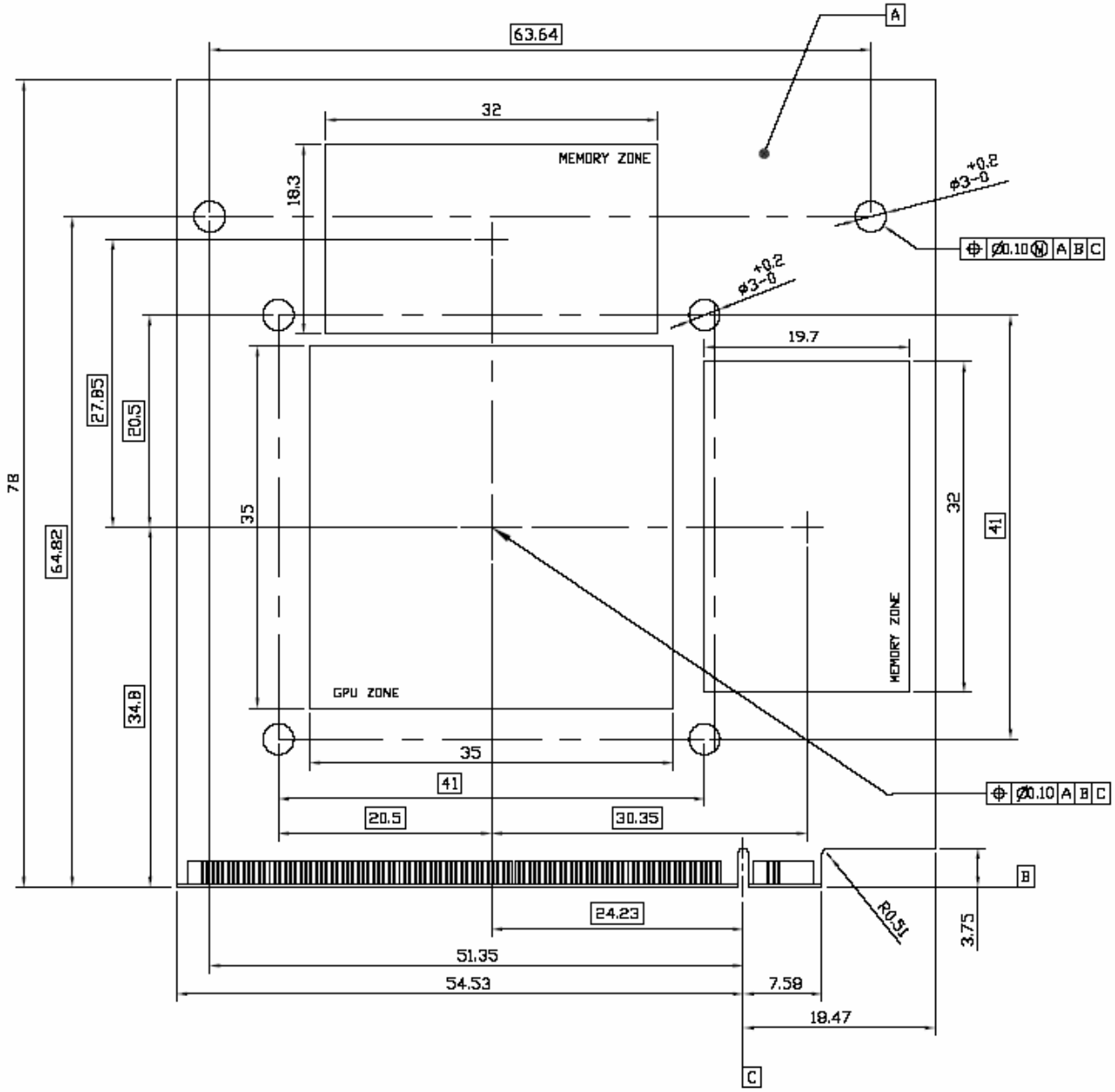

Figure 5. MXM-II PCB Top View

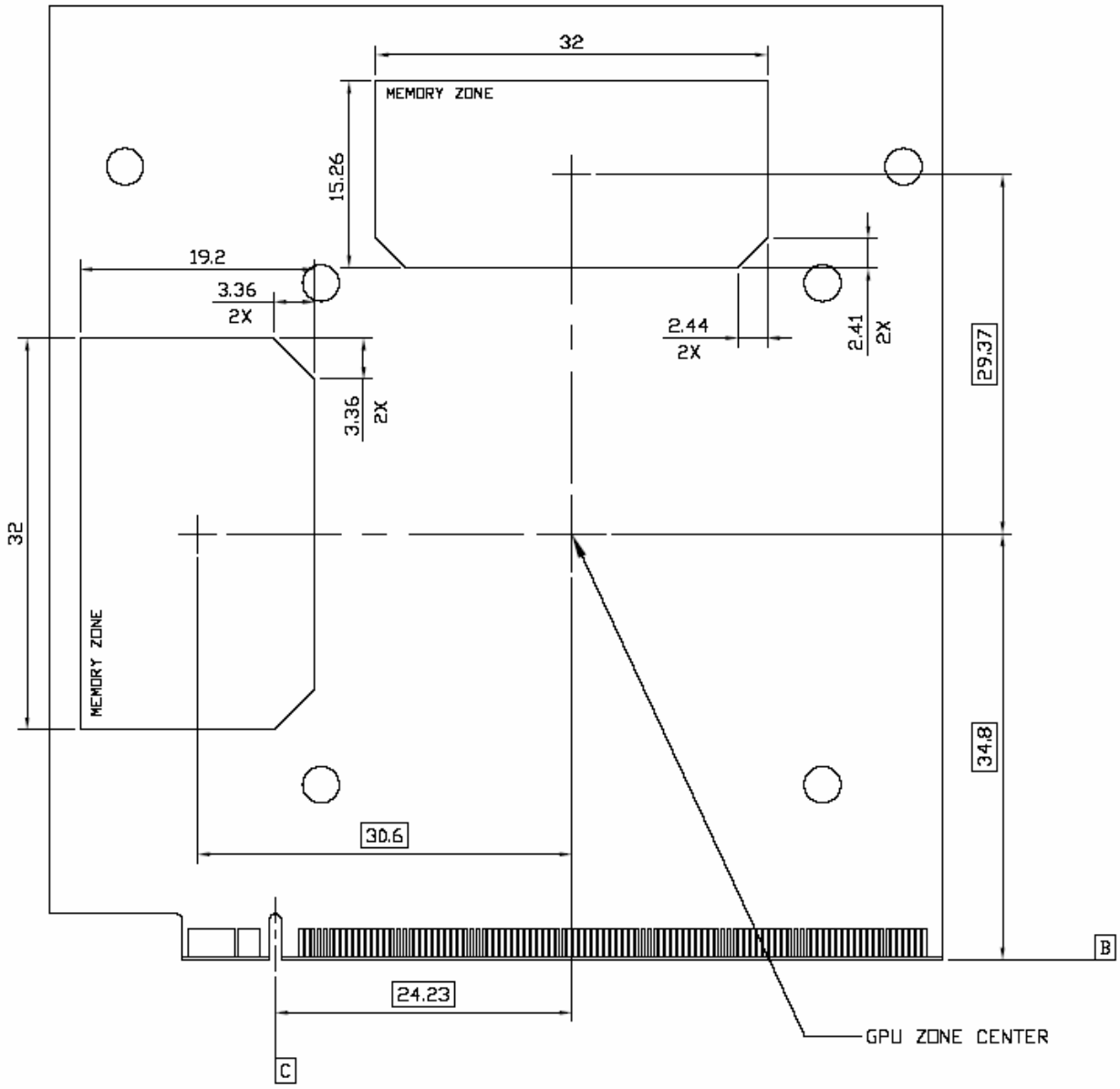

Figure 6. MXM-II PCB Bottom View

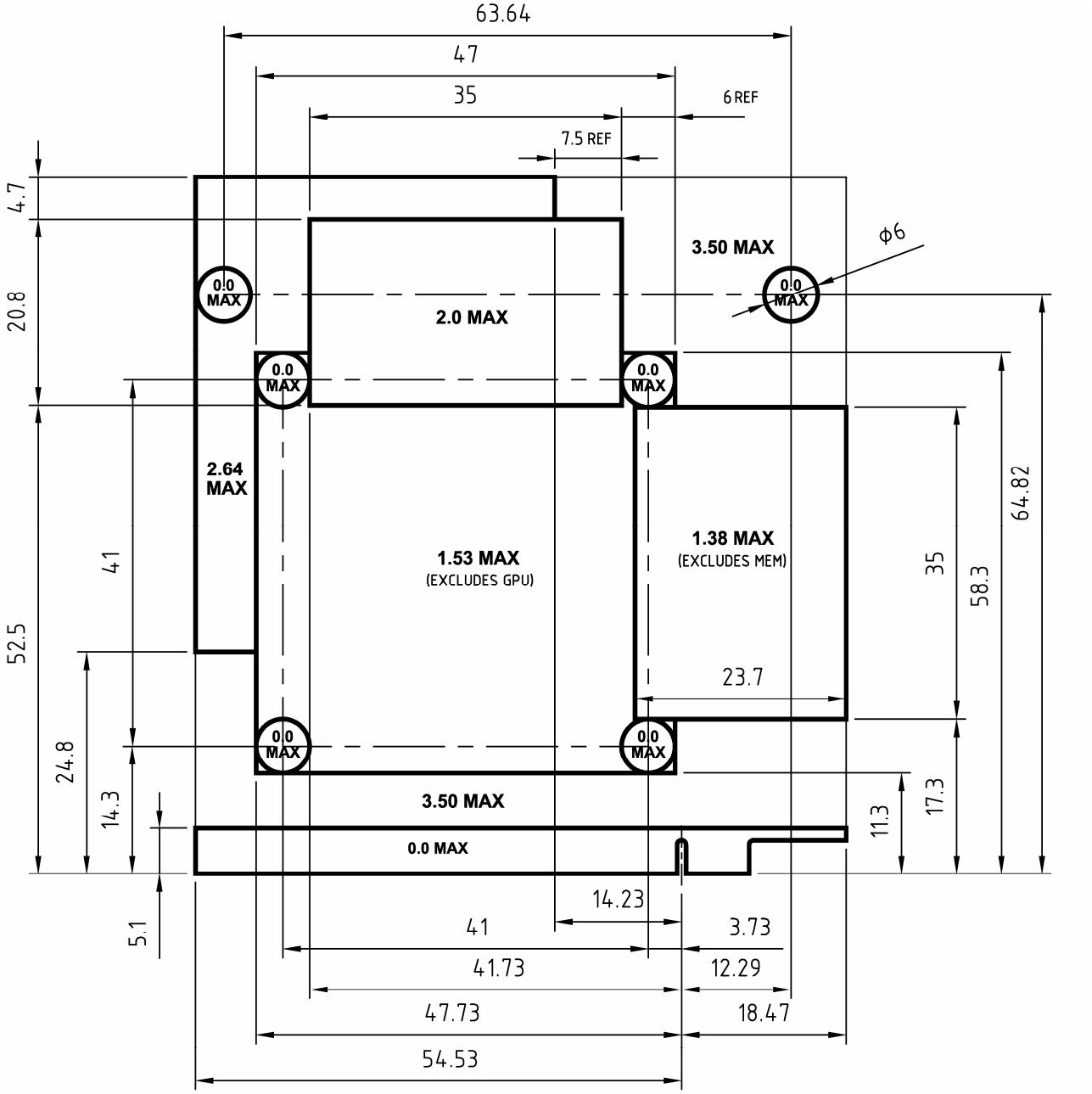

Figure 7. MXM-II Component Keep Outs Top View

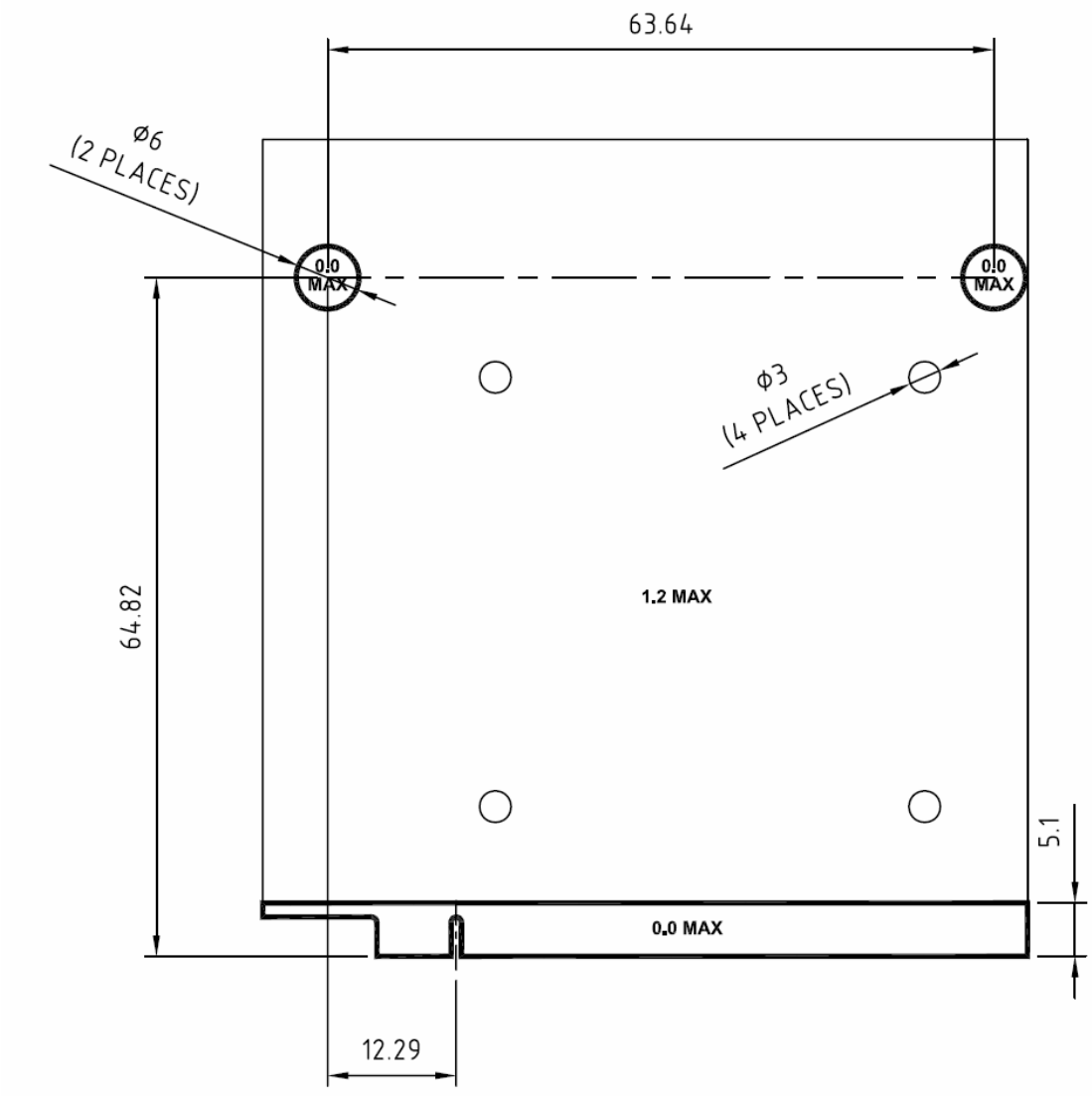

Figure 8. MXM-II Component Keep Outs Bottom View

MXM-III PCB and Component Keep Outs

Figure 9 through Figure 12 show the MXM-III PCB and component keep outs

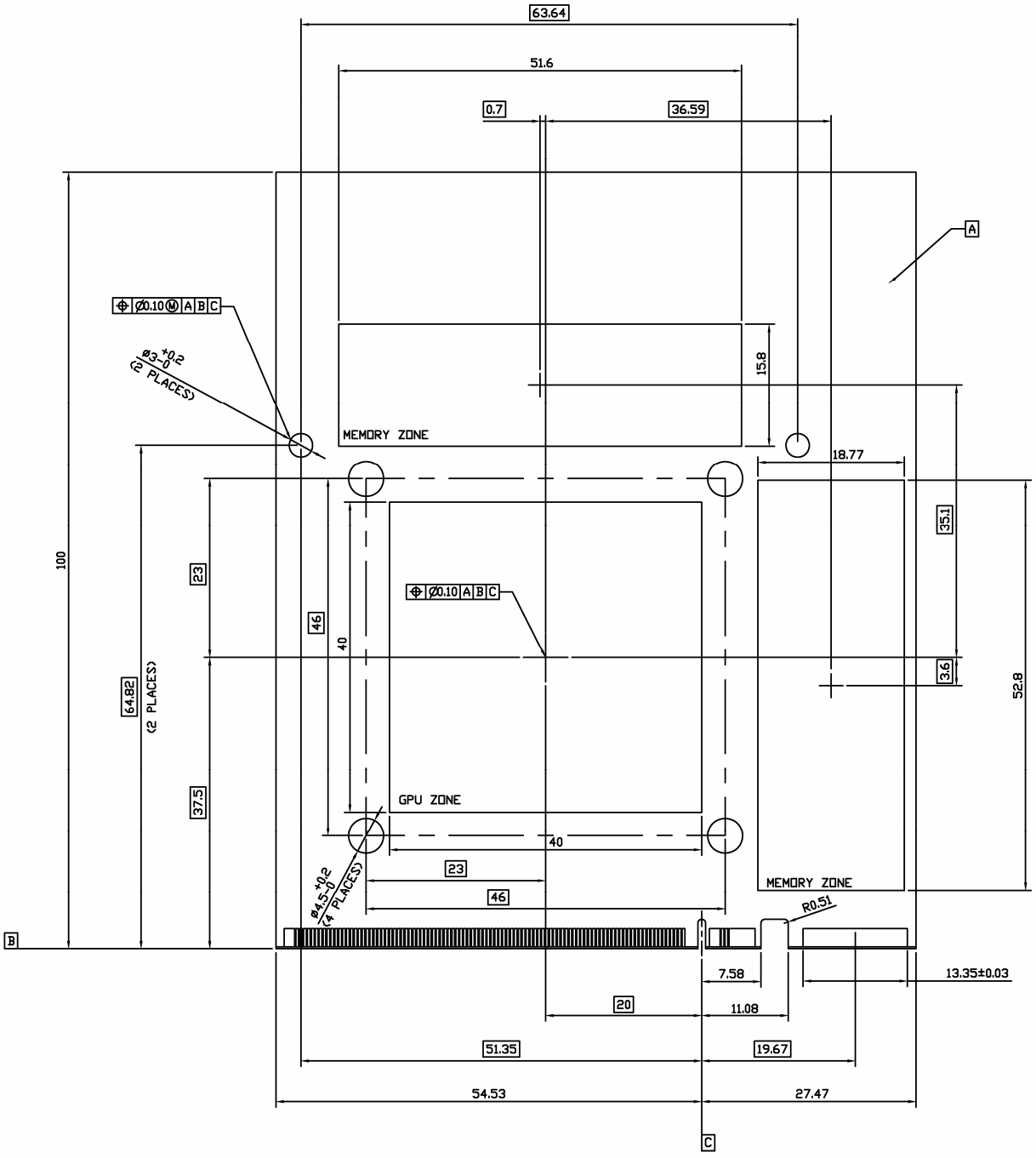

Figure 9. MXM-III PCB Top View

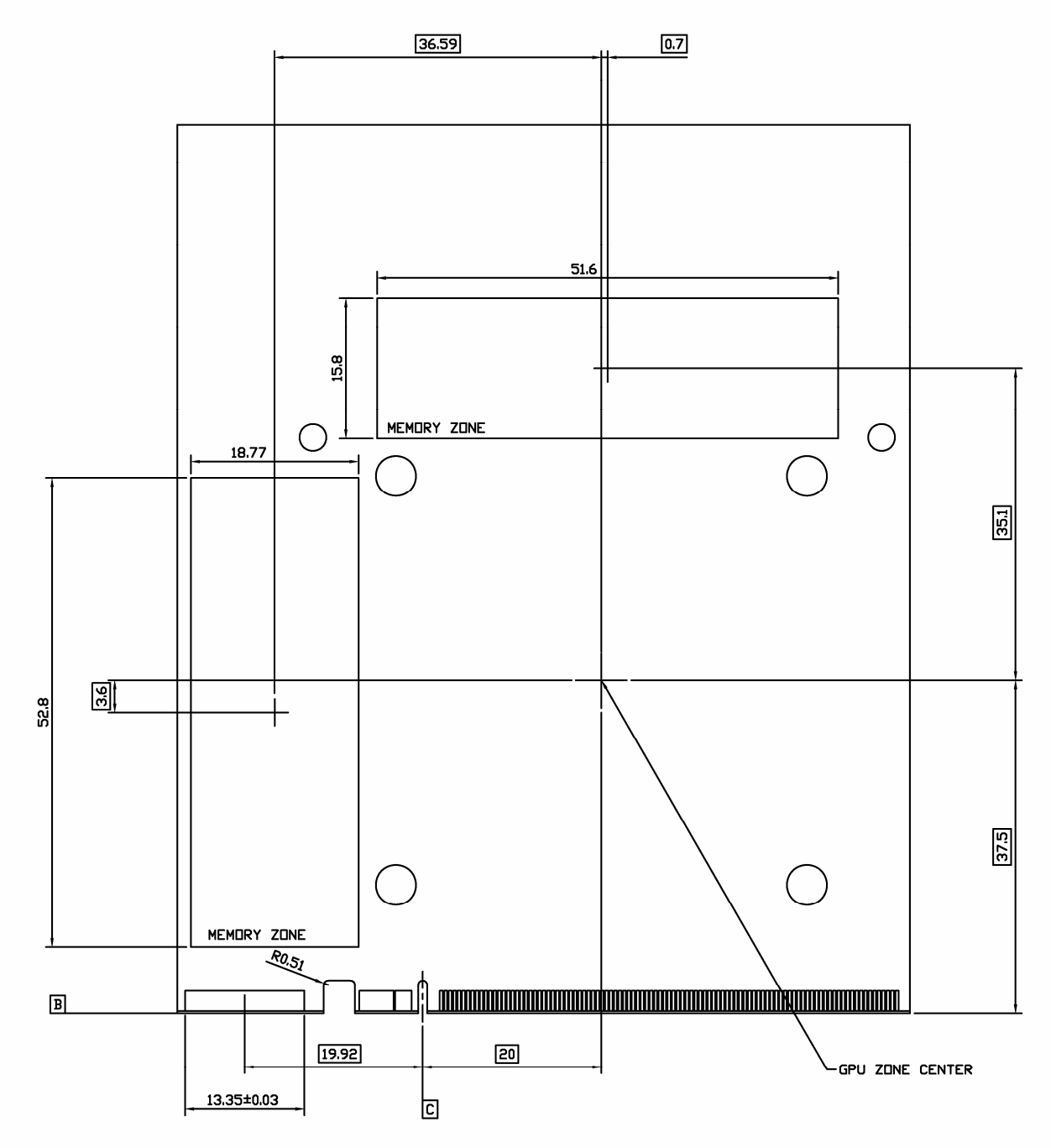

Figure 10. MXM-III PCB Bottom View

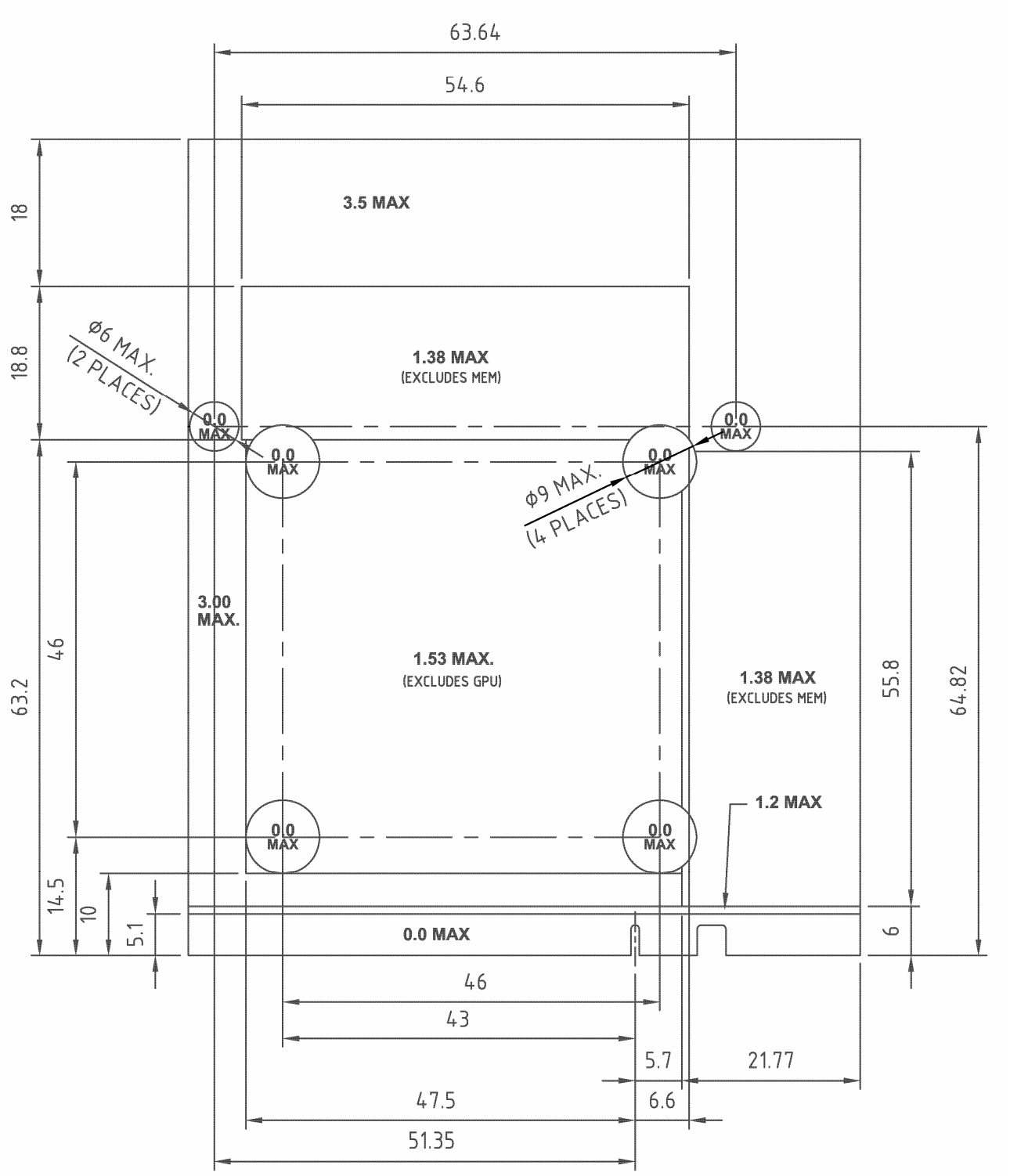

Figure 11. MXM-III Component Keep Outs Top View

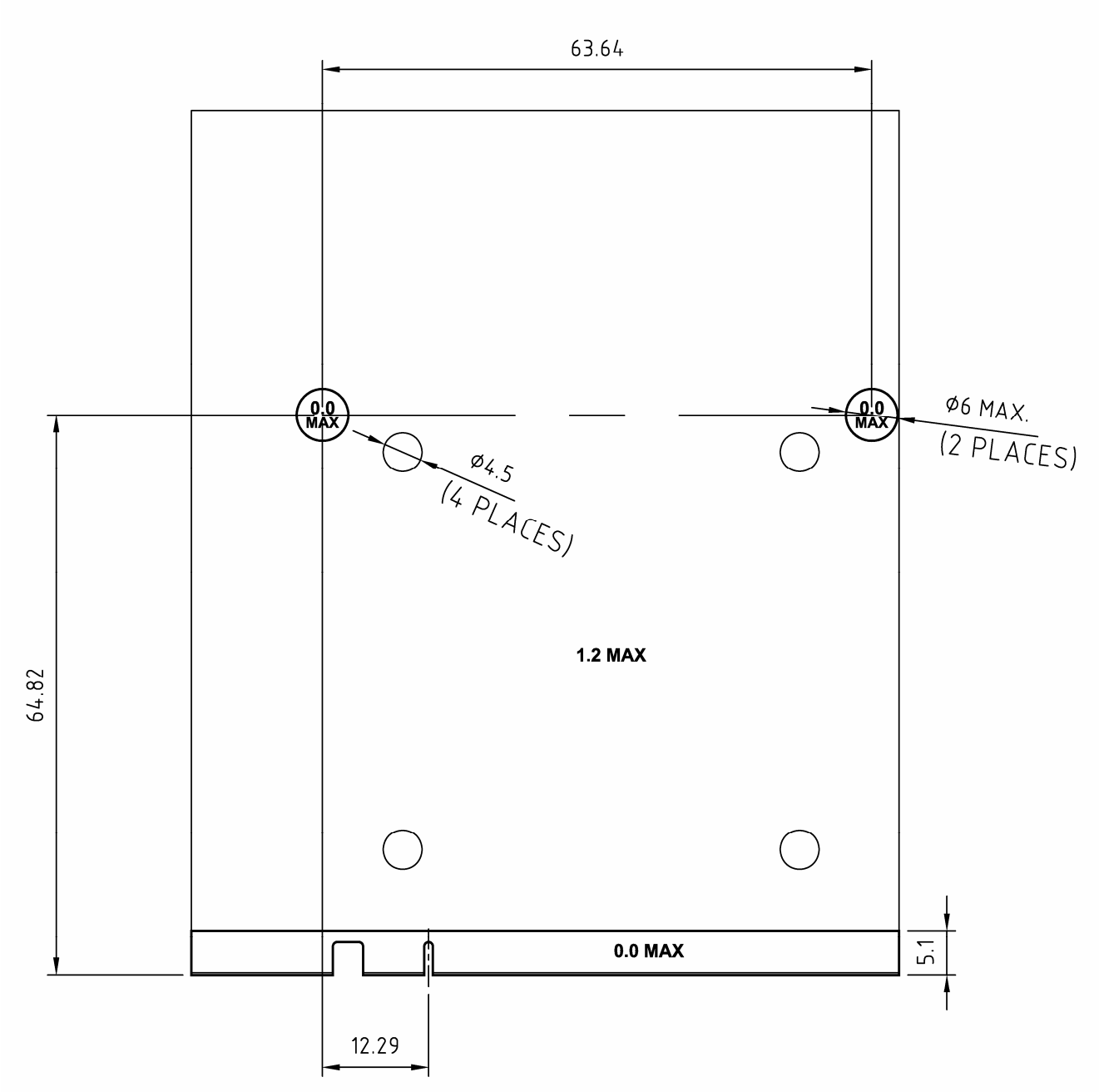

Figure 12. MXM-III Component Keep Outs Bottom View

MXM-IV PCB and Component Keep Outs

Figure 13 through Figure 16 show the MXM-IV PCB and component keep outs.

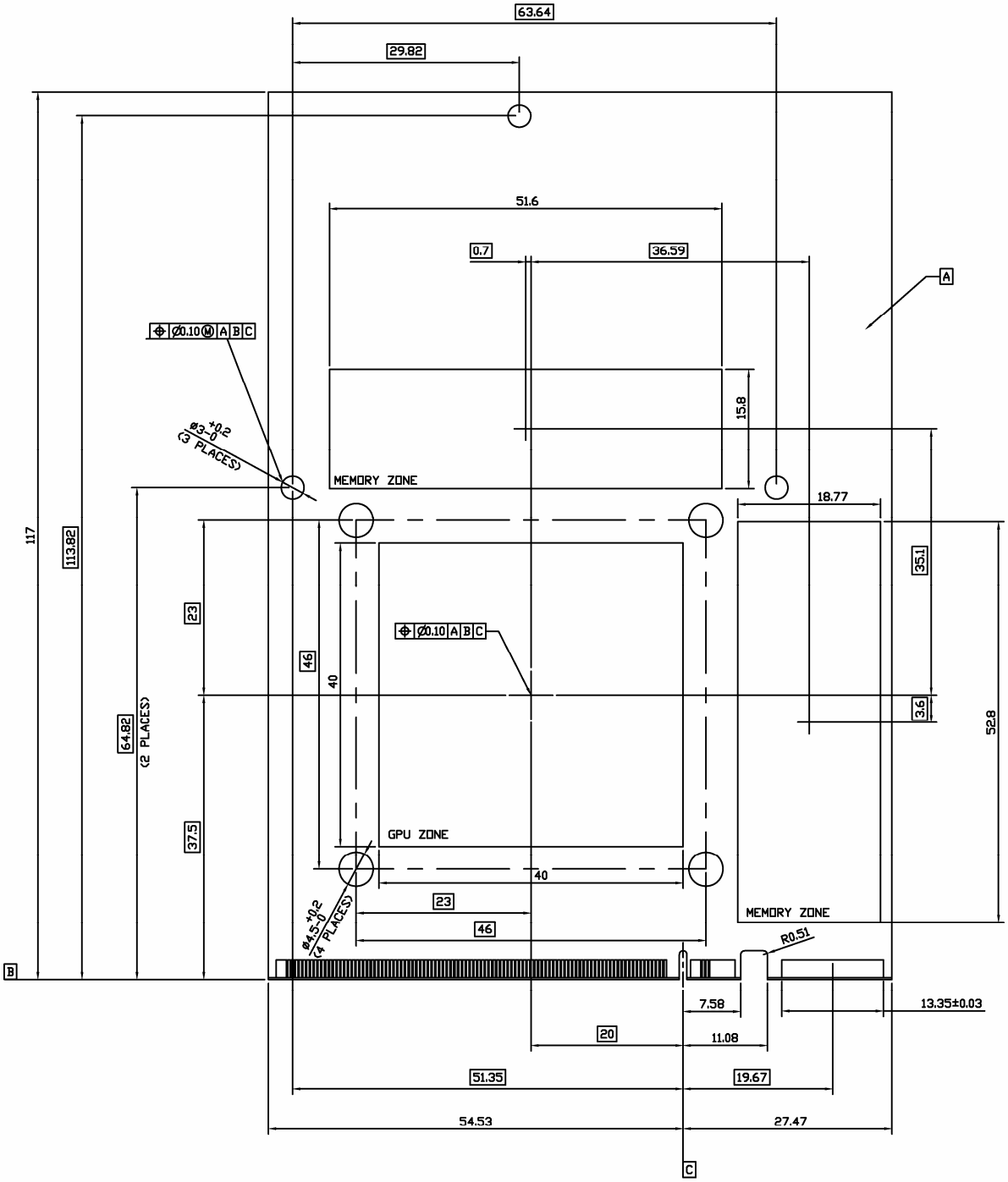

Figure 13. MXM-IV PCB Top View

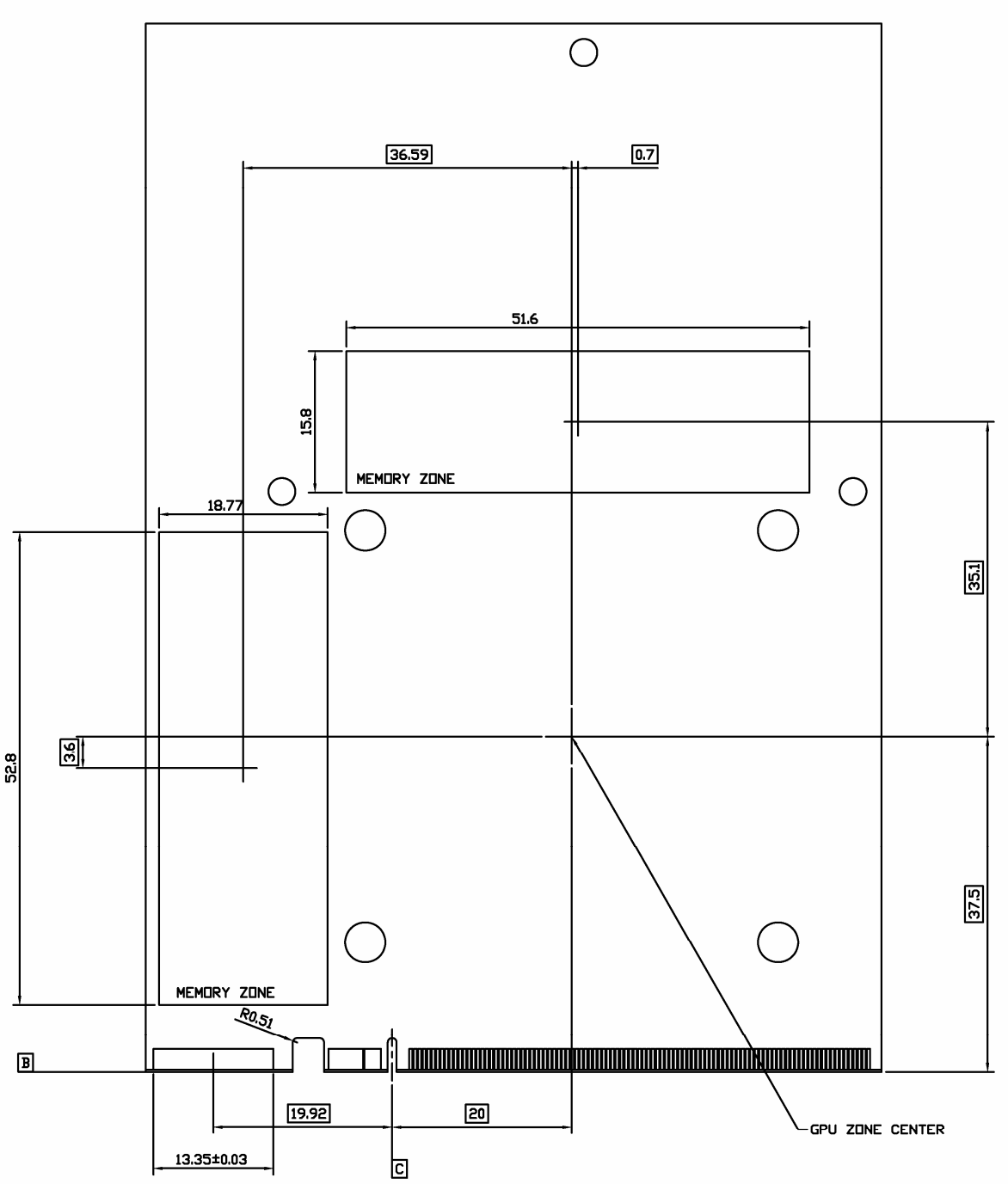

Figure 14. MXM-IV PCB Bottom View

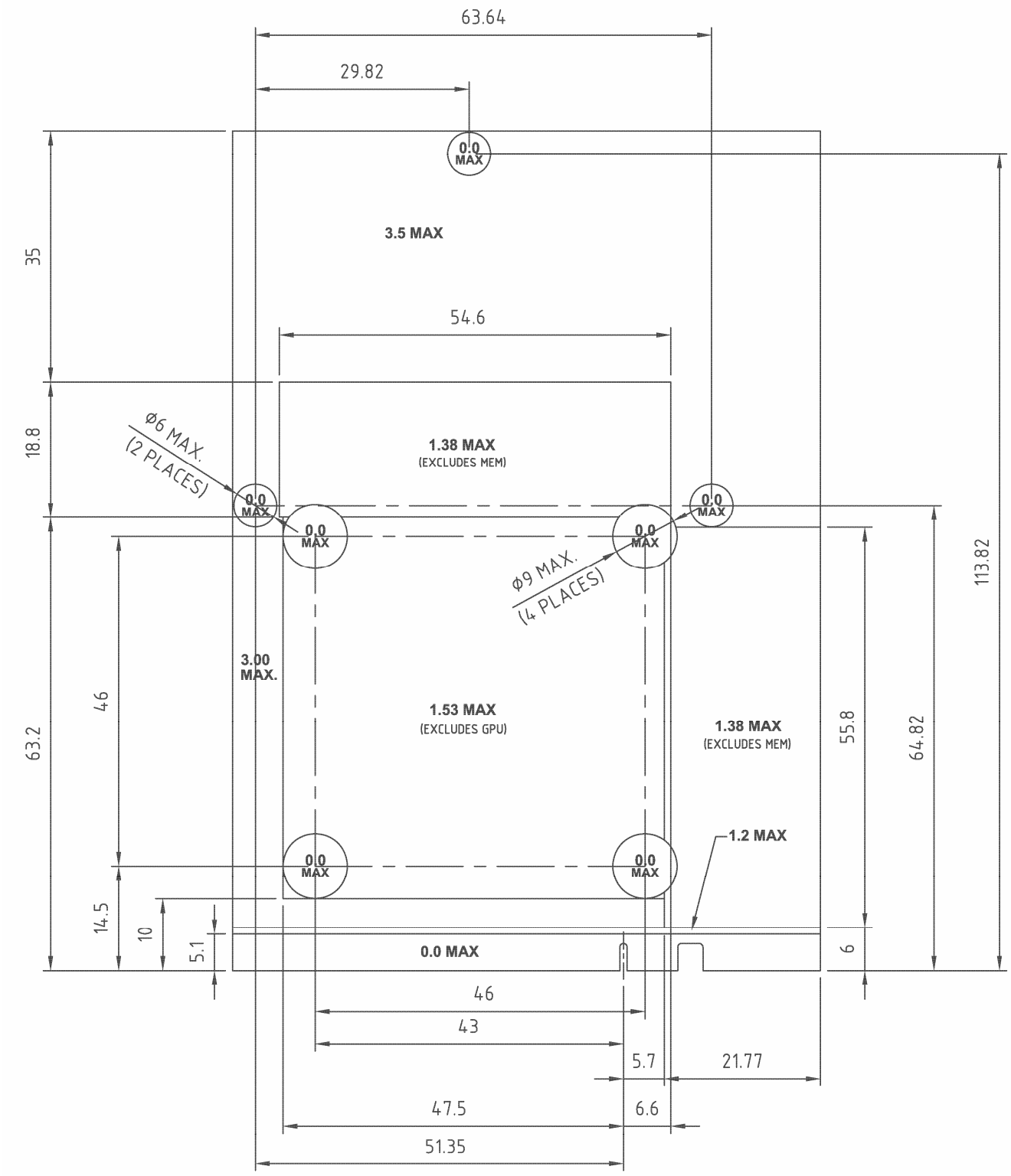

Figure 15. MXM-IV Component Keep Outs Top View

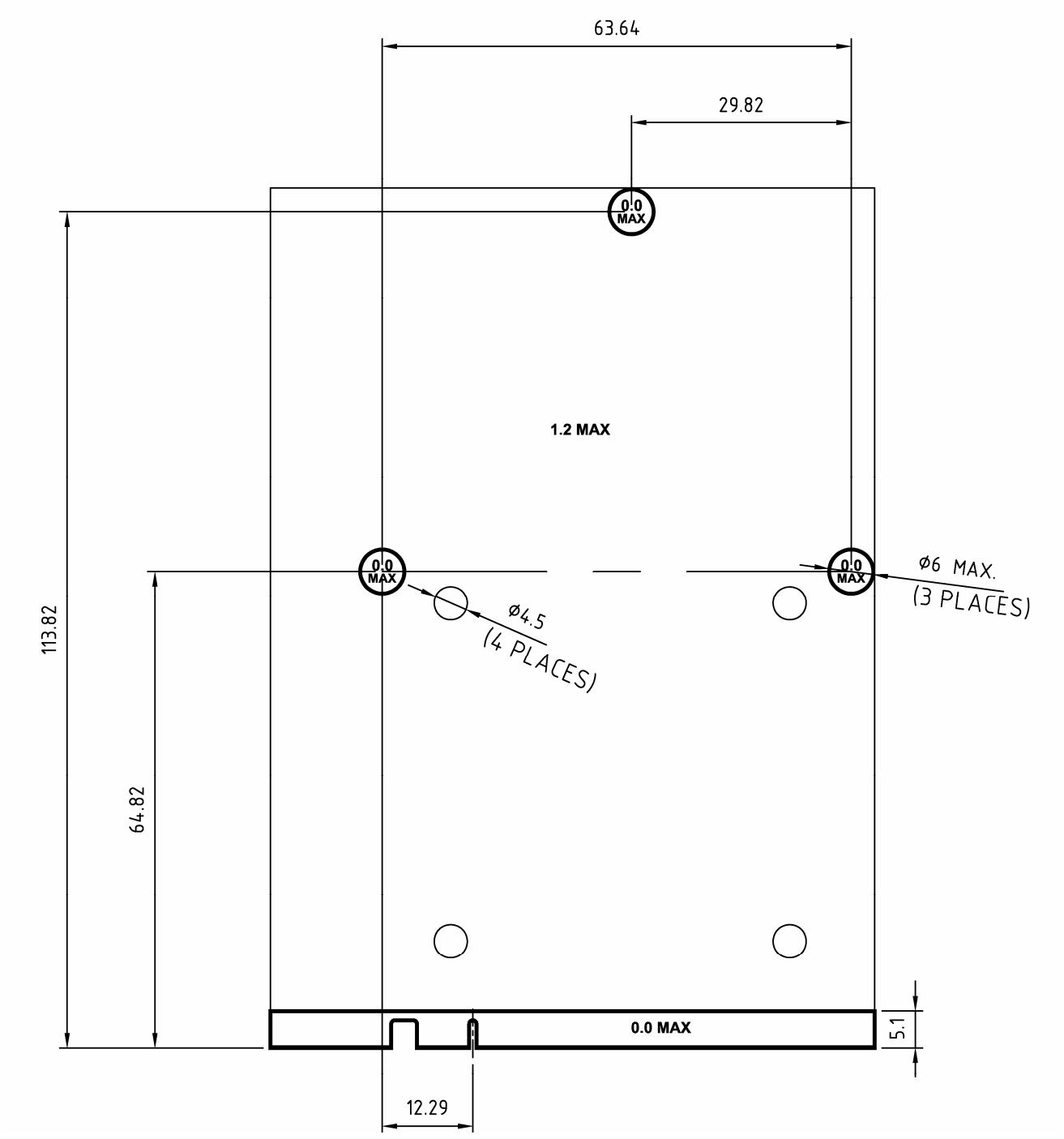

Figure 16. MXM-IV Component Keep Outs Bottom View

Thermal Keep Outs

The MXM thermal solutions can not extend below the minimum z-height specified.

MXM-I Thermal Keep Outs

Figure 17 shows the MXM-I thermal keep outs.

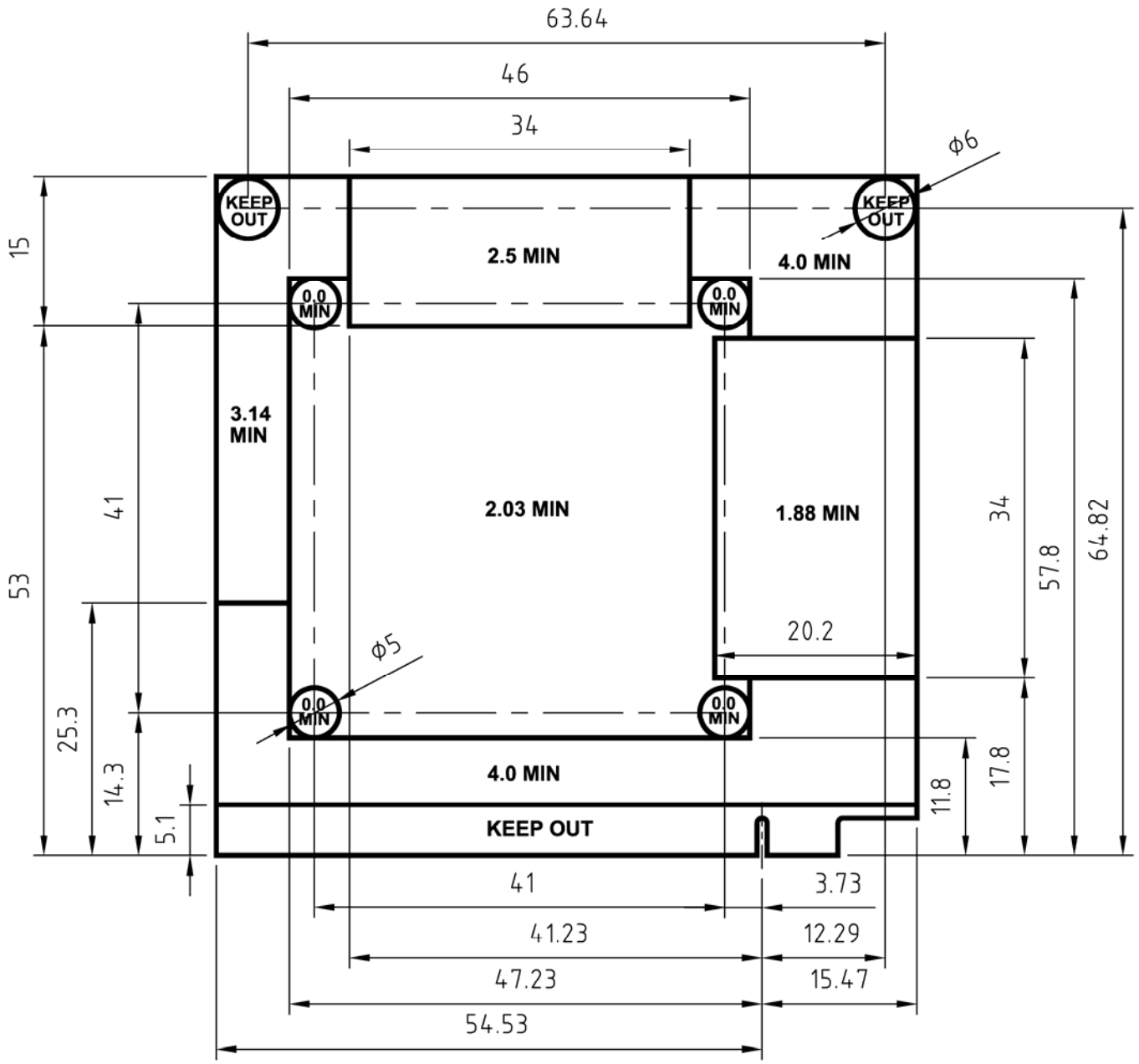

Figure 17. MXM-I Thermal Keep Outs Top View

MXM-II Thermal Keep Outs

Figure 18 shows the MXM-II thermal keep out.

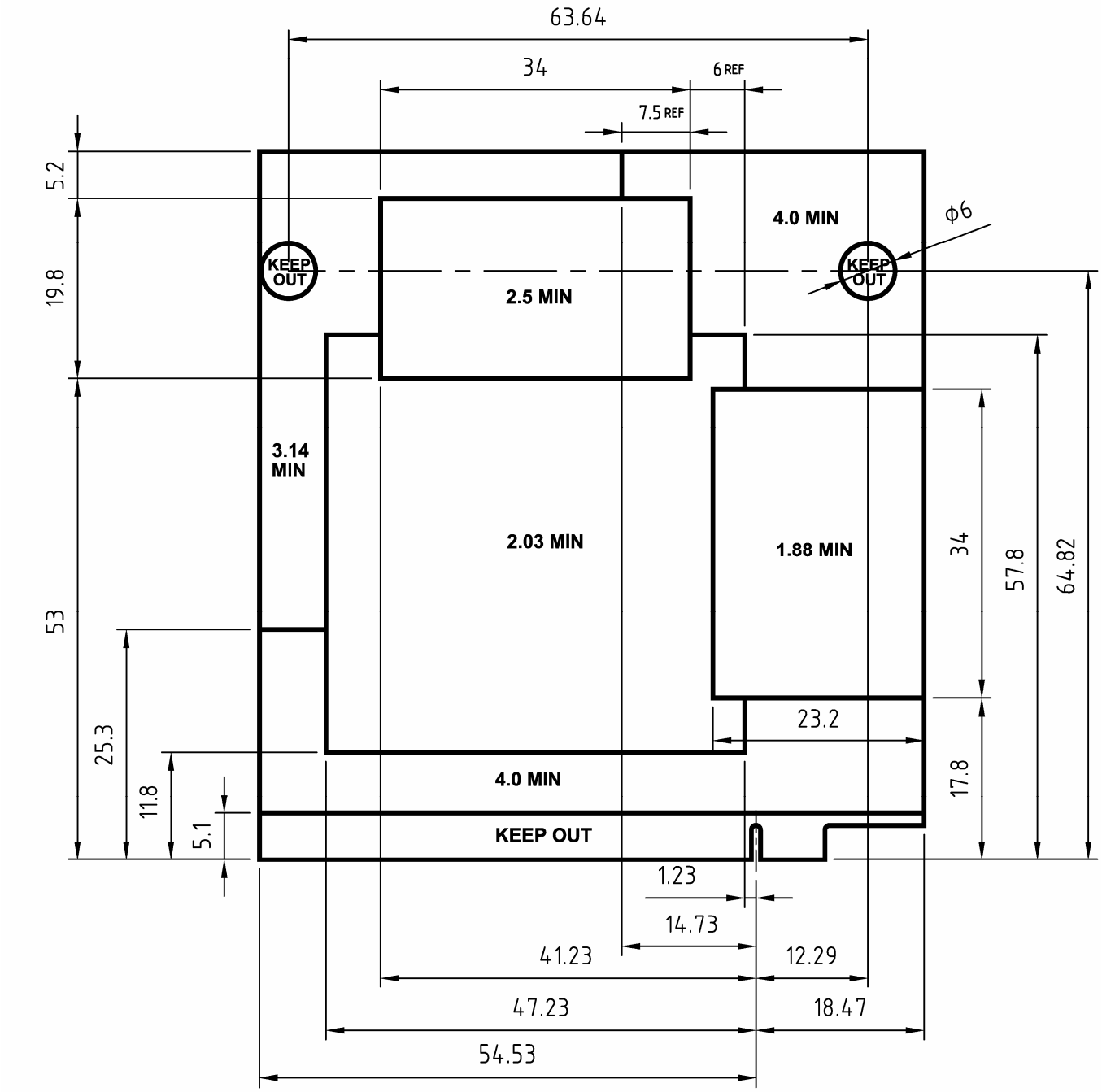

Figure 18. MXM-II Thermal Keep Outs Top View

MXM-III Thermal Keep Outs

Figure 19 shows the MXM-III thermal keep outs.

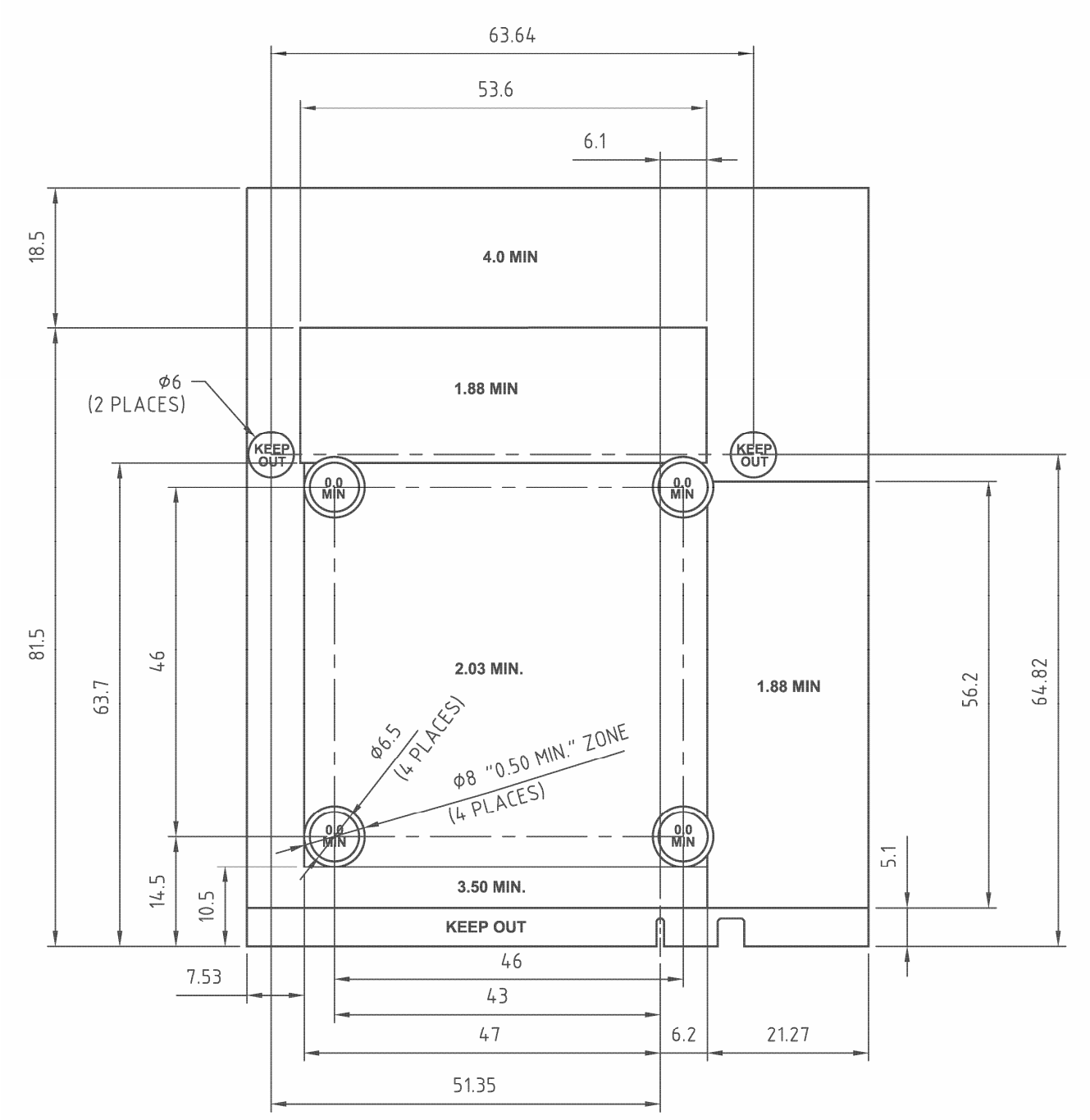

Figure 19. MXM-III Thermal Keep Outs Top View

MXM-IV Thermal Keep Outs

Figure 20 shows the MXM-IV thermal keep outs.

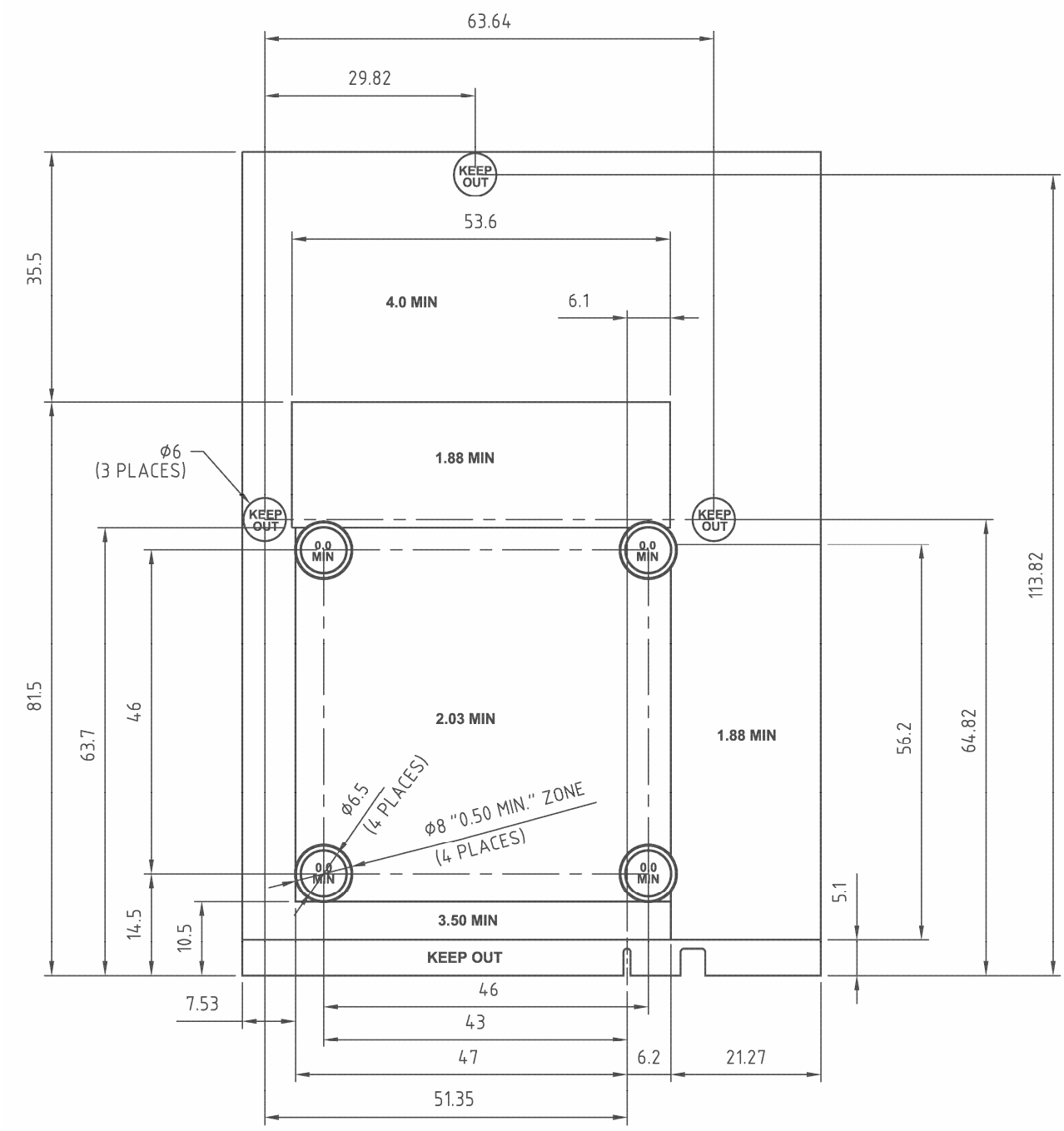

Figure 20. MXM-IV Thermal Keep Outs Top View

MXM Connectors

MXM Edge-Fingers

MXM utilizes a 0.5 mm pitch, 230-pin or 232-pin high-end (HE), card-edge connection system. Edge-fingers on the module are referenced to the PCB slot center with an overall PCB thickness of 1.1 mm to 1.3 mm measured across the fingers including plating and/or metallization. Bevel is optional, but edge shall be free of burrs and shall not have sharp edges.

For good electrical performance, all etch on internal layers under the edge-fingers shall be removed. A group of n adjacent power fingers are joined together to allow full pin to finger contact on n-1 pins of that particular group.

The module edge finger dimensions are shown in Figure 21 through Figure 25.

PCB flatness with respect to the edge-fingers shall not induce undue stress nor cause an open connection between the edge-fingers and the connector pin.

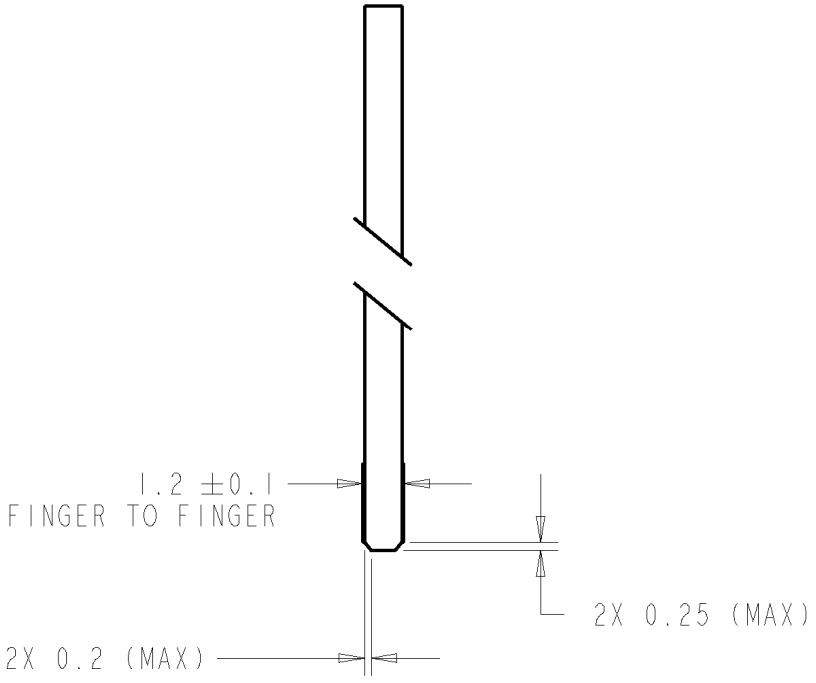

Figure 21. MXM Edge Finger Side View

MXM-I and MXM-II

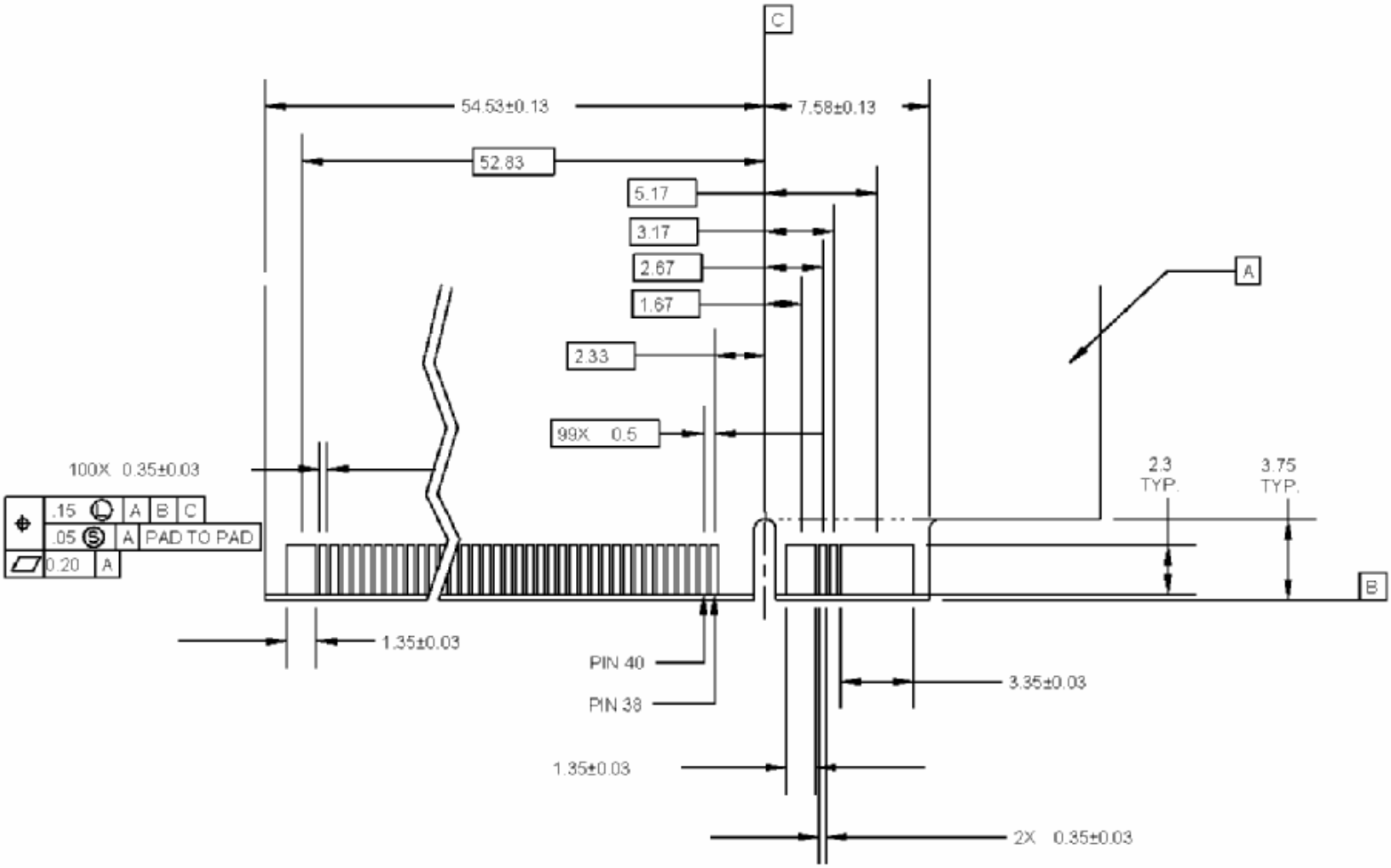

Figure 22. MXM-I and MXM-II Edge Finger Top Side

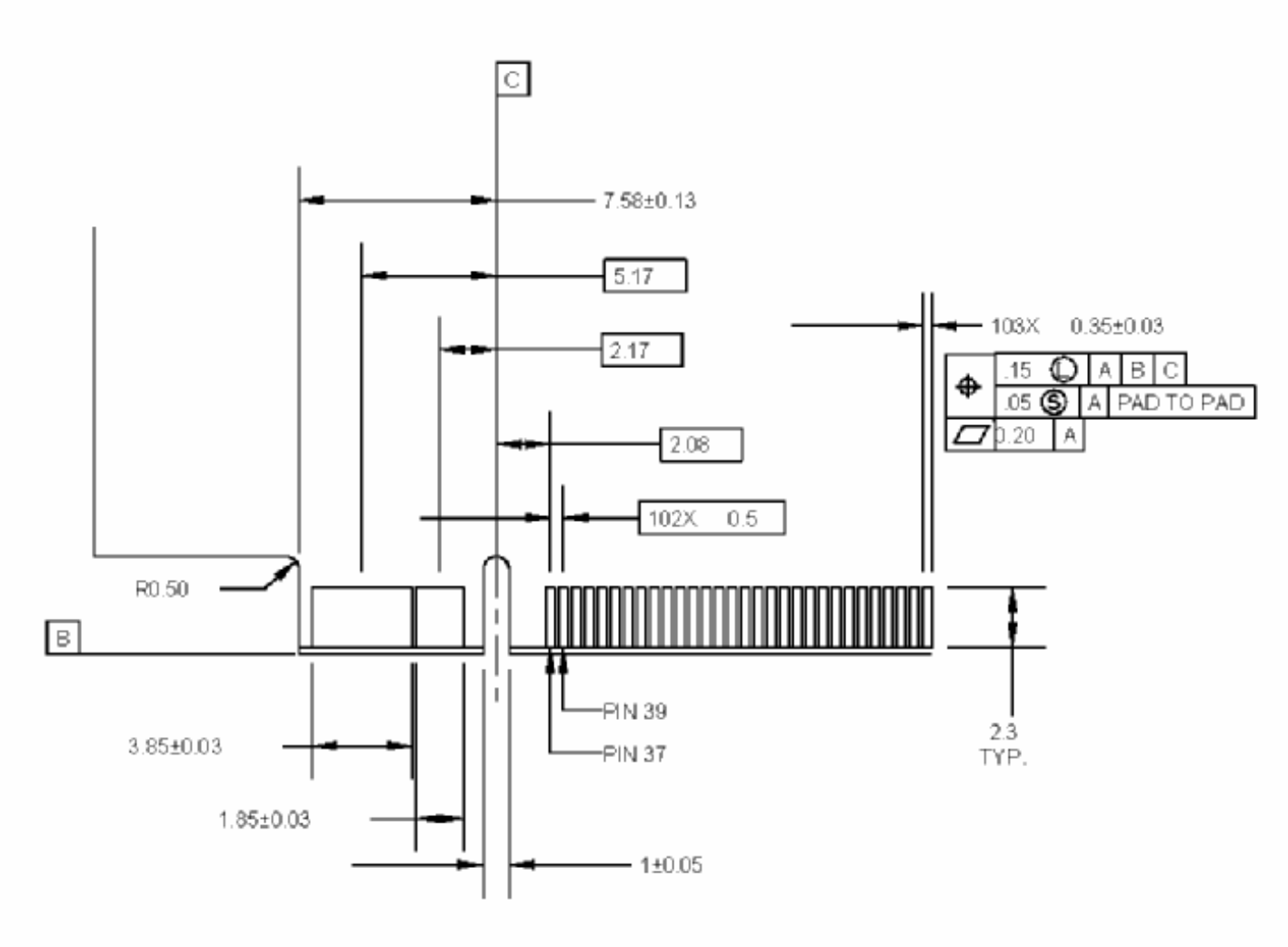

Figure 23. MXM-I and MXM-II Edge Finger Bottom Side

MXM-III and MXM-IV

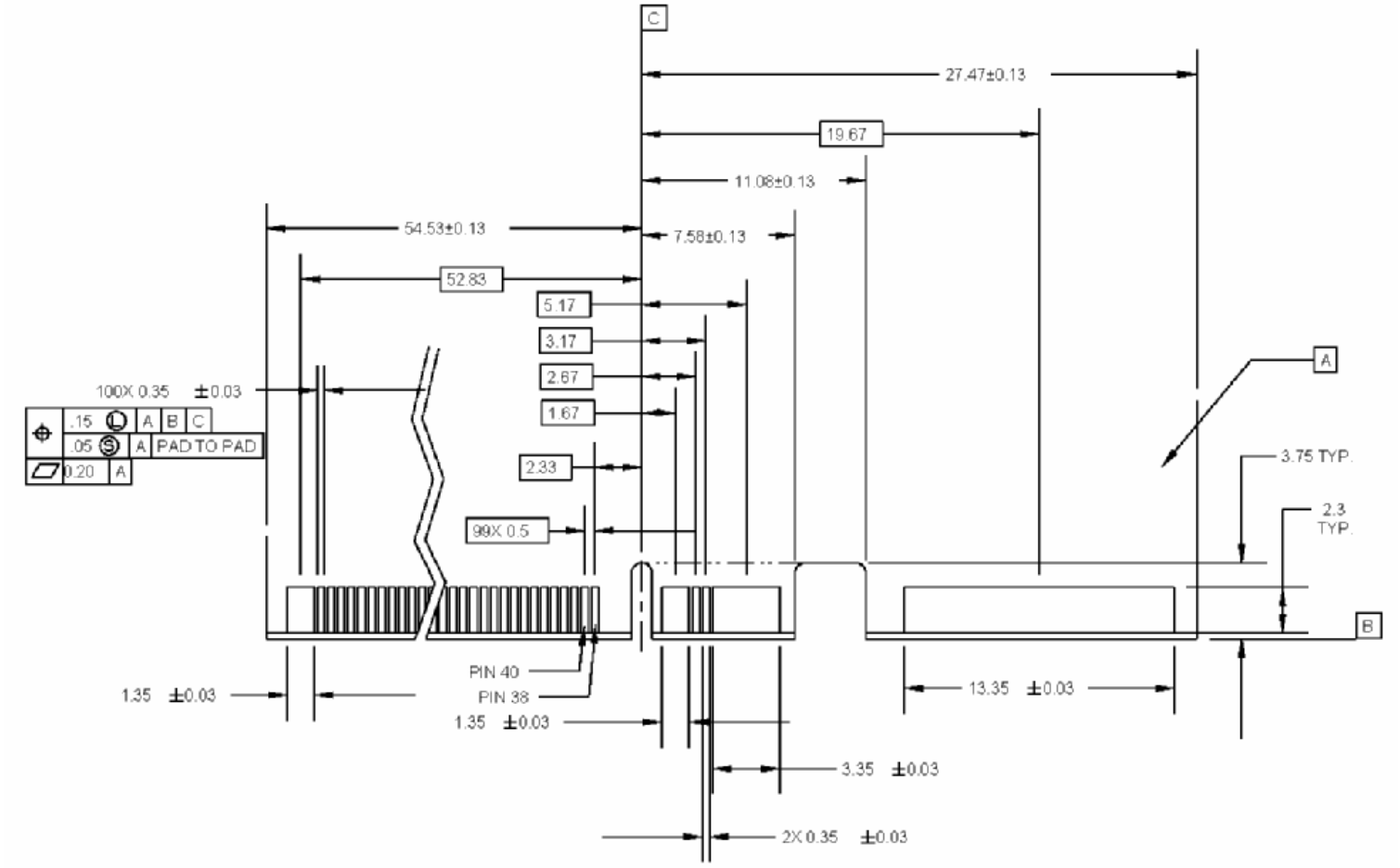

Figure 24. MXM-III and MXM-IV Edge Finger Top Side

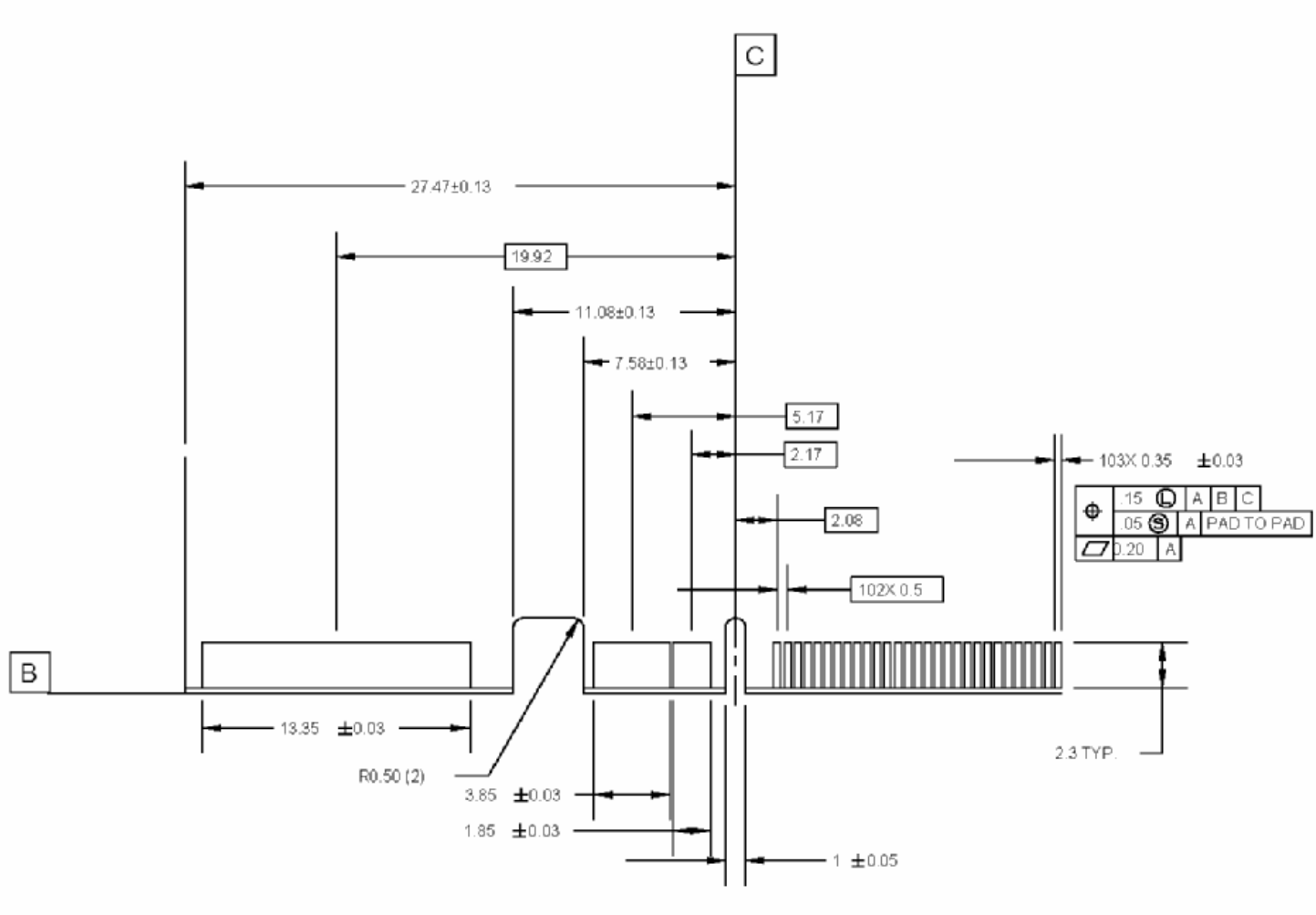

Figure 25. MXM-III and MXM-IV Edge Finger Bottom Side

MXM Connector

It is not the intention of this specification to detail connector contact and housing designs. Each connector vendor may choose to design an MXM connector of various styles as long as the design meets the form, fit and function of the MXM edge-fingers and module volume definitions.

Although many connector styles could be designed, slide-in, edge mount, surface mount thru-hole hybrid, etc, the connector shown in the specification is a Low Insertion Force (LIF) angled entry surface mount connector. The LIF angled entry connector is the most popular type for this application and defining the housing by maximum volume and the motherboard footprint allows connector vendors to make compatible connectors.

Connector height is defined as the z-height from the motherboard surface, on which the connector is mounted, to the module board surface closest to the motherboard. This specification suggests four connector heights, 8.2 mm, 5 mm, 2.7 mm and 1.5 mm. Different connector heights can be developed as needed to accommodate platform mechanical stack-ups.

Table 3. Suggested Connector Height

Connector Height	Module Orientation	Air Gap	Maximum Motherboard Component Z-Height
1.5 mm	Normal	0.3 mm	0 mm
2.7 mm	Normal	0.3 mm	1.2 mm
5.0 mm	Normal Inverted	0.3 mm 0.3 mm	3.5 mm 1.2 mm (except thermal attachment)
8.2 mm	Inverted	0.3 mm	4.4 mm (except thermal attachment)

The MXM-HE connector footprint is backwards compatible to the standard connector, thereby allowing a system designed with an MXM-HE connector to define a configuration with the standard connector utilizing one PCB.

MXM connector outlines and footprints are shown in Figure 26 through Figure 29.

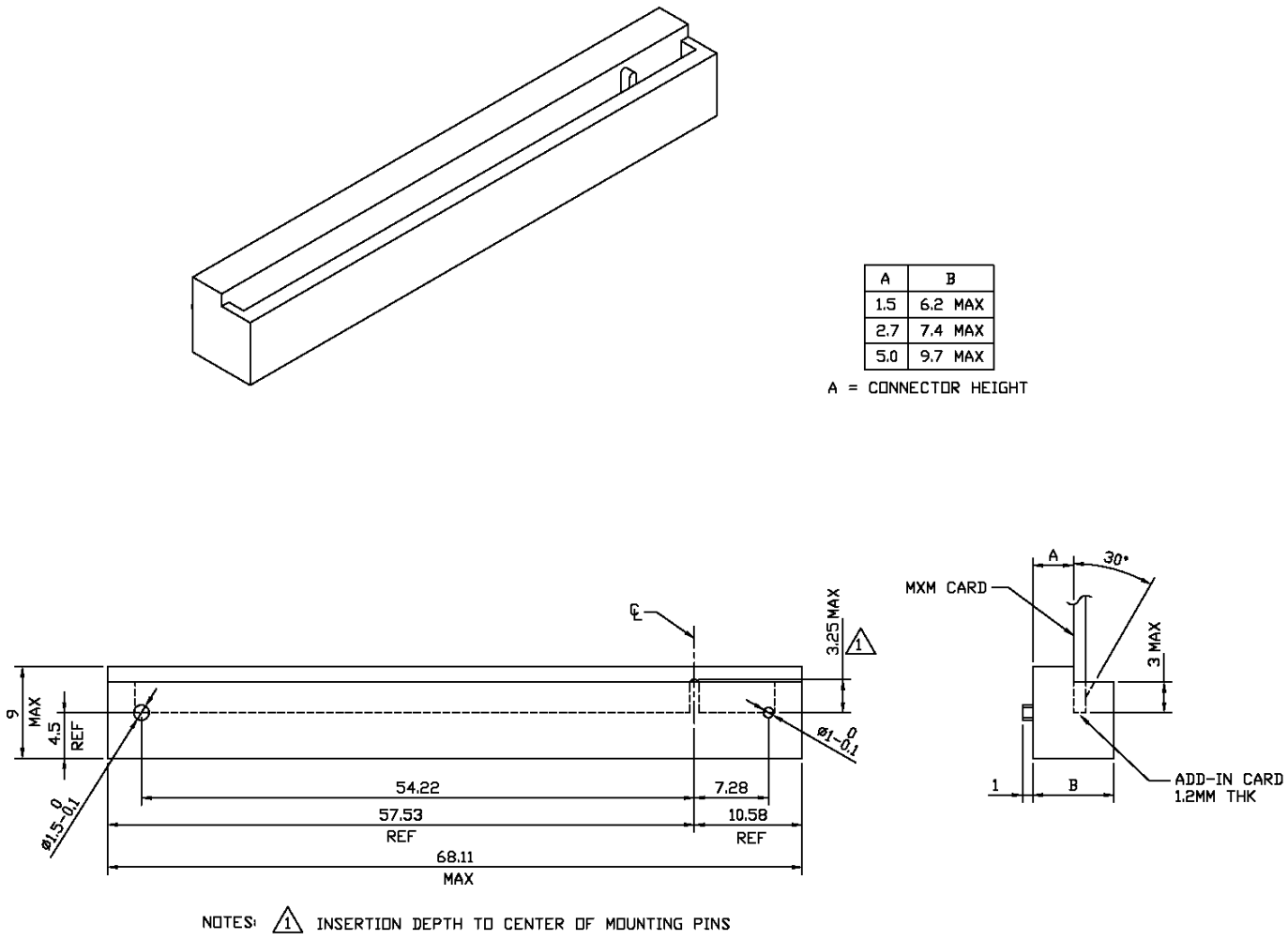

Figure 26. MXM Standard Connector

Note: Although not shown, MXM v 2.1A specification supports connectors for inverted module orientation to the motherboard.

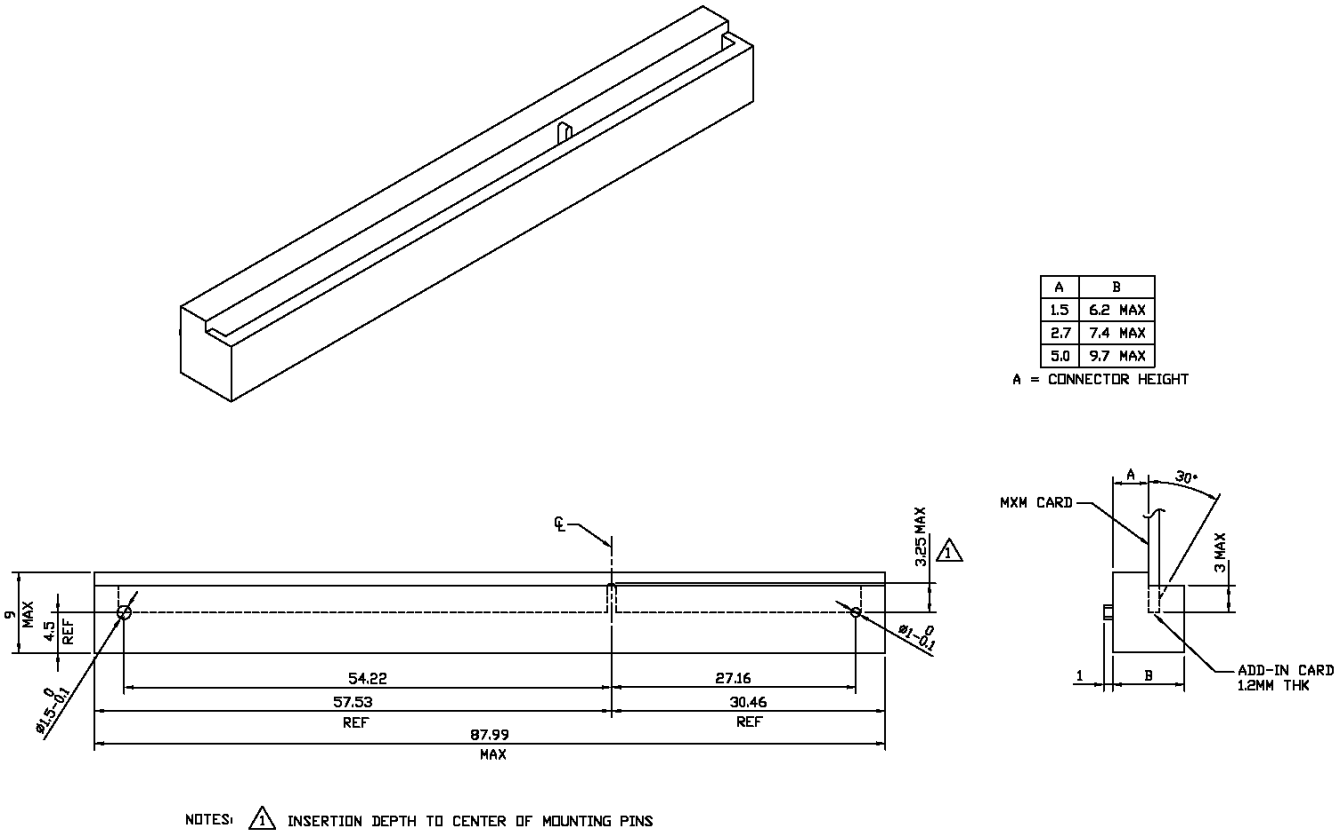

Figure 27. MXM-HE Connector

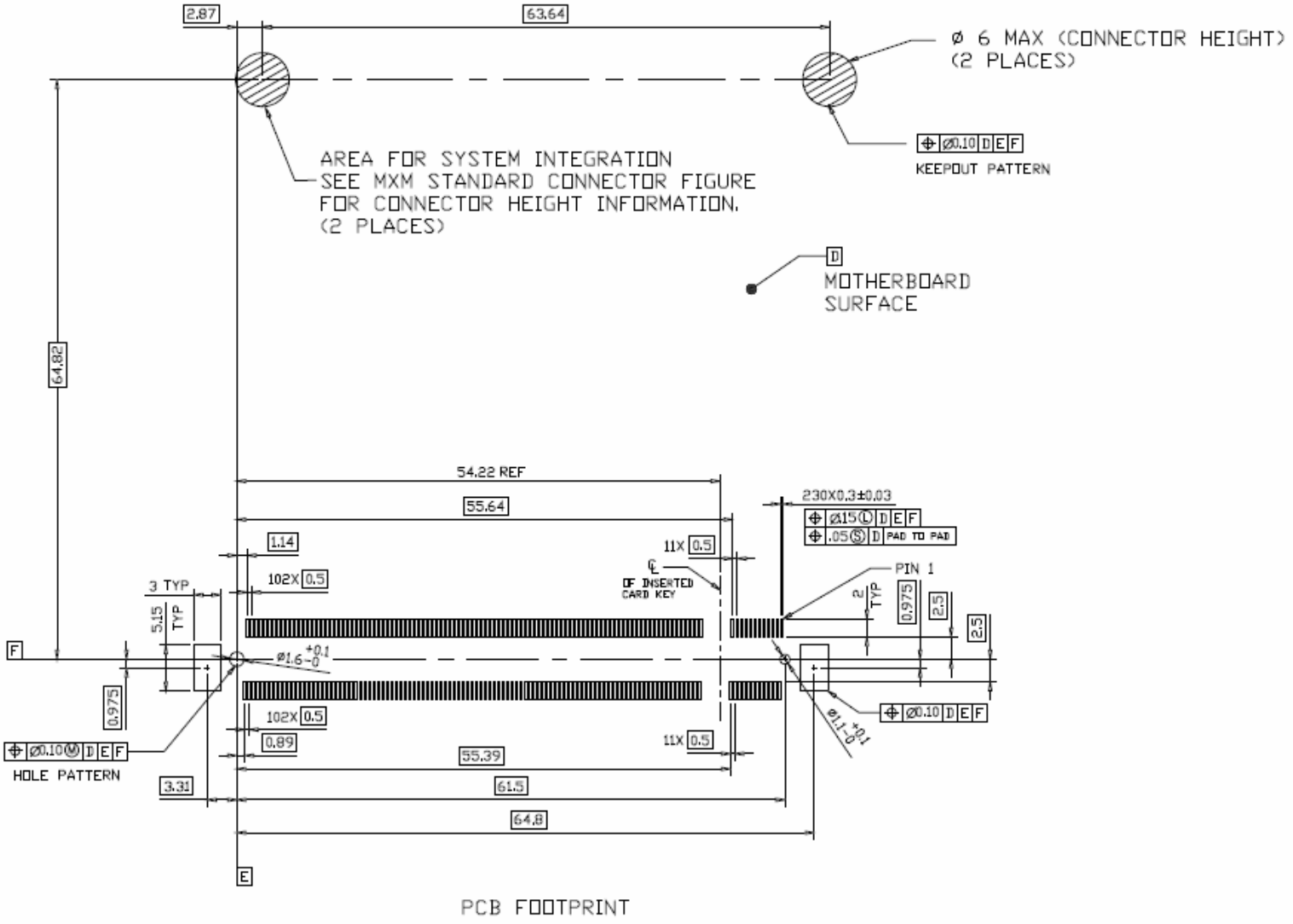

Figure 28. MXM Connector Motherboard Footprint

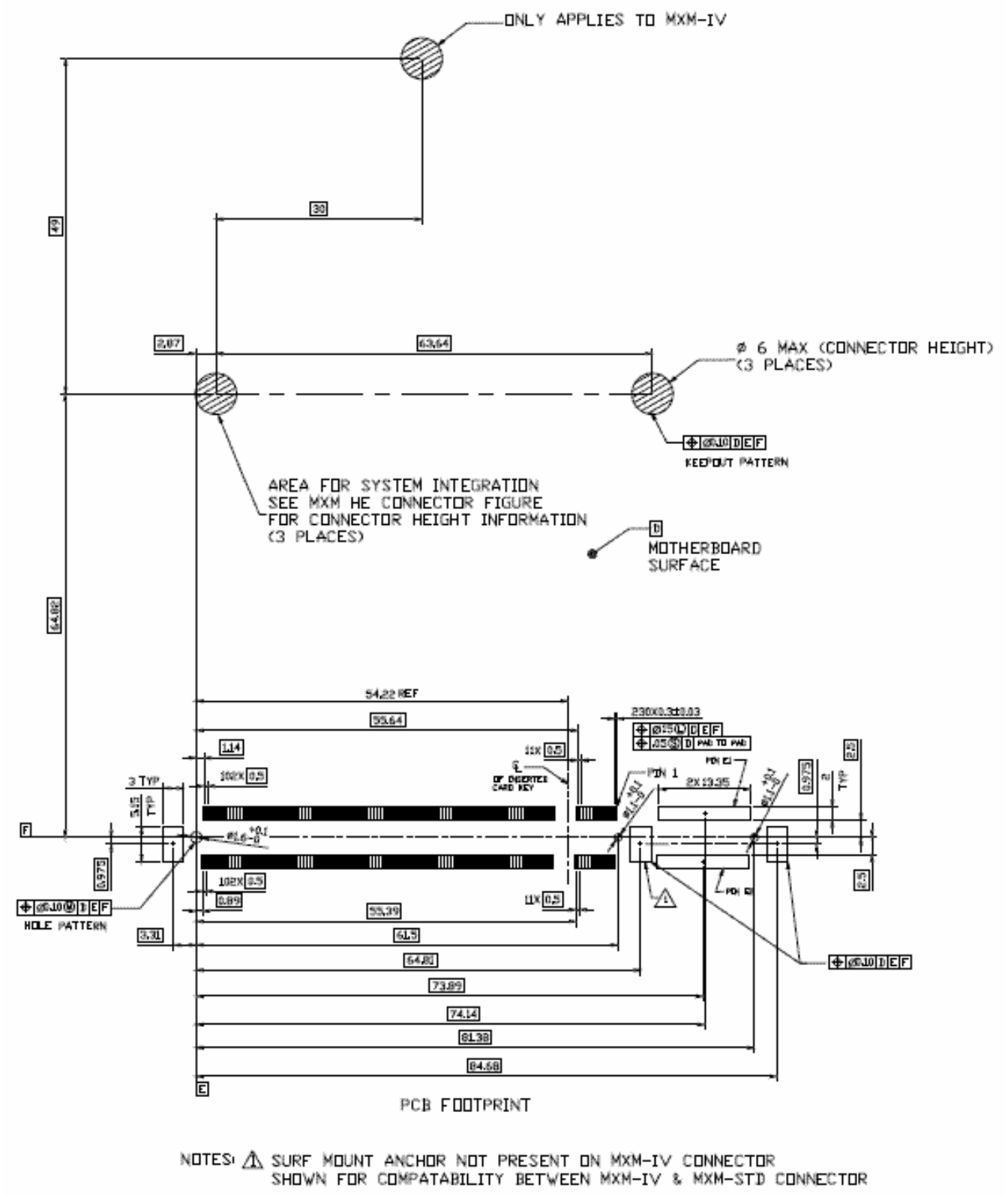

Figure 29. MXM-HE Connector Motherboard Footprint

Mounting and Retention

The MXM v 2.1A mounts to the system through an edge connector at the integration sites. The connector on the MXM is a card-edge connector consisting of only the PCB with plated contacts. One system connector option (ZIF angled insertion) allows MXM v 2.1A graphics module to be inserted at a 20 to 30 degree angle and then rotated towards the motherboard and then fastened into mechanical mounting stand-offs at the integration sites. The stand-offs will maintain separation from the motherboard, assist in the retention of the module and provide grounding to the system by mating to the grounded PCB pads. The integration sites are the same for all MXM v 2.1A graphics modules to allow the possibility of one motherboard to support all MXM v 2.1A graphics module types.

MXM v 2.1A Compatibility

There are three aspects to module compatibility in a system, module volume, connector and thermal attachment. Module volumes are designed in such a way that a smaller module type will always fit into the volume of any of the larger types. Thereby, a system designed for a certain type will always accept the modules of a smaller type.

A system may have one of two connectors, standard or HE (high-end). All modules fit and operate in both connectors.

The thermal attachment compatibility is described in Table 4.

Table 4. MXM v 2.1A Thermal Compatibility

System MXM Type	MXM Connector[1]	MXM Module Compatibility
I	Standard	I
II	Standard	I, II
III	Standard HE	III III
IV	HE	III, IV

1. Modules used with an MXM standard connector may be limited in performance due to the PWR_SRC 4A maximum current connector limitation

Mechanical Requirements

Backing Plate

Each MXM graphics module requires a mechanical backing plate design that shall be implemented as needed to compensate for a warped board resulting from thermal solution loading requirements. For all MXM modules the backing plate is contained within the 1.2 mm universal height restriction. This backing plate can be unique for each MXM design.

Thermal Solution Mounting

The thermal solution is mounted to the MXM v 2.1A with M2.5 screws from the bottom side of the PCB. A specific screw size is defined to ensure inter-board compatibility because the backing plates may be unique to each MXM.

MXM Connector Requirements

Table 5 lists the mechanical requirements for the MXM connectors.

Table 5. MXM Connector Mechanical Performance Requirements

Parameter	Specification
Durability	EIA-364-9 30 cycles
Mating and unmating force	EIA-364-13C LIF/angled insertion styled cards: Maximum insertion force: 1.3 kg Maximum extraction force: 1.6 kg Slide-in/side insertion styled cards Maximum insertion force: 6.0 kg Maximum extraction force: 4.6 kg Note: numbers tabulated using a velocity of 25 mm/min
Vibration	EIA-364-28D – Test condition VII condition D With a 40 x 40 mm block of 100 grams fastened and centered at the GPU center of a Type III PCB
Shock	EIA-364-27B – Test condition A With a 40 x 40 mm block of 100 grams fastened and centered at the GPU center of a Type III PCB

Electrical Specifications

PCI Express Support

The Mobile PCI Express Module (MXM) supports a link of up to sixteen bi-directional PCI Express differential signaling lanes. It is compliant with *PCI Express Base Specification* 1.1 or earlier except for power delivery and power management. Mobile system power requirements supersede PCI Express power specifications. The MXM does not support hot-plug insertion.

Electrical Connector

The Mobile PCI Express Module (MXM) utilizes a 230-pin or 232-pin HE card-edge connection system. The connector accommodates card thicknesses of 1.2 mm and various connector heights.

All external and internal system interfaces are routed through the MXM connector and down to the motherboard. The motherboard will then connect these signals from the MXM to the appropriate circuitry.

Table 6 lists the electrical requirements for the MXM connectors. Table 7 lists the connector pinout.

Table 6. MXM Connector Electrical Performance Requirements

Parameter	Specification
Low Level Contact Resistance	EIA-364-23B – Specify which option used. Do not use option 4. Requirement: 40 mΩ maximum for initial measurements 50 mΩ maximum or Delta R = 20 mΩ maximum, whichever is less, for measurements after other tests
Insulation Resistance	EIA-364-21C Requirements: Initial testing 250 MΩ. 50 MΩ after other test procedures
Dielectric Withstanding Voltage	EIA-364-20B – Method B on one pair of upper adjacent contacts and on one pair of lower adjacent contacts. Connector is unmated and unmounted. Barometric pressure at sea level. Apply 0.25 kV AC, (50 Hz) for 1 minute.
Current Rating	Current requirement: Pins rated for 0.5 Amp continuous (pins E1 and E2 are exceptions and are rated for 12 A continuous). The temperature rise above ambient shall not exceed 30 °C, where ambient condition is 25 °C still air.
Voltage Rating	50VDC per contact
Impedance	EIA-364-108 Impedance Requirements: 100 ± 20 Ω differential, 50 ± 10 Ω single ended.
Insertion Loss	EIA-364-101 Insertion Loss Requirements: 1 dB max up to 1.25 GHz; ≤ [1.6* (F-1.25)+1] dB for 1.25 GHz < F ≤ 3.75 GHz (for example, ≤ 5 dB at F = 3.75 GHz) where F is frequency in GHz
Return Loss	EIA-364-108 Return Loss Requirements: ≤-12 dB up to 1.3 GHz ≤ -7dB up to 2 GHz ≤-4 dB up to 3.75 GHz
Near End Crosstalk	EIA-364-90 Crosstalk(NEXT) Requirements: -32 dB max up to 1.25 GHz ≤ -[32 – 2.4* (F – 1.25)] dB for 1.25 GHz < F ≤ 3.75 GHz (for example, ≤ -26 dB at F = 3.75 GHz) where F is frequency in GHz

Table 7. Connector Pinout

Pin #	Signal Name	Pin #	Signal Name
E1	PWR_SRC	E2	GND
1	PWR_SRC	2	1V8RUN
3	PWR_SRC	4	1V8RUN
5	PWR_SRC	6	1V8RUN
7	PWR_SRC	8	1V8RUN
9	PWR_SRC	10	1V8RUN
11	PWR_SRC	12	1V8RUN
13	PWR_SRC	14	1V8RUN
15	PWR_SRC	16	RUNPWROK
17	GND	18	5VRUN
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	KEY	26	KEY
27	KEY	28	KEY
29	KEY	30	KEY
31	KEY	32	KEY
33	KEY	34	KEY
35	KEY	36	KEY
37	PEX_RX15#	38	PRSNT2# / PEX_LSW#
39	PEX_RX15	40	PEX_TX15#
41	GND	42	PEX_TX15
43	PEX_RX14#	44	GND
45	PEX_RX14	46	PEX_TX14#
47	GND	48	PEX_TX14
49	PEX_RX13#	50	GND
51	PEX_RX13	52	PEX_TX13#
53	GND	54	PEX_TX13
55	PEX_RX12#	56	GND
57	PEX_RX12	58	PEX_TX12#
59	GND	60	PEX_TX12
61	PEX_RX11#	62	GND
63	PEX_RX11	64	PEX_TX11#
65	GND	66	PEX_TX11
67	PEX_RX10#	68	GND
69	PEX_RX10	70	PEX_TX10#
71	GND	72	PEX_TX10

Pin #	Signal Name	Pin #	Signal Name
73	PEX_RX9#	74	GND
75	PEX_RX9	76	PEX_TX9#
77	GND	78	PEX_TX9
79	PEX_RX8#	80	GND
81	PEX_RX8	82	PEX_TX8#
83	GND	84	PEX_TX8
85	PEX_RX7#	86	GND
87	PEX_RX7	88	PEX_TX7#
89	GND	90	PEX_TX7
91	PEX_RX6#	92	GND
93	PEX_RX6	94	PEX_TX6#
95	GND	96	PEX_TX6
97	PEX_RX5#	98	GND
99	PEX_RX5	100	PEX_TX5#
101	GND	102	PEX_TX5
103	PEX_RX4#	104	GND
105	PEX_RX4	106	PEX_TX4#
107	GND	108	PEX_TX4
109	PEX_RX3#	110	GND
111	PEX_RX3	112	PEX_TX3#
113	GND	114	PEX_TX3
115	PEX_RX2#	116	GND
117	PEX_RX2	118	PEX_TX2#
119	GND	120	PEX_TX2
121	PEX_RX1#	122	GND
123	PEX_RX1	124	PEX_TX1#
125	GND	126	PEX_TX1
127	PEX_RX0#	128	GND
129	PEX_RX0	130	PEX_TX0#
131	GND	132	PEX_TX0
133	PEX_REFCLK#	134	PRSNT1#
135	PEX_REFCLK	136	TV_C / HDTV_Pr
137	CLK_REQ#	138	GND
139	PEX_RST#	140	TV_Y / HDTV_Y / TV_CVBS
141	HDA_SYNC	142	GND
143	HDA_BCLK	144	TV_CVBS/ HDTV_Pb

Pin #	Signal Name	Pin #	Signal Name
145	SMB_DAT	146	HDA_RST#
147	SMB_CLK	148	VGA_RED
149	THERM#	150	GND
151	VGA_HSYNC	152	VGA_GRN
153	VGA_VSYNC	154	GND
155	DDCA_CLK	156	VGA_BLU
157	DDCA_DAT	158	GND
159	HDA_SDI	160	LVDS_UCLK#
161	HDA_SDO	162	LVDS_UCLK
163	GND	164	GND
165	DP_B_L3#	166	LVDS_UTX3#
167	DP__B_L3	168	LVDS_UTX3
169	AC/BATT#	170	SPDIF
171	DP_x_AUX#	172	LVDS_UTX2#/ DVI_C_TX5#
173	DP_x_AUX	174	LVDS_UTX2/ DVI_C_TX5
175	GND	176	GND
177	DP_B_L2#	178	LVDS_UTX1#/ DVI_C_TX4#
179	DP_B_L2	180	LVDS_UTX1/ DVI_C_TX4
181	GND	182	GND
183	DP_B_L1#	184	LVDS_UTX0#/ DVI_C_TX3#
185	DP_B_L1	186	LVDS_UTX0/ DVI_C_TX3
187	GND	188	GND
189	DVI_B_CLK# / DP_A_L3#	190	LVDS_LCLK#/ DVI_C_TXC#
191	DVI_B_CLK / DP_A_L3	192	LVDS_LCLK/ DVI_C_TXC
193	DVI_B_HPD / DVI_C_HPD / DP_A_HPD	194	GND

Pin #	Signal Name	Pin #	Signal Name
195	DP_B_L0#	196	LVDS_LTX3#
197	DP_B_L0	198	LVDS_LTX3
199	GND	200	DP_B_HPD
201	DVI_B_TX2# / DP_A_L0#	202	LVDS_LTX2#/ DVI_C_TX2#
203	DVI_B_TX2 / DP_A_L0	204	LVDS_LTX2/ DVI_C_TX2
205	GND	206	GND
207	DVI_B_TX1# / DP_A_L1#	208	LVDS_LTX1#/ DVI_C_TX1#
209	DVI_B_TX1 / DP_A_L1	210	LVDS_LTX1/ DVI_C_TX1
211	GND	212	GND
213	DVI_B_TX0# / DP_A_L2#	214	LVDS_LTX0#/ DVI_C_TX0#
215	DVI_B_TX0 / DP_A_L2	216	LVDS_LTX0/ DVI_C_TX0
217	DVI_A_HPD	218	GND
219	DVI_A_CLK#	220	DDCC_DAT
221	DVI_A_CLK	222	DDCC_CLK
223	GND	224	LVDS_PPEN
225	DVI_A_TX2#	226	LVDS_BL_BRGHT
227	DVI_A_TX2	228	LVDS_BLEN
229	GND	230	DDCB_DAT
231	DVI_A_TX1#	232	DDCB_CLK
233	DVI_A_TX1	234	2V5RUN
235	GND	236	GND
237	DVI_A_TX0#	238	3V3RUN
239	DVI_A_TX0	240	3V3RUN
241	GND	242	3V3RUN

Note: Pins E1 and E2 are only present on the MXM-HE connector.

Connector Pin Descriptions

Table 8 contains pin descriptions for each signal type. All Input/Output classifications are relative to the MXM v 2.1A graphics module.

Table 8. Connector Pin Descriptions

Signal Name	Input/Output	Description	Module Support	System Support
DVI_A_TX0-2, DVI_A_TX0-2#	Output, Routed at 100 Ω Diff	TMDS output for either single-link DVI or dual-link DVI, lower link for dual-link	Required	Optional
DVI_A_CLK , DVI_A_CLK#	Output, Routed at 100 Ω Diff	TMDS clock for either single-link DVI or dual-link DVI	Required	Optional
DVI_A_HPD	Input	DVI hot plug detect for **DVI_A**	Required	Optional
DVI_B_TX0-2, DVI_B_TX0-2#	Output, Routed at 100 Ω Diff	TMDS output for either single-link DVI or dual-link DVI, upper link for dual-link.	Optional When supported, pins must remain in a high impedance state until module confirms system supports **DVI_B** from the system information structure	Optional, only available on non-IGP systems or IGP systems not supporting IGP loop-through functions
DVI_B_CLK, DVI_B_CLK#	Output, Routed at 100 Ω Diff	TMDS clock, only used for second single-link DVI.	Optional When supported, pins must remain in a high impedance state until module confirms system supports **DVI_B** from the system information structure	Optional, only available on non-IGP systems or IGP systems not supporting IGP loop-through functions
DVI_B_HPD / DVI_C_HPD / DP_A_HPD	Input	Hot plug detect for **DVI_B** or **DVI_C** or **DP_A**.	Required if **DVI_B** single-link or **DVI_C** or **DP_A** is supported	Required if **DVI_B** single-link or **DVI_C** or **DP_A** is supported on system
DVI_C_TX0-2, DVI_C_TX0-2#	Output, Routed at 100 Ω Diff	TMDS output for either single-link DVI or lower links of dual-link DVI. Note: these pins are shared with **LVDS_LTX0-2** and **LVDS_LTX0-2#**	Optional	Optional
DVI_C_TX3-5, DVI_C_TX3-5#	Output, Routed at 100 Ω Diff	TMDS output for upper links of dual-link DVI. Note: these pins are shared with **LVDS_UTX0-2** and **LVDS_UTX0-2#**	Optional	Optional

Signal Name	Input/Output	Description	Module Support	System Support
DVI_C_CLK, DVI_C_CLK#	Output, Routed at 100 Ω Diff	TMDS clock for either single-link or dual-link DVI. Note: these pins are shared with **LVDS_LCLK** and **LVDS_LCLK#**	Optional	Optional
DDCA_CLK	Output, 4.7 KΩ pull-up required on module	Serial link, can connect to **VGA**, **DVI_A**, **DVI_B** or **DVI_C**. Configuration needs to be stored in MXM system information.	Required	Required if System supports VGA or DVI interfaces
DDCA_DAT	Bi-Directional, 4.7 KΩ pull-up required on module	Serial link, can connect to **VGA**, **DVI_A**, **DVI_B** or **DVI_C**. Configuration needs to be stored in MXM system information.	Required	Required if System supports VGA or DVI interfaces
DDCB_CLK	Output, 4.7 KΩ pull-up required on module	Serial link, can connect to **VGA**, **DVI_A, DVI_B** or **DVI_C**. Configuration needs to be stored in MXM system information.	Required	Required if System supports two interfaces, VGA or DVI, on separate connectors
DDCB_DAT	Bi-Directional, 4.7 KΩ pull-up required on module	Serial link, can connect to **VGA**, **DVI_A**, **DVI_B**, **or DVI_C** Configuration needs to be stored in MXM system information.	Required	Required if System supports two interfaces, VGA or DVI, on separate connectors
DDCC_CLK	Output, 2.2 KΩ pull-up required on module	Serial link, connect to EDID LVDS Panel and to MXM System Information ROM. This link is not to be used for external interfaces	Required	Optional
DDCC_DAT	Bi-Directional, 2.2 KΩ pull-up required on module	Serial link, connect to EDID LVDS Panel and to MXM System Information Rom. This link is not to be used for external interfaces	Required	Optional
LVDS_PPEN	Output	LVDS Panel Power enable	Required	Required if System has LVDS panel
LVDS_BLEN	Output	LVDS Panel backlight enable	Required	Required if System has LVDS panel
LVDS_BL_BRGHT	PWM Output	LVDS Panel brightness control, duty cycle determines output level	Required	Optional
LVDS_UTX0-3, LVDS_UTX0-3#	Output, Routed at 100 Ω Diff	LVDS output for dual-link (upper/even link)	Required	Optional
LVDS_UCLK, LVDS_UCLK#	Output, Routed at 100 Ω Diff	LVDS clock for dual-link (upper/even link)	Required	Optional
LVDS_LTX0-3, LVDS_LTX0-3#	Output, Routed at 100 Ω Diff	LVDS output for either single-link or dual-link (lower/odd link)	Required	Optional

Signal Name	Input/Output	Description	Module Support	System Support
LVDS_LCLK, LVDS_LCLK#	Input, Routed at 100 Ω Diff	LVDS clock for either single-link or dual-link (lower/odd link)	Required	Optional
DP_A_L0-3, DP_A_L0-3#	Output, Routed at 100 Ω Diff	DisplayPort A main links, lane 0-3. DC blocking capacitors shall be placed on the MXM graphics module.	Optional (mutually exclusive with **DP_B**)	Optional
DP_B_L0-3, DP_B_L0-3#	Output, Routed at 100 Ω Diff	DisplayPort B main links, lane 0-3. DC blocking capacitors shall be placed on the MXM graphics module.	Optional (mutually exclusive with **DP_A**)	Optional
DP_x_AUX, DP_x_AUX#	Bidirectional, Routed at 100 Ω Diff	DisplayPort auxiliary channel (associated with **DP_A** or **DP_B**). AUX/DDC multiplexer function for DVI/HDMI dongle support over DP and DC blocking capacitors shall be supported by the MXM graphics module. No pull-up on the module for DDC function.	Required if **DP_A** or **DP_B** is supported	Required if **DP_A** or **DP_B** is supported
DP_B_HPD	Input	Hot plug detect for **DP_B**	Required if **DP_B** is supported	Required if **DP_B** is supported
HDA_SYNC	Input	HD Audio 48 KHz frame sync	Required if the MXM module needs HD audio to support HDMI or DP	Required if system supports HDMI or DP with audio
HDA_BCLK	Input	HD Audio 24 MHz bit clock	Required if the MXM module needs HD audio to support HDMI or DP	Required if system supports HDMI or DP with audio
HDA_RST#	Input	HD Audio reset	Required if the MXM module needs HD audio to support HDMI or DP	Required if system supports HDMI or DP with audio
HDA_SDI	Output	HD Audio serial data in	Required if the MXM module needs HD audio to support HDMI or DP	Required if system supports HDMI or DP with audio
HDA_SDO	Input	HD Audio serial data out	Required if the MXM module needs HD audio to support HDMI or DP	Required if system supports HDMI or DP with audio
TV_Y / HDTV_Y / TV_CVBS	Output, Routed at 50 Ω. 150 Ω resistor to GND near driver	**TV_OUT** Luma/**HDTV_OUT** Luma/**TV_OUT** Composite when using S-Video and no separate composite connector in the system	Optional	Optional
TV_C / HDTV_Pr	Output, Routed at 50 Ω 150 Ω resistor to GND near driver	**TV_OUT** Chroma/**HDTV_OUT** Chroma Red	Optional	Optional

Signal Name	Input/Output	Description	Module Support	System Support
TV_CVBS / HDTV_Pb	Output, Routed at 50 Ω 150 Ω resistor to GND near driver	**TV_OUT** Composite/**HDTV_OUT** Chroma Blue	Optional	Optional
VGA_BLU	Output, Routed at 50 Ω 150 Ω resistor to GND near driver	**VGA** Blue Output	Required	Optional
VGA_RED	Output, Routed at 50 Ω 150 Ω resistor to GND near driver	**VGA** Red Output	Required	Optional
VGA_GRN	Output, Routed at 50 Ω 150 Ω resistor to GND near driver	**VGA** Green Output	Required	Optional
VGA_HSYNC	Output	**VGA** Horizontal Sync	Required	Optional
VGA_VSYNC	Output	**VGA** Vertical Sync	Required	Optional
SMB_CLK	Input	Serial link for thermal sensor on GPU. Connect to motherboard's SMBus Clock signal.	Required	Optional Pull-up required if supported
SMB_DAT	Bi-Dir	Serial link for thermal sensor on GPU. Connect to motherboard's SMBus Data signal.	Required	Optional Pull-up required if supported
THERM#	Output, open drain, active low	Indicates an over temperature situation on the GPU.	Required	Optional
PRSNT1#	GND	Card present detect, indicates if MXM graphics module is present. Tie to pull-up on motherboard. If high then MXM is not present. If low then MXM is present. Can be used to control IGP upgrade multiplexers	Required	Optional
PRSNT2# / PEX_LSW#	Input	PCI-Express Mode. System tie to ground for low-swing transmitters. System shall no connect for standard-swing transmitters.	Required	Required
CLK_REQ#	Output, open drain, active low	PCI Express reference clock request	Required	Optional
PEX_RST#	Input, active low	PCI_Express reset	Required	Required
PEX_REFCLK, PEX_REFCLK#	Input, Routed at 100 Ω Diff	PCI Express reference clock.	Optional	Required
PEX_TX0-15, PEX_TX0-15#	Input, Routed at 100 Ω Diff	PCI Express 16 lanes, output from Root Complex. DC blocking capacitors shall be placed on the motherboard.	Required	Required
PEX_RX0-15, PEX_RX0-15#	Output, Routed at 100 Ω Diff	PCI Express 16 lanes, input to Root Complex. DC blocking capacitors shall be placed on the MXM graphics module.	Required	Required

Signal Name	Input/Output	Description	Module Support	System Support
RUNPWROK	Input	Indicates that all power to the MXM is within the specified tolerances	Optional	Required
SPDIF	Input, routed at 50 Ω	**SPDIF** input to the MXM module to support audio via HDMI or DP	Required if the MXM module needs SPDIF to support HDMI or DP audio	Required if system supports HDMI or DP with audio
AC/BATT#	Input, 10 KΩ pull down on module. 0 = Battery performance. 1 = AC performance.	Signals the MXM Module to transition from high performance AC mode to moderate performance battery mode within 50 ms period.	Required only if supporting high performance AC mode	Required If AC mode only, pullup to 3V3RUN with 2 KΩ resistor. If Battery mode only, no connect. If both modes supported, system sets the signals according to desired performance level.
3V3RUN	Power input	3.3 V run power	Optional	Required
5VRUN	Power input	5 V run power	Optional	Required
2V5RUN	Power input	2.5 V run power	Optional	Required
1V8RUN	Power input	1.8 V run power	Optional	Required
PWR_SRC	Power input	Battery power	Optional	Required

Power Requirements

The Mobile PCI Express Module (MXM) requires the following power to be provided by the system as shown in Table 9.

Table 9. Power Requirements

Voltage Rail	Voltage	Current	Power	Notes
3V3RUN	3.3 V +/- 5%	1.5 Amps	4.95 W	3.3 V run. Motherboard must place bulk capacitance at the MXM connector of at least 4.7 µF.
5VRUN	5 V +/- 5%	0.5 Amps	2.5 W	5 V run
2V5RUN	2.5 V +/- 5%	0.5 Amps	1.25 W	2.5 V run
1V8RUN	1.8 V +/- 5%	3.5 Amps	6.3 W	1.8 V run. Motherboard must place bulk capacitance at the MXM connector of at least 4.7 µF.
PWR_SRC	7.5 V***** to 22 V	Up to 4 Amps or up to 16 Amps for HE connector when used with MXM-III or MXM-IV modules	Platform Dependent	Primary system power rail. **PWR_SRC** power capability must be included in MXM system information. Motherboard must place bulk capacitance at the MXM connector of at least 20 µF.

***** For a platform MXM input budget greater than 30 W using the standard MXM connector, the minimum **PWR_SRC** voltage is input budget/4A. For example, an input budget of 35 W, the **PWR_SRC** Vmin = 8.75 V

Auxiliary Signals

Table 10. Auxiliary Signals DC Specification

Symbol	Parameter	Conditions	Minimum	Maximum	Units	Notes
LVDS_PPEN, LVDS_BLEN, LVDS_BL_BRGHT						
V_{OL}	Output Low Voltage	8 mA	0V	0.1 V_{3V3RUN}	V	
V_{OH}	Output High Voltage	8 mA	0.9 V_{3V3RUN}	V_{3V3RUN}	V	
C_{out}	Output Pin Capacitance			30	pF	
DVI_A_HPD, DVI_B_HPD, DVI_C_HPD						
V_{IL}	Input low voltage		-0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	5.5	V	
DP_HPD						
V_{IL}	Input low voltage		-0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	3.6	V	
HDA_SYNC, HDA_BCLK, HDA_SDO, HDA_RST#						
V_{IL}	Input low voltage		-0.5	0.35 V_{3V3RUN}	V	
V_{IH}	Input High Voltage		0.65 V_{3V3RUN}	V_{3V3RUN} +0.5	V	
C_{in}	Input Pin Capacitance			7.5	pF	
HDA_SDI						
V_{OL}	Output Low Voltage	Iout=1500 uA	0	0.1 V_{3V3RUN}	V	
V_{OH}	Output High Voltage	Iout=-500 uA	0.9 V_{3V3RUN}	V_{3V3RUN}	V	

Symbol	Parameter	Conditions	Minimum	Maximum	Units	Notes
RUNPWROK						
V_{IL}	Input low voltage		-0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{3V3RUN} +0.5	V	
I_{in}	Input Leakage Current	0 to 3.3 V	-10	10	uA	
C_{in}	Input Pin Capacitance			30	pF	
AC/BATT#, PEX_RST#						
V_{IL}	Input low voltage		-0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{3V3RUN} +0.5	V	
I_{in}	Input Leakage Current	0 to 3.3 V	-10	10	uA	
C_{in}	Input Pin Capacitance			7	pF	
THERM#, CLKREQ#						
V_{OL}	Output Low Voltage	4 mA	0V	0.2	V	
V_{HMAX}	Max High Voltage			V_{3V3RUN} + 0.5	V	1
I_{lkg}	Output Leakage Current	0 to 3.3 V	-50	50	uA	
C_{out}	Output Pin Capacitance			30	pF	

Symbol	Parameter	Conditions	Minimum	Maximum	Units	Notes
DDCA_CLK, DDCA_DAT, DDCB_CLK, DDCB_DAT, DDCC_CLK, DDCC_DAT						
V_{IL}	Input low voltage		-0.5	0.8	V	
V_{IH}	Input High Voltage		2.1	V_{3V3RUN} +0.5	V	
V_{OL}	Output Low Voltage	3 mA	0	0.4	V	
V_{HMAX}	Max High Voltage			V_{3V3RUN} + 0.5	V	2
SPDIF						
V_{IL}	Input low voltage		-0.5	0.3 V_{3V3RUN}	V	
V_{IH}	Input High Voltage		0.7 V_{3V3RUN}	V_{3V3RUN} +0.5	V	
C_{in}	Input Pin Capacitance			7	pF	
SMB_CLK, SMB_DAT						
V_{IL}	Input low voltage		-0.5	0.8	V	
V_{IH}	Input High Voltage		2.1	V_{5VRUN} +0.5	V	
V_{OL}	Output Low Voltage	3 mA	0	0.4	V	
V_{HMAX}	Max High Voltage			V_{5VRUN} + 0.5	V	1
I_{lkg}	Output Leakage Current	0 to 5 V	-10	10	uA	
C_{out}	Output (I/O) Pin Capacitance			30	pF	
VGA_VSYNC, VGA_HSYNC						
V_{OL}	Output Low Voltage	8 mA	0 V	0.1 V_{3V3RUN}	V	
V_{OH}	Output High Voltage	8 mA	0.9 V_{3V3RUN}	V_{3V3RUN}	V	
C_{out}	Output Pin Capacitance			30	pF	

1. Open-drain output a pull-up is required on the system board. There is no V_{OH} specification for these signals. The number given, V_{HMAX} is the maximum voltage that can be applied to this pin.
2. Open-drain output a pull-up is required on the module. There is no V_{OH} specification for these signals. The number given, V_{HMAX} is the maximum voltage that can be applied to this pin.

Table 11. Auxiliary Signals AC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes	Figure
T_{RPORST}	RUNPWROK to **PEX_RST#** inactive	100		ms		17,18
t_{CSTRST}	**PEX_REFCLK** stable to **PEX_RST#** inactive	100		us		17,18
t_{RST}	**PEX_RST#** active time	100		us		18
t_{RSTVUS}	**PEX_RST#** active to Voltage unstable	0		ns		18,19
t_{SPDRST}	Voltage unstable to **PEX_RST#** active		500	ns		
t_{RSTSMB}	**PEX_RST#** inactive to SMBus active	15		ms		17,18
t_{RSTTHM}	**PEX_RST#** inactive to **THERM#** active	15		ms		17,18
t_{PPLD}	**LVDS_PPEN** active to LVDS Data active	0.5	60	ms		20
t_{LDBL}	LVDS Data active to **LVDS_BLEN** active	200		ms		20
t_{BLLD}	**LVDS_BLEN** inactive to LVDS Data inactive	200		ms		20
t_{LDPP}	LVDS Data inactive to **LVDS_PPEN** inactive	0	50	ms		20
T_{PPOFF}	**LVDS_PPEN** inactive time	200		ms		20

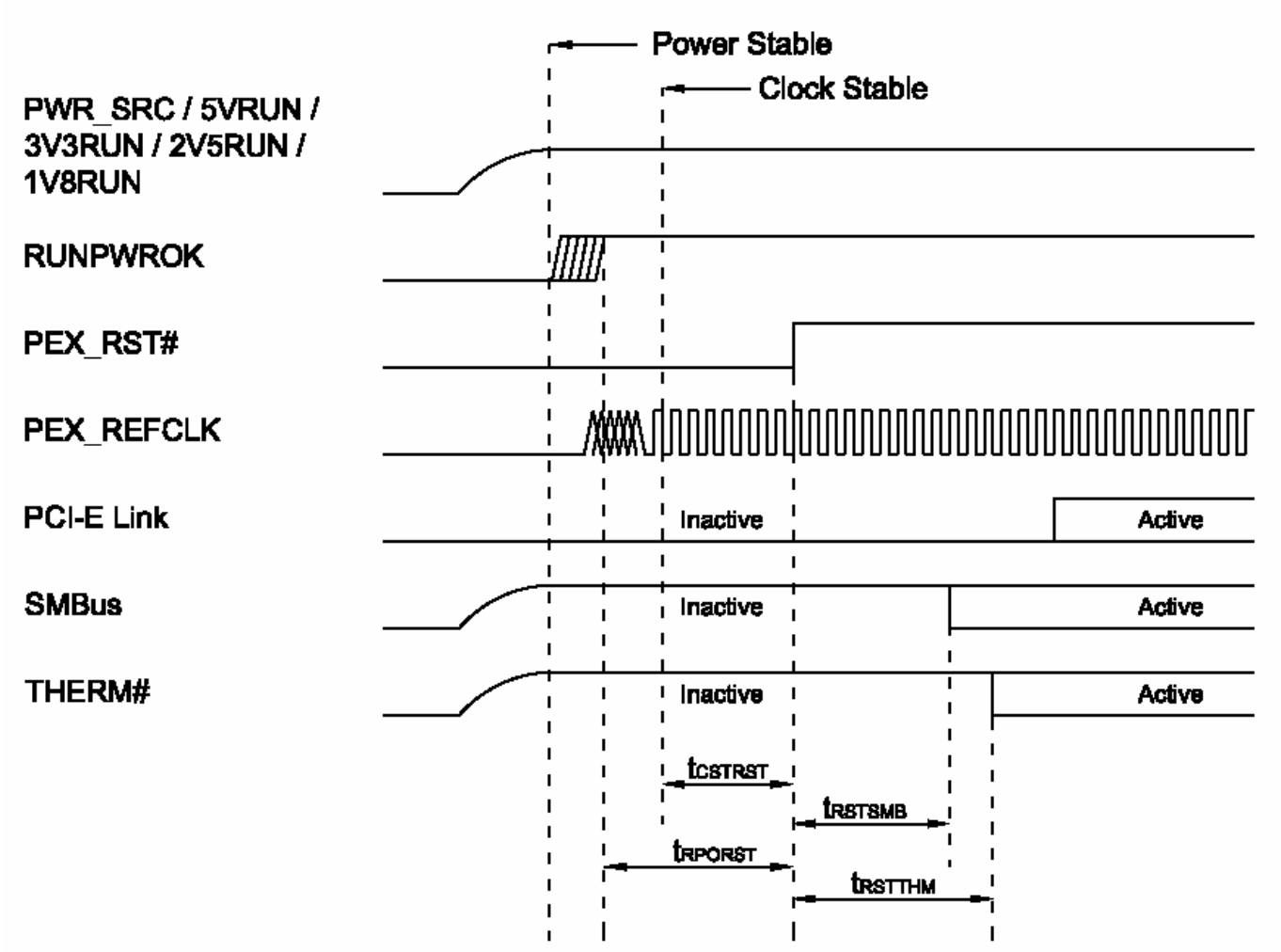

Figure 30. Power Up

Power Management States (S0 – S3/S4 – S0)

When a system enters S3/S4, the module is placed in $D3_{hot}$ state with PCI Express links in L2 prior to any power transitions. When **PEX_RST#** goes active, SMBus and **THERM#** will transition to inactive. **PWR_SRC**, all RUN voltages and **PEX_REFCLK** will go inactive and stay inactive until a wakeup event. As a result of the removal of **PWR_SRC** and all RUN voltages the module will enter $D3_{cold}$ state.

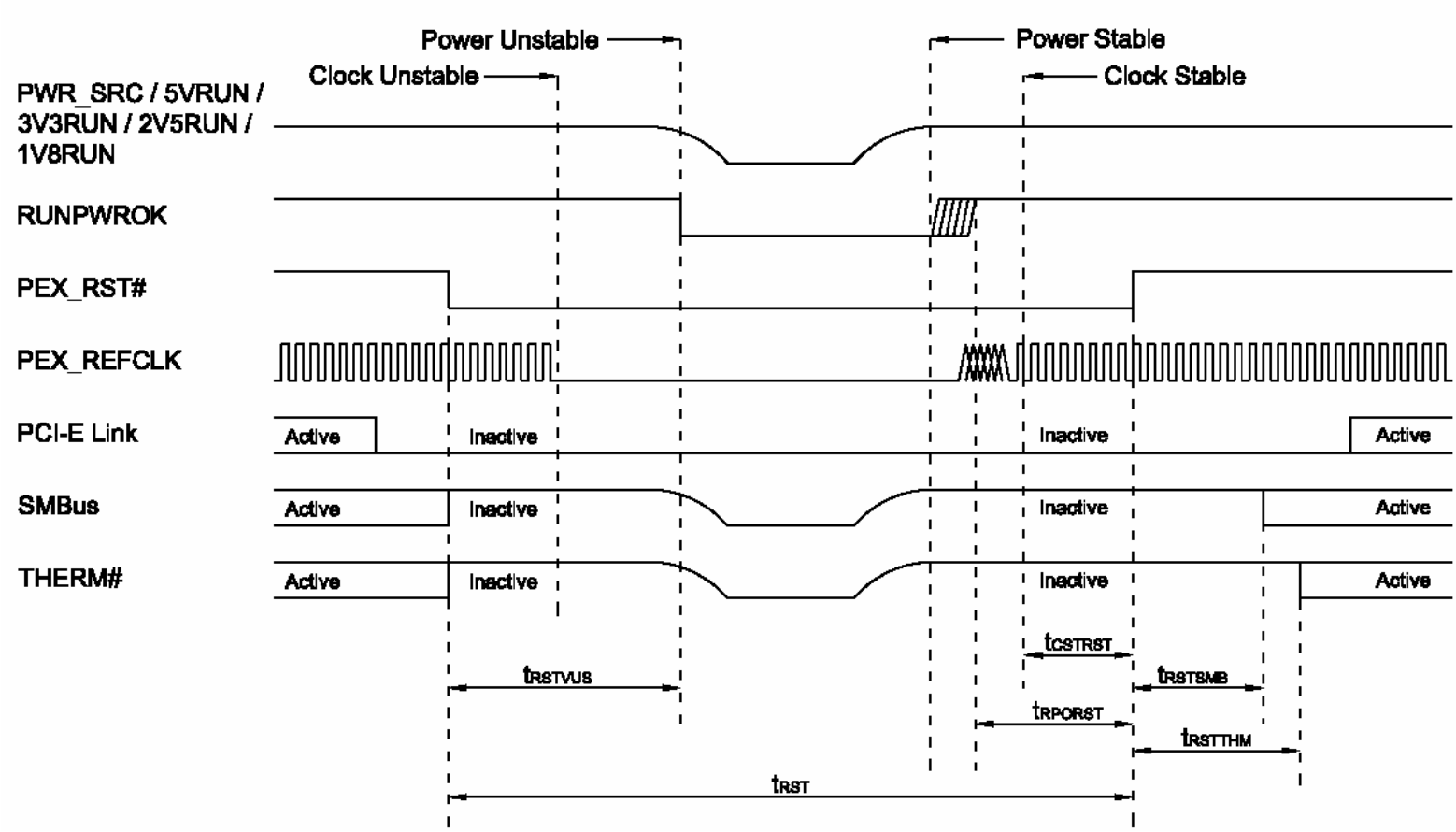

Figure 31. Power Management States (S0 S3/S4 – S0)

Power Down

PCI-Express link will go to inactive state, $D3_{hot}$, prior to **PEX_RST#** going active, except in the case of a surprise power down. SMBus and **THERM#** go inactive after **PEX_RST#** goes active. In the case of a surprise power down, **PEX_RST#** must go active t_{SPDRST} after **PWR_SRC** or any RUN voltage going out of specification.

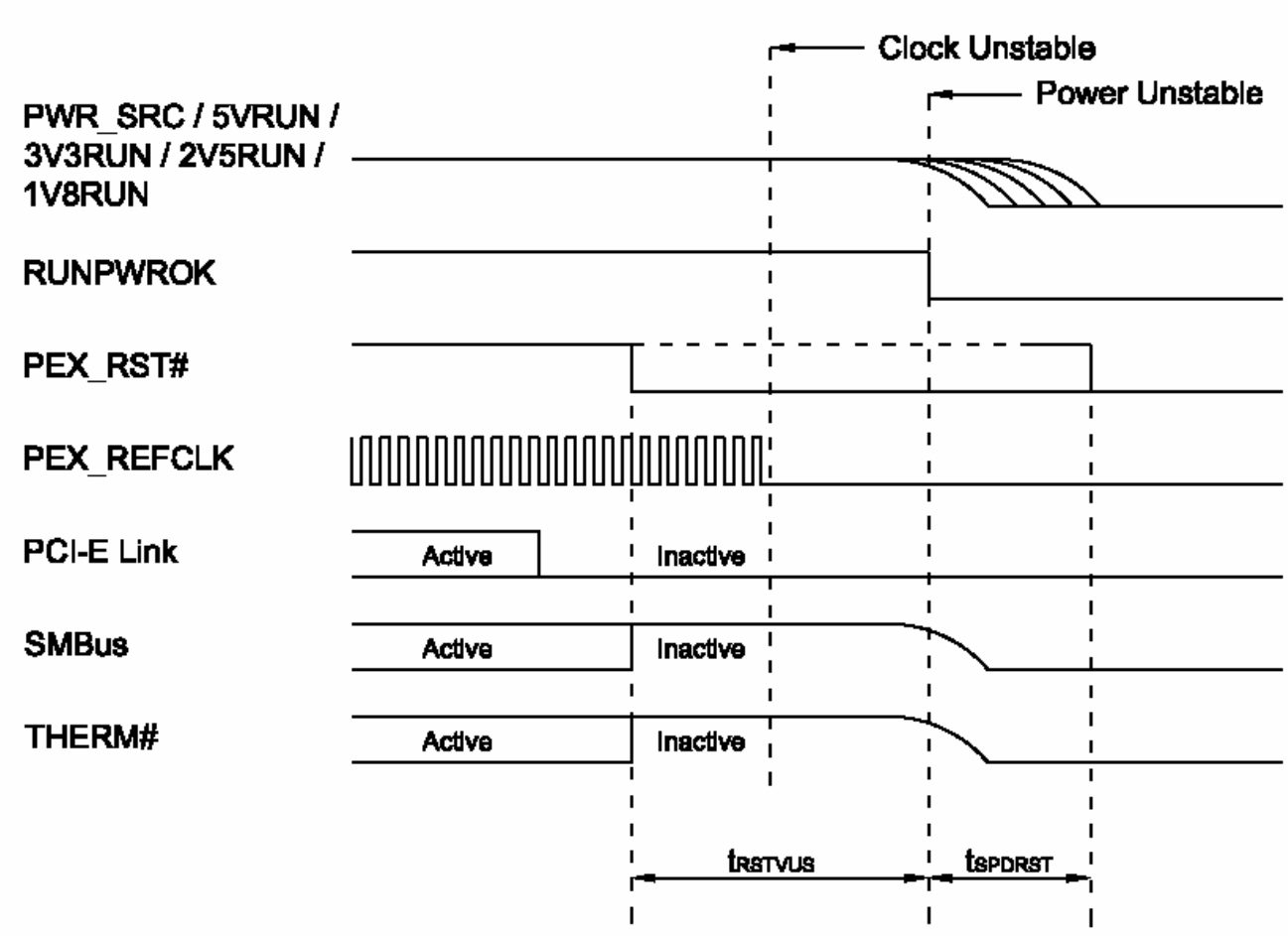

Figure 32. Power Down

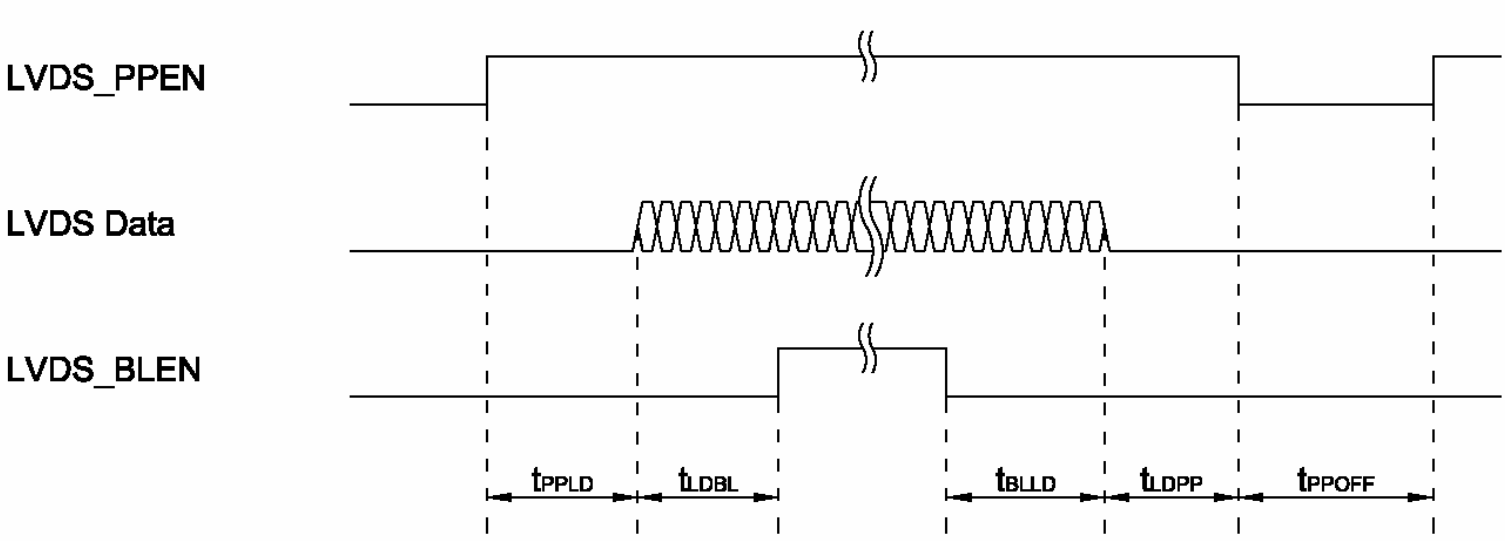

Figure 33. LVDS Panel Timing

PCI Express Electrical Budgets

PCI Express Link Topology

MXM PCI Express topology consists of two components, system board and module. The system board includes MXM connector and edge fingers of the module. The top of the module's edge fingers is defined as a common reference point for electrical budgets and parameters. The interconnect budget allocations differ with respect to the transmitter and receiver paths of the same component. This is to account for AC coupling capacitors in the transmit path of the component.

Note: Signals at the package pins for both transmit and receive follow the *PCI Express Base specification*, and *PCI-Express Mobile Graphics Low Power Addendum*, recommendations

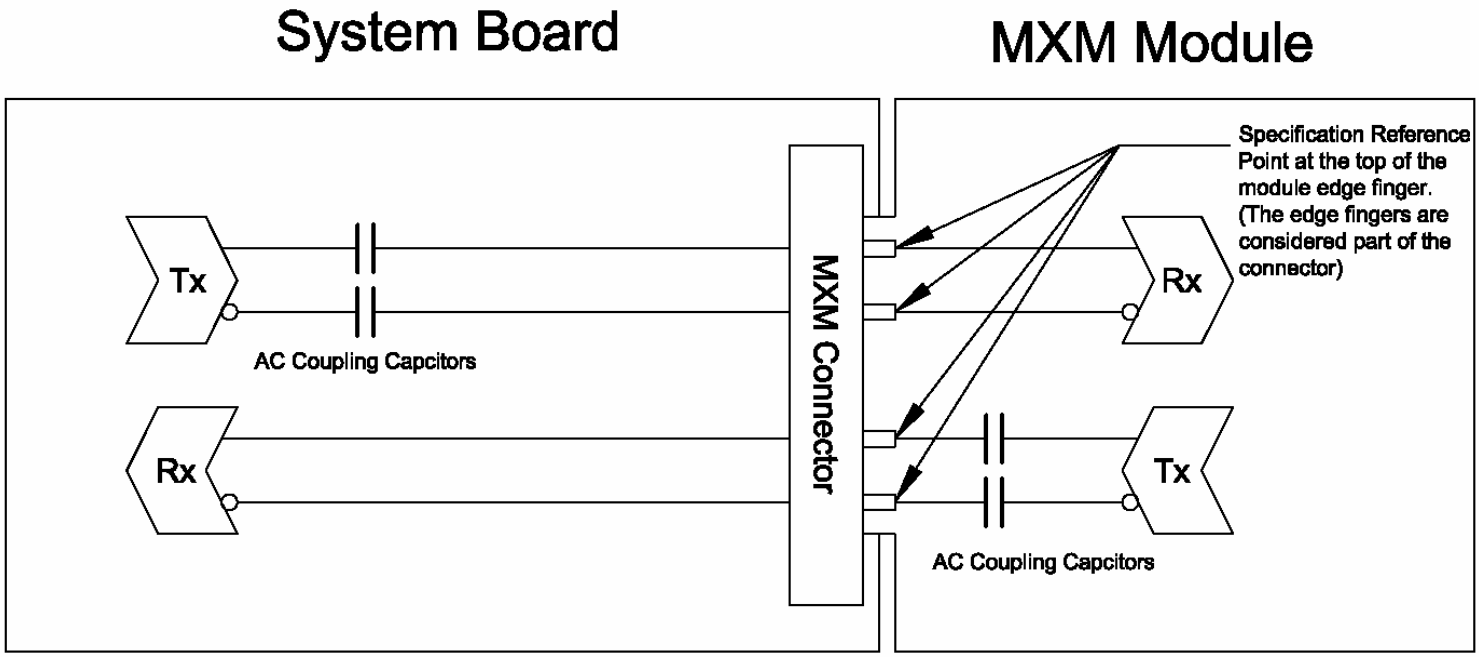

Figure 34. PCI Express Link Topology

PCI Express Insertion Loss

The maximum loss values in dB (decibels) are specified for the two components, system board and module. Insertion loss is defined as the ratio of the voltage at the ASIC package pin and the voltage at the specification reference point, terminated by 100 Ω differential termination, realized by two 50 Ω resistances referenced to ground at the end of the interconnect path. Loss budget values include all possible crosstalk impacts (near-end and far-end) and potential mismatch of the actual interconnect with respect to the 100 Ω reference load.

The *PCI Express Base Specification,* version 1.1 allows an interconnect loss of 13.2 dB for 1.25 GHz (non de-emphasized) signals and 9.2 dB for 625 MHz (de-emphasized) signals. Likewise the *PCI Express Low-Power addendum,* version 1.0 allows an interconnect loss of 7.2 dB for 1.25 GHz signals. From this, 1.25 dB is held in reserve as a guard band to allow for any additional attenuation that might occur when the module and the system board are actually mated. The allocated loss budget values in the Table 12 directly correlates to the eye diagram voltages in the PCI Express transmitter compliance and receiver sensitivity eye diagram section. Trade-offs in terms of attenuation, crosstalk, and mismatch can be made within the budget allocations specified.

All PCI Express differential trace pairs are required to be referenced to the ground plane.

Table 12. Allocation of Interconnect Path Insertion Loss

Symbol	Parameter	Insertion Loss		Units	Notes
Standard Swing at 1.25 GHz (non de-emphasized)					
L_{MTx}	Module transmitter path maximum loss	3.14		dB	1, 3
L_{MRx}	Module receiver path maximum loss		1.95	dB	1
L_{STx}	System board transmitter path maximum loss		10.00	dB	2, 3
L_{SRx}	System board receiver path maximum loss	8.81		dB	2
L_{GB}	Guard Band	1.25		dB	
L_T	Total maximum loss	13.2		dB	
Standard Swing at 625 MHz (de-emphasized)					
L_{MTx}	Module transmitter path maximum loss	2.59		dB	1, 3
L_{MRx}	Module receiver path maximum loss		1.60	dB	1
L_{STx}	System board transmitter path maximum loss		6.35	dB	2, 3
L_{SRx}	System board receiver path maximum loss	5.36		dB	2

Symbol	Parameter	Insertion Loss		Units	Notes
L_{GB}	Guard Band	1.25		dB	
L_T	Total maximum loss	9.2		dB	
Low Swing at 1.25 GHz					
L_{MTx}	Module transmitter path maximum loss	2.14		dB	1, 3
L_{MRx}	Module receiver path maximum loss		1.32	dB	1
L_{STx}	System board transmitter path maximum loss		4.63	dB	2, 3
L_{SRx}	System board receiver path maximum loss	3.81		dB	2
L_{GB}	Guard Band	1.25		dB	
L_T	Total maximum loss	7.2		dB	

1. The module budget does not include the module edge fingers or the connector.
2. The system board budget includes the MXM connector and assumes it is mated with the module's edge fingers
3. Value includes potential attenuation from the AC coupling capacitor on the transmitter interconnect

Note: The insertion loss budget distributions above are used to derive the eye diagram heights and are provided here only as a design guideline. Compliance measurements must actually be verified against the eye diagrams themselves as defined in the PCI Express transmitter compliance and receiver sensitivity eye diagram section.

As a guide for design and simulation, the following derivation of the budgets may be assumed for standard swing at 1.25 GHz:

- 13.2 dB total loss
- 1.25 dB guard band
- 5.2 dB near-end crosstalk and impedance mismatches
- The resultant loss allocations are then assumed per differential pair:

L_{MTx} = 1.10 dB; L_{MRx} = 0.70 dB; L_{STx} = 7.30 dB; L_{SRx} = 6.90 dB.

Note: Standard swing at 625 MHz and low swing at 1.25 GHz may be derived in a similar manner.

PCI Express Jitter Budgets

Maximum Jitter values in terms of percentage of Unit Interval (UI = 400 ps for 2.5 G transfers/sec) are specified for the two components, system board and module. Jitter values for each path are defined with respect to 100 Ω differential termination, realized by two 50 Ω resistances referenced to ground at the end of the interconnect path. Jitter budget values include all possible crosstalk impacts (near-end and far-end) and potential mismatch of the actual interconnect with respect to the 100 Ω reference load.

The *PCI-Express Base Specification,* version 1.1 allows an interconnect jitter budget of 0.225 UI (equivalent to 90 ps for a 400 ps unit interval). No additional guard band is specifically allocated. The allocated jitter budget values in the Table 13 directly correlates to the eye diagram width in the PCI Express transmitter compliance and receiver sensitivity eye diagram section. Trade-offs in terms of attenuation, crosstalk, and mismatch can be made within the budget allocations specified.

Table 13. Allocation of Interconnect Jitter

Symbol	Parameter	STx to MRx Path	MTx to SRx Path	Units	Notes
J_{MTx}	Module transmitter path maximum jitter		0.0600	UI	1, 3
J_{MRx}	Module receiver path maximum jitter	0.0525		UI	1
J_{STx}	System board transmitter path maximum jitter	0.1725		UI	2, 3
J_{SRx}	System board receiver path maximum jitter		0.1650	UI	2
J_T	Total maximum jitter	0.2250		UI	

1. The module budget does not include the module edge fingers or the connector.
2. The system board budget includes the MXM connector and assumes it is mated with the module's edge fingers
3. Value includes potential jitter from the AC coupling capacitor on the transmitter interconnect

Note: The jitter budget distributions above are used to derive the eye diagram widths and are provided here only as a design guideline. Compliance measurements must actually be verified against the eye diagrams themselves as defined in the PCI Express transmitter compliance and receiver sensitivity eye diagram section below.

PCI Express Transmitter and Receiver Eye Diagrams

Eye diagrams are generated with all links active and assumed to have an ideal reference clock without jitter. All values are referenced to 100 Ω differential termination, realized as two 50 Ω resistances referenced to ground at the end of the interconnect path. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating the eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

The eye diagrams for the transmitter path compliance and minimum receiver path sensitivity compliance are defined in Table 14, Table 15 and Figure 35 to Figure 38.

Table 14. Module PCI Express Eye Diagram Specifications

Symbol	Parameter	Minimum	Maximum	Units	Notes	Figure
v_{TxM}	Module differential peak-peak output voltage	557		mV	1	22
v_{TxM_D}	Module differential peak-peak output voltage de-emphasized	375		mV	1	22
t_{TxM}	Module output eye width	289		ps	3	22
J_{TxM}	Module median to peak output jitter		55.5	ps	5	
v_{RxM}	Module differential peak-peak input voltage	219		mV	2	22
v_{RxM_D}	Module differential peak-peak input voltage de-emphasized	210		mV	2	22
t_{RxM}	Module input eye width	244		ps	4	22
J_{RxM}	Module median to peak input jitter		78.0	ps	6	
v_{TxM_L}	Module differential peak-peak low swing output voltage	313		mV		23
t_{TxM_L}	Module low swing output eye width	289		ps	3	23
v_{RxM_L}	Module differential peak-peak low swing input voltage	204		mV		23
t_{RxM_L}	Module low swing input eye width	244		ps	4	23

1. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (vTxM_D).
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (vRxM_D).
3. The sample size is 106 UI. This value can be reduced to 276 ps for simulation purpose at BER 10^{-12}
4. The sample size is 106 UI. This value can be reduced to 231 ps for simulation purpose at BER 10^{-12}
5. The sample size is 106 UI. This value can be increased to 62.0 ps for simulation purpose at BER 10^{-12}
6. The sample size is 106 UI. This value can be increased to 84.5 ps for simulation purpose at BER 10^{-12}

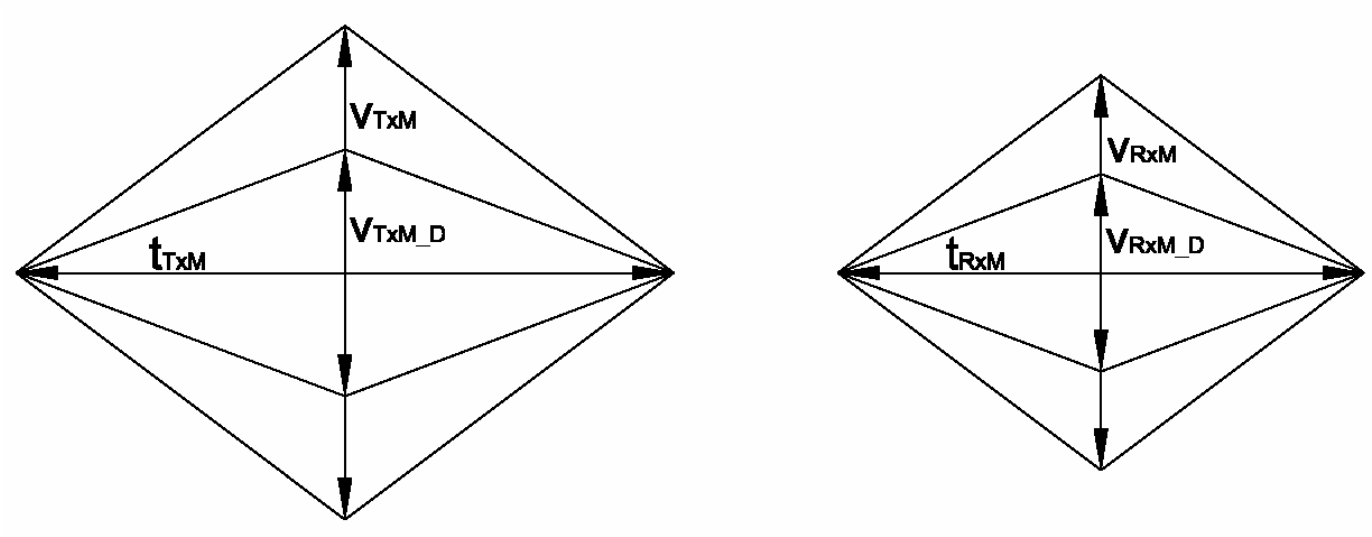

Figure 35. Module Standard Swing Composite Compliance Eye Diagram

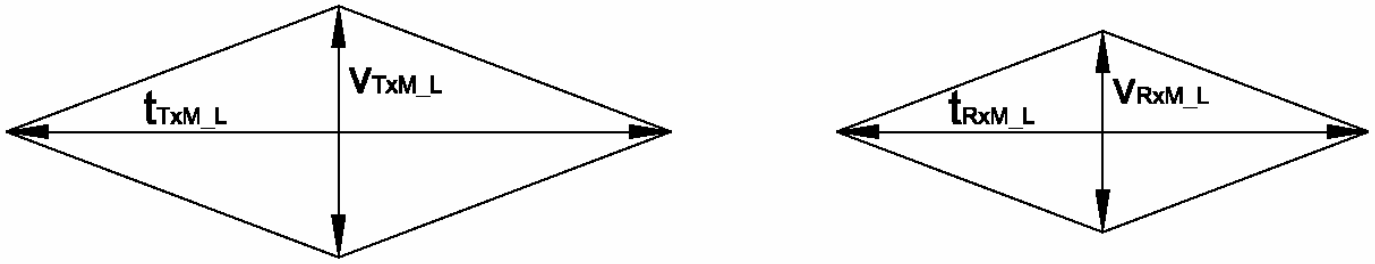

Figure 36. Module Low Swing Compliance Eye Diagram

Table 15. System Board PCI Express Eye Diagram Specifications

Symbol	Parameter	Minimum	Maximum	Units	Notes	Figure
v_{TxS}	System board differential peak-peak output voltage	253		mV	1	24
v_{TxS_D}	System board differential peak-peak output voltage de-emphasized	243		mV	1	24
t_{TxS}	System board output eye width	244		ps	3	24
J_{TxS}	System board median to peak output jitter		78.0	ps	5	
v_{RxS}	System board differential peak-peak input voltage	483		mV	2	24
v_{RxS_D}	System board differential peak-peak input voltage de-emphasized	324		mV	2	24
t_{RxS}	System board input eye width	289		ps	4	24
J_{RxS}	System board median to peak input jitter		55.5	ps	6	
v_{TxS_L}	System board differential peak-peak low swing output voltage	235		mV		25
t_{TxS_L}	System board low swing output eye width	244		ps	3	25
v_{RxS_L}	System board differential peak-peak low swing input voltage	271		mV		25
t_{RxS_L}	System board low swing input eye width	289		ps	4	25

1. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (v_{TxS_D}).
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (v_{RxS_D}).
3. The sample size is 10^6 UI. This value can be reduced to 231 ps for simulation purpose at BER 10^{-12}
4. The sample size is 10^6 UI. This value can be reduced to 276 ps for simulation purpose at BER 10^{-12}
5. The sample size is 10^6 UI. This value can be increased to 84.5 ps for simulation purpose at BER 10^{-12}
6. The sample size is 10^6 UI. This value can be increased to 62.0 ps for simulation purpose at BER 10^{-12}

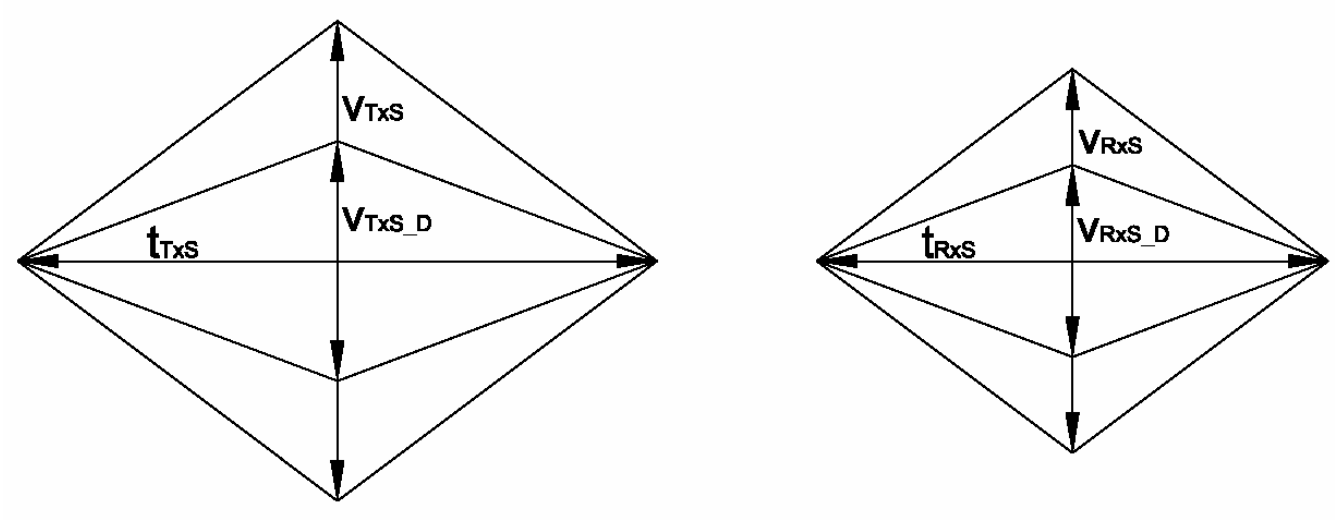

Figure 37. System Board Standard Swing Composite Compliance Eye Diagram

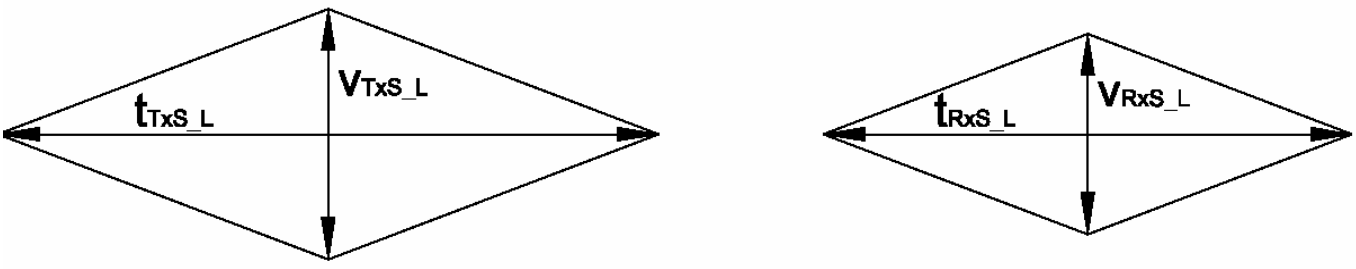

Figure 38. System Board Low Swing Compliance Eye Diagram

PCI Express Interface Skew

The skew at any point is measured using zero crossings of the differential voltage of the compliance pattern, while simultaneously transmitting on all physical lanes. The compliance pattern is defined in the *PCI Express Base Specification,* version 1.1.

Table 16. PCI Express Interface Skew

Symbol	Parameter	Value	Units	Notes
S_T	Total interconnect skew	1.60	ns	1
S_M	Module inter-pair skew	0.35	ns	
S_S	System Board inter-pair skew	1.25	ns	
S_{M_PN}	Module intra-pair skew	1	ps	
S_{S_PN}	System board intra-pair skew	2	ps	

1. This does not include transmitter output skew, $L_{TX\text{-}SKEW}$ (specified in the *PCI Express Base Specification,* revision 1.1). The total skew at the receiver, $S_T + L_{TX\text{-}SKEW}$, is smaller than $L_{RX\text{-}SKEW}$ (specified in the *PCI Express Base Specification,* revision 1.1) to minimize latency for the MXM link topology.

PCI Express Equalization

Standard swing mode: to reduce ISI, 3.5 dB ± 0.5 dB below the first bit de-emphasis in the transmitter is required for the system board and module. For implementation details, refer to Chapter 4 in the *PCI-Express Base Specification,* version 1.1.

Low swing mode: due to the reduced loss budget, the need for transmitter de-emphasis is removed and must not be implemented. This means the amplitude of each bit, as measured into the test load at the specified reference point, is uniform no matter whether it is a transition bit or whether multiple bits of the same polarity are output in succession.

Display Requirements

Panel Type

MXM system supports single-link 18 bpp, dual-link 18 bpp, single-link 24 bpp or dual-link 24 bpp panels. Panel can be EDID or non-EDID. In order to support non-EDID panels the SBIOS must support INT15h callback function 0x5F80, function 2 as described in the *MXM Version 2.1 Software Specification*.

LVDS Panel Power

The motherboard shall provide power to the system's LVDS panel. The power is controlled by **LVDS_PPEN**.

VGA, TV_Out Impedance

The motherboard shall route all **VGA** signals and **TV_OUT** signals with 50 Ω impedance. A 150 Ω termination resistor to ground shall be placed at the end of the trace as close as possible to the output filters.

The MXM graphics module must route all **VGA** and **TV_OUT** signals with 50 Ω impedance and place a 150 Ω termination resistor to ground as close as possible to the signal driver.

Output Filters

The motherboard is recommended to have output filters on all **VGA** output lines and on all TV output lines. These filters should be placed as close as possible to the external connectors.

Other Requirements

Video BIOS Expansion ROM

The MXM v 2.1A module shall have a video BIOS expansion ROM local to the module.

MXM System Information ROM

The motherboard is required to store the MXM System Information in either the SBIOS or in the MXM System Information ROM. The implementation is a design decision left to the system provider's discretion. Information regarding the data stored in the MXM System Information is found in the *MXM Version 2.1 Software Specification*.

For MXM System Information ROM implementations, the Motherboard is required to place a 256 Byte serial ROM that connects to **DDCC_CLK** and **DDCC_DAT** with a device address of 0xAC. The ROM must be compatible to an Atmel 24C02 and operate with 3.3 V signaling.

MXM modules compliant to the *MXM Graphics Module Thermal Electromechanical Specification*, version 2.1 or higher, must support MXM System Information, version 2.1 or higher.

Power Throttling

The MXM module will automatically detect power supply limitations for each performance mode and thermal limitations of the platform and will automatically throttle its clocks to stay within the power and thermal limits. If the platform's power supply and system thermal solution are equal to or exceeds the MXM module power and thermal requirements, the MXM module will run at full speed. The MXM system information data contains the necessary information for MXM throttling. This data is stored in either the SBIOS or the MXM system information ROM on the system's motherboard.

AC/BATT#

AC/BATT# (pin 169) signals a module to change performance level based on the logic state. A logic high indicates high performance AC graphics mode. A logic low indicates moderate performance battery graphics mode. There are corresponding entries in the MXM system information to support parameters for each mode. Refer to the *MXM Version 2.1 Software Specification* (SP-03494-001) for more information.

When **AC/BATT#** is a logic high, then transitions to a logic low, the module must transition from AC performance mode to a performance level equal to or less than battery performance mode within 50mS. After transitioning, the module may then adjust to battery performance mode as indicated by the logic low.

When **AC/BATT#** is a logic low, then transitions to a logic high, the module must transition from battery performance mode to AC performance mode.

A 10 KΩ pull down resistor to ground is required on the MXM module.

A system that supports battery mode only shall not connect to **AC/BATT#.**

A system that only supports AC performance mode is required to have a 2 KΩ pull up to **3V3RUN** on **AC/BATT#.**

SMBUS

The MXM v 2.1A module shall connect a thermal sensor, compatible to the MAX6649 or LM99, to the SMBus for reading the GPU die temperature. The system may access the GPU die temperature at one of four possible SMBus addresses 0x98, 0x9E, 0x56, or 0x32. Although a module may only respond to one or more of the four addresses, the system must reserve all four addresses to avoid system address contention. The SMBus address shown here is the 8-bit address, where the 7 most significant bits are the address and the least significant bit is the read/write bit.

Table 17. Module SMBus Address

SMBus Address	7-bit Address	Write Address	Read Address
0x98	1001 100	0x98	0x99
0x9E	1001 111	0x9E	0x9F
0x56	0101 011	0x56	0x57
0x32	0011 001	0x32	0x33

5 V Tolerance

The motherboard shall provide back drive isolation and level shifting for all DDC lines, **VGA_HSYNC** and **VGA_VSYNC**. The MXM graphics modules do not drive output signals at 5 V output levels and its inputs are not 5 V tolerant unless specifically stated.

DVI Detection Circuitry

The motherboard may have EMI filters on each **DVI_HPD** line used. The MXM v 2.1A graphics module is required to provide all other signal conditioning as needed.

MXM Grounding

The MXM v 2.1A graphics module is grounded through the MXM connector and the integration sites. Each integration site shall have a 6.0 mm pad top and bottom, void of solder mask, for the standoff grounding. The thermal solution will be grounded through the thermal mounting holes and the landing area around the holes.

Power Up Sequencing

There is no requirement for power up sequencing on the motherboard to support MXM v 2.1A graphics modules. If power up sequencing is required, each MXM v 2.1A graphics module is responsible for its own power up sequencing.

Additional Function Support

In order to facilitate additional functions implemented with GPIOs not supported in this specification, such as Japan-D connector or multiplexing TV out to separate connectors for component-out and s-video, the motherboard is required to place a serial link GPIO expander that connects to **DDCC_CLK** and **DDCC_DAT.** An address of 0x4C allows the motherboard designer to utilize GPIO and ROM combination devices to reduce overall implementation costs. The specific function of each GPIO shall be stored in the MXM System Information. The MXM System Information is found in the *MXM version 2.1 Software Specification*, (SP-03494-001). The hardware definition of the functions is defined in Table 18.

Table 18. External GPIO Functions

GPIO Function	Input/Output Type	Active Level	Default Output State	Description
LCD self test	Output	High	Low	
LCD lamp status	Input	High		
DDC select	Output	High	Low	Enables either DDCA or DDCB to a particular output connector. To create a multiplexer, one DDC select is needed for each connector and the selects are mutually exclusive by software control
Japan-D line 1	3-state Output	High		By placing a voltage divider on the output from 5V to GND and set the divider voltage to the mid voltage of Japan-D specification. The output can be High for logic High, Low for Logic Low and Hi-Z for logic Mid
Japan-D line 2	3-state Output	High		
Japan-D line 3	3-state Output	High		
Japan-D spare line 1	3-state Output	High		
Japan-D spare line 2	3-state Output	High		
Japan-D spare line 3	3-state Output	High		
Japan-D plug insertion detect	Input	Low		Pull-up required on system board
HDTV select	Output	High	Low	HDTV/SDTV multiplexer select control
HDTV Alt-detect	Input	Low		HDTV/SDTV alternate display detect. Allows detection of display not currently selected

MXM Cooling Fan

If it is necessary for the MXM graphics module to have its own dedicated fan in the system's chassis, the motherboard is required to provide power and speed control for the fan.

MXM Environmental

Table 19 and Table 20 list the environmental parameters the MXM v 2.1A graphics modules and connectors shall meet.

Table 19. MXM v 2.1A Module Environmental Requirements

	Parameter	Specification
Temperature	Operating	0 °C to 70 °C
Humidity	Steady State	Preconditioning at 40 °C for 24 hours then 40 °C at 90% RH for 96 hours.
Vibration	Operating – Sinusoidal	0.25 G Zero to Peak, 10 to 500 Hz, 0.25 oct/min. Minimum of one sweep/axis (X, Y and Z) from 10 to 500 to 10 Hz.
	Operating – Random	0.002 G^2/Hz, 10 to 500 Hz, nominal of 1.0 Grms. Minimum test duration of 15 min/axis (X, Y and Z)
	Non-operating – Sinusoidal	0.75 G Zero to Peak, 10 to 500 Hz, 0.5 oct/min. Test duration of one sweep from 10 to 500 to 10 Hz per each axis.
	Non-operating – Random	0.008 G^2/Hz, 10 to 500 Hz, nominal of 2.0 Grms. Minimum test duration of 1hour/axis (X, Y and Z)
Shock	Operating – Half Sine Wave	40 G, 2 ms duration, one shock per each axis, total of 3 (X, Y and Z)
	Non-operating – Half Sine Wave	140 G, 2 ms duration, one shock per each axis, total of 6 (X1, X2, Y1, Y2, Z1 and Z2)
	Non-operating – Half Swine Wave	140 G, 2 ms duration, 20 G, 1.8 ms duration, 500 G, 1.3 ms duration, 1300 G, 0.78 ms duration, one shock per drop.
Altitude	Operating	0 to 10,000 feet, 14.7 to 10.10 psia. Altitude change rate 2000 ft per minute.
	Non-operating	0 to 30,000 feet, 14.7 to 4.36 psia. Altitude change rate 2000 ft per minute.

Table 20. MXM Connector Environmental Requirements

Parameter	Specification
Operating Temperature	0 °C to 85 °C
Environmental Test Methodology	EIA-364-1000.01 - Test Group 1, 2, 3 and 4 Use temperature life (preconditioning) of 92 Hours at 105 °C for all temperature life tests.
Useful Field Life	5 years
Flammability	Meet or exceed UL-94V-A flammability requirements.
ROHS	ROHS compliant
Solderability Process Temperature	260 °C for 10 seconds and 245 °C for 30 seconds.

For environmental test purposes only, the module edge-fingers shall have a minimum plating thickness of 30 microinches of gold over 50 microinches of nickel.

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MXM GRAPHICS MODULE