PORTATILE PER ACUBE ACB_0001_0

Version Control

Version	Date	Modifications
V0.1	2018/12	First release of Schematics

PROTO

PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: PAGE LISTING		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 1 of 41	REV. 0	Format B

SYSTEM BLOCK DIAGRAM

PROTO

Power Progress Community	Project **ACB_0001_0**			
Creation Date Wednesday, July 10, 2019	Last modify date	Page title BLOCK DIAGRAM		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 2 of 41	REV. 0	Format A3

T2080 DDR3L MEMORY INTERFACE

U1I

DDR1 (G1VDD)

T2080

TP1 TP4 TP5 TP6 TP7 TP2 TP8 TP3

DDR_ECC0	N25	D1_MECC0
DDR_ECC1	N23	D1_MECC1
DDR_ECC2	N26	D1_MECC2
DDR_ECC3	N27	D1_MECC3
DDR_ECC4	R27	D1_MECC4
DDR_ECC5	R26	D1_MECC5
DDR_ECC6	R23	D1_MECC6
DDR_ECC7	P24	D1_MECC7

1V35 R1 4.7K

	E30	D1_MAPAR_ERR_B
	AA30	D1_MAPAR_OUT

DDR_MDM[0..8]

DDR_MDM0	A25	D1_MDM0
DDR_MDM1	E27	D1_MDM1
DDR_MDM2	G26	D1_MDM2
DDR_MDM3	K25	D1_MDM3
DDR_MDM4	T28	D1_MDM4
DDR_MDM5	W25	D1_MDM5
DDR_MDM6	AA26	D1_MDM6
DDR_MDM7	AJ27	D1_MDM7
DDR_MDM8	P25	D1_MDM8

DDR_MDQS0_P	A26	D1_MDQS0
DDR_MDQS1_P	F28	D1_MDQS1
DDR_MDQS2_P	G27	D1_MDQS2
DDR_MDQS3_P	L26	D1_MDQS3
DDR_MDQS4_P	V28	D1_MDQS4
DDR_MDQS5_P	W27	D1_MDQS5
DDR_MDQS6_P	AB25	D1_MDQS6
DDR_MDQS7_P	AH26	D1_MDQS7
DDR_MDQS8_P	P27	D1_MDQS8
DDR_MDQS0_N	B25	D1_MDQS0_B
DDR_MDQS1_N	F27	D1_MDQS1_B
DDR_MDQS2_N	H27	D1_MDQS2_B
DDR_MDQS3_N	L25	D1_MDQS3_B
DDR_MDQS4_N	U27	D1_MDQS4_B
DDR_MDQS5_N	W26	D1_MDQS5_B
DDR_MDQS6_N	AC26	D1_MDQS6_B
DDR_MDQS7_N	AH27	D1_MDQS7_B
DDR_MDQS8_N	P28	D1_MDQS8_B

DDR_MBA[0..2]

DDR_MBA0	AC30	D1_MBA0
DDR_MBA1	AA29	D1_MBA1
DDR_MBA2	D28	D1_MBA2

DDR_MA[0..15]

DDR_MA0	Y30	D1_MA00
DDR_MA1	W29	D1_MA01
DDR_MA2	M30	D1_MA02
DDR_MA3	L30	D1_MA03
DDR_MA4	L29	D1_MA04
DDR_MA5	J30	D1_MA05
DDR_MA6	J29	D1_MA06
DDR_MA7	G29	D1_MA07
DDR_MA8	H30	D1_MA08
DDR_MA9	F30	D1_MA09
DDR_MA10	AB30	D1_MA10
DDR_MA11	G30	D1_MA11
DDR_MA12	E29	D1_MA12
DDR_MA13	AG29	D1_MA13
DDR_MA14	D30	D1_MA14
DDR_MA15	C29	D1_MA15

DDR_MCS0_N	AD30	D1_MCS0_B
DDR_MCS1_N	AH30	D1_MCS1_B
	AK28	D1_MCS2_B
	AJ28	D1_MCS3_B
DDR_MCKE0	B29	D1_MCKE0
DDR_MCKE1	B28	D1_MCKE1
	C30	D1_MCKE2
	A28	D1_MCKE3
DDR_MCK0_P	P30	D1_MCK0
DDR_MCK0_N	N30	D1_MCK0_B
DDR_MCK1_P	R30	D1_MCK1
DDR_MCK1_N	R29	D1_MCK1_B
	U29	D1_MCK2
	U30	D1_MCK2_B
	W30	D1_MCK3
	V30	D1_MCK3_B

DDR_DQ[0..63]

B24	DDR_DQ0	D1_MDQ00
A24	DDR_DQ1	D1_MDQ01
C25	DDR_DQ2	D1_MDQ02
D24	DDR_DQ3	D1_MDQ03
D25	DDR_DQ4	D1_MDQ04
C26	DDR_DQ5	D1_MDQ05
B27	DDR_DQ6	D1_MDQ06
C27	DDR_DQ7	D1_MDQ07
H23	DDR_DQ8	D1_MDQ08
G23	DDR_DQ9	D1_MDQ09
F24	DDR_DQ10	D1_MDQ10
F25	DDR_DQ11	D1_MDQ11
E25	DDR_DQ12	D1_MDQ12
E26	DDR_DQ13	D1_MDQ13
D27	DDR_DQ14	D1_MDQ14
G25	DDR_DQ15	D1_MDQ15
J23	DDR_DQ16	D1_MDQ16
H24	DDR_DQ17	D1_MDQ17
H25	DDR_DQ18	D1_MDQ18
J26	DDR_DQ19	D1_MDQ19
J25	DDR_DQ20	D1_MDQ20
J27	DDR_DQ21	D1_MDQ21
H28	DDR_DQ22	D1_MDQ22
K28	DDR_DQ23	D1_MDQ23
L23	DDR_DQ24	D1_MDQ24
M25	DDR_DQ25	D1_MDQ25
K24	DDR_DQ26	D1_MDQ26
K27	DDR_DQ27	D1_MDQ27
M24	DDR_DQ28	D1_MDQ28
L27	DDR_DQ29	D1_MDQ29
M27	DDR_DQ30	D1_MDQ30
M28	DDR_DQ31	D1_MDQ31
T27	DDR_DQ32	D1_MDQ32
V27	DDR_DQ33	D1_MDQ33
U25	DDR_DQ34	D1_MDQ34
U26	DDR_DQ35	D1_MDQ35
R25	DDR_DQ36	D1_MDQ36
T25	DDR_DQ37	D1_MDQ37
T24	DDR_DQ38	D1_MDQ38
U23	DDR_DQ39	D1_MDQ39
Y28	DDR_DQ40	D1_MDQ40
Y27	DDR_DQ41	D1_MDQ41
Y25	DDR_DQ42	D1_MDQ42
Y24	DDR_DQ43	D1_MDQ43
V25	DDR_DQ44	D1_MDQ44
Y23	DDR_DQ45	D1_MDQ45
V24	DDR_DQ46	D1_MDQ46
W23	DDR_DQ47	D1_MDQ47
AA27	DDR_DQ48	D1_MDQ48
AB28	DDR_DQ49	D1_MDQ49
AB27	DDR_DQ50	D1_MDQ50
AC27	DDR_DQ51	D1_MDQ51
AB24	DDR_DQ52	D1_MDQ52
AB23	DDR_DQ53	D1_MDQ53
AA23	DDR_DQ54	D1_MDQ54
AA25	DDR_DQ55	D1_MDQ55
AD28	DDR_DQ56	D1_MDQ56
AD27	DDR_DQ57	D1_MDQ57
AE27	DDR_DQ58	D1_MDQ58
AC25	DDR_DQ59	D1_MDQ59
AF28	DDR_DQ60	D1_MDQ60
AF27	DDR_DQ61	D1_MDQ61
AG27	DDR_DQ62	D1_MDQ62
AE26	DDR_DQ63	D1_MDQ63

AG30	DDR_MODT0	D1_MODT0
AH29	DDR_MODT1	D1_MODT1
AF30		D1_MODT2
AJ29		D1_MODT3

1V35 — R3 187 1% — N29 D1_MDIC1
R4 187 1% — K30 D1_MDIC0

T2080 REV 1.0: 187 ohm

AE29	DDR_MCRAS_N	D1_MCAS_B
AC29	DDR_MRAS_N	D1_MRAS_B
AE30	DDR_MWE_N	D1_MWE_B

OVDD D1_DDRCLK E23 — DDR_REFCLK 32

C23 D1_TPA

G1VDD/2 F21 D1_MVREF — MVREF — C9 0.1uF

TP9 TP10 TP11

DDR_MDM8
DDR_MDQS8_P
DDR_MDQS8_N

13 DDR_RST_N

1V35 R2 1K

SPD ADDR = 0x51

3V3 197 SA0 201 SA1

7,12,33,34 I2C1_SCL 202 SCL
7,12,33,34 I2C1_SDA 200 SDA

DDR_MODT0 116 ODT0
DDR_MODT1 120 ODT1

DDR_MCKE0 73 CKE0
DDR_MCKE1 74 CKE1

DDR_MCK0_P 101 CK0P
DDR_MCK0_N 103 CK0N

DDR_MCK1_P 102 CK1P
DDR_MCK1_N 104 CK1N

DDR_MCS0_N 114 S0_N
DDR_MCS1_N 121 S1_N

DDR_MCRAS_N 115 CAS_N
DDR_MRAS_N 110 RAS_N
30 RST_N
DDR_MWE_N 113 WE_N

1V35

C10 C11 C12 C13 C14 C15 C16 — 0.1uF each

C17 C18 C19 C20 C21 C22 C23 — 0.1uF each

1.35V DDR3L SDRAM SODIMM

4GB (x64, DDR3L)

J3F1A

CONN204_DDR3_SODIMM

1G6 For DDR3L-1600

M1

MT8KTF51264HZ-1G6

DDR_MA[0..15]

DDR_MA15	78	A<15>/BA3
DDR_MA14	80	A<14>
DDR_MA13	119	A<13>
DDR_MA12	83	A<12>/BC_N
DDR_MA11	84	A<11>
DDR_MA10	107	A<10>/AP
DDR_MA9	85	A<9>
DDR_MA8	89	A<8>/A7
DDR_MA7	86	A<7>/A8
DDR_MA6	90	A<6>/A5
DDR_MA5	91	A<5>/A6
DDR_MA4	92	A<4>/A3
DDR_MA3	95	A<3>/A4
DDR_MA2	96	A<2>
DDR_MA1	97	A<1>
DDR_MA0	98	A<0>

DDR_MBA[0..2]

DDR_MBA0	109	BA0/BA1
DDR_MBA1	108	BA1/BA0
DDR_MBA2	79	BA2

DDR_MDM[0..8]

DDR_MDM0	11	DM0
DDR_MDM1	28	DM1
DDR_MDM2	46	DM2
DDR_MDM3	63	DM3
DDR_MDM4	136	DM4
DDR_MDM5	153	DM5
DDR_MDM6	170	DM6
DDR_MDM7	187	DM7

DDR_MDQS0_P	12	DQS0P
DDR_MDQS0_N	10	DQS0N
DDR_MDQS1_P	29	DQS1P
DDR_MDQS1_N	27	DQS1N
DDR_MDQS2_P	47	DQS2P
DDR_MDQS2_N	45	DQS2N
DDR_MDQS3_P	64	DQS3P
DDR_MDQS3_N	62	DQS3N
DDR_MDQS4_P	137	DQS4P
DDR_MDQS4_N	135	DQS4N
DDR_MDQS5_P	154	DQS5P
DDR_MDQS5_N	152	DQS5N
DDR_MDQS6_P	171	DQS6P
DDR_MDQS6_N	169	DQS6N
DDR_MDQS7_P	188	DQS7P
DDR_MDQS7_N	186	DQS7N

DDR_DQ[0..63]

DQ<63>	194	DDR_DQ63
DQ<62>	192	DDR_DQ62
DQ<61>	182	DDR_DQ61
DQ<60>	180	DDR_DQ60
DQ<59>	193	DDR_DQ59
DQ<58>	191	DDR_DQ58
DQ<57>	183	DDR_DQ57
DQ<56>	181	DDR_DQ56
DQ<55>	176	DDR_DQ55
DQ<54>	174	DDR_DQ54
DQ<53>	166	DDR_DQ53
DQ<52>	164	DDR_DQ52
DQ<51>	177	DDR_DQ51
DQ<50>	175	DDR_DQ50
DQ<49>	165	DDR_DQ49
DQ<48>	163	DDR_DQ48
DQ<47>	160	DDR_DQ47
DQ<46>	158	DDR_DQ46
DQ<45>	148	DDR_DQ45
DQ<44>	146	DDR_DQ44
DQ<43>	159	DDR_DQ43
DQ<42>	157	DDR_DQ42
DQ<41>	149	DDR_DQ41
DQ<40>	147	DDR_DQ40
DQ<39>	142	DDR_DQ39
DQ<38>	140	DDR_DQ38
DQ<37>	132	DDR_DQ37
DQ<36>	130	DDR_DQ36
DQ<35>	143	DDR_DQ35
DQ<34>	141	DDR_DQ34
DQ<33>	131	DDR_DQ33
DQ<32>	129	DDR_DQ32
DQ<31>	70	DDR_DQ31
DQ<30>	68	DDR_DQ30
DQ<29>	58	DDR_DQ29
DQ<28>	56	DDR_DQ28
DQ<27>	69	DDR_DQ27
DQ<26>	67	DDR_DQ26
DQ<25>	59	DDR_DQ25
DQ<24>	57	DDR_DQ24
DQ<23>	52	DDR_DQ23
DQ<22>	50	DDR_DQ22
DQ<21>	42	DDR_DQ21
DQ<20>	40	DDR_DQ20
DQ<19>	53	DDR_DQ19
DQ<18>	51	DDR_DQ18
DQ<17>	41	DDR_DQ17
DQ<16>	39	DDR_DQ16
DQ<15>	36	DDR_DQ15
DQ<14>	34	DDR_DQ14
DQ<13>	24	DDR_DQ13
DQ<12>	22	DDR_DQ12
DQ<11>	35	DDR_DQ11
DQ<10>	33	DDR_DQ10
DQ<9>	23	DDR_DQ9
DQ<8>	21	DDR_DQ8
DQ<7>	18	DDR_DQ7
DQ<6>	16	DDR_DQ6
DQ<5>	6	DDR_DQ5
DQ<4>	4	DDR_DQ4
DQ<3>	17	DDR_DQ3
DQ<2>	15	DDR_DQ2
DQ<1>	7	DDR_DQ1
DQ<0>	5	DDR_DQ0

EVENT_N 198

TEST 125

1 OF 2

CONN
E85705-003

J3F1B

CONN204_DDR3_SODIMM

1V35

75	VDD	GND 3
81	VDD	GND 9
87	VDD	GND 13
93	VDD	GND 19
99	VDD	GND 25
76	VDD	GND 31
82	VDD	GND 37
88	VDD	GND 43
94	VDD	GND 49
100	VDD	GND 2
105	VDD	GND 8
111	VDD	GND 14
117	VDD	GND 20
123	VDD	GND 26
106	VDD	GND 32
112	VDD	GND 38
118	VDD	GND 44
124	VDD	GND 48
		GND 55
		GND 61
		GND 65
		GND 71
		GND 54
199	VDDSPD	GND 60
		GND 66
1	VREF/DQ	GND 72
		GND 127
126	VREFCA	GND 133
		GND 139
		GND 145
		GND 151
		GND 155
203	VTT	GND 128
204	VTT	GND 134
		GND 138
		GND 144
		GND 150
		GND 156
		GND 161
77	NC	GND 167
122	NC	GND 173
		GND 179
		GND 185
		GND 189
		GND 195
		GND 162
		GND 168
		GND 172
		GND 178
		GND 184
		GND 190
		GND 196

2 OF 2

3V3 — C1 0.1uF — MVREF

VTT

CONN
E85705-003

1V35: C2 22uF, C3 22uF
VTT: C4 22uF, C5 0.1uF, C6 0.1uF
MVREF: C7 0.1uF, C8 0.1uF

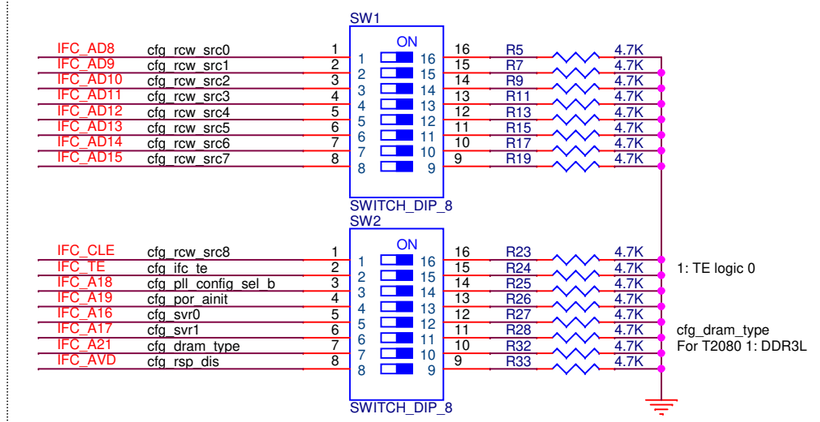
PROTO

PPC Power Progress Community	Project ACB_0001_0		
Creation Date: Saturday, April 20, 2013	Last modify date: Wednesday, July 10, 2019	Page title: DDR3	
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>	
PCB Code	BOM file	Sheet 3 of 41	REV. 0 / Format A3

T2080 IFC INTERFACE

T2080 RESET CONFIGURATION

cfg_rcw_src[0:8]
0_0010_0111: NOR FLASH BOOT
0_0100_0000: SD CARD BOOT
0_0100_0101: SPI BOOT
1_0001_1001: NAND FLASH BOOT

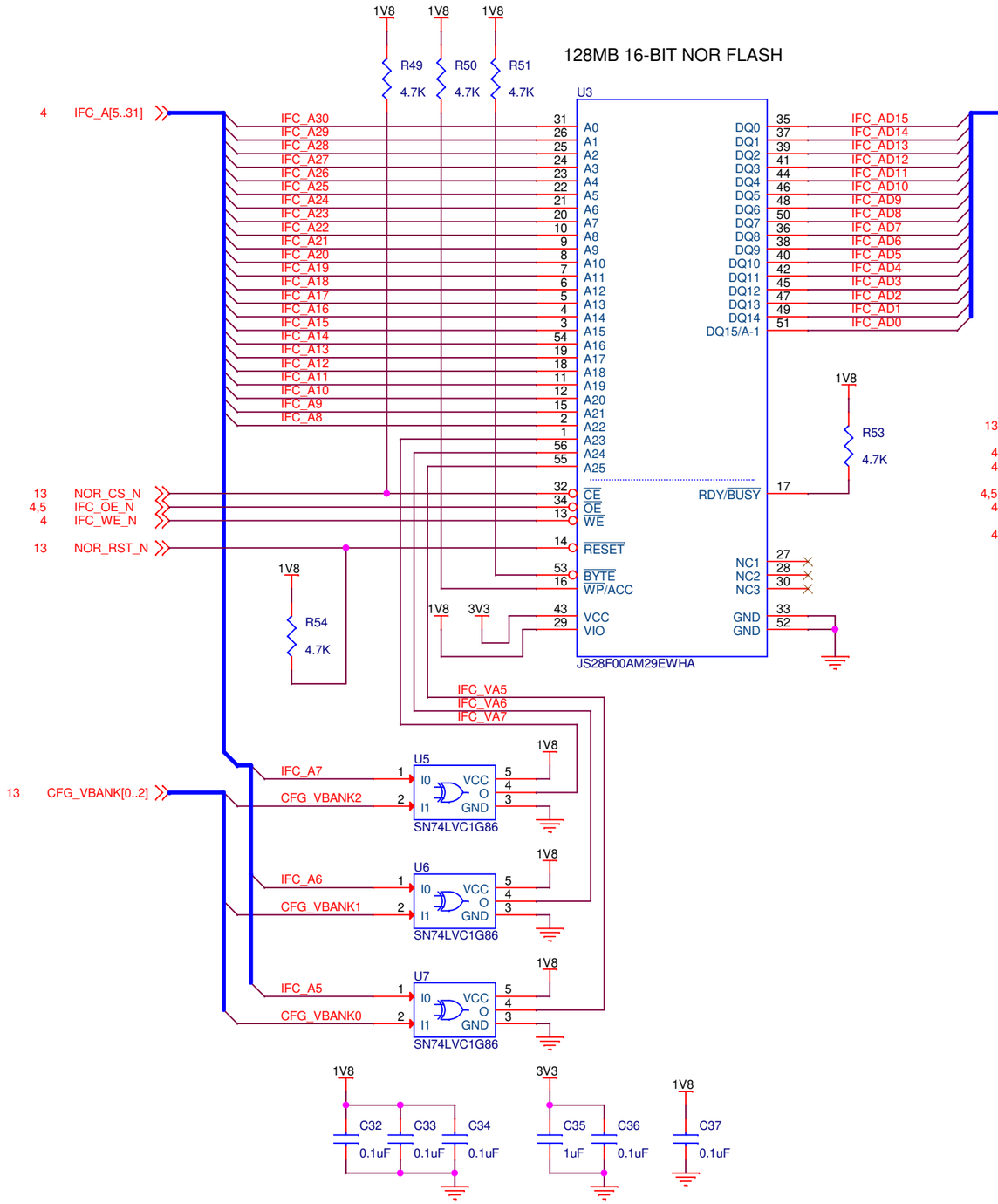


PROTO

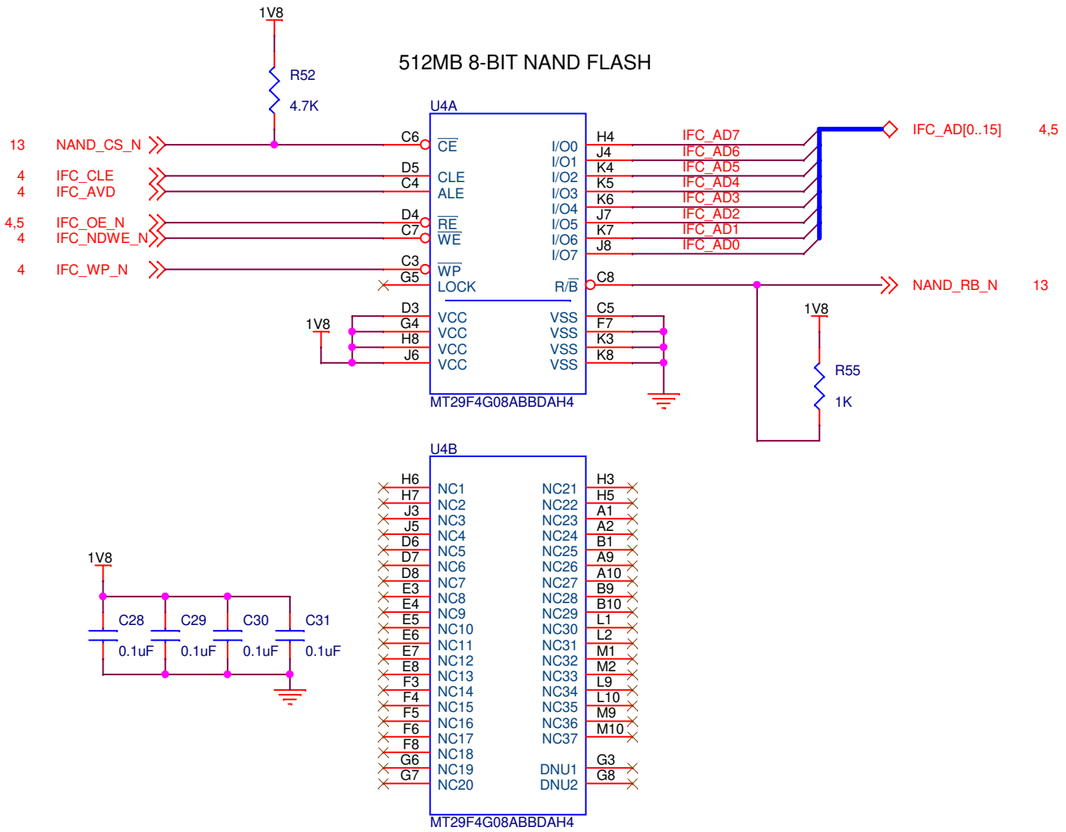
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, July 10, 2019	Last modify date:	Page title: IFC
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 4 of 41 · REV. 0 · Format A3

T2080 NOR and NAND FLASH INTERFACE

128MB 16-BIT NOR FLASH



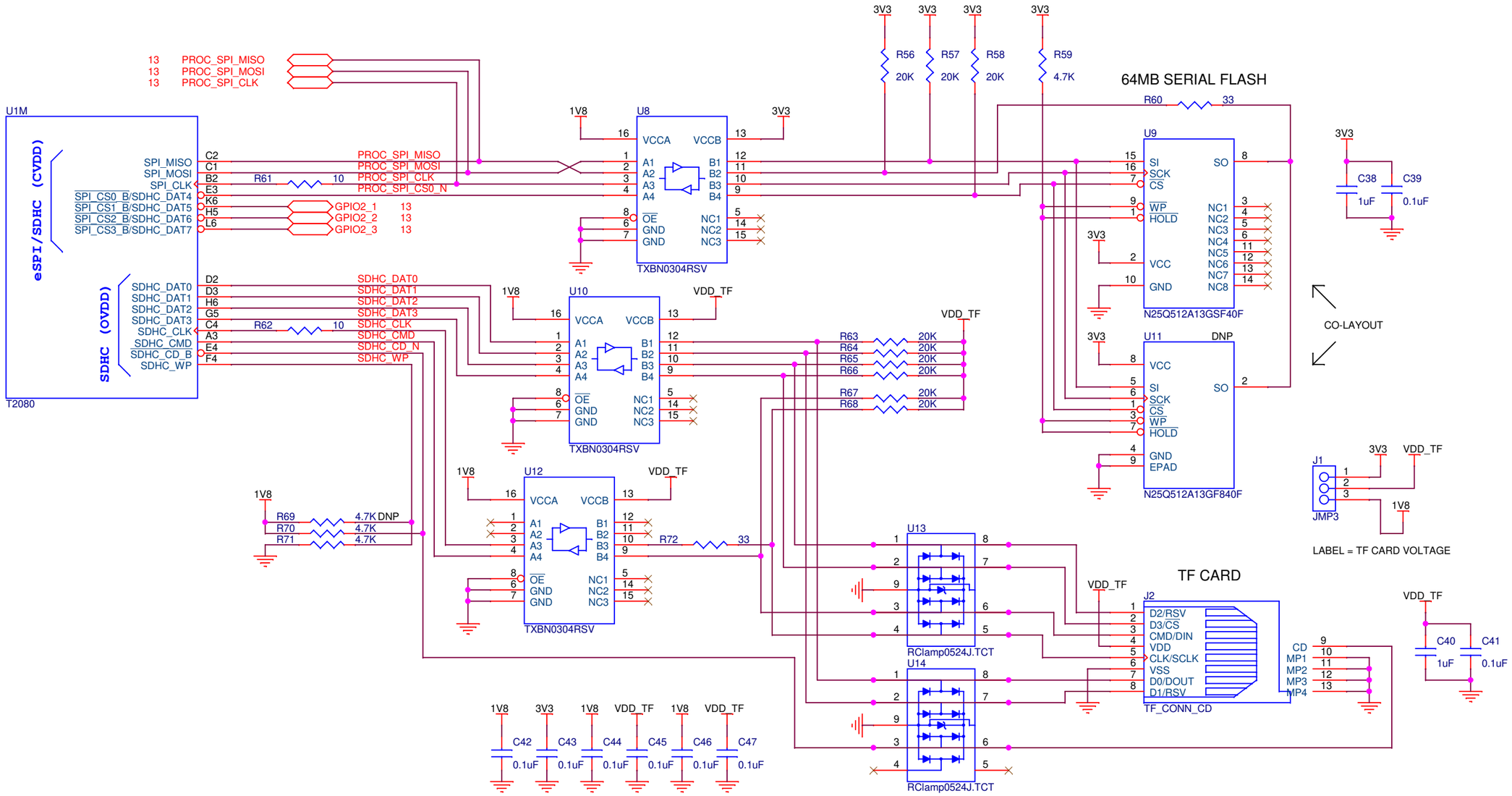
512MB 8-BIT NAND FLASH



PROTO

Power Progress Community	Project ACB_0001_0		
Creation Date: Wednesday, July 10, 2019	Last modify date:	Page title: FLASH	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 5 of 41 / REV. 0	Format A3

T2080 SPI FLASH and SDHC INTERFACE



PROTO

PPC Power Progress Community	Project ACB_0001_0		
Creation Date: Wednesday, July 10, 2019	Last modify date:	Page title: SPI&SDHC	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 6 of 41	REV. 0 / Format A3

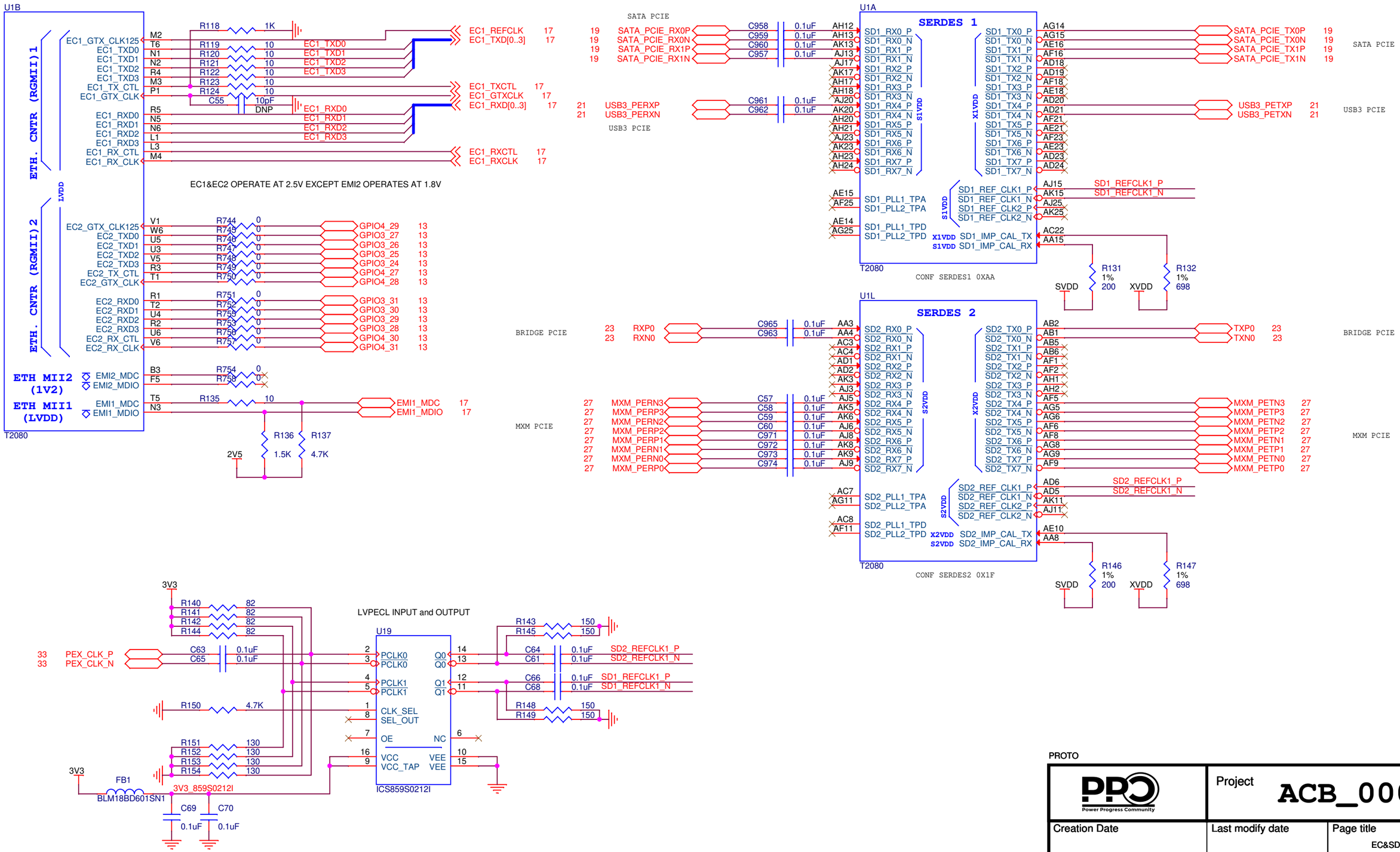
T2080 SYSTEM LOGIC INTERFACE

U1E
CNTR & MISC
T2080
SYS CNTR.
DEBUG
DFT (OVDD)
CLOCK
JTAG
DMA (DVDD)
MPIC
OVDD
LVDD
CVDD
DVDD
VDD_LP
13 GPIO4_6
13 GPIO4_5
13 GPIO4_4
13 PORESET_N
13 HRESET_N
13 RESET_REQ_N
cfg_test_port_mux_sel
PORESET_B
HRESET_B
RESET_REQ_B
ASLEEP
XVDD use 1.35V
cfg_xvdd_sel
EVT0_B
EVT1_B
EVT2_B
EVT3_B
EVT4_B
CKSTP_OUT_B
CLK_OUT
CKSTP_OUT_N
SCAN_MODE_B
TEST_SEL_B
TEST_SEL_B
FOR T2080, PULL-UP
32 SYS_REFCLK
SYSCLK
RTC
TDI
TMS
TCK
TDO
TRST_B
JTAG_TDI
JTAG_TMS
JTAG_TCK
JTAG_TDO
JTAG_TRST_N
DMA1_DREQ0_B
DMA1_DACK0_B
DMA1_DDONE0_B
DMA2_DREQ0_B
DMA2_DACK0_B/EVT_B7
DMA2_DDONE0_B/EVT_B8
IRQ00
IRQ01
IRQ02
IRQ03/SDHC_VS
IRQ04
IRQ05
IRQ06
IRQ07
IRQ08
IRQ09
IRQ10/SDHC_SYNC_IN
IRQ11
IRQ_OUT_B/EVT_B9
TMP_DETECT_B
LP_TMP_DETECT_B
TD1_ANODE
TD1_CATHODE
IRQ00 13
IRQ01 13
IRQ02 13
RTC_INT_N 12
EC1_INT_N 17
EC1_PME_N 17
IRQ08 13
IRQ09 13
LP_TMPDET_N 39
TEMP_DIODE_P 12
TEMP_DIODE_N 12
R73 4.7K
R74 4.7K
R75 4.7K
R76 4.7K
R77 4.7K
R81 4.7K
R82 4.7K
R83 4.7K
R84 4.7K
R85 4.7K
R86 4.7K
R87 4.7K
R88 4.7K
R89 4.7K
R78 4.7K
R90 4.7K
R91 4.7K
R92 4.7K
R93 4.7K
R97 10K
U15 FXLP34P5X
U16 FXLP34P5X
D1 GRN
R94 510
C48 0.1uF
C49 0.1uF
C50 0.1uF
C51 0.1uF
R95 1K
R96 1K
TP12
TP13
U17 TXBN0304RSV
VCCA
VCCB
OE
GND
NC1
NC2
NC3
C52 0.1uF
C53 0.1uF
J3 HTST-108-01-L-DV
COP_TDO
COP_TDI
COP_TCK
COP_TMS
COP_CKSTP_OUT_N
R104 10K
R109 10K
R108 10K
R111 10K
R112 10K
R114 10K
R105 10
R106 10K
R117 0
R870 0
U1D
I2C (DVDD)
IIC1_SCL
IIC1_SDA
IIC2_SCL
IIC2_SDA
IIC3_SCL
IIC3_SDA
IIC4_SCL/EVT_B5
IIC4_SDA/EVT_B6
R113 4.7K
R115 4.7K
R98 4.7K
R99 4.7K
R100 4.7K
R101 4.7K
R110 4.7K
R107 4.7K
U92 PCA9306DCT
U93 PCA9306DCT
U91 PCA9306DCT
U94 PCA9306DCT
VREF1
VREF2
ENABLE
SCL1
SDA1
SCL2
SDA2
GND
C1046 0.1uF
C1048 0.1uF
C1050 0.1uF
C1047 0.1uF
C1049 0.1uF
C1051 0.1uF
C1052 0.1uF
C1053 0.1uF
R734 220K
R735 220K
R738 220K
R741 220K
R102 4.7K
R103 4.7K
R736 4.7K
R737 4.7K
R739 4.7K
R740 4.7K
R742 4.7K
R743 4.7K
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
I2C3_SCL
I2C3_SDA
I2C4_SCL
I2C4_SDA

PROTO

PPC Power Progress Community	Project ACB_0001_0	
Creation Date: Wednesday, July 10, 2019	Last modify date:	Page title: SYS
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 7 of 41 / REV. 0 / Format A3

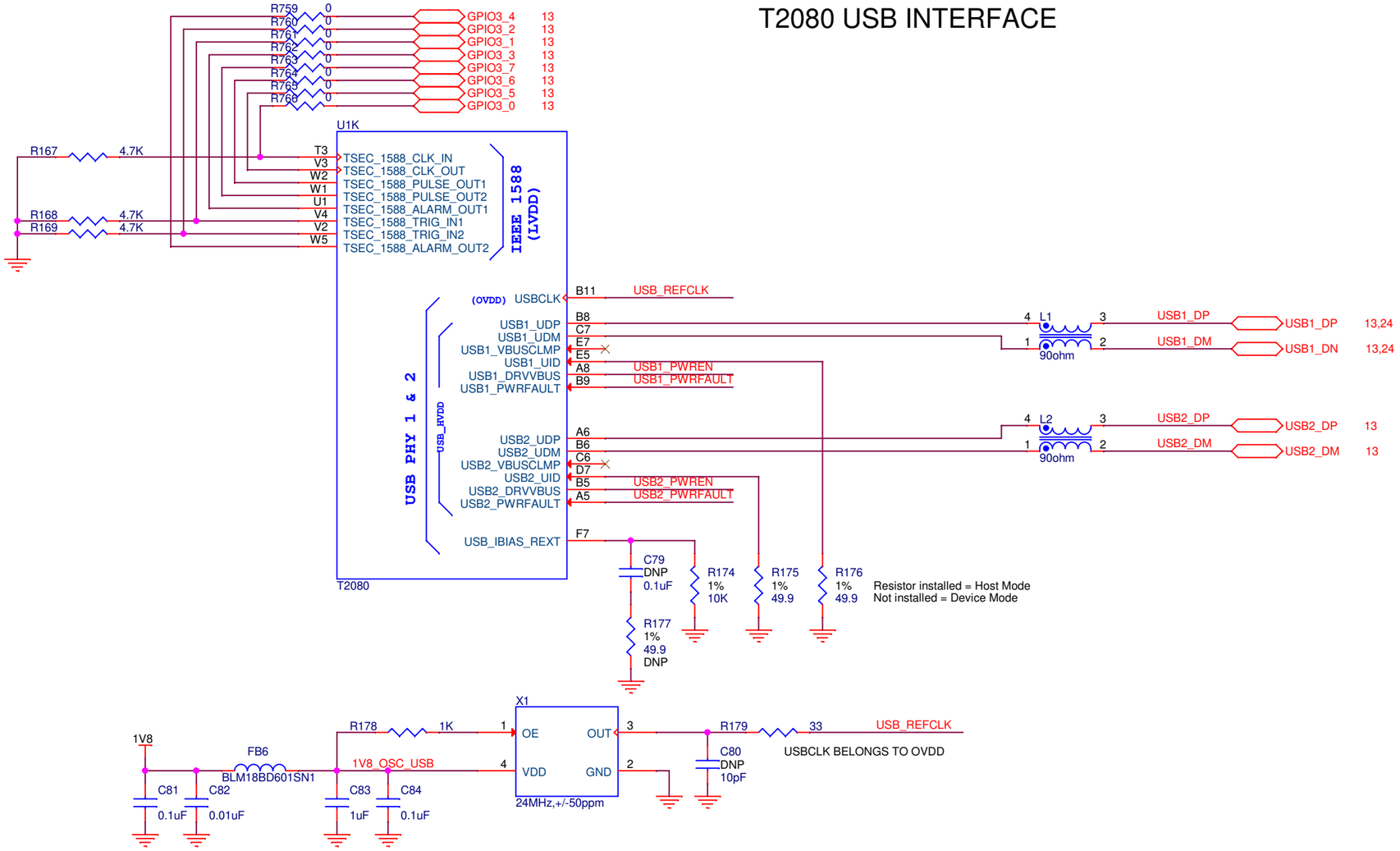
T2080 ETHERNET and SERDES INTERFACE



PROTO

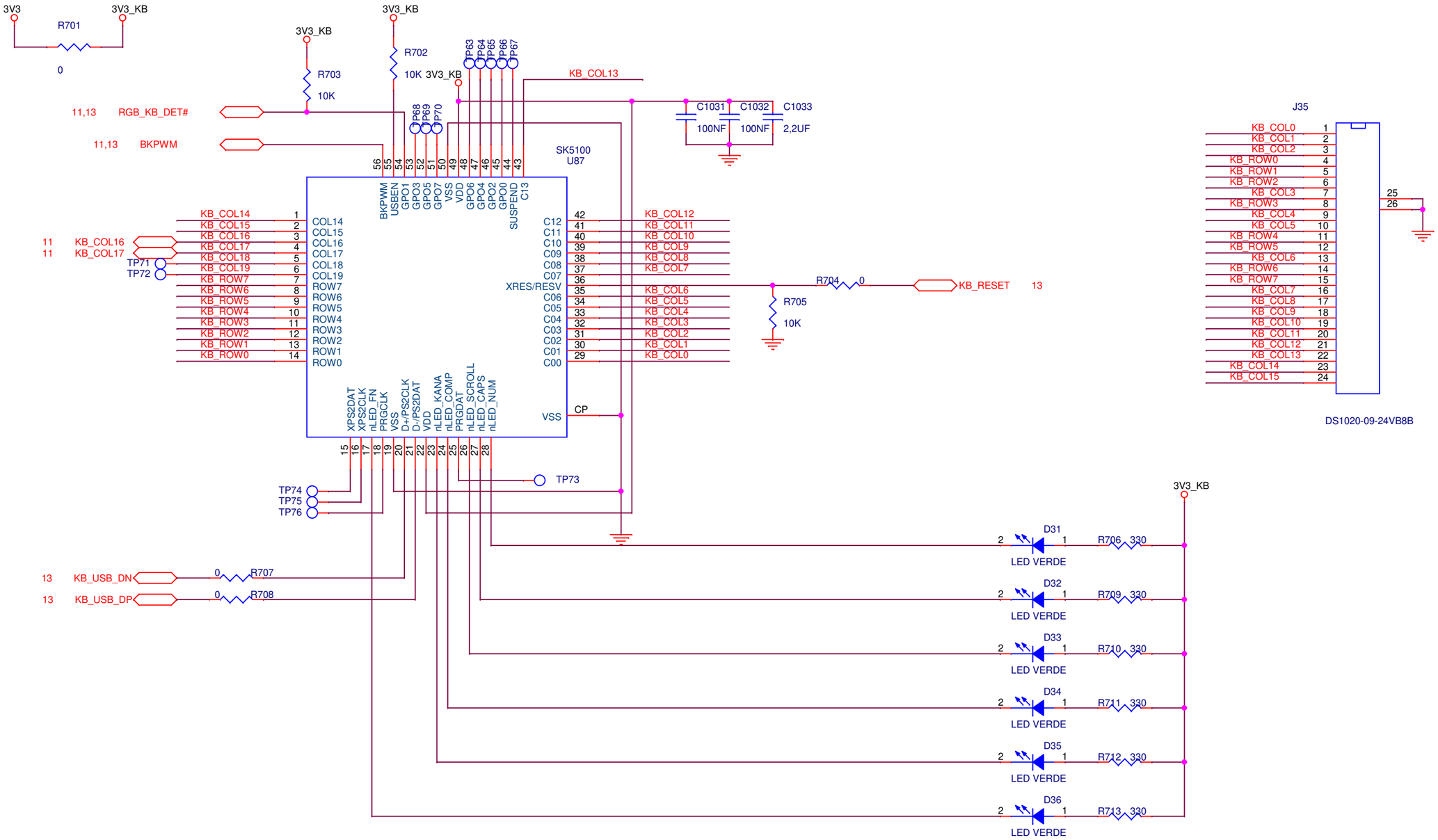
PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date	Last modify date	Page title: EC&SD
Designed by: Wednesday, July 10, 2019	Controlled by:	approved by:
PCB Code	BOM file	Sheet 8 of 41 / REV. 0 / Format A3

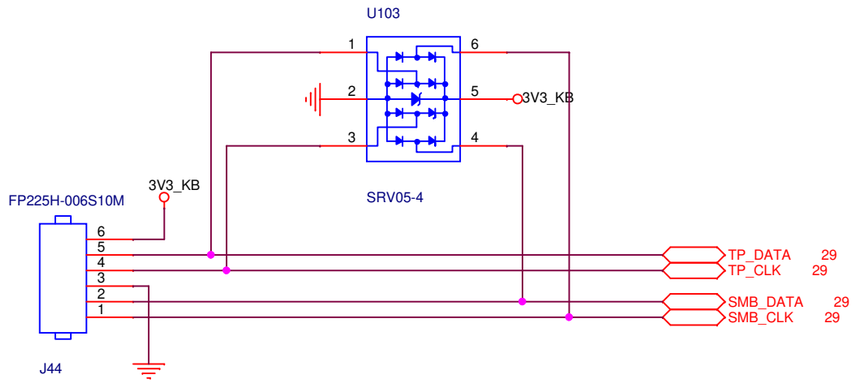
T2080 USB INTERFACE



PROTO

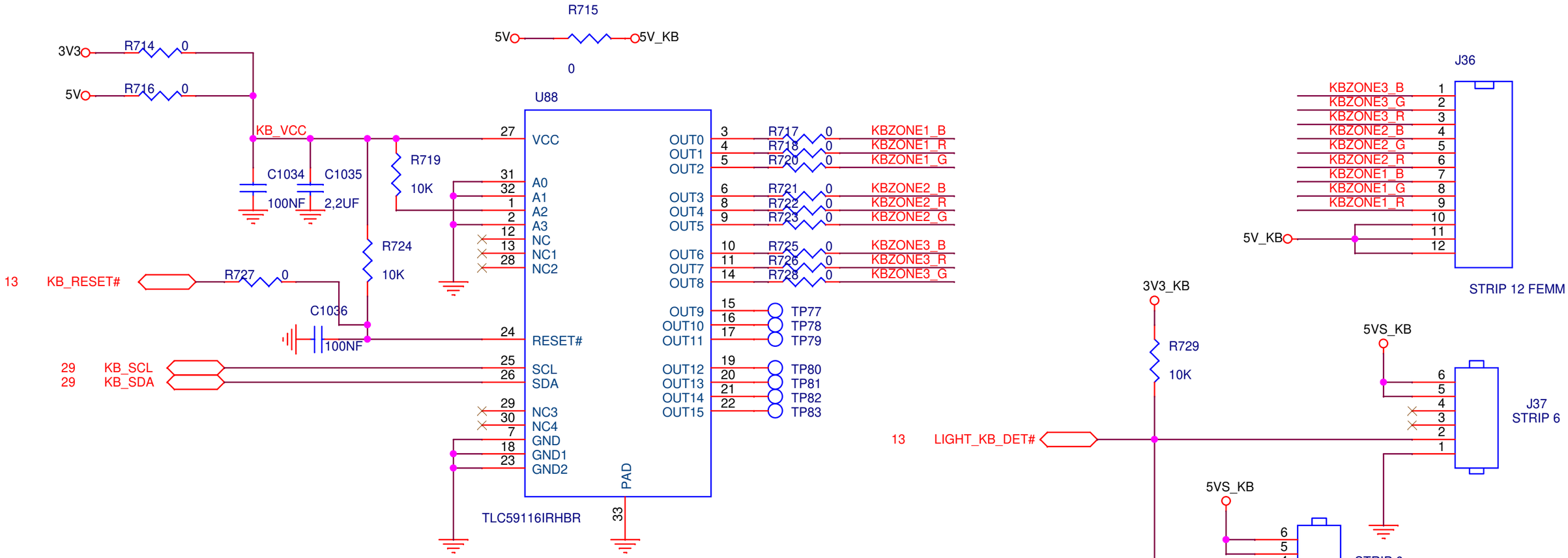
Power Progress Community	Project ACB_0001_0		
Creation Date	Last modify date	Page title: USB	
Designed by: Wednesday, July 10, 2019	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 9 of 41 / REV. 0	Format A3





PROTO

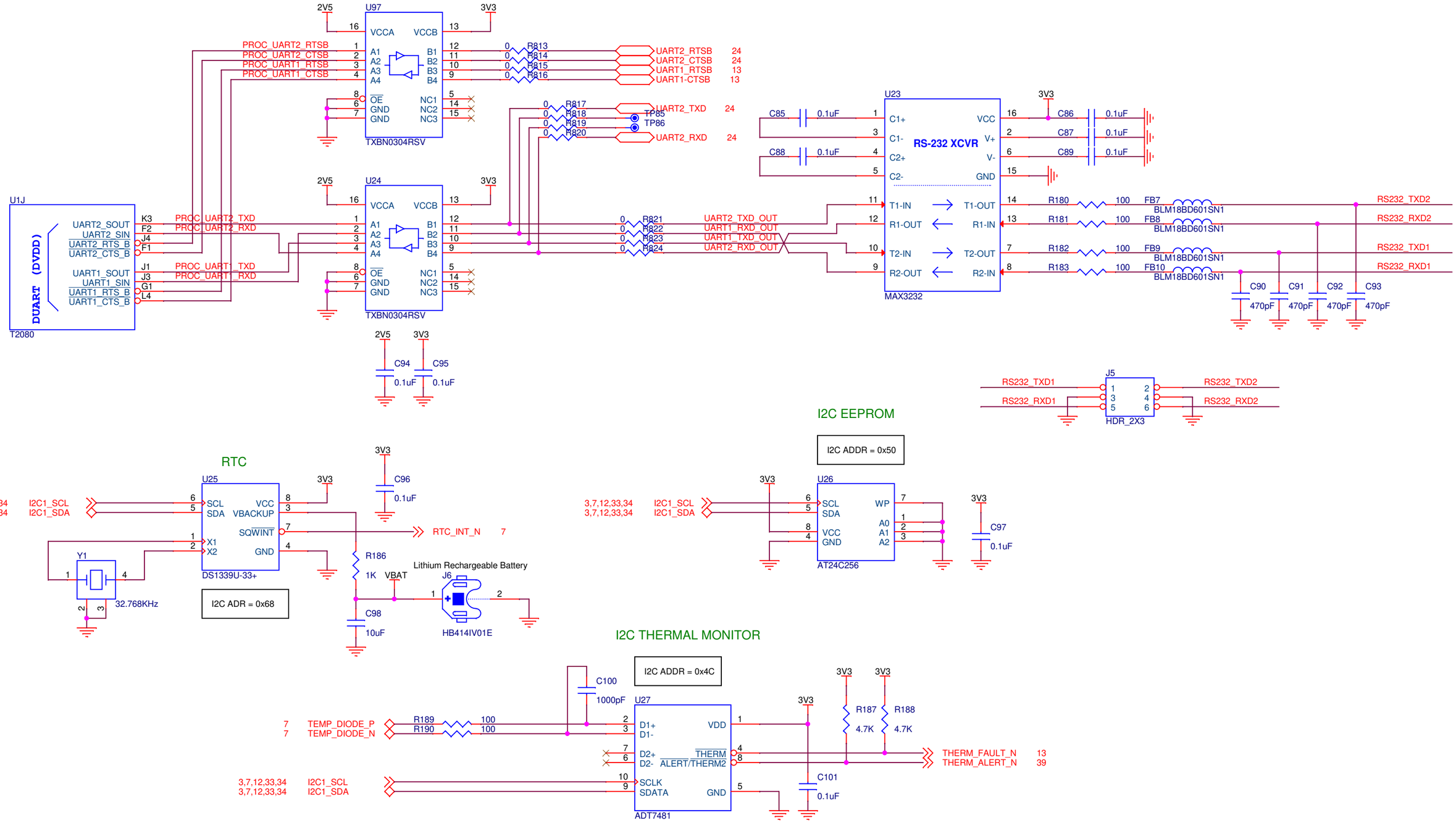
Project ACB_0001_0				
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: KEYBOARD		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 10 of 41	REV. 0	Format A3



PROTO

PPC Power Progress Community	Project **ACB_0001_0**			
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: KB_LED		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 11 of 41	REV. 0	Format A4

T2080 DUART and I2C DEVICE INTERFACE



I2C EEPROM

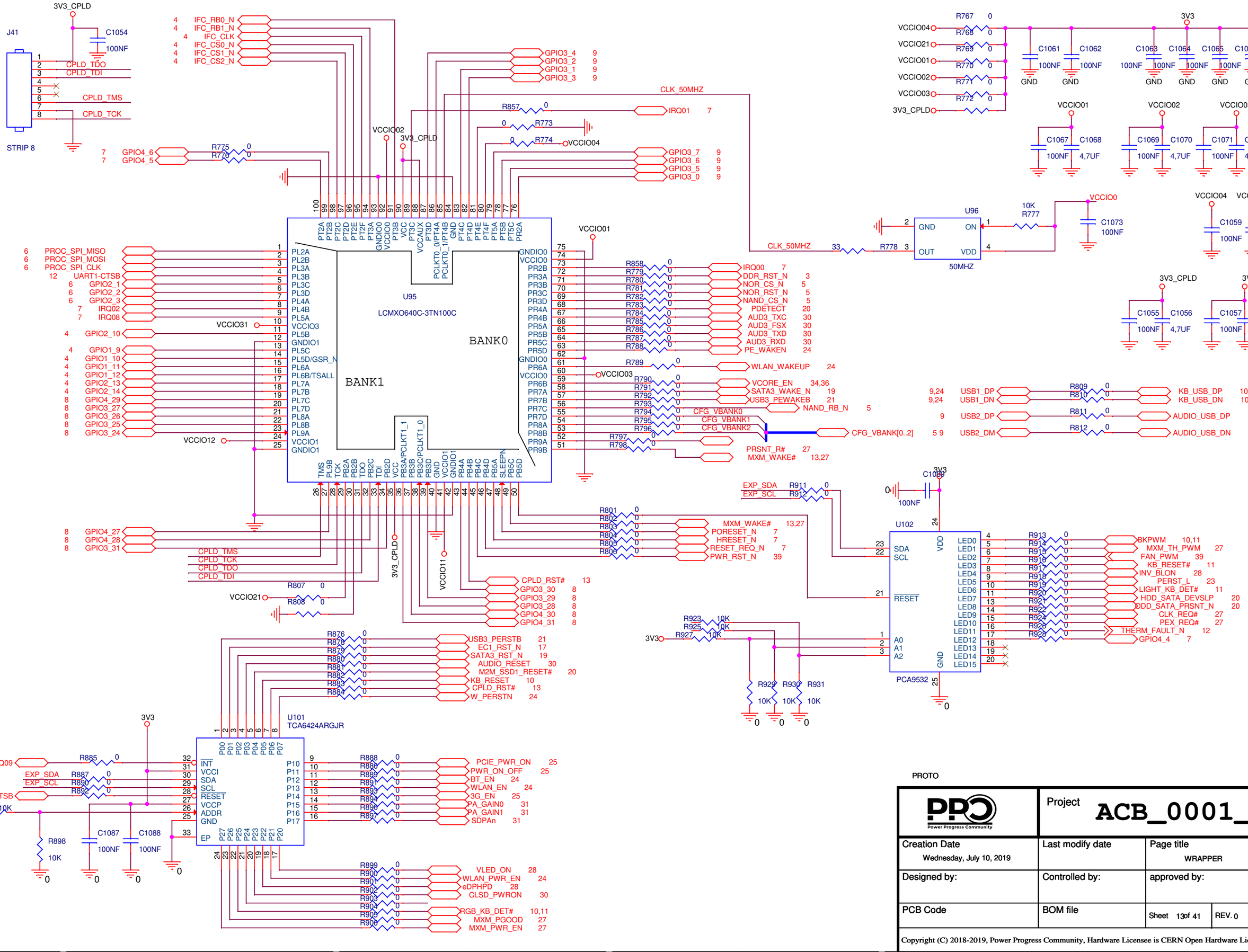
I2C ADDR = 0x50

RTC

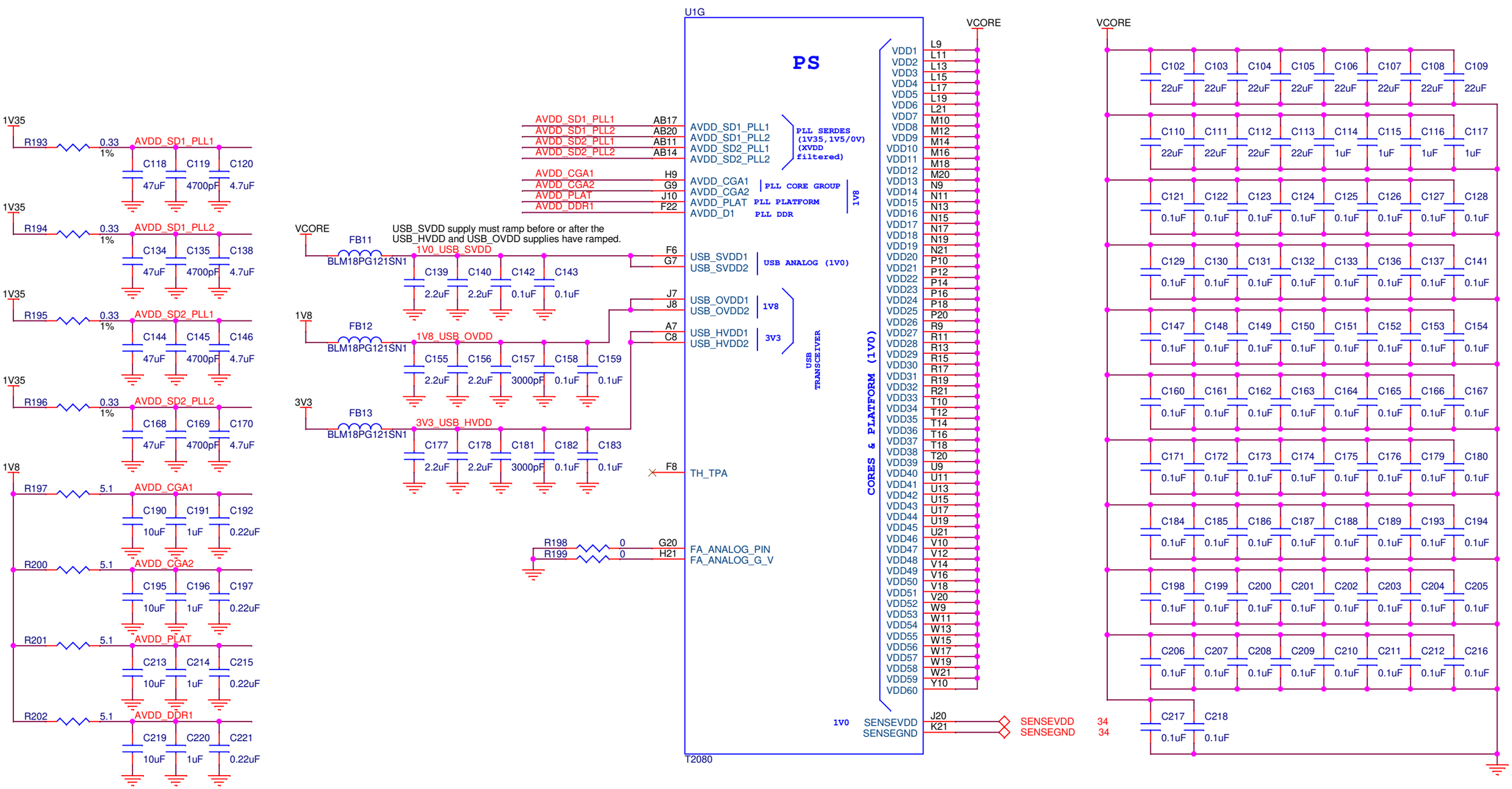
I2C THERMAL MONITOR

PROTO

Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: UART&I2C
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 12of 41 / REV. 0 / Format A3


J41
STRIP 8
CPLD_TDO
CPLD_TDI
CPLD_TMS
CPLD_TCK
C1054
100NF
U95
LCMXO640C-3TN100C
BANK0
BANK1
VCCIO01
VCCIO02
VCCIO31
VCCIO12
3V3_CPLD
CLK_50MHZ
U96
50MHZ
U101
TCA6424ARGJR
U102
PCA9532
3V3
PROTO
Project
ACB_0001_0
Power Progress Community
Creation Date
Wednesday, July 10, 2019
Last modify date
Page title
WRAPPER
Designed by:
Controlled by:
approved by:
PCB Code
BOM file
Sheet 13of 41
REV. 0
Format A3
Copyright (C) 2018-2019, Power Progress Community, Hardware Licensee is CERN Open Hardware Licence v1.2

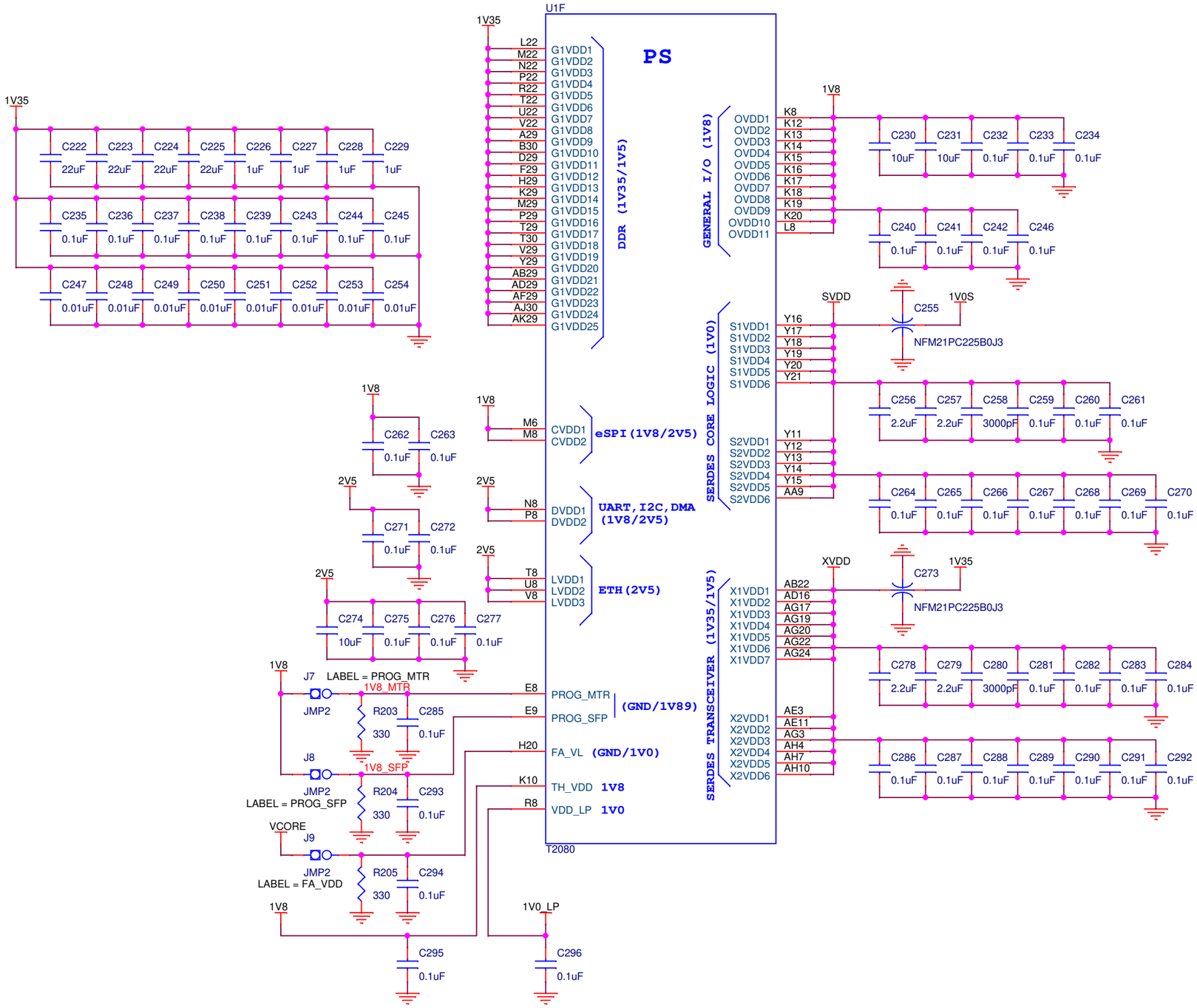
T2080 POWER SUPPLY



PROTO

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, July 10, 2019	Last modify date:	Page title: PROC PWR1
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 14 of 41 / REV. 0 / Format A3

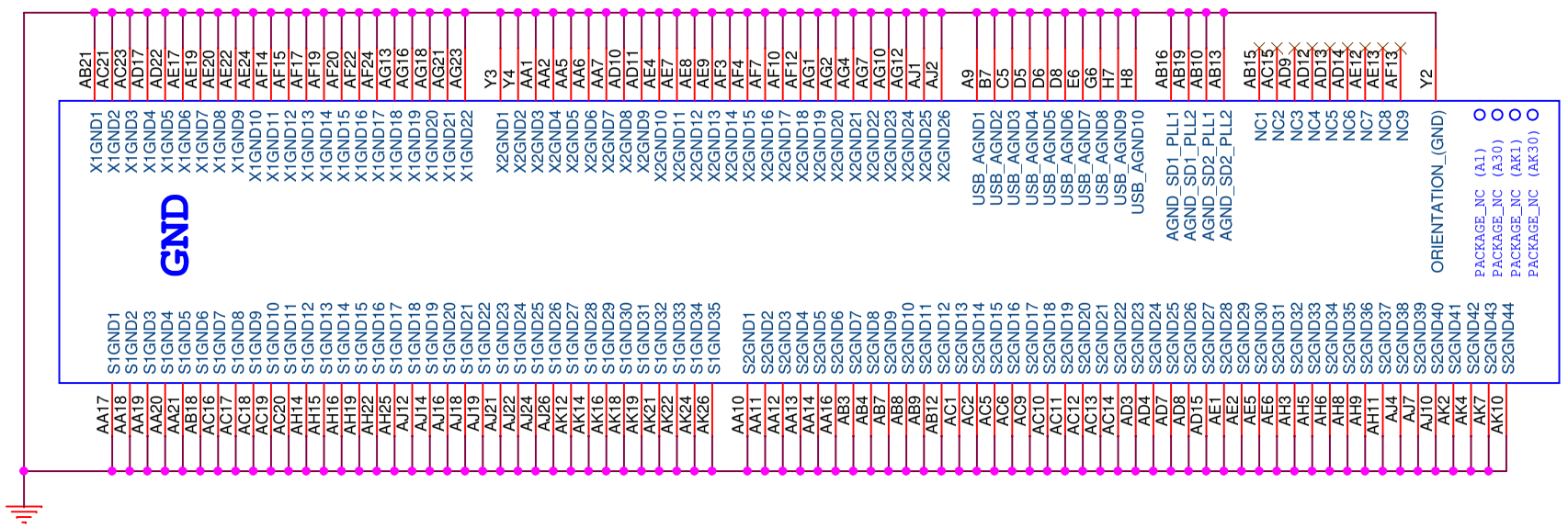
T2080 POWER SUPPLY (cont.)

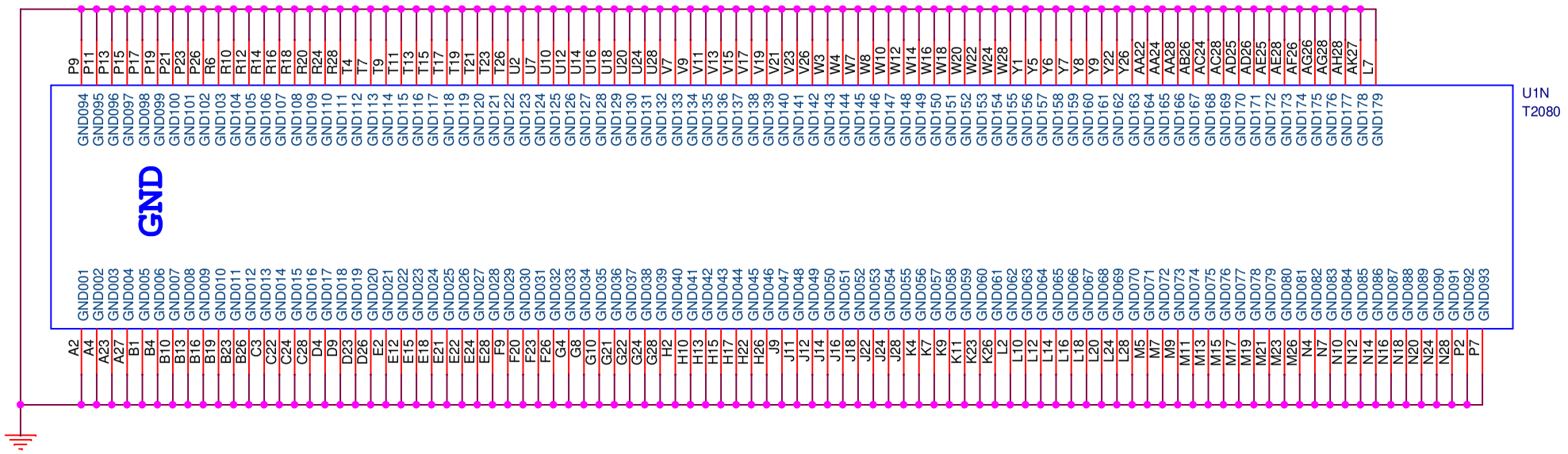


PROTO

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, July 10, 2019	Last modify date:	Page title: PROC PWR2
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 15 of 41 · REV. 0 · Format A3

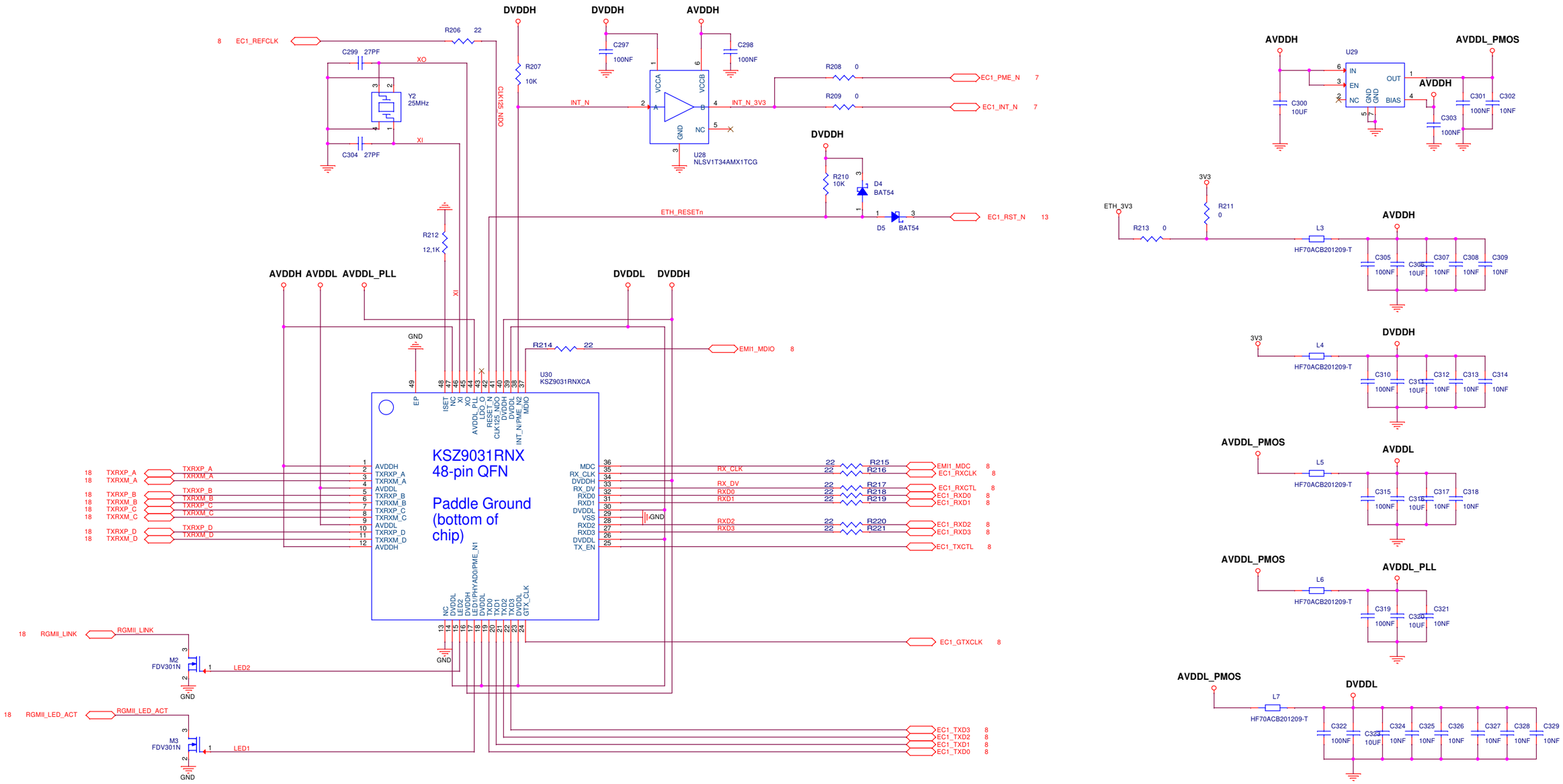
T2080 GROUND



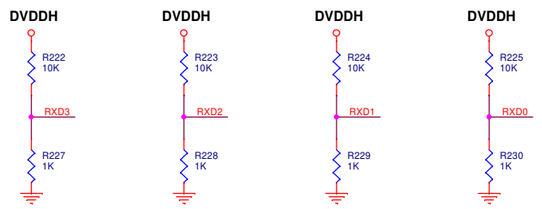


PROTO

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: PROC GND
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet16 of 41 / REV. 0 / Format A3



Strapping Pins

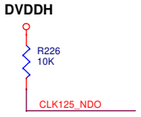


MODE[3:0]	Description
0000	reserved
0001	reserved
0010	reserved
0011	reserved
0100	NAND Tree mode
0101	reserved
0110	reserved
0111	Chip Power Down

MODE[3:0]	Description
1000	reserved
1001	reserved
1010	reserved
1011	reserved
1100	Advertise 1000BT full-duplex only (RGMII)
1101	Advertise 1000BT full- and half-duplex only (RGMII)
1110	Advertise all capabilites, except 1000BT half-duplex (RGMII)
1111	Advertise all capabilites (RGMII)

Strapping Pin

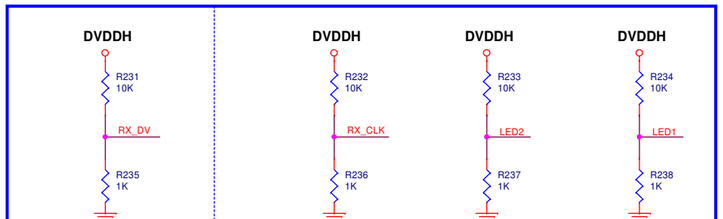
Single LED Mode



Single LED Mode

Pin	Description
LED2	1 : Link off 0 : Link on (any speed), solid color
LED1	Blinking : Activity (RX, TX)

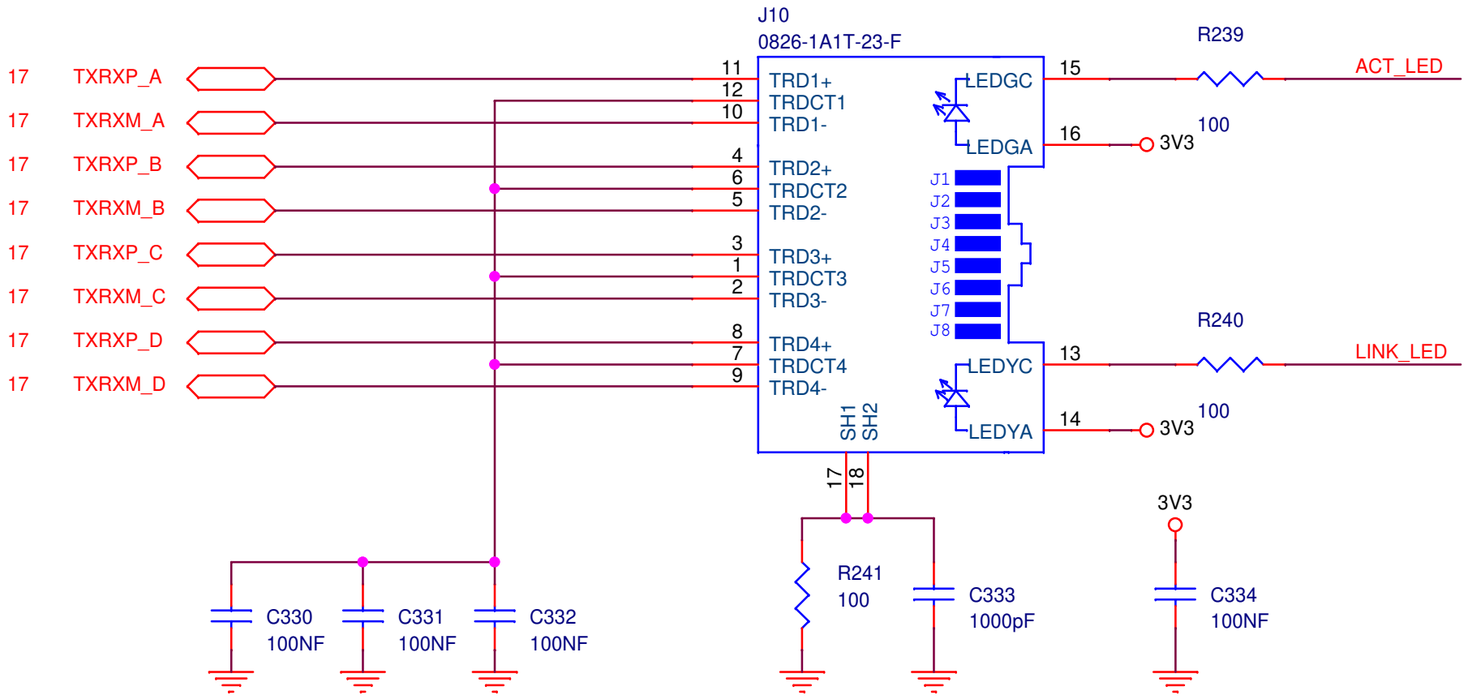
Strapping Pins



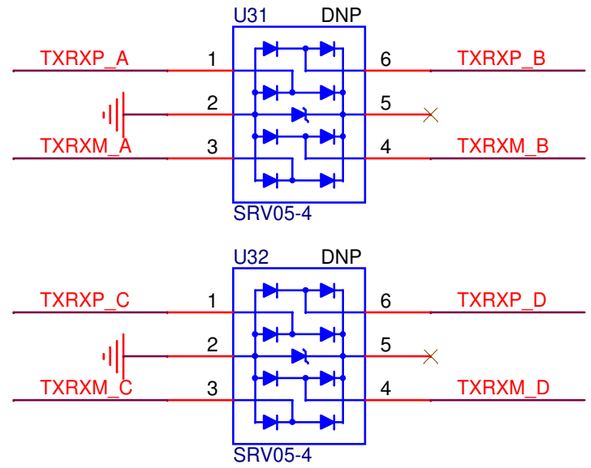
PROTO

Power Progress Community	Project: ACB_0001_0		
Creation Date: Friday, August 17, 2018	Last modify date: Wednesday, July 10, 2019	Page title: EC1 PHY	
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>	
PCB Code	BOM file	Sheet 17 of 41 / REV. 0	Format A2

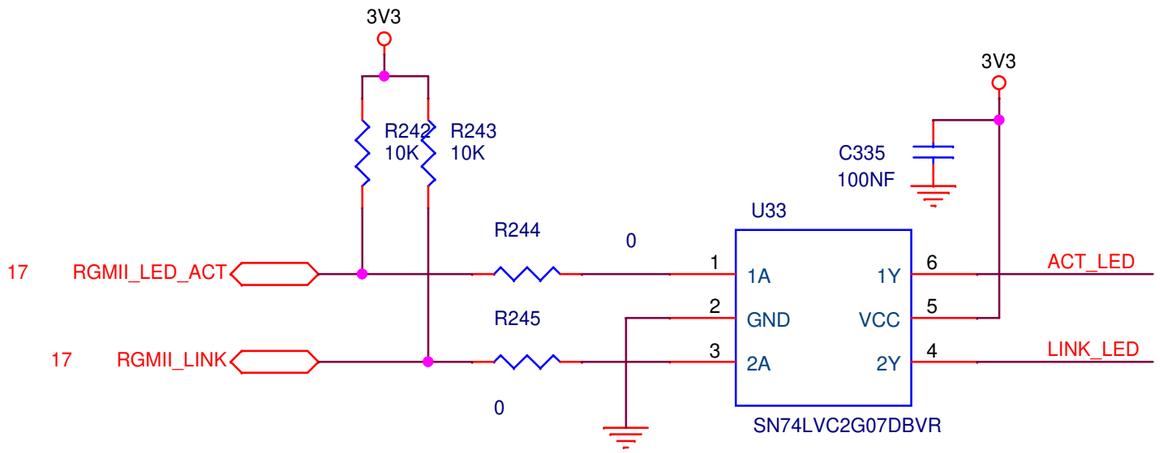
Gigabit Ethernet



For Gigabit Ethernet protection, place close to magnetics



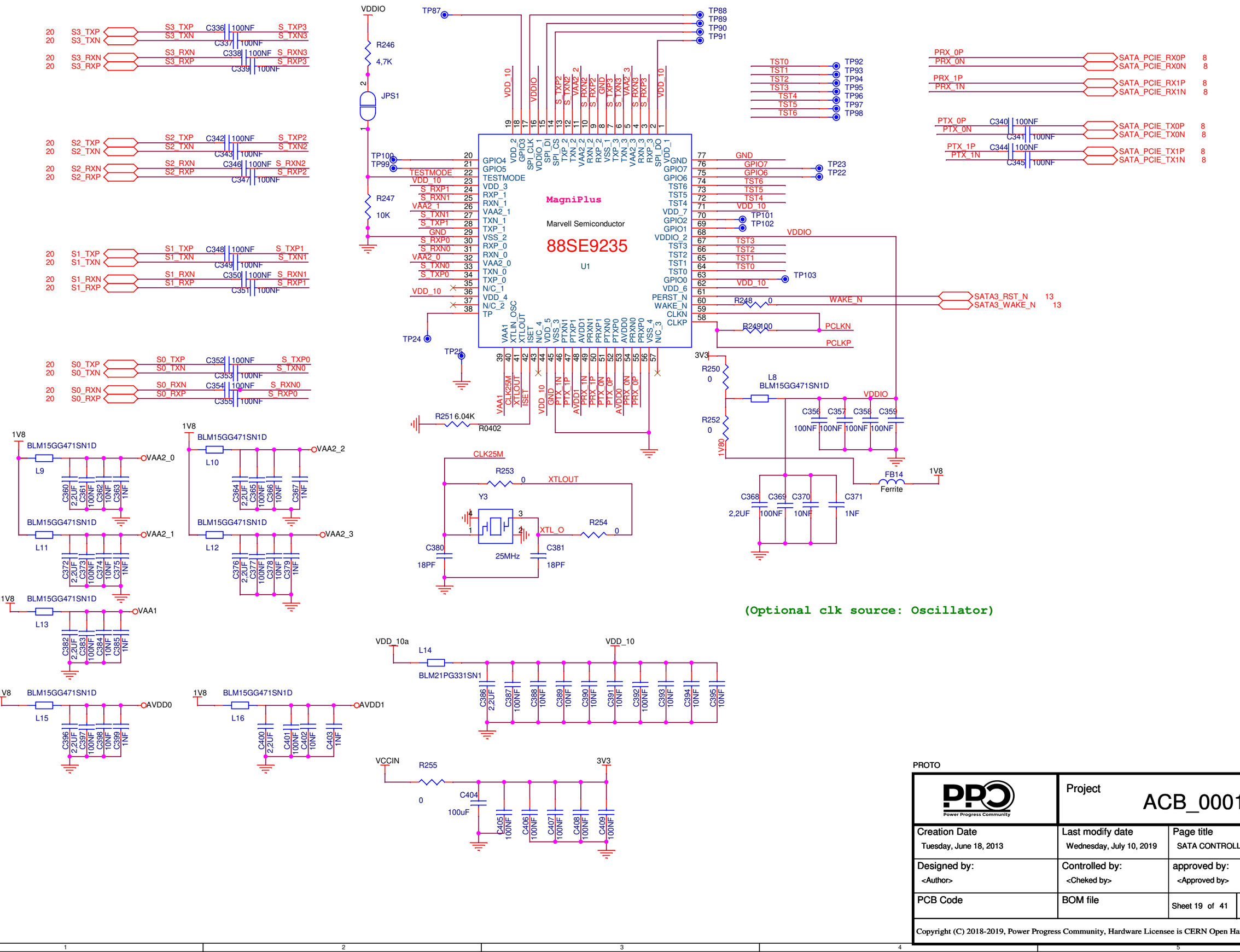
Led Ethernet Buffer



PROTO

PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Friday, August 17, 2018	Last modify date: Wednesday, July 10, 2019	Page title: ETHERNET CONN		
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>		
PCB Code	BOM file	Sheet 18 of 41	REV. 0	Format A4

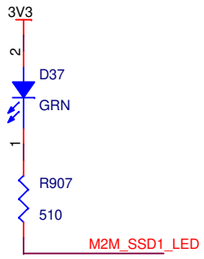
MagniPlus -SATA Interface



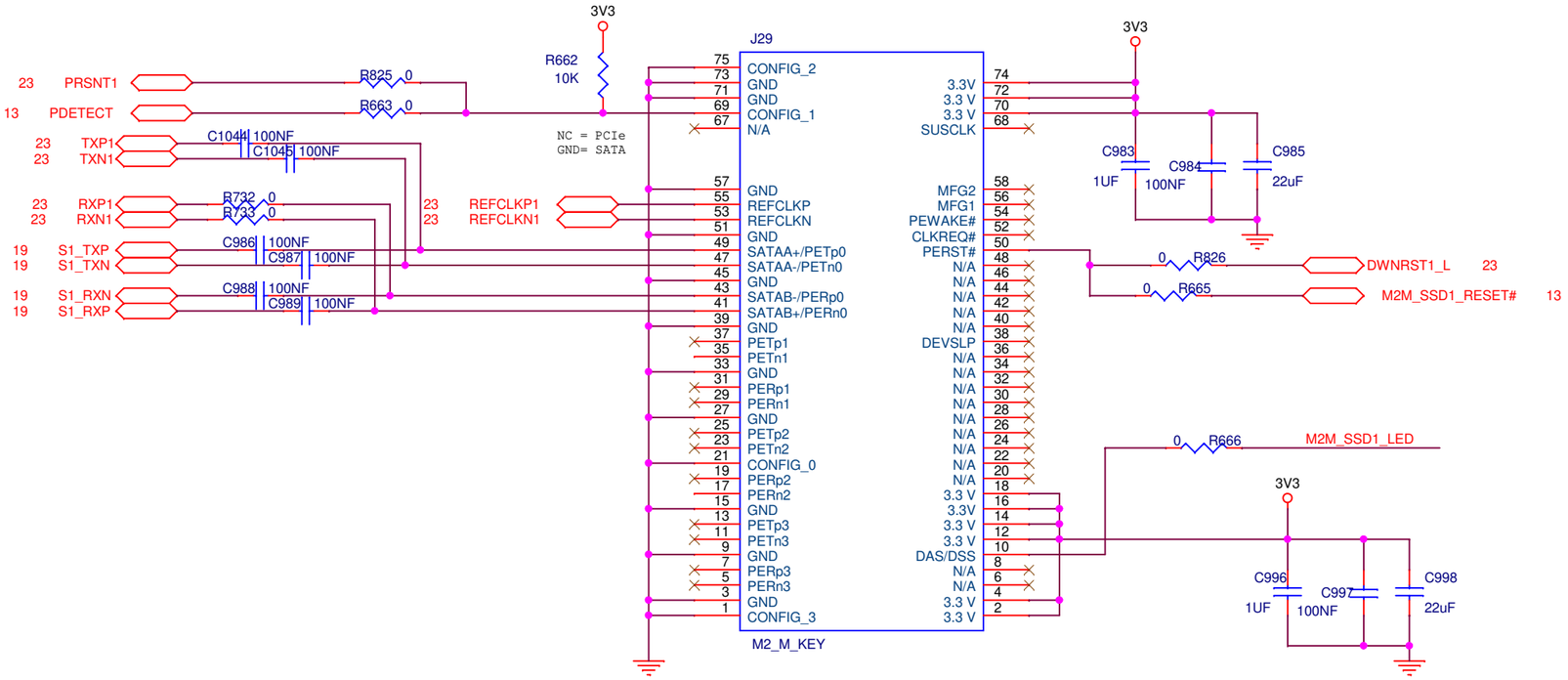
(Optional clk source: Oscillator)

PROTO

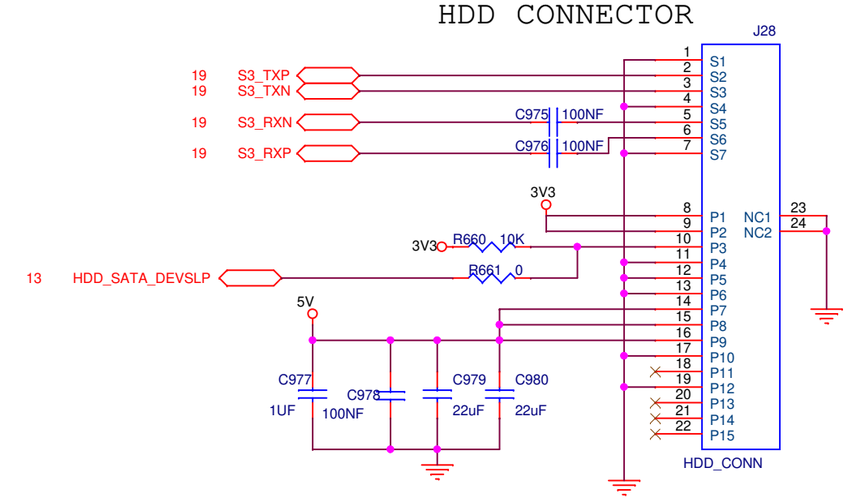
PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Tuesday, June 18, 2013	Last modify date: Wednesday, July 10, 2019	Page title: SATA CONTROLLER		
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>		
PCB Code	BOM file	Sheet 19 of 41	REV. 0	Format A3



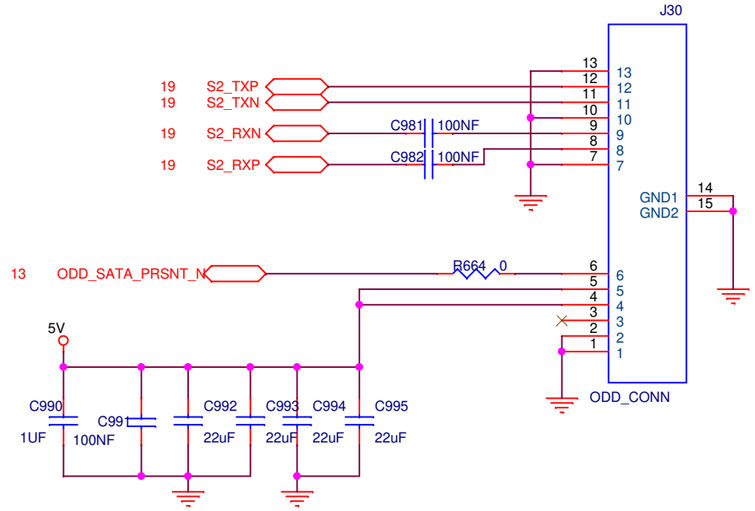
M2 SSD1 PCIEx1 CONNECTOR



HDD CONNECTOR

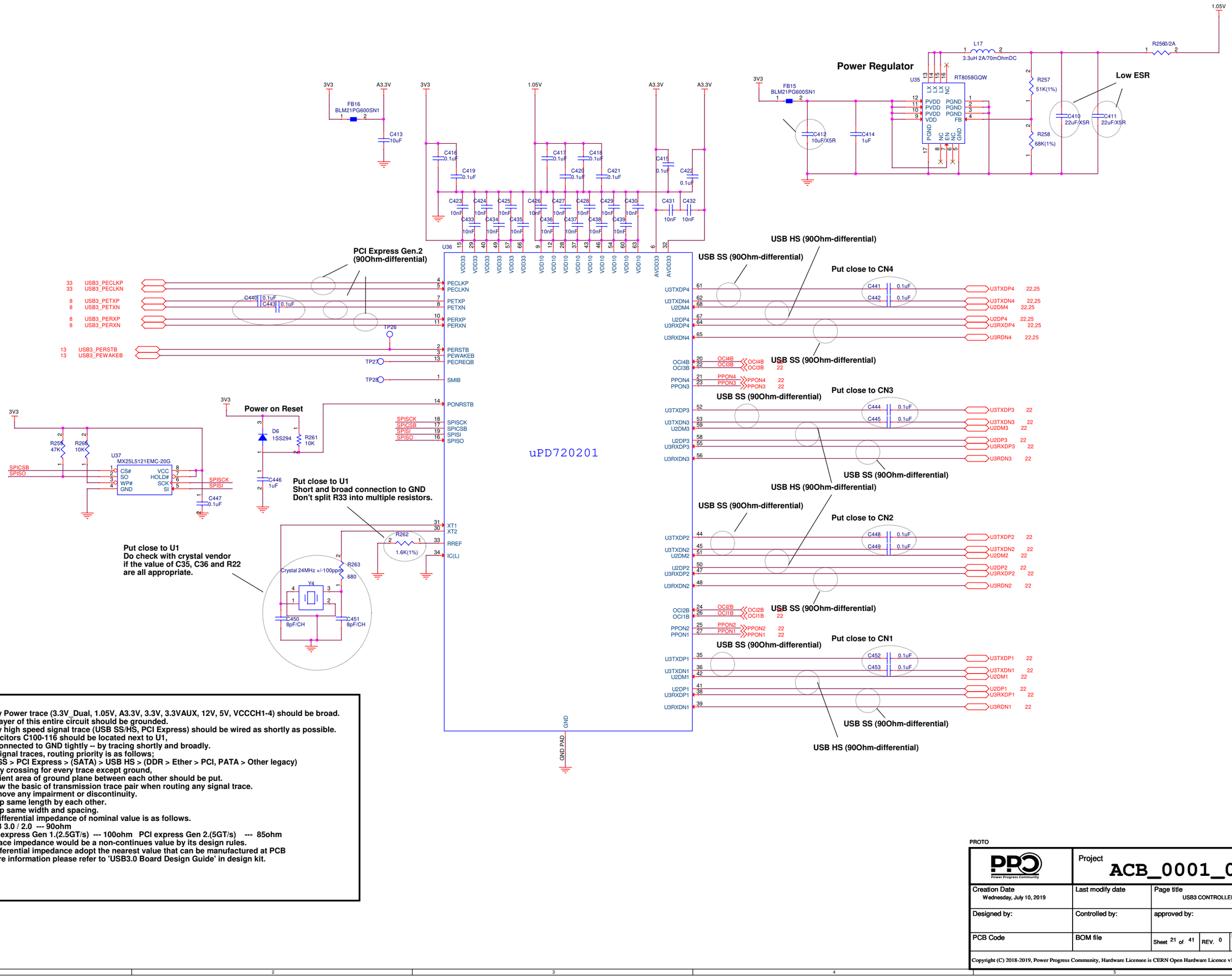


ODD CONNECTOR



PROTO

Power Progress Community	Project ACB_0001_0			
Creation Date: Friday, November 30, 2018	Last modify date: Wednesday, July 10, 2019	Page title: SATA CONNECTOR		
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>		
PCB Code	BOM file	Sheet 20 of 41	REV. 0	Format A3

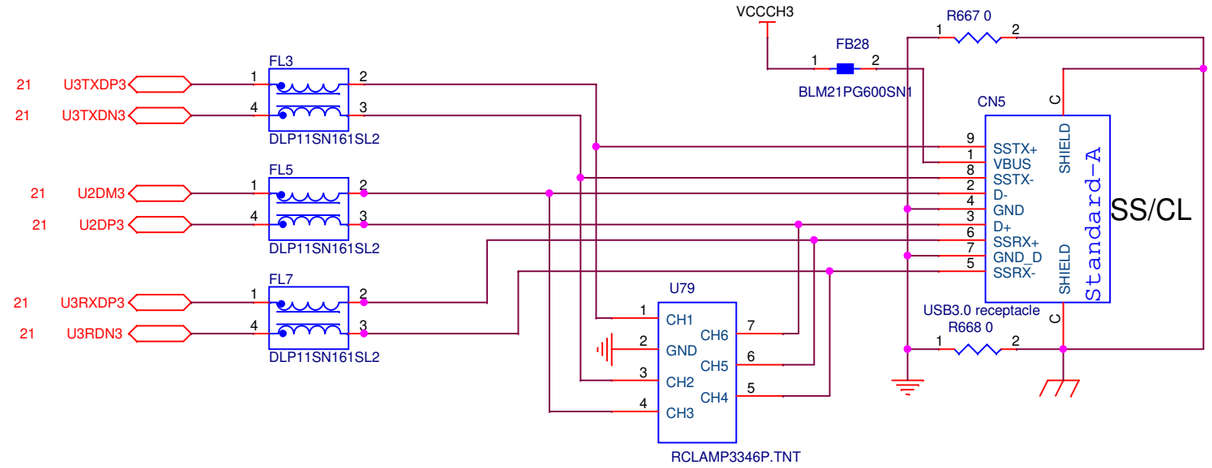


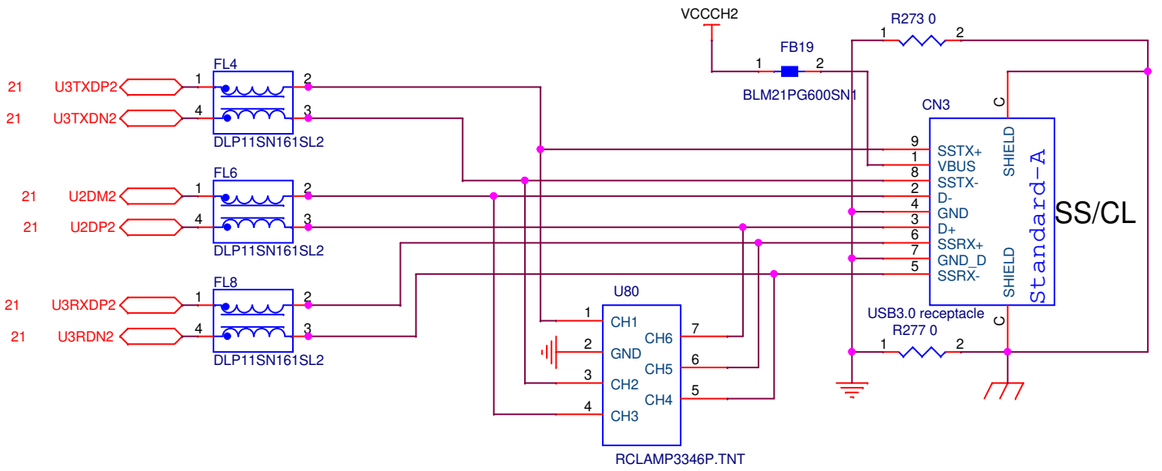
Note:

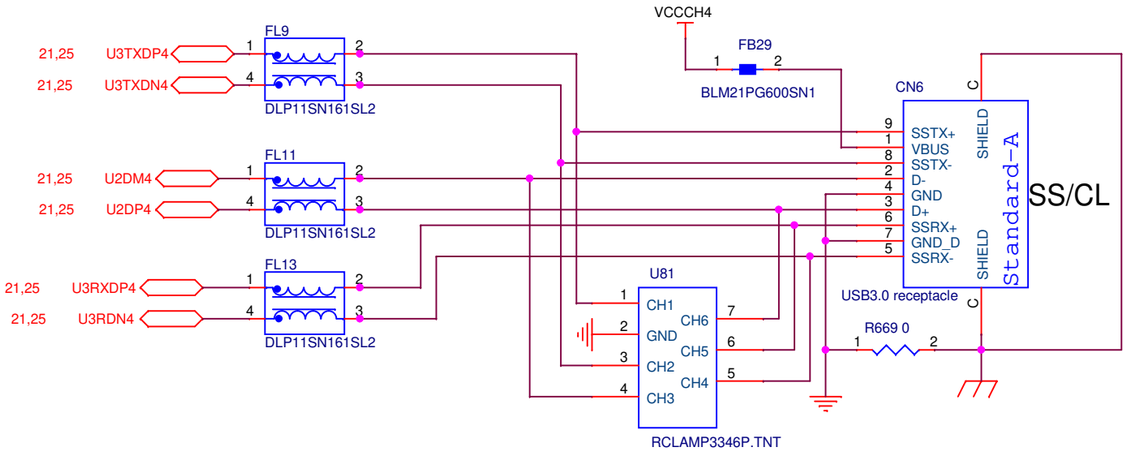
1. Every Power trace (3.3V_Dual, 1.05V, A3.3V, 3.3V, 3.3VAUX, 12V, 5V, VCCCH1-4) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB SS/HS, PCI Express) should be wired as shortly as possible.
4. Capacitors C100-116 should be located next to U1,
   and connected to GND tightly -- by tracing shortly and broadly.
5. For signal traces, routing priority is as follows;
   USB SS > PCI Express > (SATA) > USB HS > (DDR > Ether > PCI, PATA > Other legacy)
6. At any crossing for every trace except ground,
   sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
   > Remove any impairment or discontinuity.
   > Keep same length by each other.
   > Keep same width and spacing.
8. The differential impedance of nominal value is as follows.
   > USB 3.0 / 2.0 --- 90ohm
   > PCI express Gen 1.(2.5GT/s) --- 100ohm PCI express Gen 2.(5GT/s) --- 85ohm
   PCB trace impedance would be a non-continues value by its design rules.
   The differential impedance adopt the nearest value that can be manufactured at PCB
   For more information please refer to 'USB3.0 Board Design Guide' in design kit.

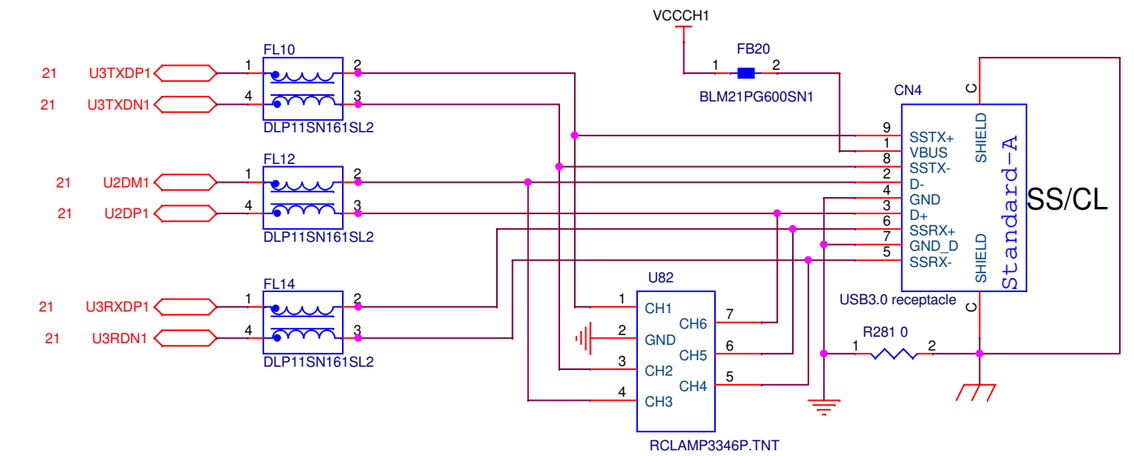
PROTO

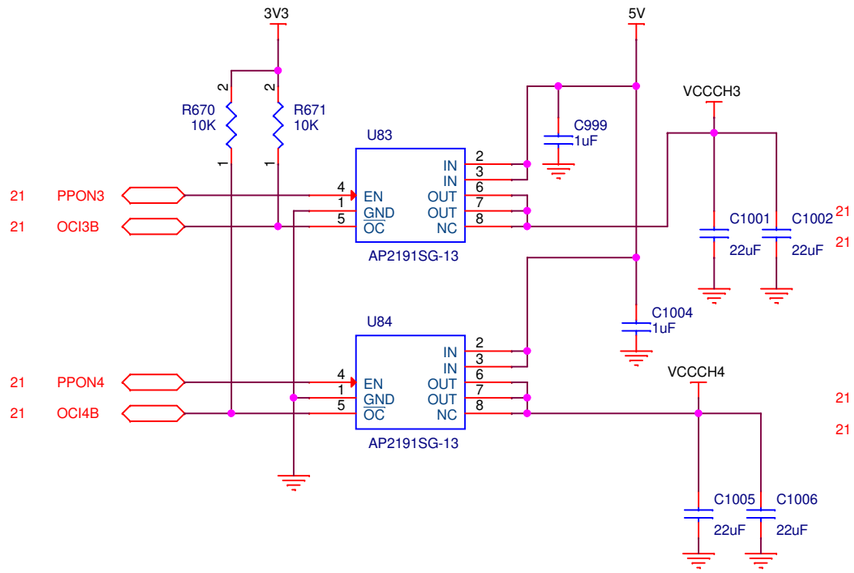
PRO Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: USB3 CONTROLLER
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 21 of 41 · REV. 0 · Format A2

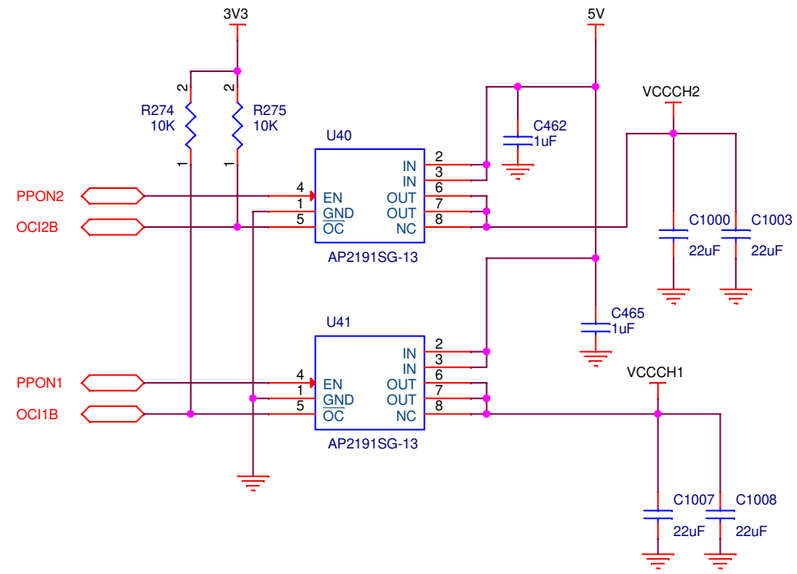






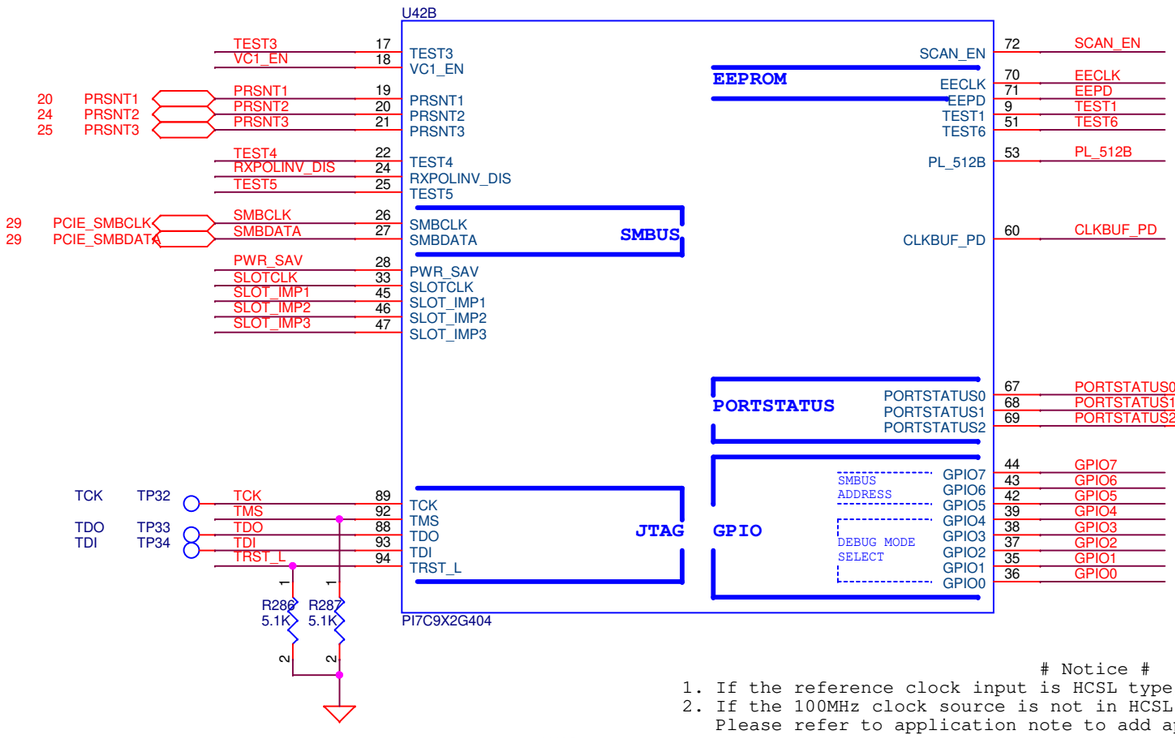


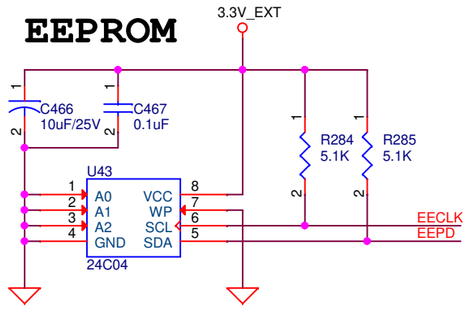


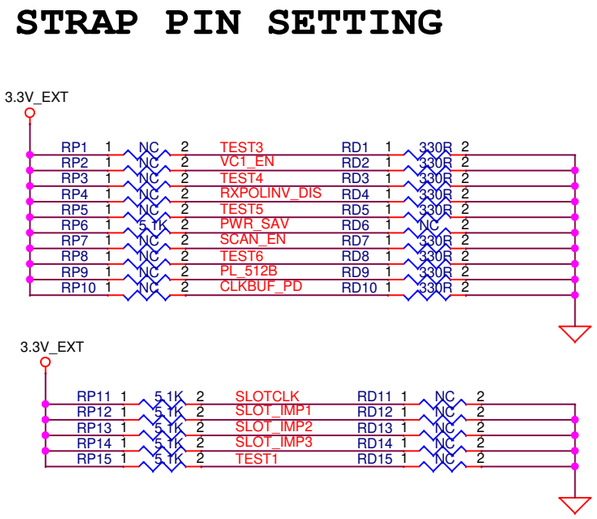


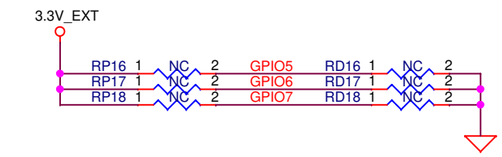
PROTO

PPC Power Progress Community	Project ACB_0001_0		
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: USB3 PORTS	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 22of 41 / REV. 0	Format A3

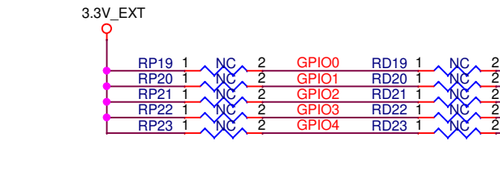






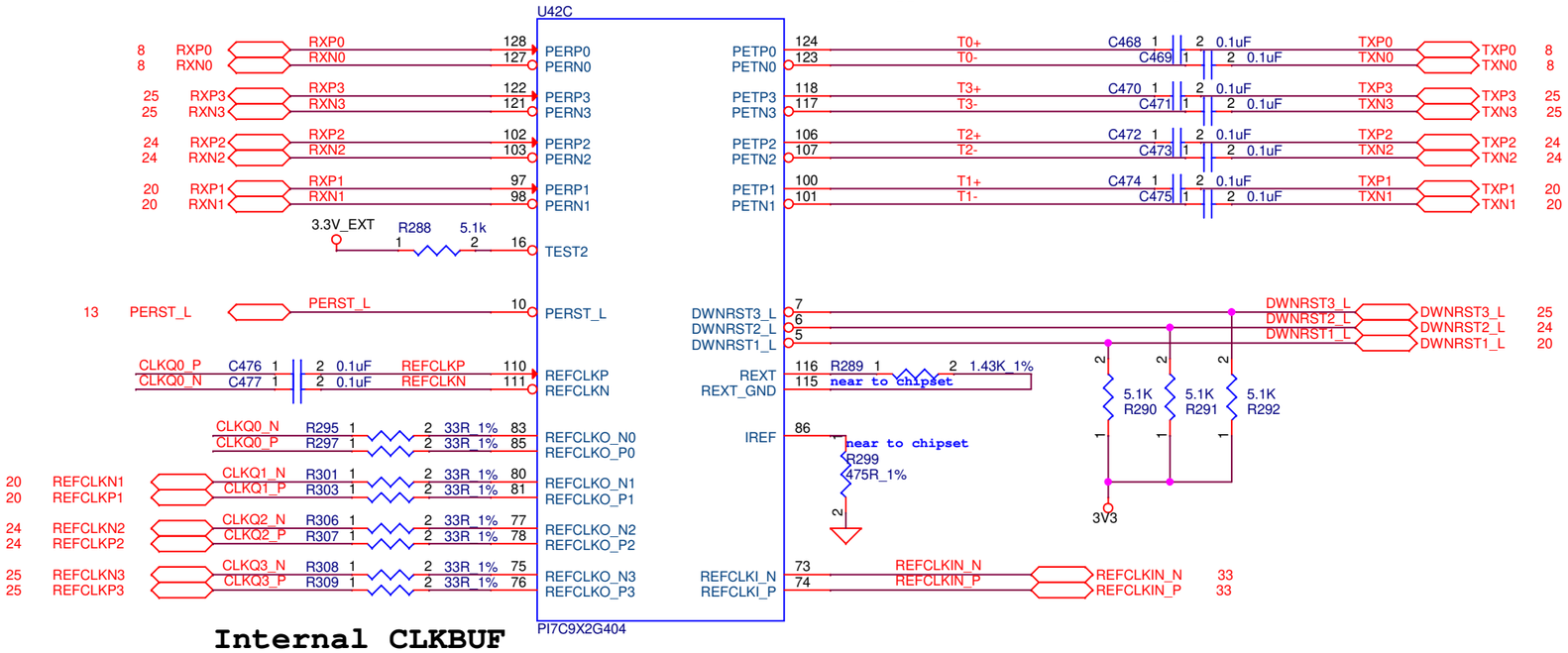


BIT	SMBus Address
0	GPIO[5]
1	GPIO[6]
2	GPIO[7]
3	1
4	0
5	1
6	1
7	0

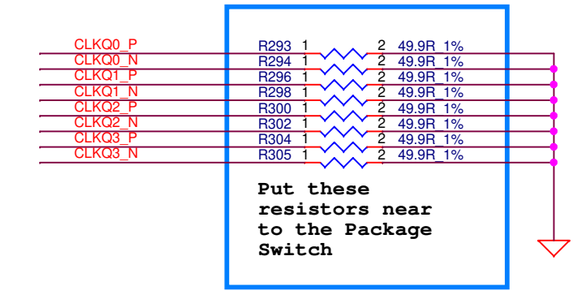


Notice

1. If the reference clock input is HCSL type, it can be AC or DC coupling.
2. If the 100MHz clock source is not in HCSL protocol (ex: LVPECL, LVDS , etc), Please refer to application note to add application circuit.



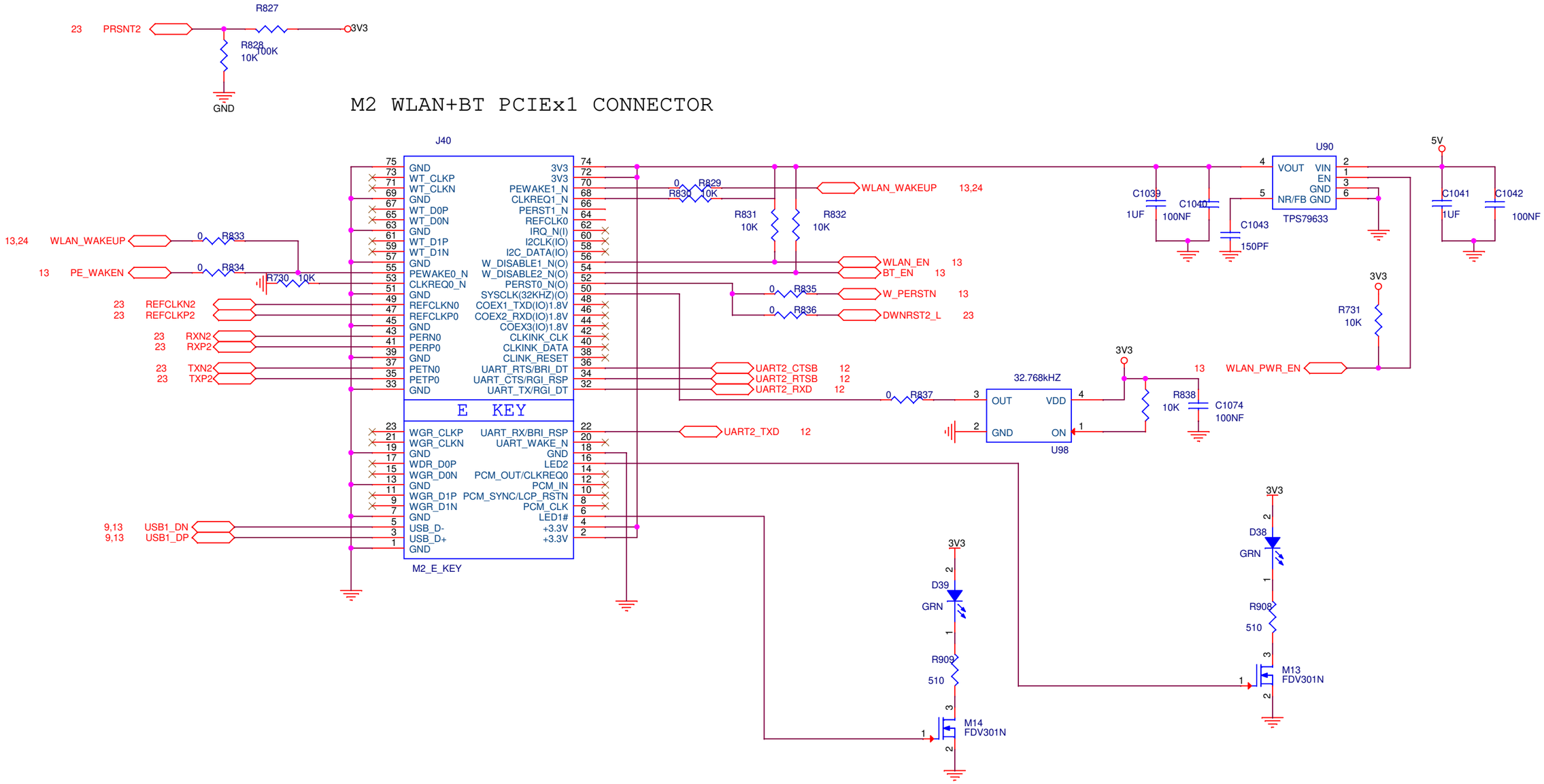
Internal CLKBUF



PROTO

PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Tuesday, June 25, 2013	Last modify date: Wednesday, July 10, 2019	Page title: PCIE BRIDGE		
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>		
PCB Code	BOM file	Sheet 23 of 41	REV. 0	Format A3

M2 WLAN+BT PCIEx1 CONNECTOR

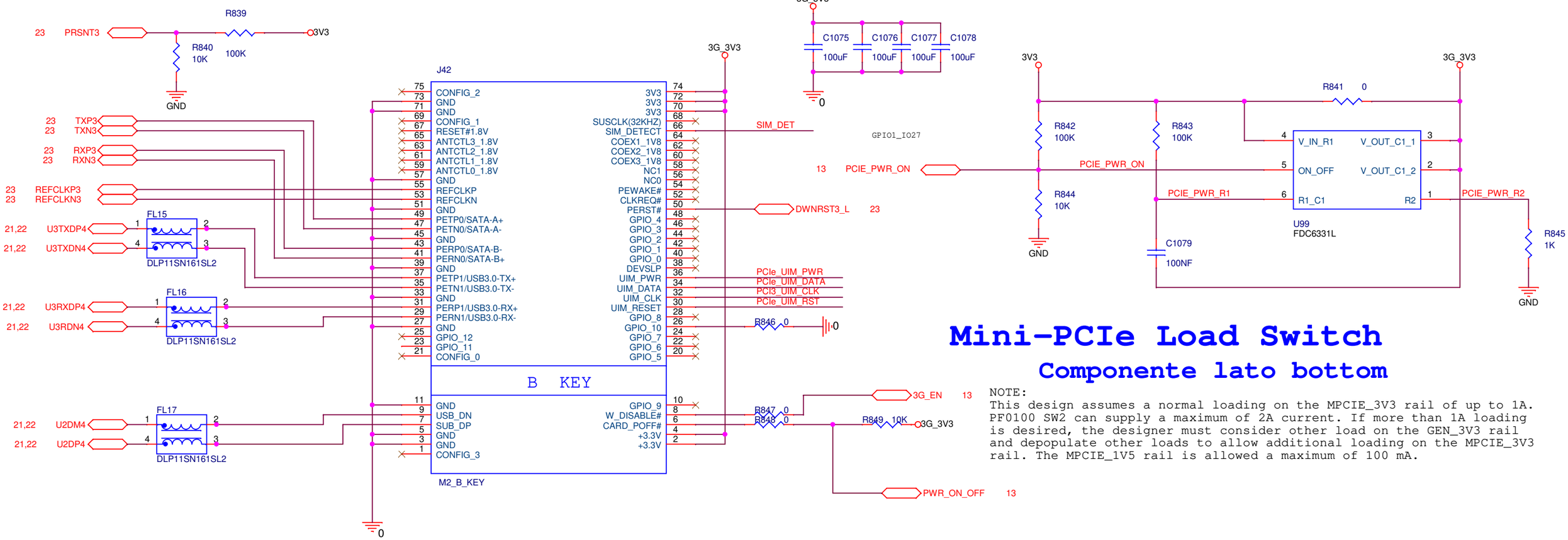


PROTO

PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Friday, December 28, 2018	Last modify date: Wednesday, July 10, 2019	Page title: SATA CONTROLLER		
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>		
PCB Code	BOM file	Sheet 24 of 41	REV. 0	Format A3

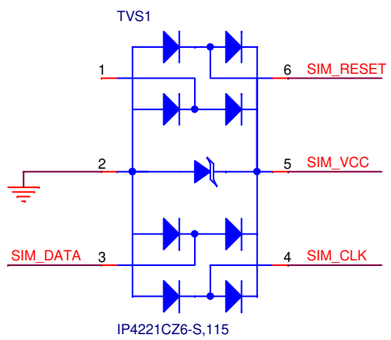
Mini-PCIe Load Switch

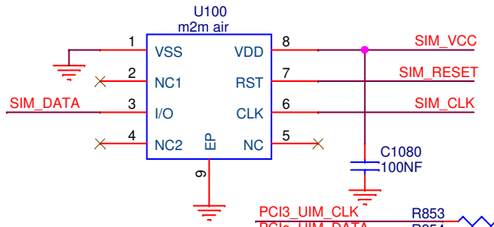
Componente lato bottom



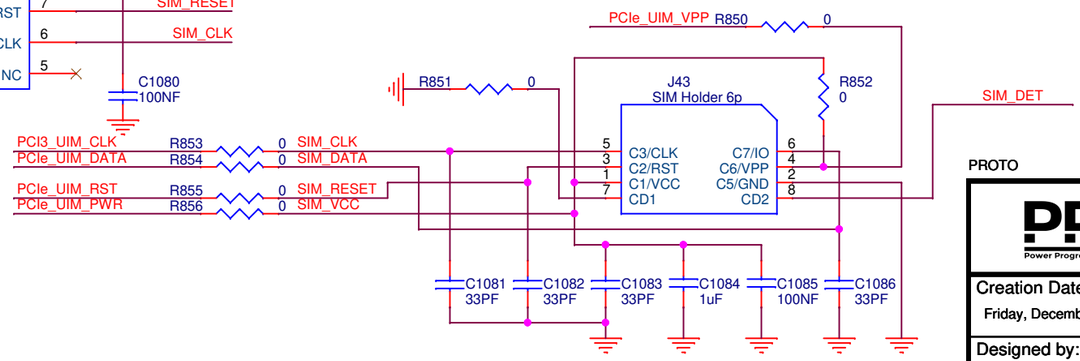
NOTE:
This design assumes a normal loading on the MPCIE_3V3 rail of up to 1A. PF0100 SW2 can supply a maximum of 2A current. If more than 1A loading is desired, the designer must consider other load on the GEN_3V3 rail and depopulate other loads to allow additional loading on the MPCIE_3V3 rail. The MPCIE_1V5 rail is allowed a maximum of 100 mA.

SIM ON CHIP



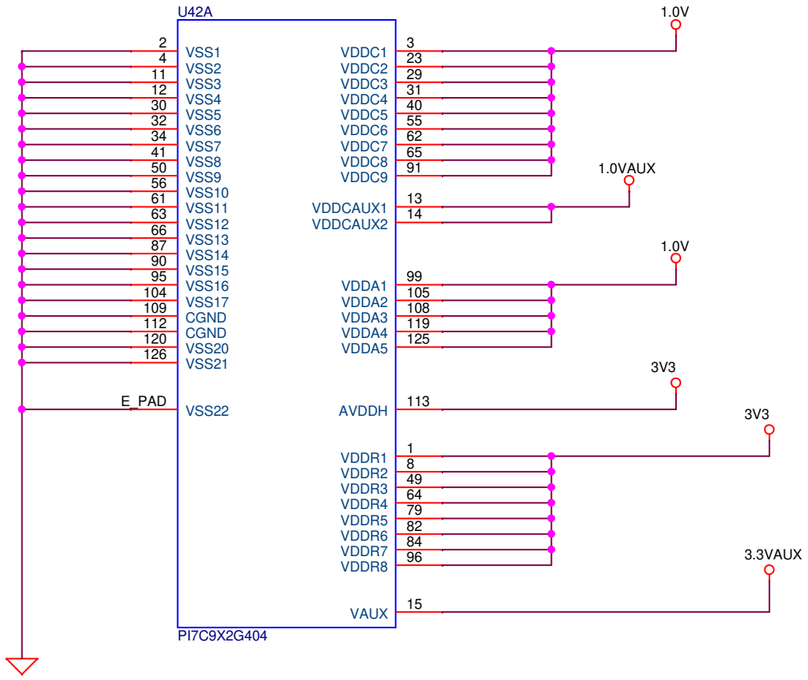


SIM HOLDER

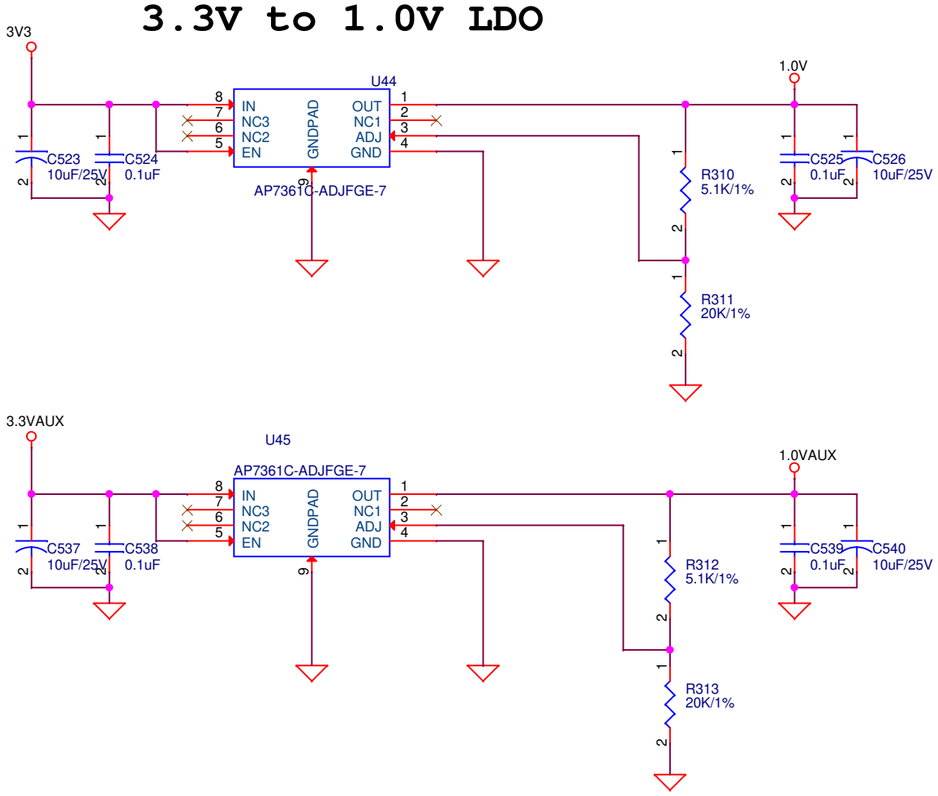


PROTO

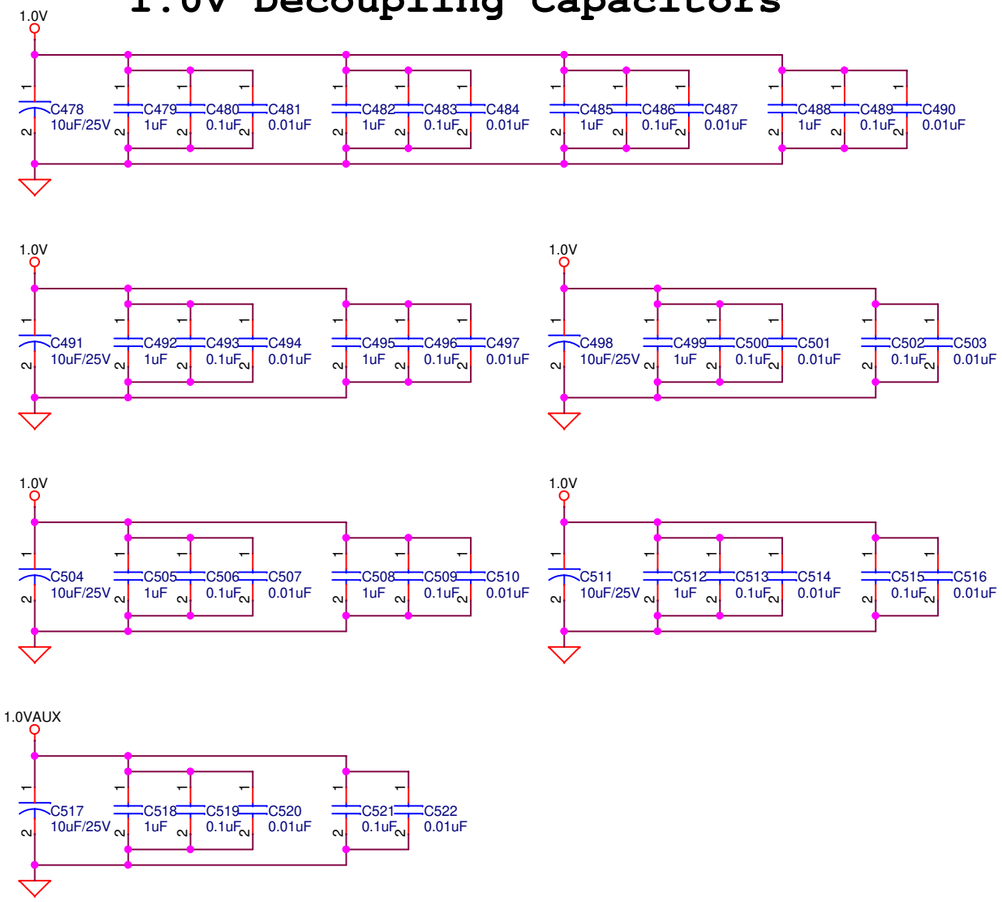
Project: ACB_0001_0			
Creation Date: Friday, December 28, 2018	Last modify date: Wednesday, July 10, 2019	Page title: 3G MODEM	
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>	
PCB Code	BOM file	Sheet 25 of 41 / REV. 0	Format A3



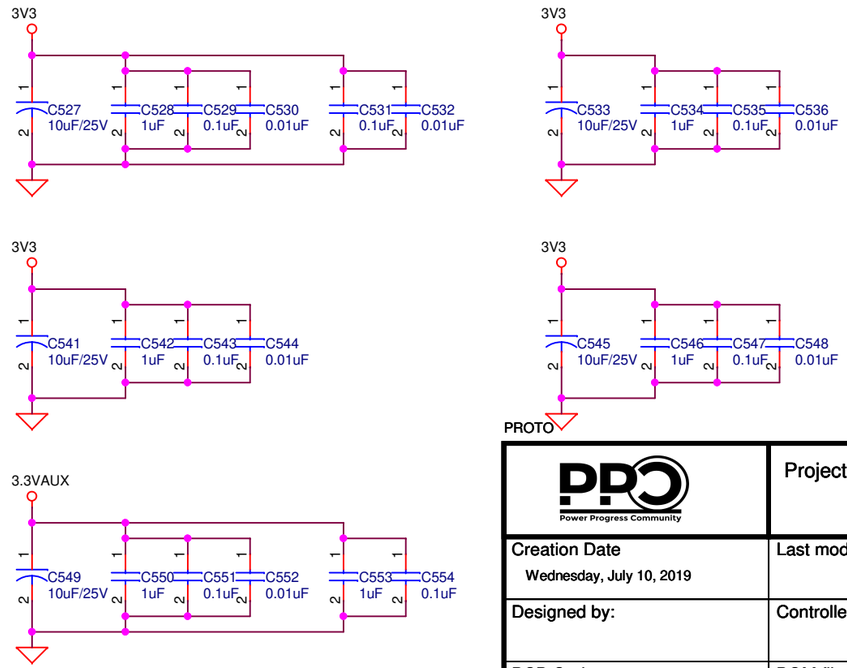
3.3V to 1.0V LDO



1.0V Decoupling Capacitors

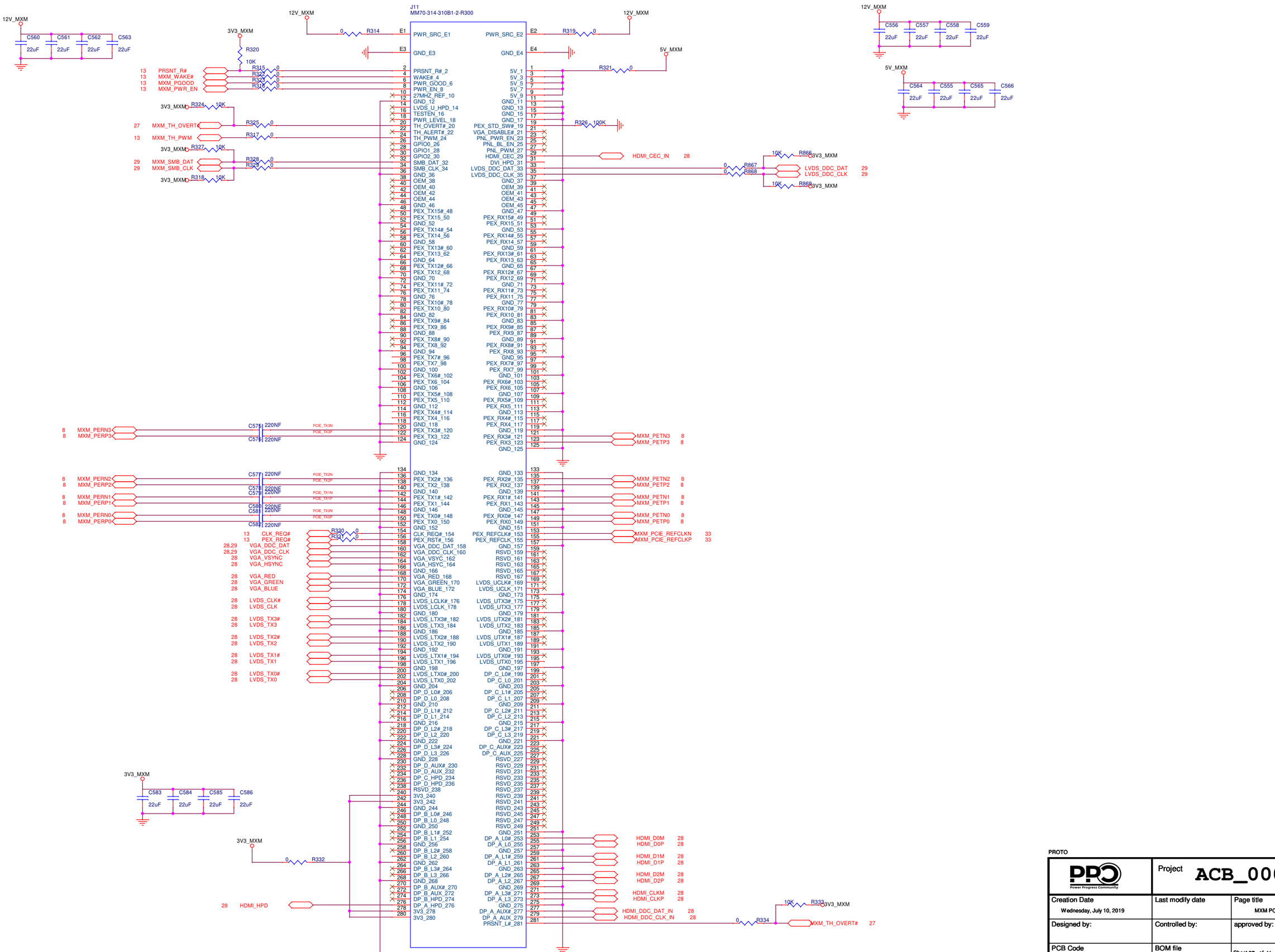


3.3V Decoupling Capacitors



PROTO

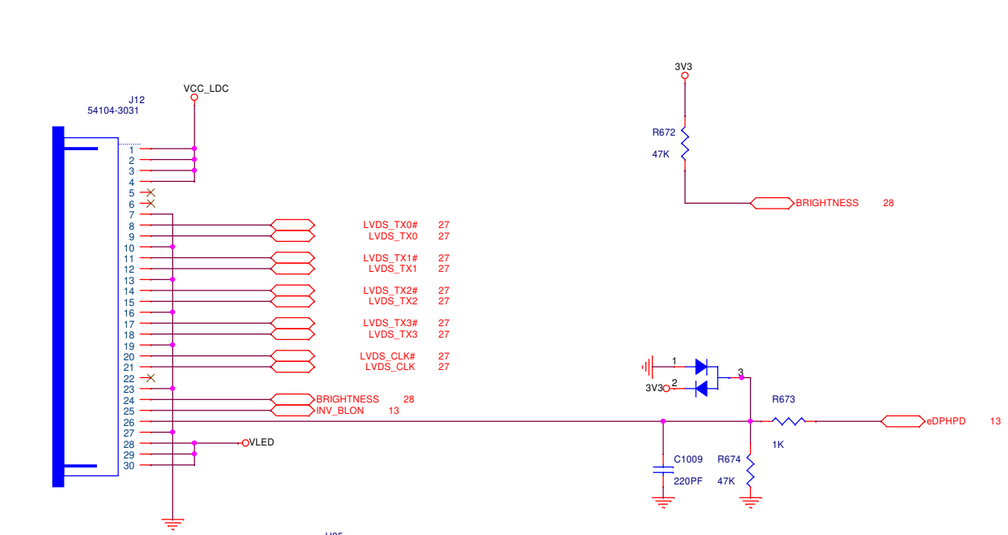
Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: PCIE BRIDGE POWER
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 26 of 41 / REV. 0 / Format A3

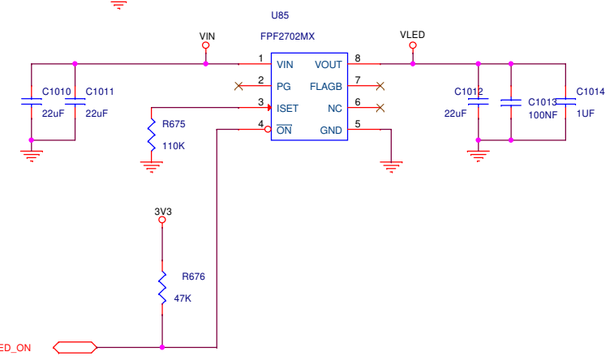


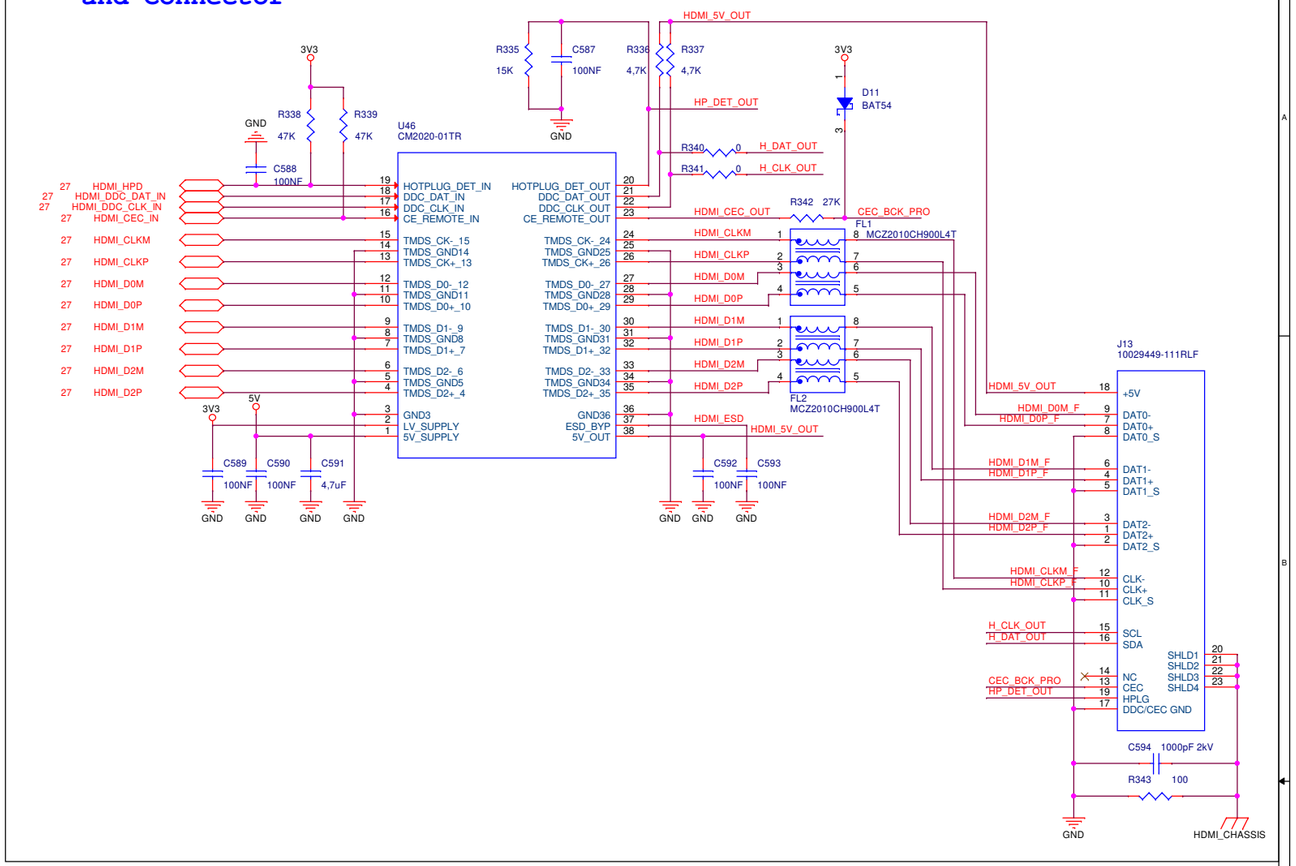
PROTO

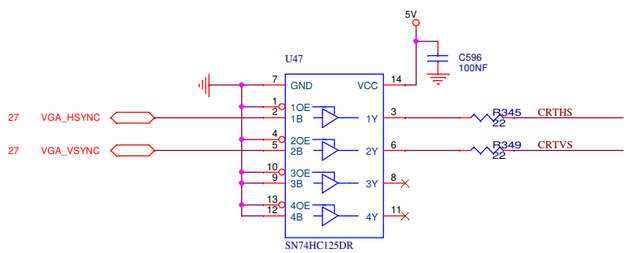
Power Progress Community	Project ACB_0001_0		
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: MXM PCIE	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 27 of 41	REV. 0 / Format A2

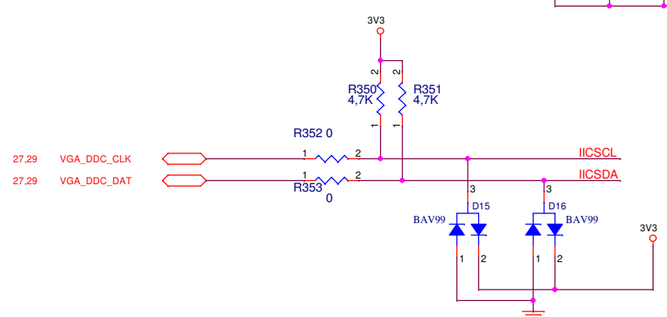
HDMI Port protections and Connector

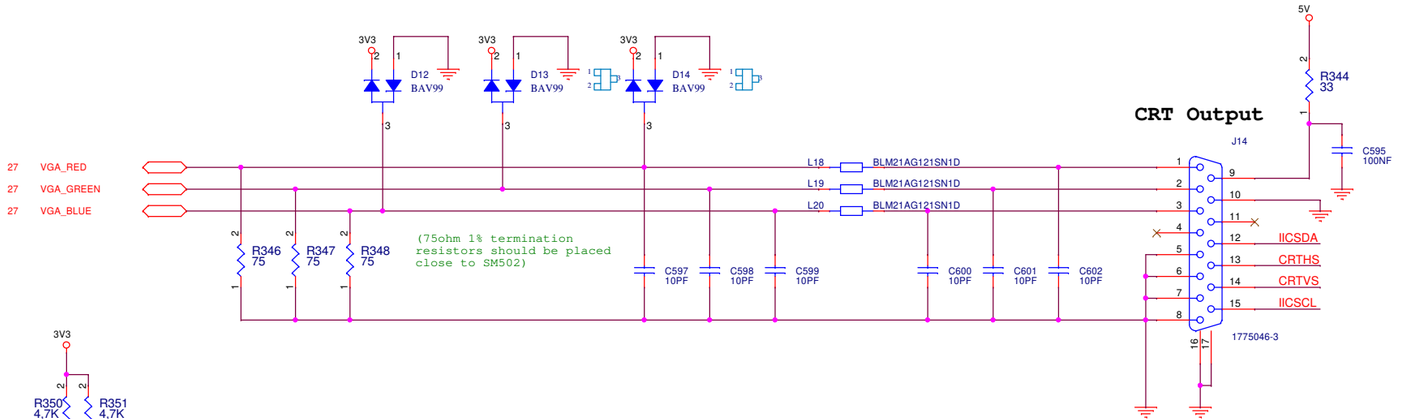






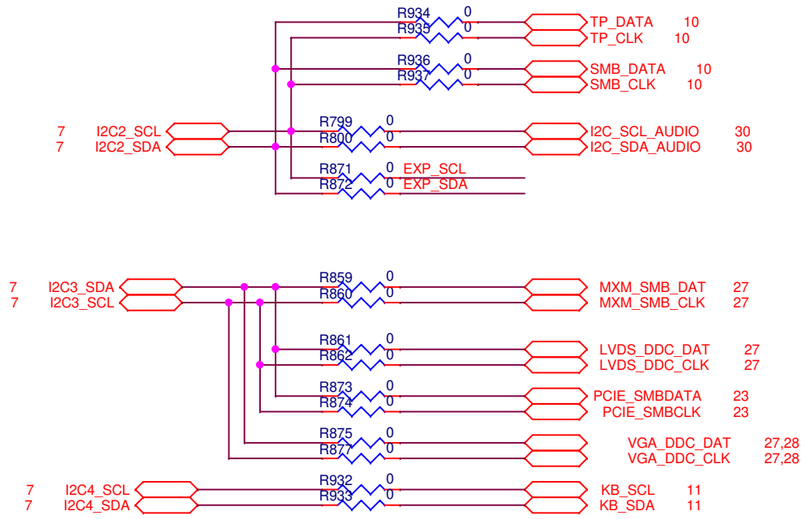






PROTO

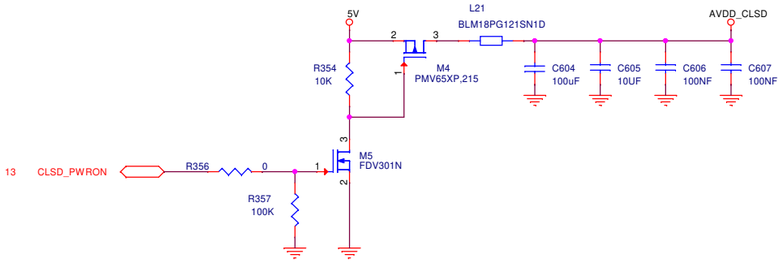
PPC Power Progress Community	Project ACB_0001_0		
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: MXM VIDEO OUT	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 28 of 41 / REV. A	Format A2

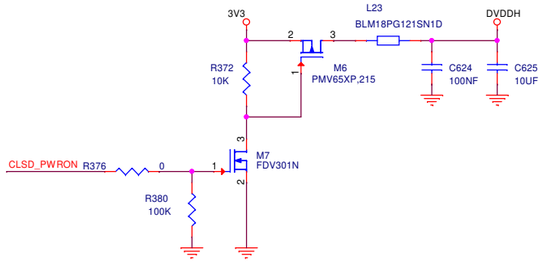


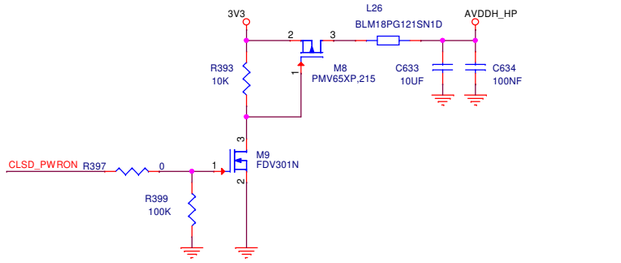
PROTO

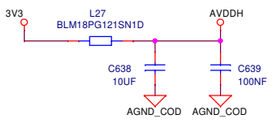
PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: I2C WRAP		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 29 of 41	REV. 0	Format A3

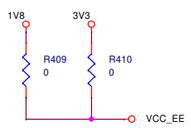
Power Switches



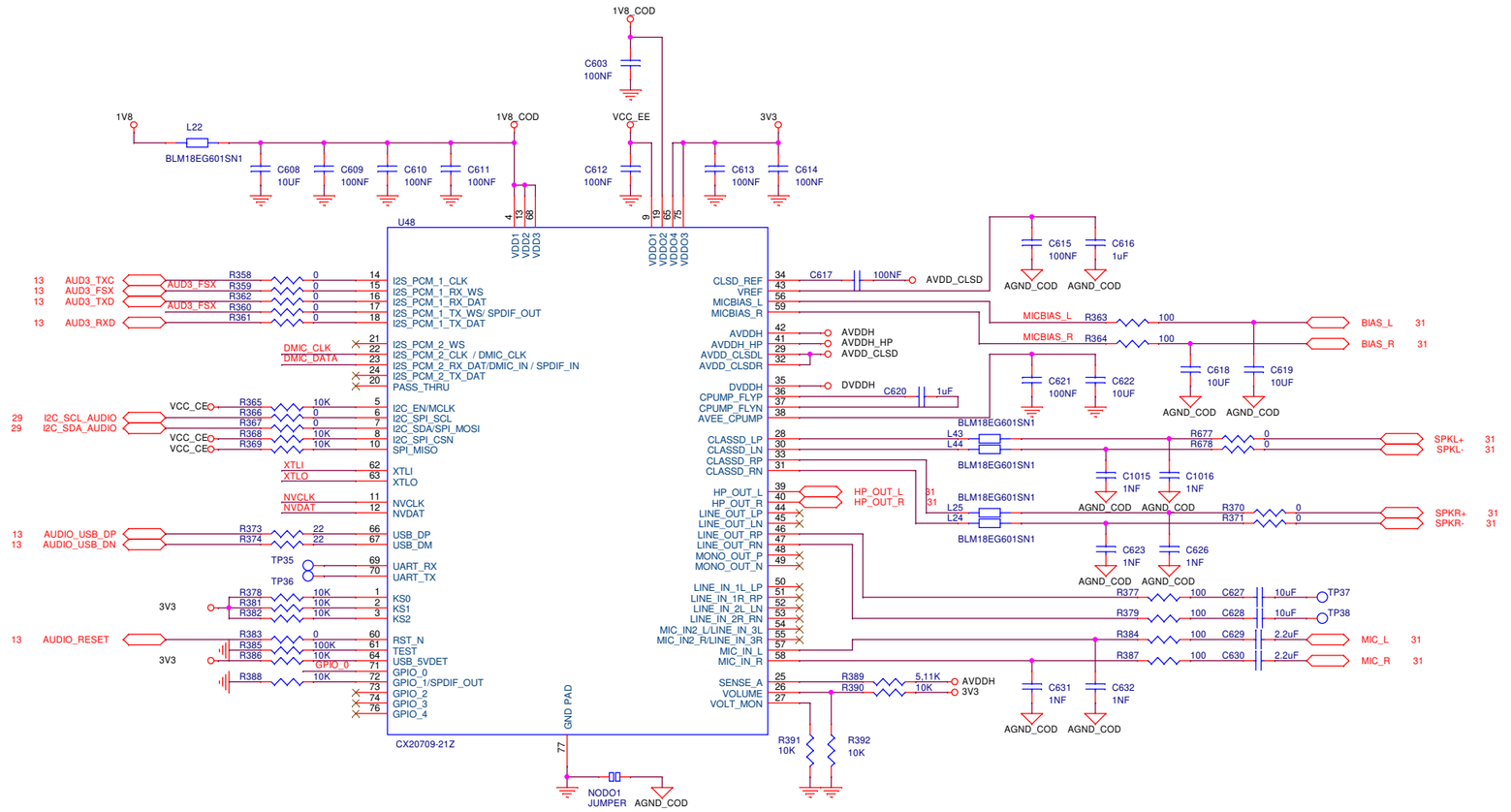


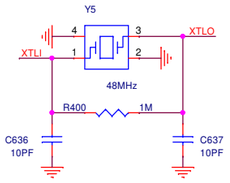


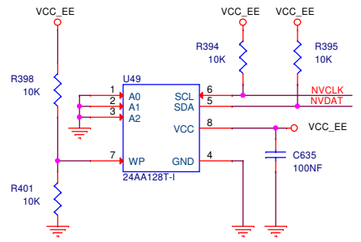




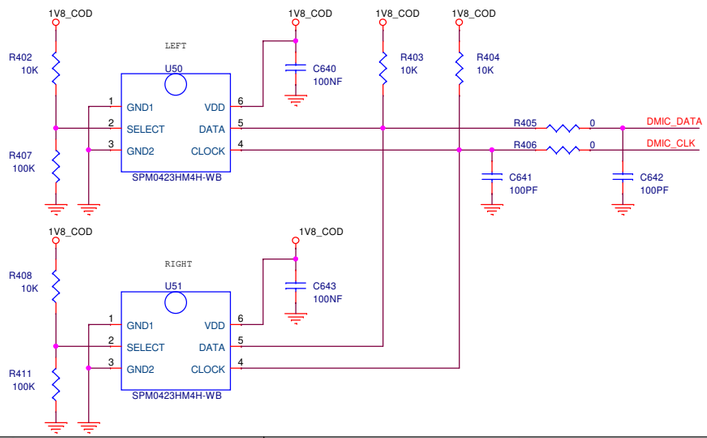
Codec







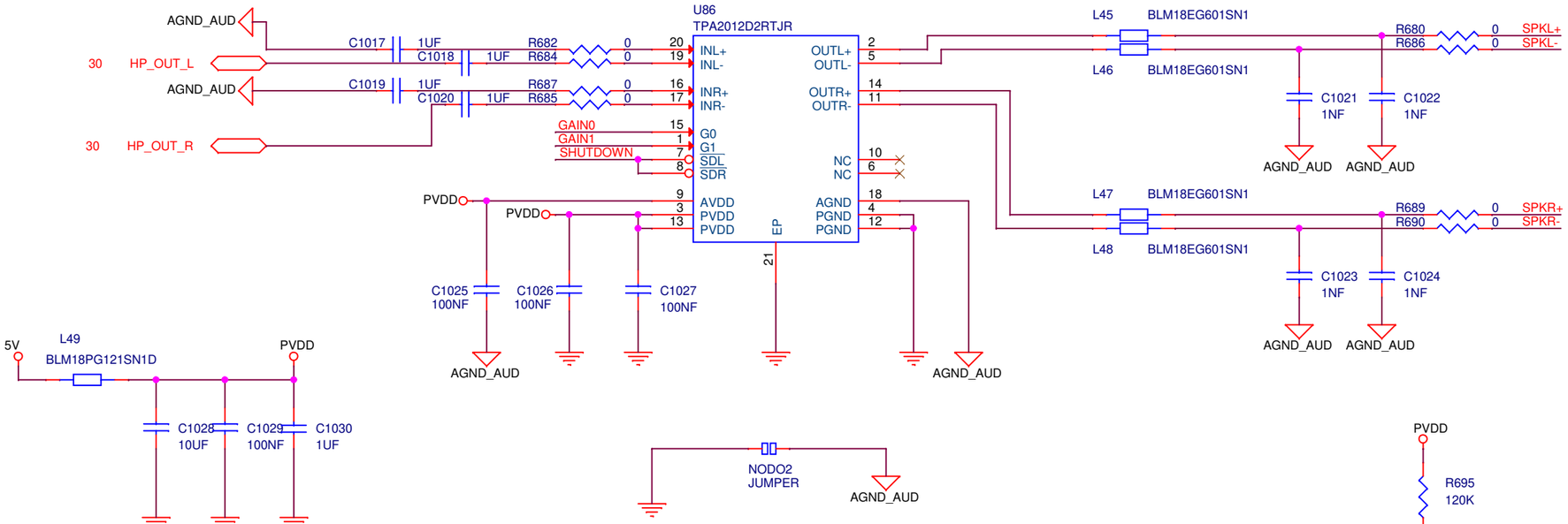
Digital Mics

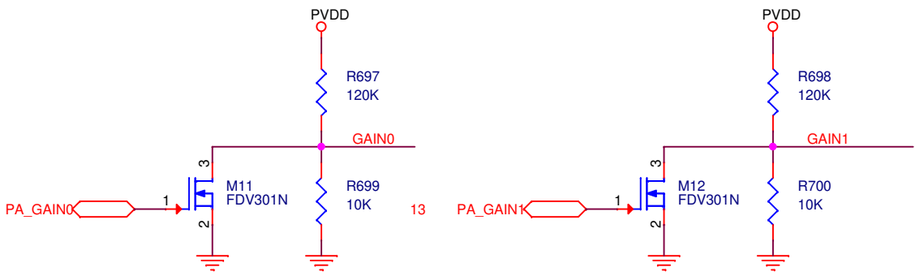


PROTO

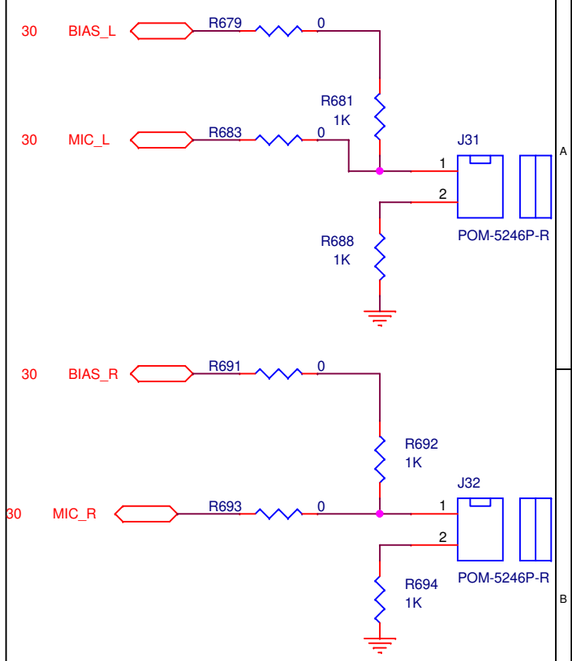
PRO Power Progress Community	Project ACB_0001_0	
Creation Date: Wednesday, July 10, 2019	Last modify date:	Page title: AUDIO USB
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 30 of 41 / REV. A / Format A2

Class D Audio Amplifier

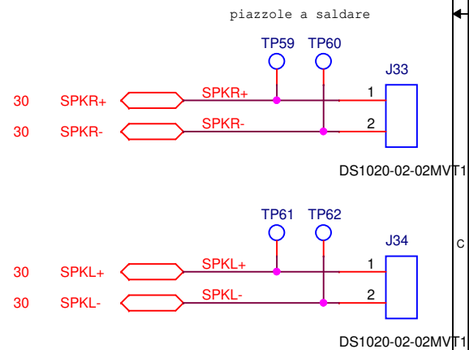




Analog MICs



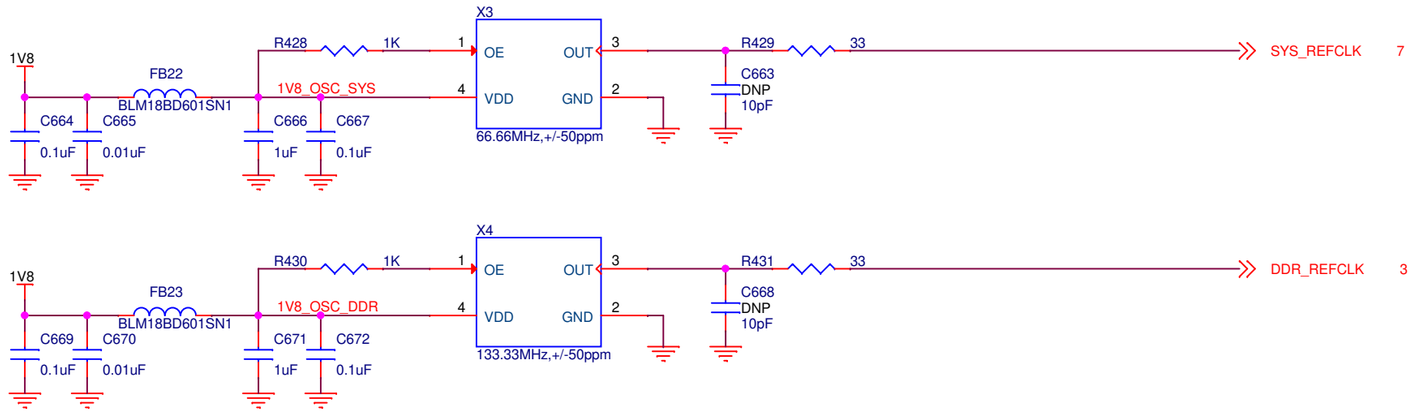
Speakers Conn.



PROTO

PPC Power Progress Community	Project ACB_0001_0	
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: AUDIO AMPL
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 31 of 41 / REV. 0 / Format A3

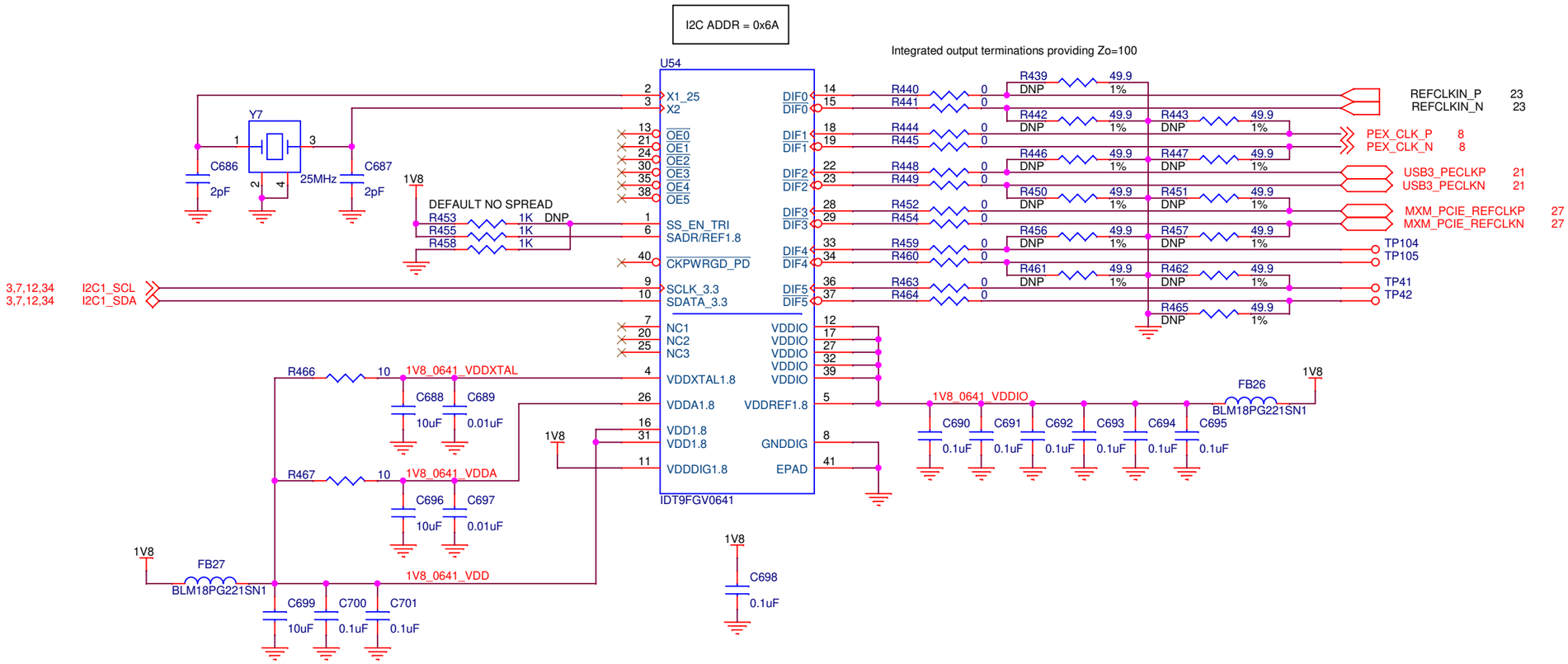
SYSTEM CLOCK GENERATORs



PROTO

Power Progress Community	Project **ACB_0001_0**			
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: CLOCK 1		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 32 of 41	REV. 0	Format A3

SYSTEM CLOCK GENERATORs (cont.)



PROTO

PPC Power Progress Community	Project ACB_0001_0		
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: CLOCK 2	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 33 of 41	REV. 0 / Format A3

T2080 CORE POWER CONVERTOR

For the first programming
of the internal flash:
VR_HOT, EN
need to be connected to GND. via
short Jumper and CPLD will drive
both enables low.
(I2C address in this mode 0Ah)

PROGRAMING CONNECTOR

VCORE_HOT_N — J16 — JMP2
LABEL = PROG_VCORE
SM_DIO — J17 — 1
SM_CLK — 2, 3
HDR_1X3

12V — R474 13K — R478 1K — C713 0.01uF

3V3

VCORE_VCC — R475 0 — C714 1uF — C715 0.1uF

VCORE_VSEN1
VCORE_VRTN1

VCORE — R468 100 — R469 0 — SENSEVDD 14 — SENSEGND 14 — R471 0 — R473 100

C717 3000pF

POWER ON AFTER IO PWER

13,36 VCORE_EN
34 VCORE_PGOOD

R481 4.7K
R482 10K

R486 1K
R487 4.7K DNP
R488 4.7K DNP
R479 0
R489 0
R490 4.7K
R491 4.7K
R492 845 1%
C723 0.01uF

3,7,12,33 I2C1_SCL
3,7,12,33 I2C1_SDA

PMBus Address offset to "+0"

34 VCORE_HOT_N

PLACE
THERMISTOR
NEAR L13&L14

R494 10K
R495 1% 3.4K
R497 2.87K 1%
R493 2.87K 1%
C732 100pF

R500 10K

R507 10K
R508 7.5K 1%

R509 75 — 3V3
C751 4.7uF

U56 — IR36021

22	VCC	VSEN1	2
9	VINSEN	VRTN1	3
12	EN1		
7	PGOOD1		
8	EN2		
1	PGOOD2		
16	SM_CLK		
15	SM_DIO		
14	SM_ALERT		
13	ADDR_PROT		
11	VRHOT_ICRIT		
31	RCSP1	PWM1A	17
32	RCSM1	ISEN1A	29
23	RCSM2	IRTN1A	30
24	RCSP2	PWM1B	18
5	TSEN	ISEN1B	27
4	RRES	IRTN1B	28
6	V18A	PWM2	19
		ISEN2	25
		IRTN2	26
		VSEN2	21
		VRTN2	20
		NC	10
		EPAD	33

VCORE_PWM1A
VCORE_ISEN1A
VCORE_IRTN1A
VCORE_PWM1B
VCORE_ISEN1B
VCORE_IRTN1B

R498 301 1%
R499 301 1%
R502 0
R503 0

34 VCORE_PGOOD
34 VCORE_HOT_N

U55 — IR3550 STUFF IR3553

7V0_DRV	3	VCC	
		VIN	18
		VIN	20
		VIN	21
		VIN	22
		VIN	23
7V0_DRV	25	PHSFLT	
	26	PWM	
	27	BBRK	
	30	IOUT	
	29	REFIN	
	28	LGND	
	31	TGND	
		BOOST	24
		SW	6
		SW	7
		GATEL1	5
		GATEL2	32
		CSIN+	2
		CSIN-	1
		PGND	4
		PGND	16

C710 0.22uF
R476 10K

12VF — L28 1uH — 12V

C704 0.1uF, C702 10uF, C705 10uF, C706 22uF, C707 22uF, C703 100uF 25V
C708 10uF, C709 10uF, C711 0.1uF, C712 0.01uF

R477 0 — C716 0.22uF
VCORE_SW1 — L29 215nH
R480 3.57K 1% — C718 0.22uF
C719 1000pF DNP — R485 1 DNP — Snubber Circuit
R483 301 1%
R484 301 1%

FP1007R3-R22-R
Irms = 61A
Isat@125 = 43A
DCR = 0.29mohm +/-5%

4 x POSCAP
2R5TPE470M7
ESR = 7mohm

C720 470uF 2.5V, C721 470uF 2.5V
C730 470uF 2.5V, C731 470uF 2.5V

U57 — IR3550 STUFF IR3553

7V0_DRV	3	VCC	
		VIN	18
		VIN	20
		VIN	21
		VIN	22
		VIN	23
7V0_DRV	25	PHSFLT	
	26	PWM	
	27	BBRK	
	30	IOUT	
	29	REFIN	
	28	LGND	
	31	TGND	
		BOOST	24
		SW	6
		SW	7
		GATEL1	5
		GATEL2	32
		CSIN+	2
		CSIN-	1
		PGND	4
		PGND	16

C722 0.22uF

12VF — C725 0.1uF, C726 10uF, C724 10uF, C727 22uF, C728 22uF, C729 100uF 25V

R496 0 — C733 0.22uF
VCORE_SW2 — L30 215nH
R501 3.57K 1% — C739 0.22uF
C740 1000pF DNP — R506 1 DNP — Snubber Circuit
R504 301 1%
R505 301 1%

FP1007R3-R22-R
Irms = 61A
Isat@125 = 43A
DCR = 0.29mohm +/-5%

COPPER PLANE
16 x 22uF,0805,6.3V
VCORE

C734 22uF, C735 22uF, C736 22uF, C737 22uF, C738 22uF
C741 22uF, C742 22uF, C743 22uF, C744 22uF, C745 22uF
C746 22uF, C747 22uF, C748 22uF, C749 22uF, C750 22uF

PowIRstage MOSFET Driver power supply

Make sure 7.0V supply is applied
after 3.3V is ready
7.0V supply is ramped down
before 3.3V supply

12V — C752 1uF — R510 49.9K 1% — R512 20.0K 1% — C754 2.2uF

U58 — MIC39102YM

12V	2	IN	
	1	EN	
	5	GND	
	6	GND	
	3	OUT	
	4	ADJ	
	7	GND	
	8	GND	

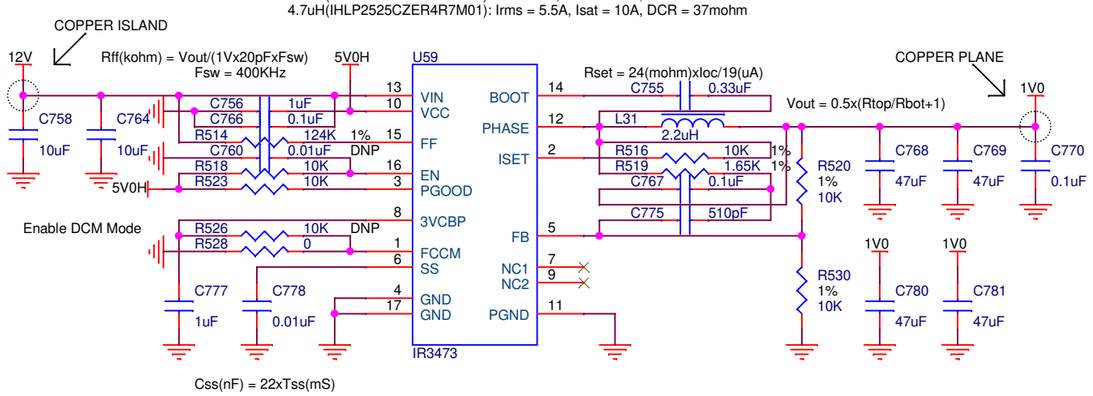
R511 46.4K 1% — 7V0_DRV
R513 10K 1%
C753 10uF

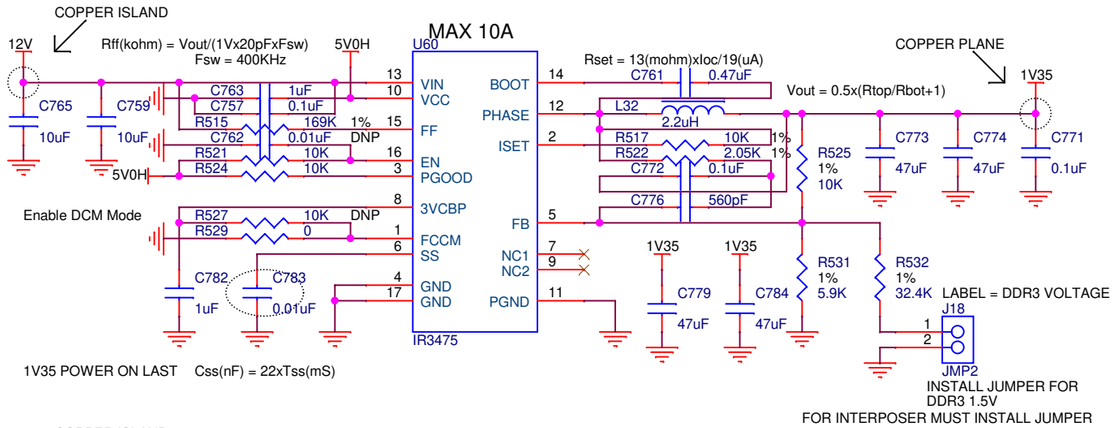
PROTO

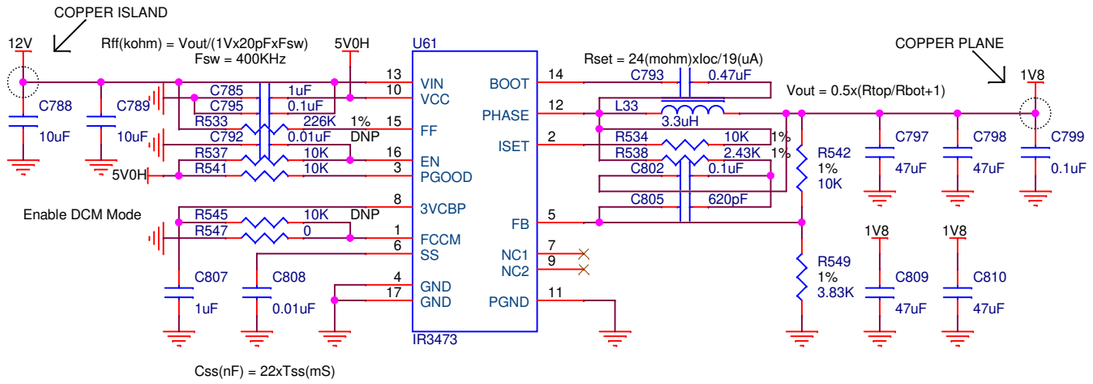
PPC Power Progress Community	Project ACB_0001_0		
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: CORE PWR	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 34 of 41	REV. 0 / Format A3

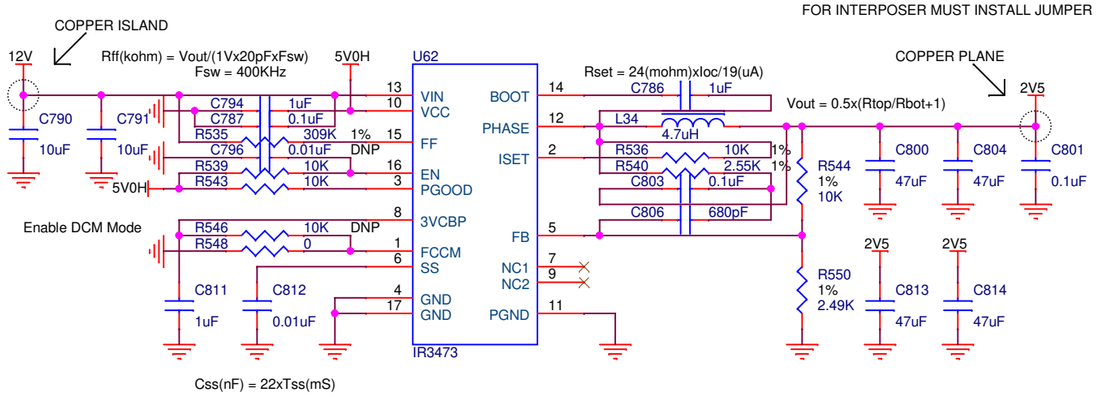
SYSTEM POWER CONVERTORs

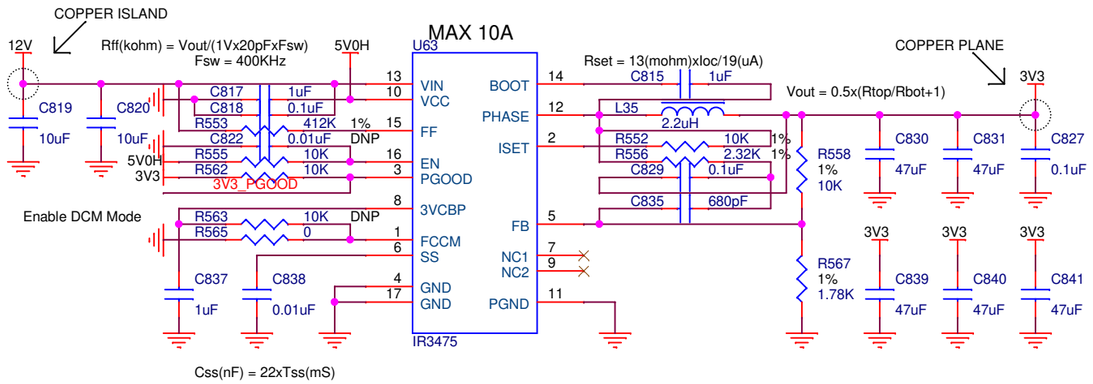
2.2uH(IHLP2525CZER2R2M01): Irms = 8A, Isat = 14A, DCR = 18mohm
3.3uH(IHLP2525CZER3R3M01): Irms = 6A, Isat = 13.5A, DCR = 28mohm
4.7uH(IHLP2525CZER4R7M01): Irms = 5.5A, Isat = 10A, DCR = 37mohm

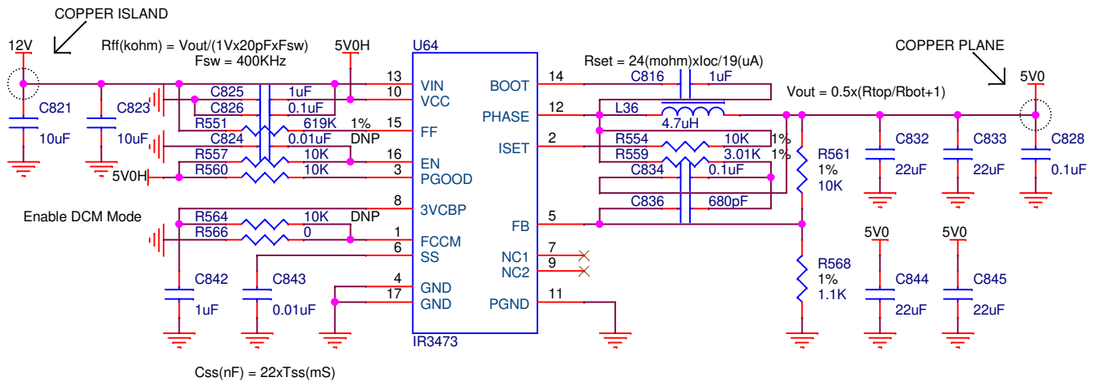




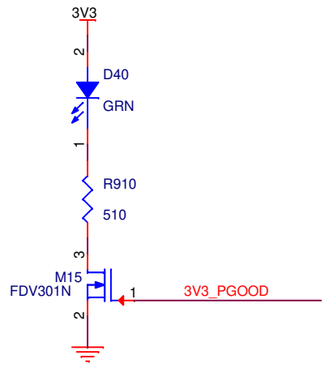








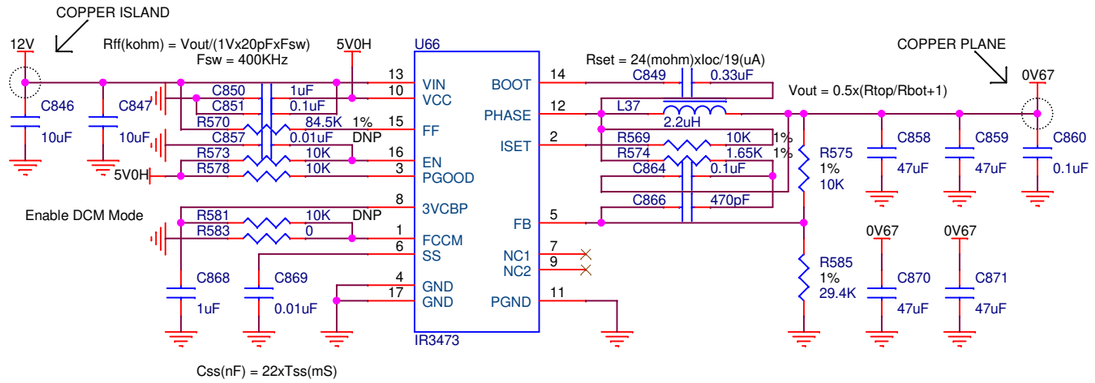
Caution: separate analog and power ground and make connection at GND plane

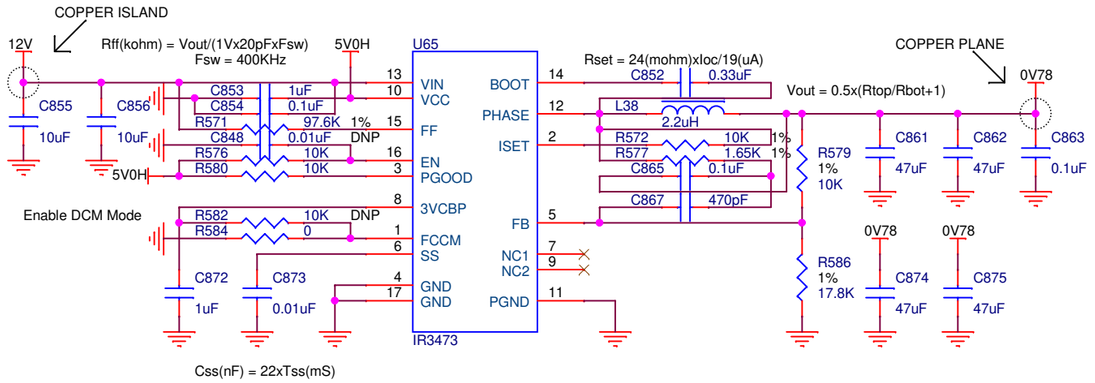


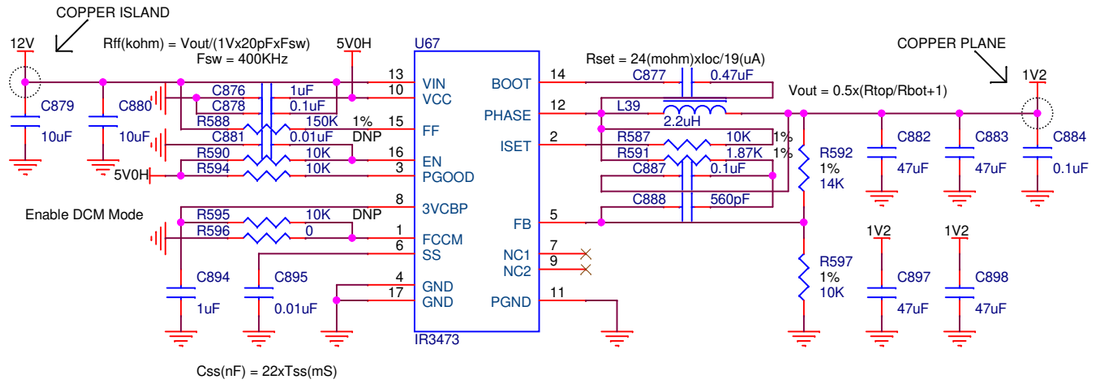
PROTO

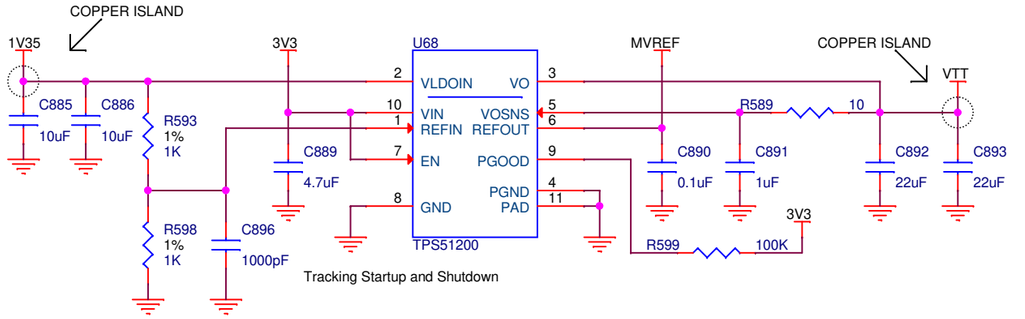
PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: OTHER PWR1		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 35 of 41	REV. 0	Format A3

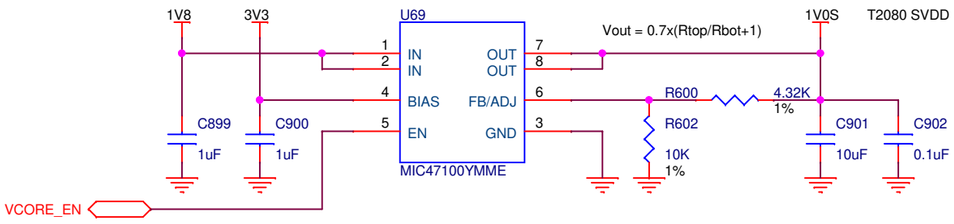
SYSTEM POWER CONVERTORs (cont.)

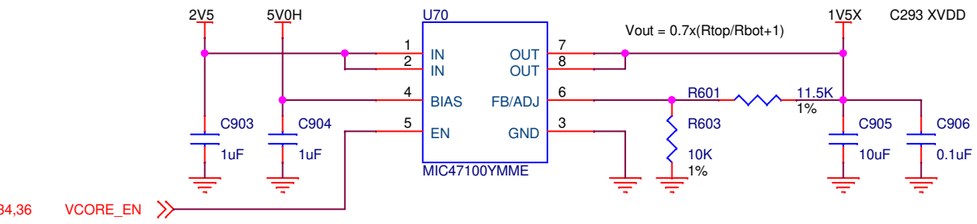


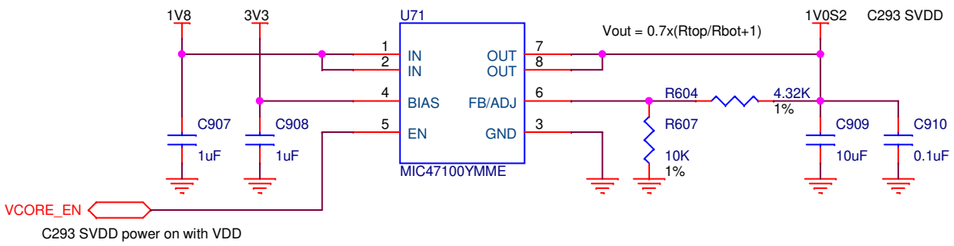


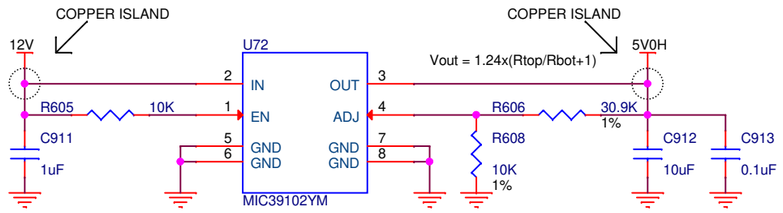






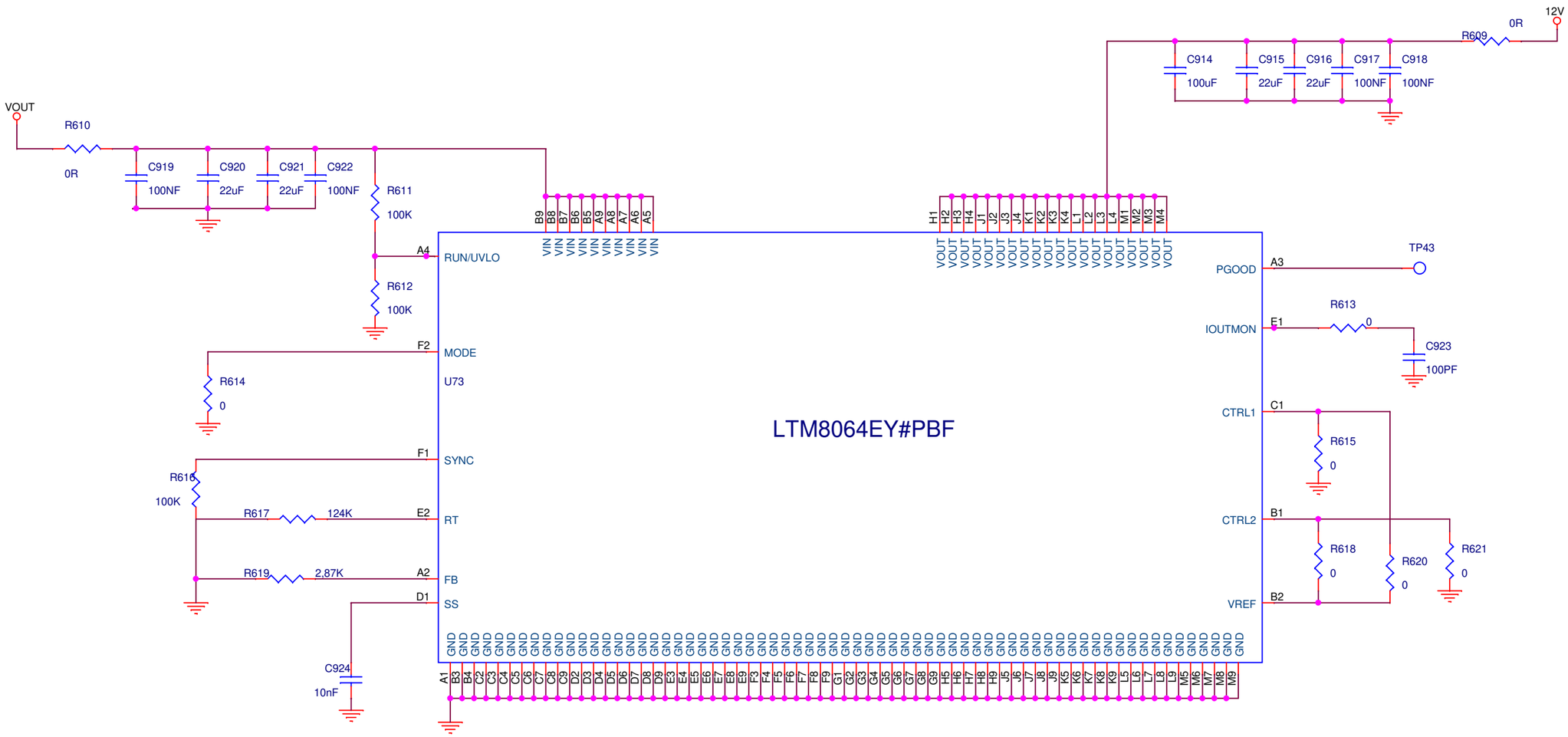






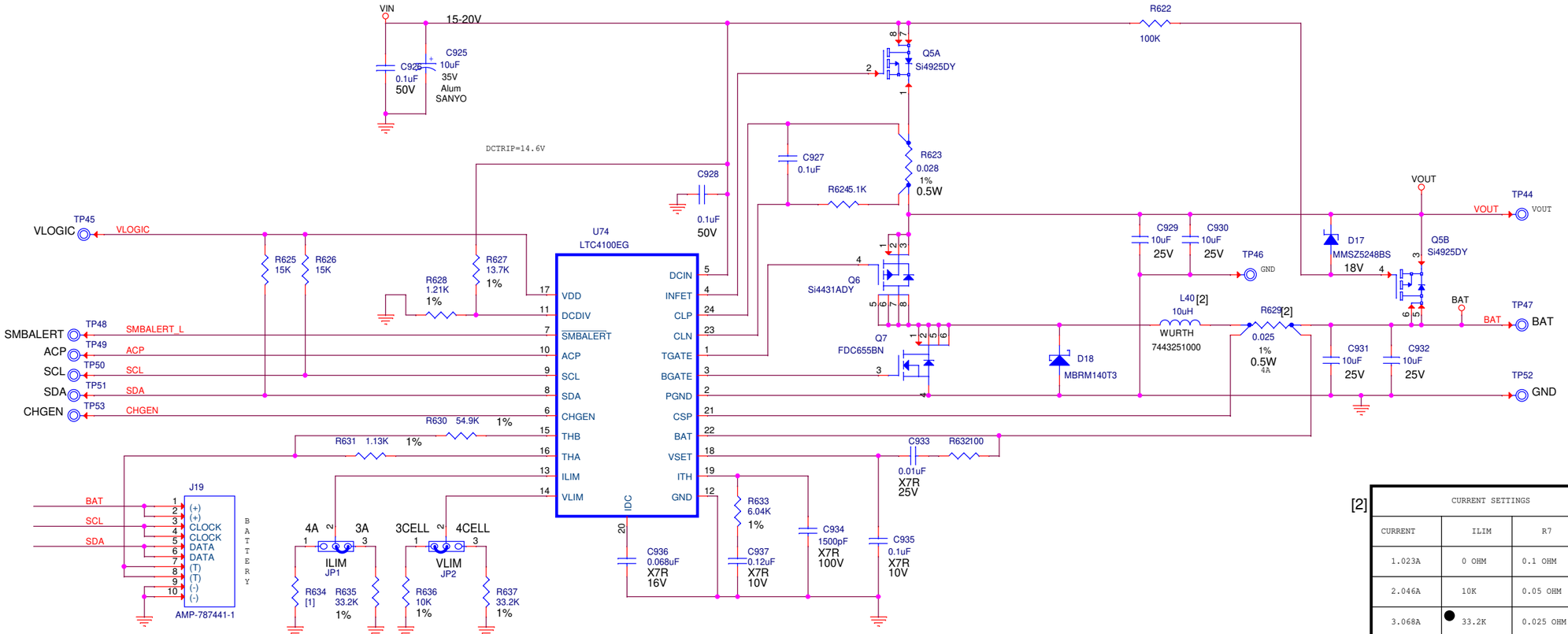
PROTO

PPC Power Progress Community	Project **ACB_0001_0**	
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: OTHER PWR2
Designed by:	Controlled by:	approved by:
PCB Code	BOM file	Sheet 36 of 41 / REV. 0 / Format A3



PROTO

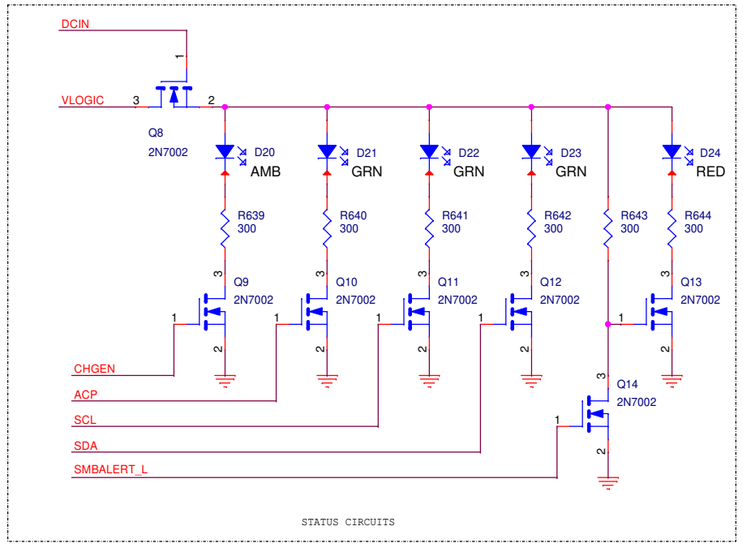
PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: MAIN POWER		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 37 of 41	REV. 0	Format A3

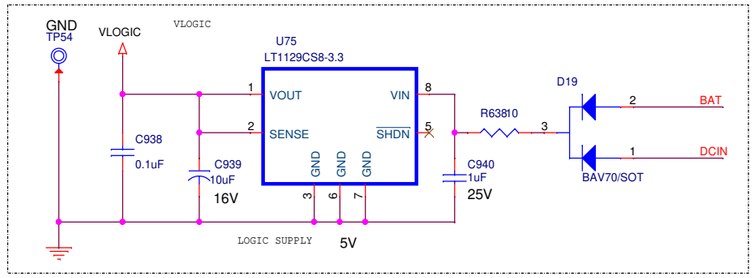


[2]

CURRENT SETTINGS				VOLTAGE SETTINGS	
CURRENT	ILIM	R7	L1	VOLTAGE	VLIM
1.023A	0 OHM	0.1 OHM	40uH	8.438V	0 OHM
2.046A	10K	0.05 OHM	20uH	12.646V	● 10K
3.068A	● 33.2K	0.025 OHM	10uH	16.870V	33.2K
N/A	N/A	N/A	N/A	21.062V	100K
4.094A	OPEN/VDD	0.025 OHM	10uH	32.758V	OPEN/VDD

● DEFAULT VALUE

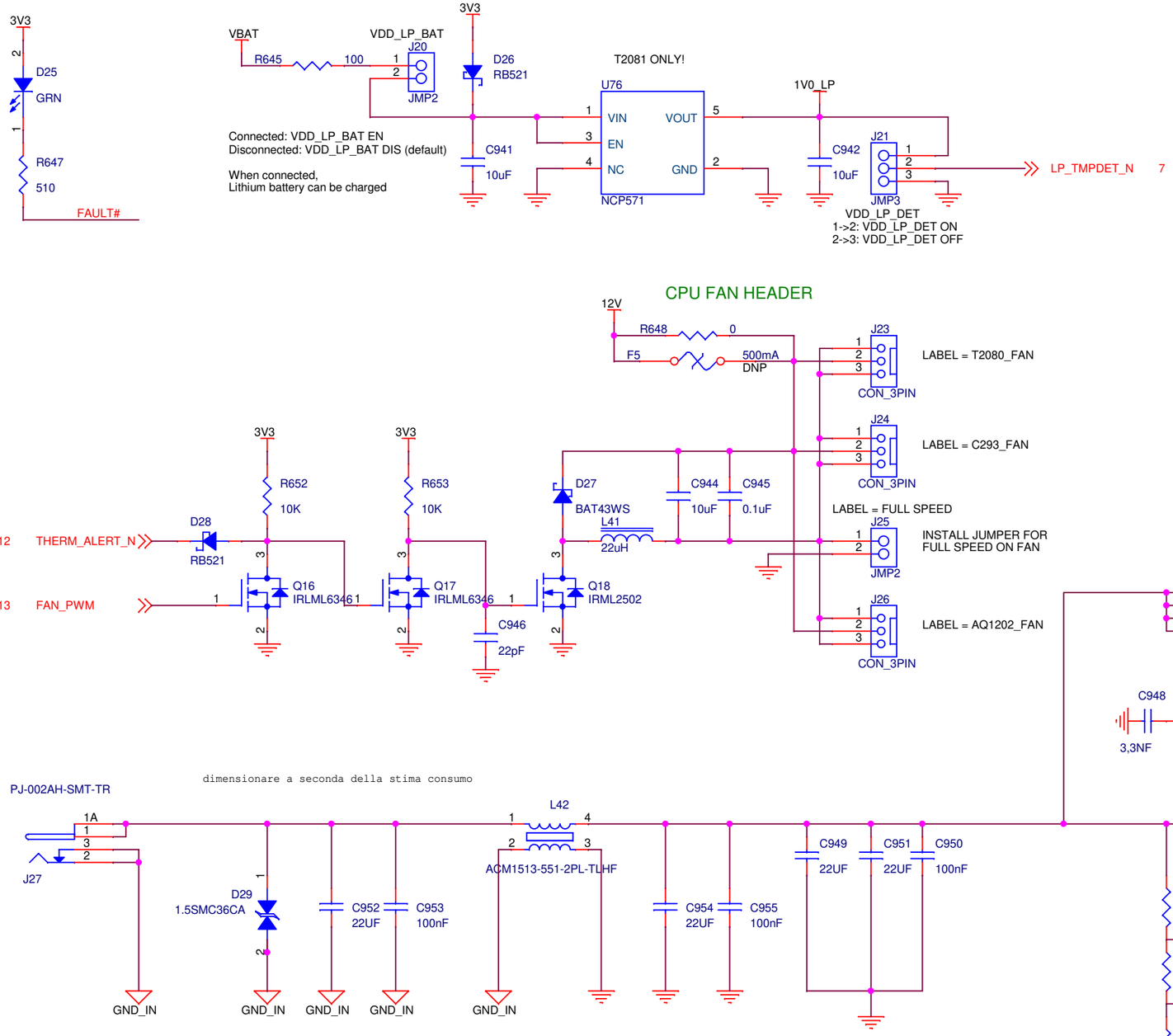




PROTO

PPC Power Progress Community	Project ACB_0001_0			
Creation Date: Wednesday, August 08, 2018	Last modify date: Wednesday, July 10, 2019	Page title: BATTERY CHARGE		
Designed by: <Author>	Controlled by: <Cheked by>	approved by: <Approved by>		
PCB Code	BOM file	Sheet 38 of 41	REV. 0	Format: Custom

SYSTEM POWER INPUT



PROTO

Power Progress Community	Project **ACB_0001_0**		
Creation Date: Wednesday, July 10, 2019	Last modify date:	Page title: PWR IN	
Designed by:	Controlled by:	approved by:	
PCB Code	BOM file	Sheet 39 of 41 / REV. 0	Format A3

PROTO

PPC Power Progress Community	Project **T2080PCIe**			
Creation Date Wednesday, July 10, 2019	Last modify date	Page title MECANICAL		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet of	REV. 0	Format B

CHANGE LIST

PROTO

PPC Power Progress Community	Project **ACB_0001_0**			
Creation Date: Wednesday, July 10, 2019	Last modify date	Page title: CHANGE LIST		
Designed by:	Controlled by:	approved by:		
PCB Code	BOM file	Sheet 41 of 41	REV. 0	Format B