CM9882A

7.1+2 CHANNEL HIGH-PERFORMANCE HDA CODEC

NOTICES

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REVISION HISTORY

Revision	Release Date	Summary
0.1	2009/08/26	First release.
0.2	2010/03/09	Formal release
1.0	2011/09/05	
1.1	2012/07/04	-update block diagram

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1. General Description

The CM9882A provides ten DAC channels that simultaneously support 7.1 sound playback, plus 2 channels of independent stereo sound output (multiple streaming) through the front panel stereo outputs. Three stereo ADC and one stereo digital microphone converter are integrated. The CM9882A incorporates Cmedia proprietary converter technology to achieve 108dB Signal-to-Noise ratio (SNR) playback (DAC) quality and 104dB SNR recording (ADC) quality, and is designed for Windows Vista premium desktop and laptop systems

All analog I/O are input and output capable, and headphone amplifiers are also integrated at six analog output ports. All analog I/Os can be re-tasked according to user's definitions.

Support for 16/20/24-bit SPDIF input and output with up to 192kHz sample rate offers easy connection of PCs to consumer electronic products such as digital decoders and speakers. The CM9882A also features secondary SPDIF-OUT output.

The CM9882A supports host/soft audio from the Intel ICH series chipset, and also from any other HDA compatible audio controller. With EAX/Direct Sound 3D compatibility, the CM9882A provides an excellent home entertainment package and game experience for PC users.

2. Features

2.1. Hardware Features

- High performance DACs with 108dB signal-to-noise ratio(A-weighting)
- High performance ADCs with 104dB signal-to-noise ratio (A-weighting).
- Meets Microsoft WLP3.10 and future WLP audio requirements
- Ten DAC channels support 16/20/24-bit PCM format for 7.1 sound playback, plus 2 channels of concurrent independent stereo sound output (multiple streaming) through the front panel output
- Three stereo ADC support 16/20/24-bit PCM format, multiple stereo recording
- All DACs supports 44.1k/48k/88.2k/96k/176.4k/192kHz sample rate
- ADC supports 44.1k/48k/88.2k/96k/176.4k/192kHz sample rate
- Primary 16/20/24-bit SPDIF-OUT supports 32k/44.1k/48k/88.2k/96k/192kHz sample rate
- Secondary 16/20/24-bit SPDIF-OUT supports 32k/44.1k/48k/88.2k/96k/192kHz sample rate
- 16/20/24-bit SPDIF-IN supports 32k/44.1k/48k/96k/192kHz sample rate
- All analog jacks are stereo input and output re-tasking
- Software selectable boost gain (+10/+20/+30dB) for analog microphone input
- High-quality analog differential CD input
- Software selectable 2.5V/3.2V/4.0V VREFOUT
- Two jack detection pins each designed to detect up to 4 jacks plugging
- Supports analog GPIO2 to be jack detection for CD input which is used as 9th analog port
- Supports legacy analog mixer architecture
- Up to 3 GPIOs (General Purpose Input and Output) for customized applications. GPIO0 and GPIO1 share pin with DMIC-CLK and DMIC-DATA.
- Supports mono and stereo digital microphone interface (pins shared with GPIO0 and GPIO1)
- Supports anti-pop mode when analog power AVDD is on and digital power is off.
- Hardware Zero-Detect output volume control
- 1dB per step output volume and input volume control
- Supports 3.3V digital core power, 1.5V or 3.3V digital I/O power for HD Audio link, and 5.0V analog power
- 48-pin LQFP ‘Green’ package

3. Block Diagram

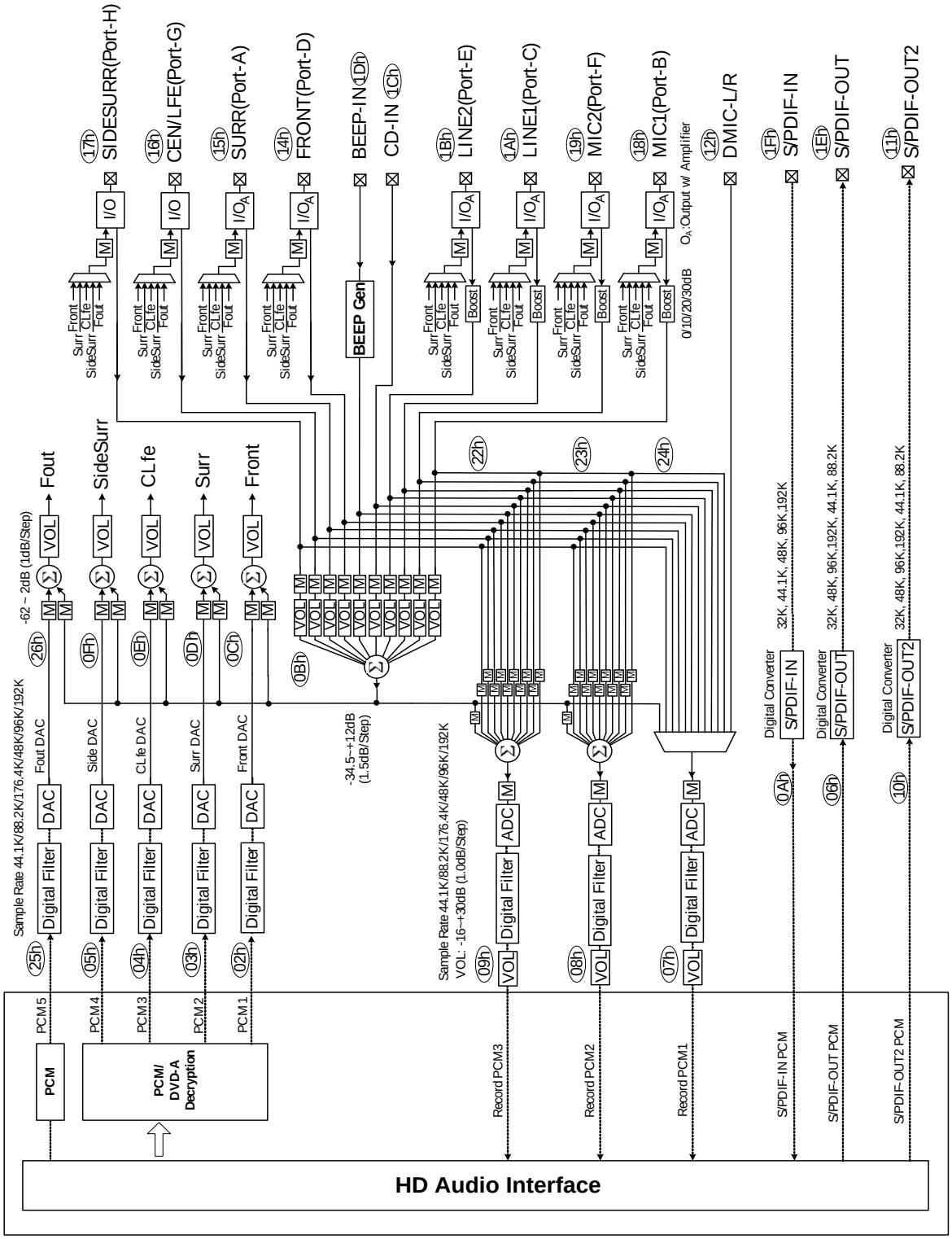


Figure 1. Block Diagram

4. Pin Assignments

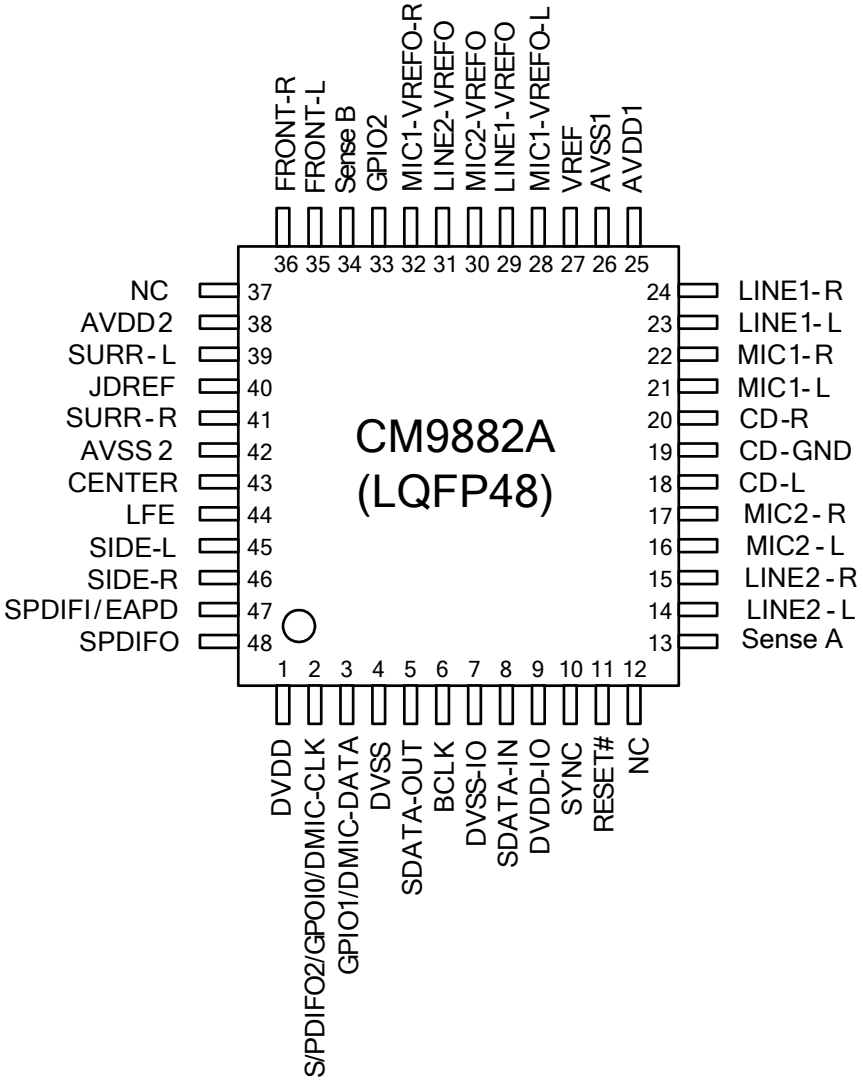


Figure 2 Pin Assignments

4.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 2. The silicon version and step numbers are shown in the location marked 'V' and 'S'.

5. Pin Descriptions

Table 1. Pin Descriptions

Name	Type	Pin	Description	Characteristic Definition
DVDD	P	1	Digital Core Power	Digital VDD (3.3V)
GPIO0/ DMIC-CLK/ SPDIF-OUT2	IO*	2	General Purpose Input/Output/ Digital MIC Clock Output/ Secondary SPDIF Out to HDMI Transmitter	Digital Input: Schmitt trigger, V_{IL} =0.4*DVDD, V_{IH} =0.6*DVDD, internal 50K pull up Digital Output: V_{OL} <0.1*DVDD, V_{OH} >0.9*DVDD 6mA@75Ω Output driving
GPIO1/ DMIC-DATA	IO*	3	General Purpose Input/Output/ Digital MIC Stereo Channel Input	Digital Input: Schmitt trigger, V_{IL} =0.4*DVDD, V_{IH} =0.6*DVDD, internal 50K pull up Digital Output: V_{OL} <0.1*DVDD, V_{OH} >0.9*DVDD
DVSS	G	4	Digital Ground	Digital ground
SDATA-OUT	I	5	Serial TDM Data Input	Digital Input: Schmitt trigger, V_{IL} =0.4*DVDD-IO, V_{IH} =0.6*DVDD-IO
BITCLK	I	6	24MHz Clock	Digital Input: Schmitt trigger, V_{IL} =0.4*DVDD-IO, V_{IH} =0.6*DVDD-IO
DVSS	G	7	Digital Ground	Digital ground
SDATA-IN	IO	8	Serial TDM Data Output	Digital Input: Schmitt trigger, V_{IL} =0.4*DVDD-IO, V_{IH} =0.6*DVDD-IO Digital Output: V_{OL} <0.1*DVDD-IO, V_{OH} >0.9*DVDD-IO
DVDD-IO	P	9	Digital Power for HD Link	Scalable Digital VDD (1.5V~3.3V)
SYNC	I	10	48KHz Frame SYNC Signal	Digital Input: Schmitt trigger, V_{IL} =0.4*DVDD-IO, V_{IH} =0.6*DVDD-IO
RESET#	I	11	H/W Reset Input	Digital Input: Schmitt trigger, V_{IL} =0.4*DVDD-IO, V_{IH} =0.6*DVDD-IO
NC	-	12	Not Connected	
Sense A	-	13	Jack Detect for Resistor Network	Connect {5.1K, 10K, 20K, 39.2K} with 1% accuracy
LINE2-L	IO	14	Analog Input and Output with Multiple Function – Left Channel	Analog I/O, default 2nd line input. Recommended to be re-tasking port at front panel
LINE2-R	IO	15	Analog Input and Output with Multiple Function – Right Channel	Analog I/O, default 2nd line input. Recommended to be re-tasking port at front panel
MIC2-L	IO	16	Analog Input and Output with Multiple Function – Left Channel	Analog I/O, default 2nd mic input. Recommended to be re-tasking port at front panel
MIC2-R	IO	17	Analog Input and Output with Multiple Function – Right Channel	Analog I/O, default 2nd mic input. Recommended to be re-tasking port at front panel
CD-L	I	18	CD Input Left Channel	Analog Input: 1.6Vrms of full-scale input
CD-GND	I	19	CD Input Reference Ground	Analog Input: 1.6Vrms of full-scale input
CD-R	I	20	CD Input Right Channel	Analog Input: 1.6Vrms of full-scale input

Name	Type	Pin	Description	Characteristic Definition
MIC1-L	IO	21	Analog Input and Output with Multiple Function – Left Channel	Analog I/O, default 1st mic input. Recommended to be microphone input at rear panel
MIC1-R	IO	22	Analog Input and Output with Multiple Function – Right Channel	Analog I/O, default 1st mic input. Recommended to be microphone input at rear panel
LINE1-L	IO	23	Analog Input and Output with Multiple Function – Left Channel	Analog I/O, default 1st line input. Recommended to be line level input at rear panel
LINE1-R	IO	24	Analog Input and Output with Multiple Function – Right Channel	Analog I/O, default 1st line input. Recommended to be line level input at rear panel
AVDD1	P	25	Analog Power for Mixer & Amp	Analog VDD (5.0V)
AVSS1	G	26	Analog Ground for Mixer & Amp	Analog GND
VREF	-	27	2.5V Reference Voltage	1μf capacitor to analog ground
VREFO-L	O	28	Bias Voltage for MIC1	Analog Output: 2.5V/3.2V/4.0V reference voltage
VREFO	O	29	Bias Voltage for LINE1	Analog Output: 2.5V/3.2V/4.0V reference voltage
VREFO	O	30	Bias Voltage for MIC2	Analog Output: 2.5V/3.2V/4.0V reference voltage
VREFO	O	31	Bias Voltage for LINE2	Analog Output: 2.5V/3.2V/4.0V reference voltage
VREFO-R	O	32	Secondary Bias Voltage for MIC1	Analog Output: 2.5V/3.2V/4.0V reference voltage
GPIO2	IO	33	General Purpose Input/Output Power by AVDD	Analog Input: Schmitt trigger, V_{IL} =0.4*AVDD , V_{IH} =0.6*AVDD; Floating Analog Output: V_{OL} <0.1*AVDD, V_{OH} >0.9*AVDD
Sense B	-	34	Jack Detect for Resistor Network	Connect {5.1K, 10K, 20K, 39.2K} with 1% accuracy
FRONT-L	IO	35	Analog Input and Output – Left	Analog I/O, default front channel output.
FRONT-R	IO	36	Analog Input and Output – Right	Analog I/O, default front channel output.
NC	-	37	Not Connected	Leave this pin be floated.
AVDD2	P	38	Analog Power for DAC and ADC	Analog VDD (5.0V)
SURR-L	IO	39	Analog Input and Output – Left	Analog I/O, default surround channel.
JDREF	-	40	Reference for Jack Detect	20K, 1% resistor to AGND
SURR-R	IO	41	Analog Input and Output – Right	Analog I/O, default surround channel.
AVSS2	G	42	Analog Ground for DAC & ADC	Analog GND
CENTER	IO	43	Analog Input and Output – Left	Analog I/O, default center channel.
LFE	IO	44	Analog Input and Output – Right	Analog I/O, default LFE channel.
SIDE-L	IO	45	Analog Input and Output – Left	Analog I/O, default side channel.
SIDE-R	IO	46	Analog Input and Output – Right	Analog I/O, default side channel.
SPDIF-IN/ EAPD	IO	47	SPDIF Input/ External Amplifier Power Down	Digital Input: Schmitt trigger (5V tolerance), V_{IL} =0.44*DVDD, V_{IH} =0.56*DVDD Digital Output: V_{OL} <0.1*DVDD, V_{OH} >0.9*DVDD
SPDIF-OUT	O	48	Primary SPDIF Out	Digital Output: V_{OL} <0.1*DVDD, V_{OH} >0.9*DVDD 10mA@75Ω Output driving
				Total: 48 Pins

Note: Pins 2 and 3 have multiple functions. Their default operation is as GPIOs. They functions as digital MIC pins when the configuration register of the digital MIC pin widget is enabled, and exclusively function as secondary SPDIF-OUT when the configuration register of the SPDIF-OUT2 pin widget is enabled.

6. High Definition Audio Link Protocol

6.1. Link Signals

The High Definition Audio (HDA) link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 3 shows the basic concept of the HDA link protocol.

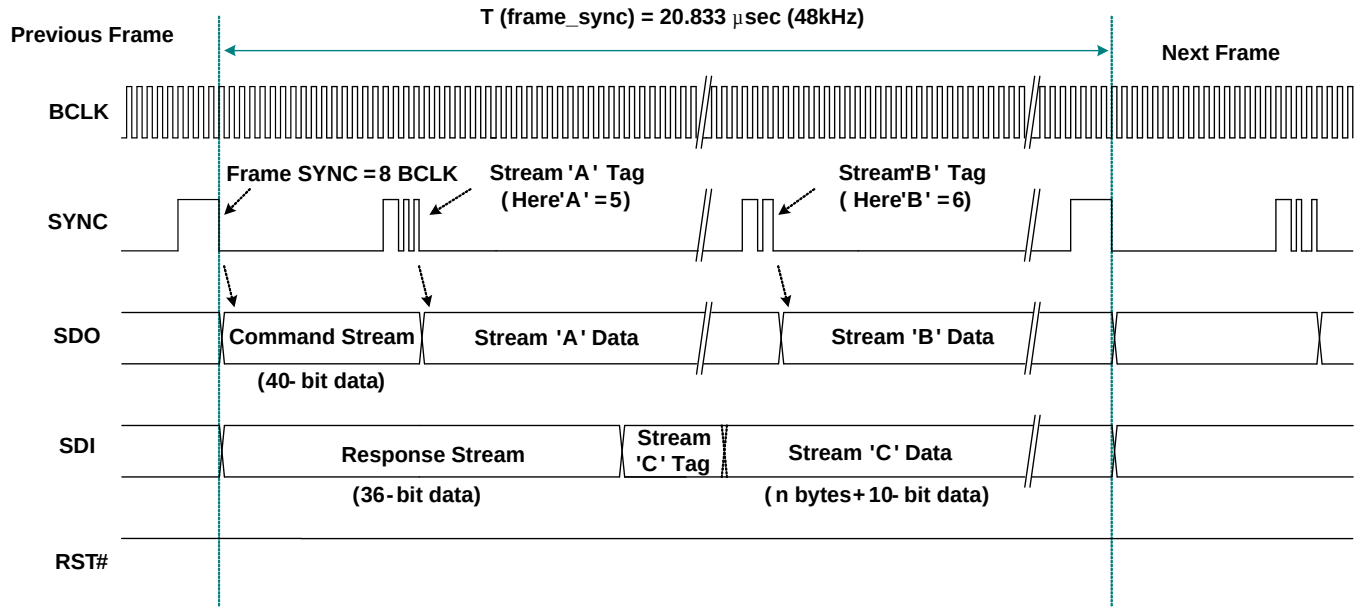


Figure 3. HDA Link Protocol

6.1.1. Signal Definitions

Table 2. Link Signal Definitions

Item	Description
BCLK	24.0MHz bit clock sourced from the HDA controller and connecting to all codecs
SYNC	48kHz signal used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs
SDO	Serial data output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported
SDI	Serial data input signal driven by the codec. This is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI, and up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID
RST#	Active low reset signal. Asserted to reset the codec to default power on state. RST# is sourced from the HDA controller and connects to all codecs

Table 3. HDA Signal Definitions

Signal Name	Source	Type for Controller	Description
BCLK	Controller	Output	Global 24.0MHz bit clock
SYNC	Controller	Output	Global 48kHz Frame Sync and outbound tag signal
SDO	Controller	Output	Serial data output from the controller
SDI	Codec/Controller	Input/Output	Serial data input from codec. Weakly pulled down by the controller
RST#	Controller	Output	Global active low reset signal

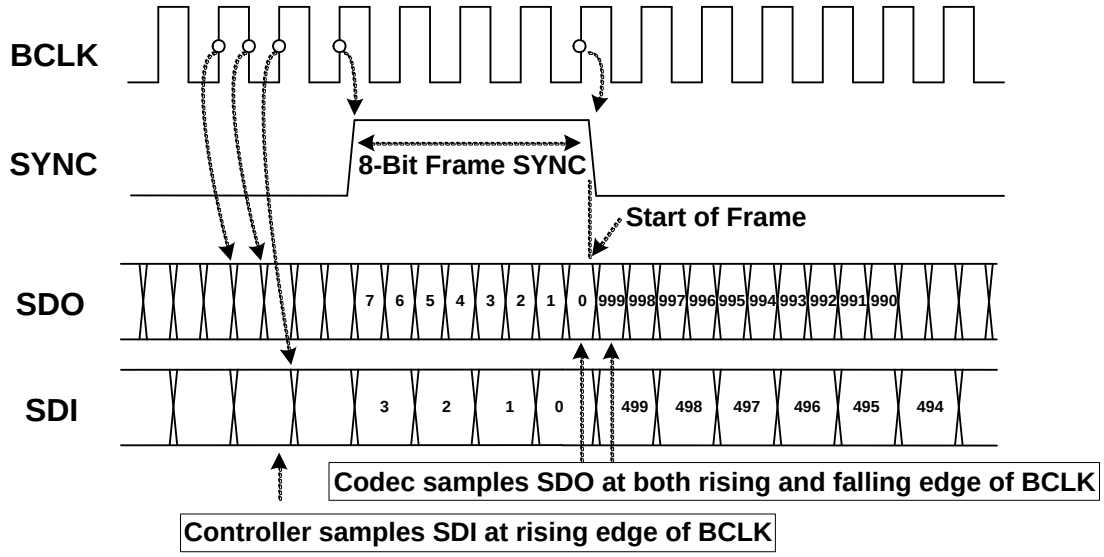


Figure 4. Bit Timing

6.1.2. Signaling Topology

The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RST#, BCLK, SYNC, SDO0, and SDO1 are driven by controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 5 shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 6.2 Frame Composition, page 10 describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 5 can be implemented concurrently in an HDA system. The CM9882A is designed to receive a single SDO stream.

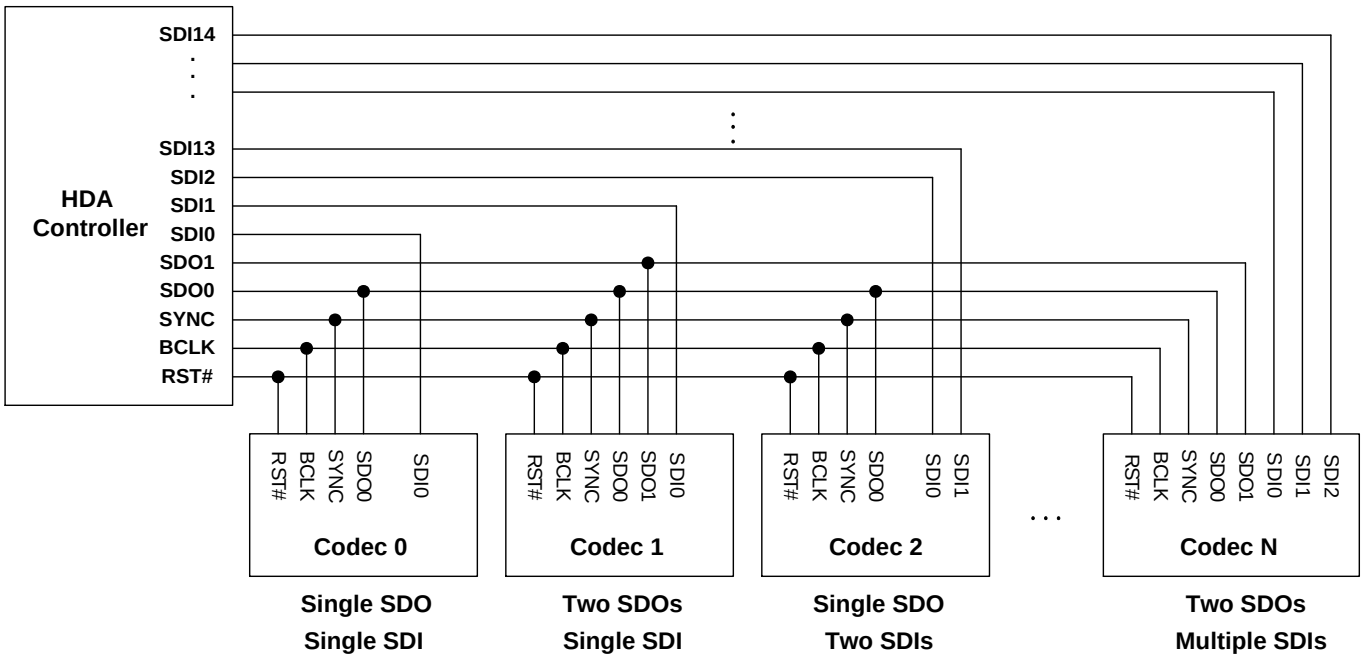


Figure 5. Signaling Topology

6.2. Frame Composition

6.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be two blocks in the same stream to carry 96kHz samples (Figure 6).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-bit preamble and 4-bit stream ID (Figure 7).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

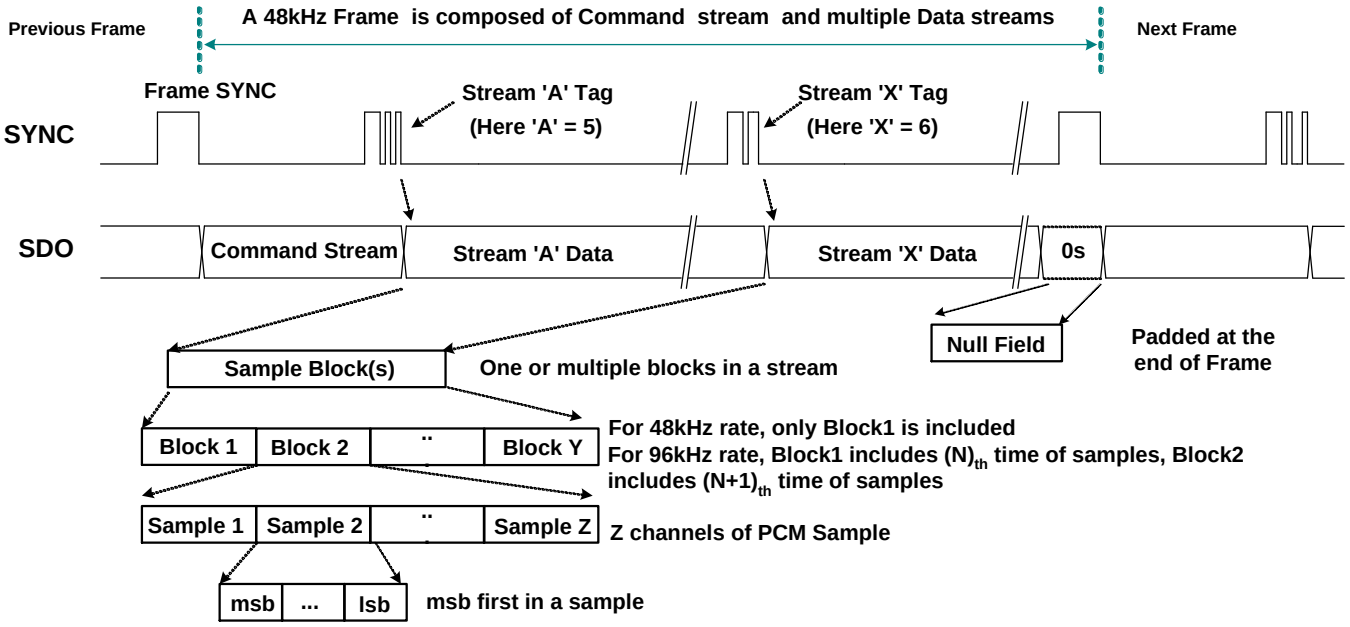


Figure 6. SDO Outbound Frame

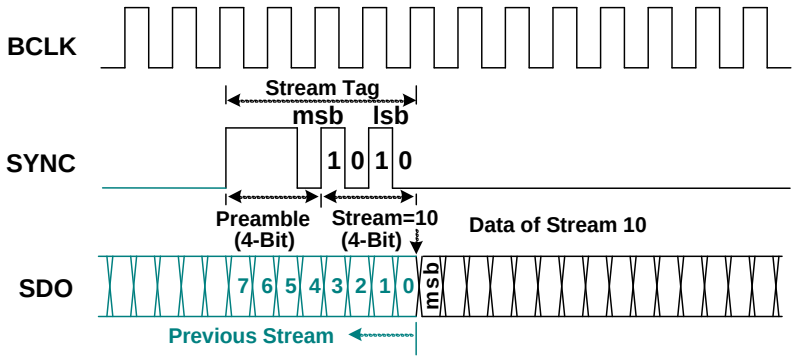


Figure 7. SDO Stream Tag is Indicated in SYNC

6.2.2. Outbound Frame – Multiple SDOs

The HDA controller allows two SDO signals to be used to stripe outbound data, completing transmission in less time to get more bandwidth. If software determines the target codec supports multiple SDO capability, it enables the 'Stripe Control' bit in the controller's Output Stream Control Register to initiate a specific stream (Stream 'A' in Figure 8) to be transmitted on multiple SDOs. In this case, the MSB of the data stream is always carried on SDO0, the second bit on SDO1 and so forth.

SDO1 is for transmitting a striped stream. The codec does not support multiple SDOs connected to SDO0.

To guarantee all codecs can determine their corresponding stream, the command stream is not striped. It is always transmitted on SDO0, and copied on SDO1.

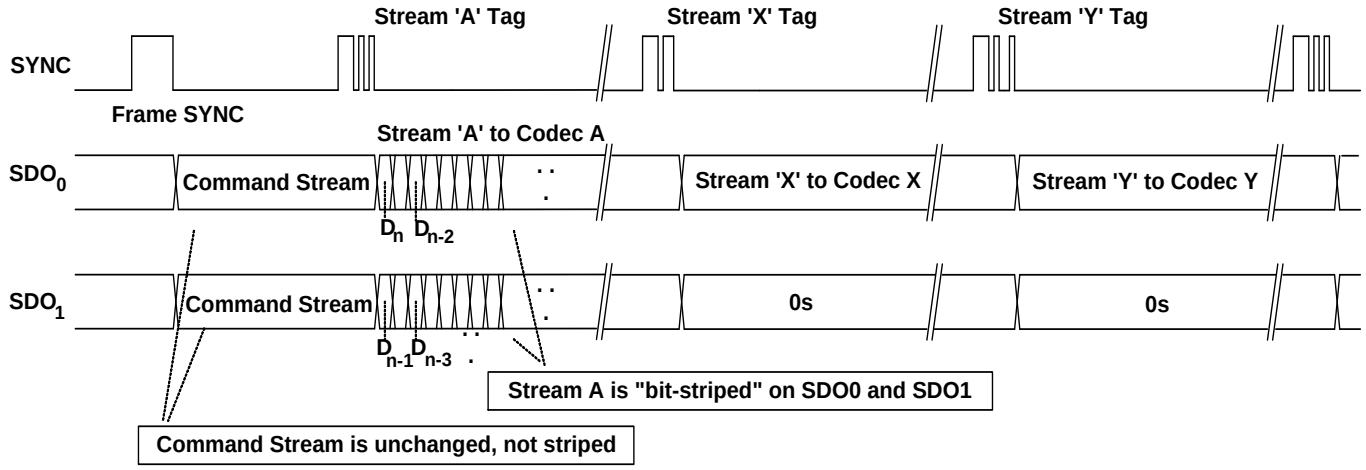


Figure 8. Striped Stream on Multiple SDOs

6.2.3. Inbound Frame – Single SDI

An Inbound Frame – A single SDI is composed of one 36-bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), the SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK.

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-bit stream tag, one 6-bit data length, and n-bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 10).

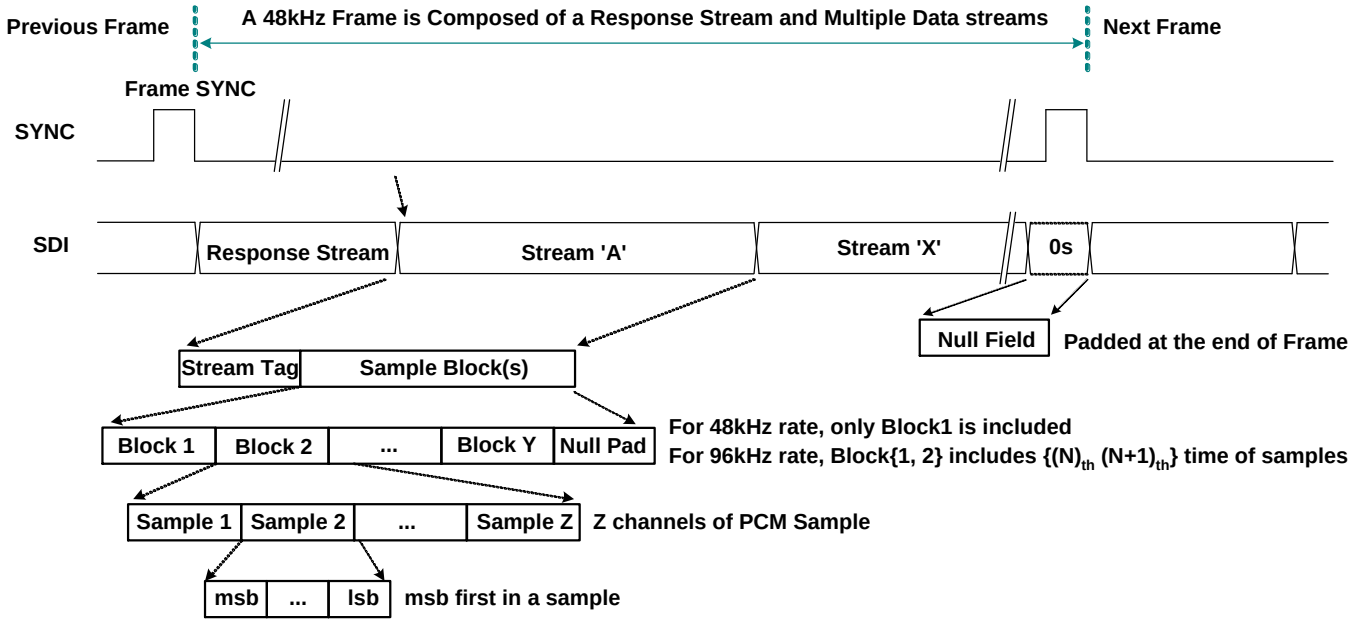


Figure 9. SDI Inbound Stream

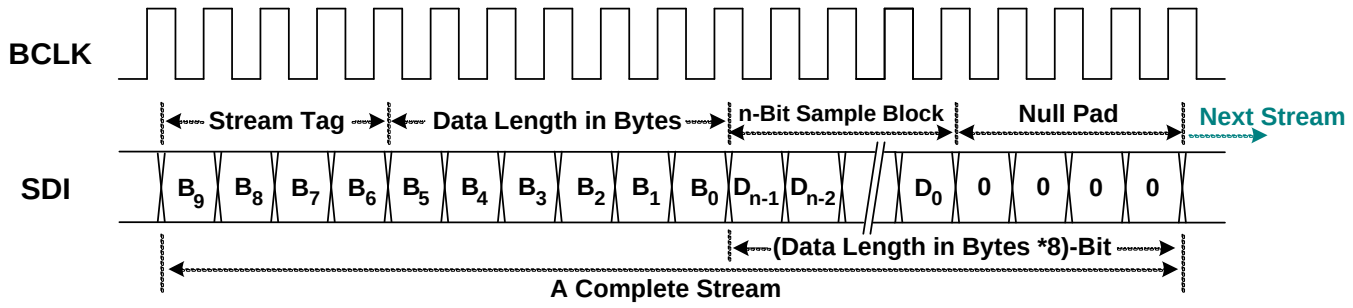


Figure 10. SDI Stream Tag and Data

6.2.4. Inbound Frame – Multiple SDIs

A codec can deliver data to the controller on multiple SDIs to achieve higher bandwidth. If an inbound stream exceeds the data transfer limits of a single SDI, the codec can divide the data into separate SDI signals, each of which operate independently, with different stream numbers at the same frame time. This is similar to having multiple codecs connected to the controller. The controller samples the divided stream into separate memory with multiple DMA descriptors, then software re-combines the divided data into a meaningful stream.

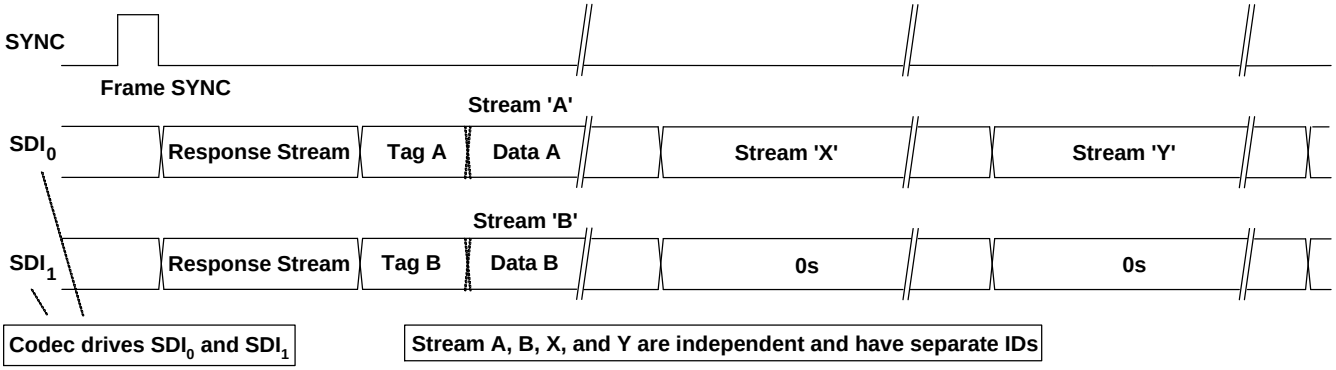


Figure 11. Codec Transmits Data Over Multiple SDIs

6.2.5. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable rates of sample are delivered in multiple or sub-multiple rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 4, page 14, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaving n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 5, page 14, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames.

The cadence '12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)' interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence AND interleave n empty frames. Rates in multiples (n) of 44.1kHz applying this cadence contain n sample blocks in the non-empty frame AND interleave an empty frame between non-empty frames (Table 6, 15).

Table 4. Defined Sample Rate and Transmission Rate

(Sub) Multiple	48kHz Base	44.1kHz Base
1/6	8kHz (1 sample block every 6 frames)	-
1/4	12kHz (1 sample block every 4 frames)	11.025kHz (1 sample block every 4 frames)
1/3	16kHz (1 sample block every 3 frames)	-
1/2	-	22.05kHz (1 sample block every 2 frames)
2/3	32kHz (2 sample blocks every 3 frames)	-
1	48kHz (1 sample block per frame)	44.1kHz (1 sample block per frame)
2	96kHz (2 sample blocks per frame)	88.2kHz (2 sample blocks per frame)
4	192kHz (4 sample blocks per frame)	176.4kHz (4 sample blocks per frame)

Table 5. 48kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence	Description
8kHz	YNNNNN (repeat)	One sample block is transmitted in every 6 frames
12kHz	YNNN (repeat)	One sample block is transmitted in every 4 frames
16kHz	YNN (repeat)	One sample block is transmitted in every 3 frames
32kHz	Y^2NN (repeat)	Two sample blocks are transmitted in every 3 frames
48kHz	Y (repeat)	One sample block is transmitted in every frame
96kHz	Y^2 (repeat)	Two sample blocks are transmitted in each frame
192kHz	Y^4 (repeat)	Four sample blocks are transmitted in each frame

N: No sample block in a frame

Y: One sample block in a frame

Y^x: X sample blocks in a frame

Table 6. 44.1kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence
11.025kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-} (repeat)
22.05kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-} (repeat)
44.1kHz	12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)
88.2kHz	12^2-11^2-11^2-12^2-11^2-11^2-12^2-11^2-11^2-12^2-11^2-11^2-11^2- (repeat)
174.4kHz	12^4-11^4-11^4-12^4-11^4-11^4-12^4-11^4-11^4-12^4-11^4-11^4-11^4- (repeat)

11.025kHz: {12}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN

{11}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN

{ - }=NNNN

22.050kHz: {12}=YNYNYNYNYNYNYNYNYNYNYNYN

{11}=YNYNYNYNYNYNYNYNYNYNYN

{ - }=NN

44.1kHz 12- =Contiguous 12 frames containing 1 sample blocks each, followed by one frame with no sample block.

88.2kHz 12^2- =Contiguous 12 frames containing 2 sample blocks each, followed by one frame with no sample block.

174.4kHz 12^4- =Contiguous 12 frames containing 4 sample blocks each, followed by one frame with no sample block.

6.3. Reset and Initialization

There are two types of reset within an HDA link:

- Link Reset. Generated by assertion of the RST# signal, all codecs return to their power on state
- Codec Reset. Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

- Link Reset
- Codec Reset
- Codec changes its power state (for example, hot docking a codec to an HDA system)

6.3.1. Link Reset

A link reset may be caused by 3 events:

1. The HDA controller asserts RST# for any reason (power up, or PCI reset)

2. Software initiates a link reset via the 'CRST' bit in the Global Control Register (GCR) of the HDA controller

3. Software initiates power management sequences. Figure 12, shows the 'Link Reset' timing including the 'Enter' sequence (❶~❺) and 'Exit' sequence (❻~❾)

Enter 'Link Reset':

❶ Software writes a 0 to the 'CRST' bit in the Global Control Register of the HDA controller to initiate a link reset

❷ When the controller completes the current frame, it does not signal the normal 8-bit frame SYNC at the end of the frame

❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low

❹ The controller asserts the RST# signal to low, and enters the 'Link Reset' state

❺ All link signals driven by controller and codecs should be tri-state by internal pull low resistors

Exit from 'Link Reset':

❻ If BCLK is re-started for any reason (codec wake-up event, power management, etc.)

❼ Software is responsible for de-asserting RST# after a minimum of 100µs BCLK running time (the 100µsec provides time for the codec PLL to stabilize)

❽ Minimum of 4 BCLK after RST# is de-asserted, the controller starts to signal normal frame SYNC

❾ When the codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC, it means the codec requests an initialization sequence)

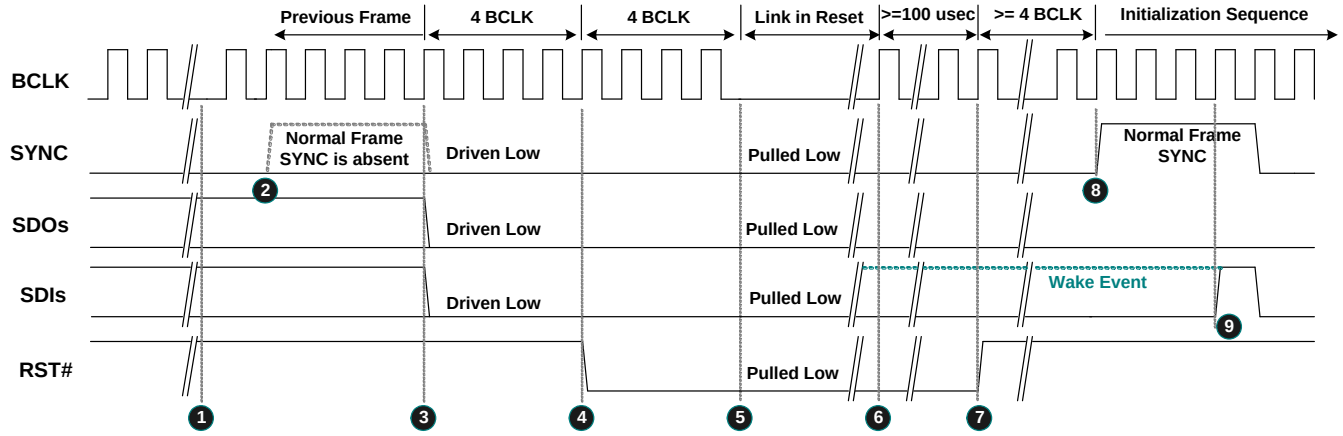


Figure 12. Link Reset Timing

6.3.2. Codec Reset

A 'Codec Reset' is initiated via the codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence is requested.

6.3.3. Codec Initialization Sequence

❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller

❷ The codec will stop driving the SDI during this turnaround period

❸❹❺❻ The controller drives SDI to assign a CAD to the codec

❼ The controller releases the SDI after the CAD has been assigned

❽ Normal operation state

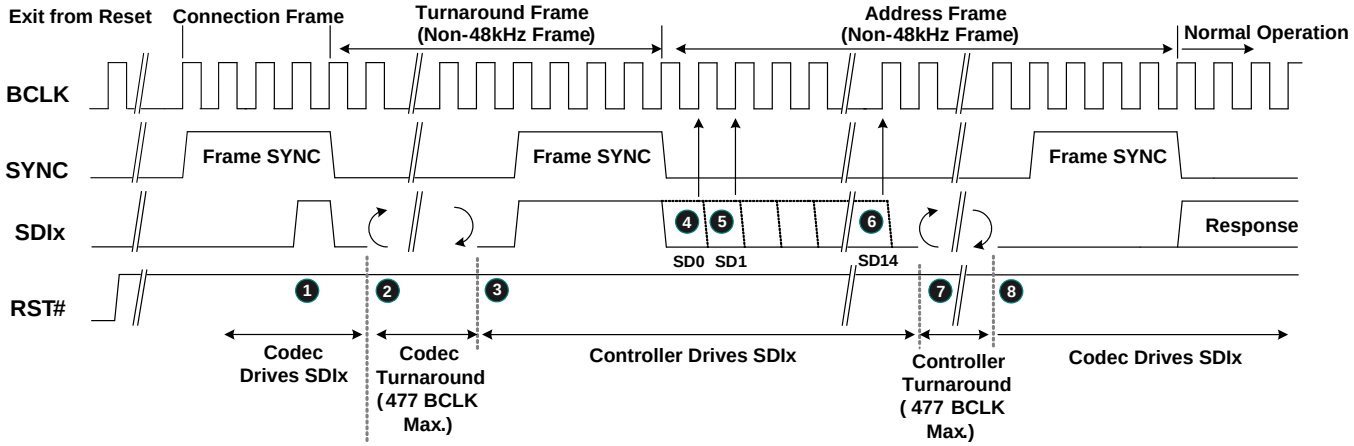


Figure 13. Codec Initialization Sequence

6.4. Verb and Response Format

6.4.1. Command Verb Format

There are two types of verbs: one with 4-bit identifiers (4-bit verbs) and 16-bits of data, the other with 12-bit identifiers (12-bit verbs) and 8-bits of data. Table 7 shows the 4-bit verb structure of a command stream sent from the controller to operate the codec. Table 8 is the 12-bit verb structure that gets and controls parameters in the codec.

Table 7. 40-Bit Commands in 4-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:16]	Bit [15:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

Table 8. 40-Bit Commands in 12-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:8]	Bit [7:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

Table 9. Verbs Supported by the CM9882A (Y=Supported)

Supported Verb	Get Verb	Set Verb	Root Node	Audio Function Group	Modem Function Group	HDMI Function Group	Vendor Define Group	Audio Out Converter	Audio In Converter	Pin Widget	Sum Widget	Selector Widget	Power Widget*1	Volume Knob	Beep Generator	Vendor Defined Widget
Get parameter	F00	-	Y	Y	-	-	-	Y	Y	Y	Y	Y	Y	Y	Y	Y
Connection Select	F01	701	-	-	-	-	-	-	Y	Y	-	Y	-	-	-	-
Get Connection List Entry	F02	-	-	-	-	-	-	-	Y	Y	Y	Y	-	-	-	-
Processing State	F03	703	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Coefficient Index	D-	5-	-	-	-	-	-	-	-	-	-	-	-	-	-	Y
Processing Coefficient	C-	4-	-	-	-	-	-	-	-	-	-	-	-	-	-	Y
Amplifier Gain/Mute	B-	3-	-	-	-	-	-	-	Y	Y	Y	-	-	-	-	-
Stream Format	A-	2-	-	-	-	-	-	Y	Y	-	-	-	-	-	-	-
Digital Converter 1	F0D	70D	-	-	-	-	-	Y	Y	-	-	-	-	-	-	-
Digital Converter 2	F0D	70E	-	-	-	-	-	Y	Y	-	-	-	-	-	-	-
Power State	F05	705	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Channel / Stream ID	F06	706	-	-	-	-	-	Y	Y	-	-	-	-	-	-	-
SDI Select	F04	704	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Pin Widget Control	F07	707	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
Unsolicited Enable	F08	708	-	-	-	-	-	-	-	Y	-	-	-	Y	-	-
Pin Sense	F09	709	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
EAPD / BTL Enable	F0C	70C	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
All GPIO Control	F15-F19	715-719	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Beep Generator Control	F0A	70A	-	-	-	-	-	-	-	-	-	-	-	-	Y	-
Volume Knob Control	F0F	70F	-	-	-	-	-	-	-	-	-	-	-	Y	-	-
Subsystem ID, Byte 0	F20	720	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Subsystem ID, Byte 1	F20	721	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Subsystem ID, Byte 2	F20	722	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Subsystem ID, Byte 3	F20	723	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Config Default, Byte 0	F1C	71C	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
Config Default, Byte 1	F1C	71D	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
Config Default, Byte 2	F1C	71E	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
Config Default, Byte 3	F1C	71F	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
RESET	-	7FF	-	Y	-	-	-	-	-	-	-	-	-	-	-	-

Table 10. Parameters in the CM9882A (Y=Supported)

Supported Parameter	Parameter ID	Root Node	Audio Function Group	Modem Function Group	HDMI Function Group	Vendor Define Group	Audio Out Converter	Audio In Converter	Pin Widget	Sum Widget	Selector Widget	Power Widget*1	Volume Knob	Beep Generator	Vendor Defined Widget
Vendor ID	00	Y	-	-	-	-	-	-	-	-	-	-	-	-	-
Revision ID	02	Y	-	-	-	-	-	-	-	-	-	-	-	-	-
Subordinate Node Count	04	Y	Y	-	-	-	-	-	-	-	-	-	-	-	-
Function Group Type	05	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Audio Function Group Capabilities	08	-	Y	-	-	-	-	-	-	-	-	-	-	-	-
Audio Widget Capabilities	09	-	-	-	-	-	Y	Y	Y	Y	Y	Y	Y	Y	Y
Sample Size, Rate	0A	-	Y	-	-	-	Y	Y	-	-	-	-	-	-	-
Stream Formats	0B	-	Y	-	-	-	Y	Y	-	-	-	-	-	-	-
Pin Capabilities	0C	-	-	-	-	-	-	-	Y	-	-	-	-	-	-
Input Amp Capabilities	0D	-	-	-	-	-	-	Y	-	Y	Y	-	-	-	-
Output Amp Capabilities	12	-	-	-	-	-	-	-	Y	Y	-	-	-	-	-
Connection List Length	0E	-	-	-	-	-	-	Y	Y	Y	Y	-	-	-	-
Supported Power States	0F	-	Y	-	-	-	Y	Y	Y	Y	Y	-	-	-	Y
Processing Capabilities	10	-	-	-	-	-	-	-	-	-	-	-	-	-	Y
GPI/O Count	11	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Volume Knob Capabilities	13	-	-	-	-	-	-	-	-	-	-	-	Y	-	-

6.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-bit Response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The 'Tag' in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

Table 11. Solicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:0]
Valid	Unsol=0	Reserved	Response

Table 12. Unsolicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:28]	Bit [27:0]
Valid	Unsol=1	Reserved	Tag	Response

Note: The response stream in the link protocol is 36-bits wide. The response is placed in the lower 32-bit field. Bit-35 is a 'Valid' bit to indicate the response is 'Ready'. Bit-34 is set to indicate that an unsolicited response was sent.

6.5. Power Management

All power management state changes in widgets are driven by software. Table 13 shows the System Power State Definitions. To simplify power management in the CM9882A, only the Audio Function supports power control. Output converters (DACs) and input converters (ADCs) have no individual power control. Software can configure whole codec power states through the audio function. Software may have various power states depending on system configuration.

Table 14 indicates those nodes that support power management.

6.5.1. System Power State Definitions

Table 13. System Power State Definitions

Power States	Definitions
D0	All Power On. Individual DACs and ADCs can be powered up or down as required
D1	All Converters (DACs and ADCs) are Powered Down. State maintained, analog reference stays up
D2	Power is still supplied. All amplifiers and converters (DACs and ADCs) are powered down. Codec stops PLL. State maintained. Jack-detection/GPI work.
D3 (Hot)	Power is still supplied. All amplifiers and converters (DACs and ADCs) are powered down. Codec stops PLL. State maintained. Jack-detection/GPI work.
D3 (Cold)	Power still supplied. All amplifiers and converters (DACs and ADCs) are powered down. Codec stops PLL. State maintained. Jack-detection/GPI work when internal OSC powers up.

6.5.2. Power Controls

Table 14. Power Controls

Item	Description	D0	D1	D2	D3	Link Reset
Audio Function	HD LINK State	Normal	Normal	Normal	Normal	PD
	Front DAC	Normal	PD	PD	PD	PD
	Surr DAC	Normal	PD	PD	PD	PD
	Cen/Lfe DAC	Normal	PD	PD	PD	PD
	Side DAC	Normal	PD	PD	PD	PD
	Fout DAC	Normal	PD	PD	PD	PD
	MIC ADC	Normal	PD	PD	PD	PD
	LINE ADC	Normal	PD	PD	PD	PD
	MIX ADC	Normal	PD	PD	PD	PD
	All Headphone Drivers	Normal	Normal	PD	PD	PD
	All Mixers	Normal	Normal	PD	PD	PD
	All Reference	Normal	Normal	Normal	Normal	Normal
	Jack Detection with Unsolicited Response	Normal	Normal	PD	Normal	Normal[2]

Note 1: PD=Powered Down
Note 2: Jack detection with unsolicited response is issued when a Link Reset occurs in D3 state.

6.5.3. Powered Down Conditions

Table 15. Powered Down Conditions

Condition	Description
LINK Response Powered Down	Internal Clock is Stopped SDATA-IN and S/PDIF-OUT are floated with internally pulled low 47K resistors. S/PDIF-IN is also floated. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences are supported. All states are maintained if DVDD is supplied.
FRONT DAC Powered Down	Analog Block and Digital Filter are Powered Down
SURR DAC Powered Down	Analog Block and Digital Filter are Powered Down
CEN/LFE DAC Powered Down	Analog Block and Digital Filter are Powered Down
SIDESURR DAC Powered Down	Analog Block and Digital Filter are Powered Down
FOUT DAC Powered Down	Analog Block and Digital Filter are Powered Down
LINE ADC Powered Down	Analog Block and Digital Filter are Powered Down Data on SDATA-IN is quiet.
MIX ADC Powered Down	Analog Block and Digital Filter are Powered Down Data on SDATA-IN is quiet.
MIC ADC Powered Down	Analog Block and Digital Filter are Powered Down Data on SDATA-IN is quiet.
Headphone Driver Powered Down	All Headphone Drivers are Powered Down
Mixers Powered Down	All Internal Mixer Widgets are Powered Down The DC reference and VREFOUTx at individual pin complexes are still alive.
Reference Power Down	All Internal References, DC Reference, and VREFOUTx at Individual Pin Complexes are Off

7. Electrical Characteristics

7.1. DC Characteristics

7.1.1. Absolute Maximum Ratings

Table 16. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply					
Digital Power for Core	DVDD	2.7	3.3	3.6	V
Digital Power for HDA Link	DVDD-IO*	1.5	3.3	3.6	V
Analog	AVDD**	4.5	5.0	5.25	V
Ambient Operating Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts	-	-	+125	°C
ESD (Electrostatic Discharge)					
	Susceptibility Voltage				
All Pins	3500				

**: The digital link power DVDD-IO must be lower than the digital core power DVDD.*

***: The standard testing condition before shipping is AVDD = 5.0V unless specified. Customers designing with a different AVDD should contact Cmedia technical support representatives for special testing support.*

7.1.2. Threshold Voltage

DVDD-IO= 1.5V±5% / 3.3V±5%, DVDD= 3.3V±5%, $T_{ambient}$=25°C, with 50pF external load.

Table 17. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V_{in}	-0.30	-	DVDD+0.30	V
Low Level Input Voltage (HDA link)	V_{IL}	-	-	0.4*DVDD-IO	V
High Level Input Voltage (HDA link)	V_{IH}	0.6*DVDD-IO	-	-	V
High Level Output Voltage (HDA link)	V_{OH}	0.9*DVDD-IO	-	-	V
Low Level Output Voltage (HDA link)	V_{OL}	-	-	0.1*DVDD-IO	V
Low Level Input Voltage (SPDIF-IN, GPIOs)	V_{IL}	-	-	0.44*DVDD (1.45)	V
High Level Input Voltage (SPDIF-IN, GPIOs)	V_{IH}	0.56*DVDD (1.85)	-	-	V
High Level Output Voltage (SPDIF-OUT, GPIOs)	V_{OH}	0.9*DVDD		-	V
Low Level Output Voltage (SPDIF-OUT, GPIOs)	V_{OL}	-	-	0.1*DVDD	V
Input Leakage Current	-	-10	-	10	µA
Output Leakage Current (Hi-Z)	-	-10	-	10	µA
Output Buffer Drive Current	-	-	5	-	mA
Internal Pull Up Resistance	-	-	50k	-	Ω

7.1.3. Digital Filter Characteristics

Table 18. Digital Filter Characteristics

Filter	Description	Minimum	Typical	Maximum	Units
ADC Filter	Passband (Upper Band < -0.030dB)	-	0.4350*Fs	-	KHz
	Passband (Upper Band < -1.0dB)	-	0.4571*Fs	-	KHz
	Passband Ripple	-	-	±0.030	dB
	Stopband	0.565*Fs	-	-	KHz
	Stopband Attenuation	80	-	-	dB
ADC Highpass Filter	Passband Frequency Response: -0.15dB (Fs=192000)	-	20	-	Hz
DAC Lowpass Filter	Passband Frequency Response: -0.03dB	-	0.441*Fs	-	KHz
	Stopband	0.559*Fs	-	1.5*Fs	KHz
	Stopband Rejection	90	-	-	dB
	Passband Ripple	-	-	±0.030	dB
DAC Highpass Filter	Passband Frequency Response: -0.15dB (Fs=192000)	-	20	-	Hz

Note: Fs=Sample rate.

7.1.4. SPDIF Input/Output Characteristics

DVDD= 3.3V, $T_{ambient}$=25°C, with 75Ω external load.

Table 19. SPDIF Input/Output Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
SPDIF-OUT High Level Output	V_{OH}	3.0	3.3	-	V
SPDIF-OUT Low Level Output	V_{OL}	-	0	0.3	V
SPDIF-IN High Level Input	V_{IH}	1.85	-	-	V
SPDIF-IN Low Level Input	V_{IL}	-	-	1.45	V
SPDIF-IN Bias Level	Vt	-	1.65	-	V

7.2. AC Characteristics

7.2.1. Link Reset and Initialization Timing

Table 20. Link Reset and Initialization Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# Active Low Pulse Width	T_{RST}	1.0	-	-	µs
RESET# Inactive to BCLK Startup Delay for PLL Ready Time	T_{PLL}	20	-	-	µs
SDI Initialization Request	T_{FRAME}	-	-	1	Frame Time

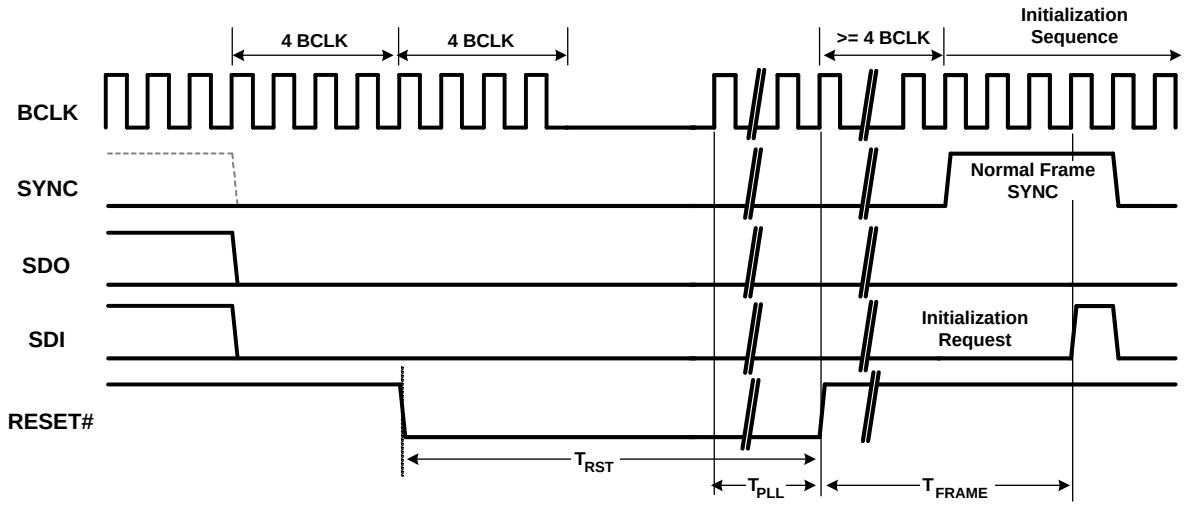


Figure 14. Link Reset and Initialization Timing

7.2.2. Link Timing Parameters at the Codec

Table 21. Link Timing Parameters at the Codec

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK Frequency		-	24.0	-	MHz
BCLK Period	T_{cycle}	-	41.67	-	ns
BCLK Jitter	T_{jitter}	-	-	2.0	ns
BCLK High Pulse Width	T_{high}	17.5	-	24.16	ns
BCLK Low Pulse Width	T_{low}	17.5	-	24.16	ns
SDO Setup Time at Both Rising and Falling Edge of BCLK	T_{setup}	2.1	-	-	ns
SDO Hold Time at Both Rising and Falling Edge of BCLK	T_{hold}	2.1	-	-	ns
SDI Valid Time After Rising Edge of BCLK (1:50pF External Load)	T_{tco}	-	7.5	8.0	ns
SDI Flight Time	T_{flight}	-	2.0	-	ns

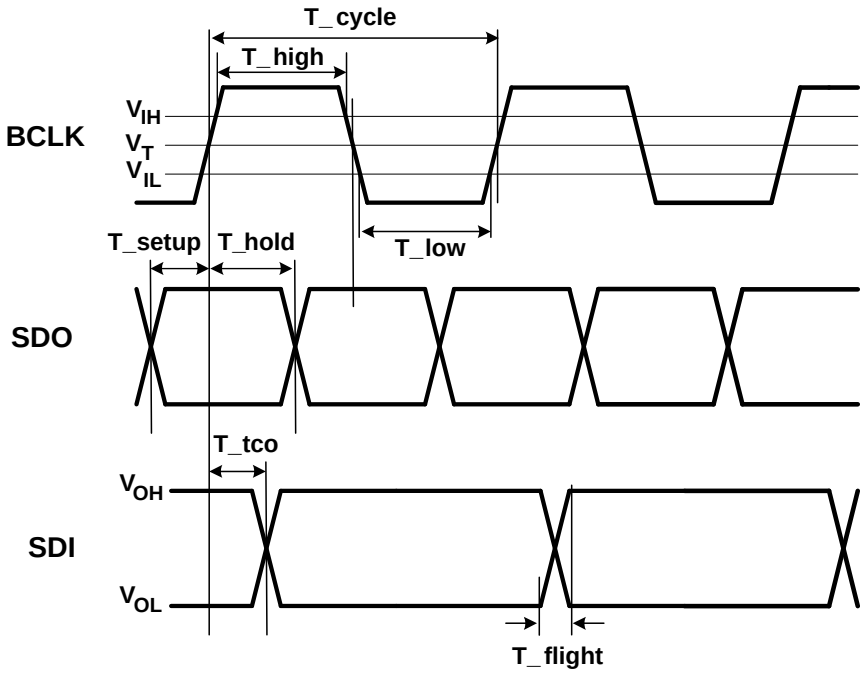


Figure 15. Link Signals Timing

7.2.3. SPDIF Output and Input Timing

Table 22. SPDIF Output and Input Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
SPDIF-OUT Frequency	-	-	3.072	-	MHz
SPDIF-OUT Period *1	T_{cycle}	-	325.6	-	ns
SPDIF-OUT Jitter	T_{jitter}	-	-	4	ns
SPDIF-OUT High Level Width	T_{High}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
SPDIF-OUT Low Level Width	T_{Low}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
SPDIF-OUT Rising Time	T_{rise}	-	2.0	-	ns
SPDIF-OUT Falling Time	T_{fall}	-	2.0	-	ns
SPDIF-IN Period *2	T_{cycle}	-	325.6	-	ns
SPDIF-IN Jitter	T_{jitter}	-	-	10	ns
SPDIF-IN High Level Width	T_{High}	146.4 (45%)	162.8 (50%)	179 (55%)	ns (%)
SPDIF-IN Low Level Width	T_{Low}	146.4 (45%)	162.8 (50%)	179 (55%)	ns (%)

**1: Bit parameters for 48kHz sample rate of SPDIF-OUT.*

**2: Bit parameters for 48kHz sample rate of SPDIF-IN.*

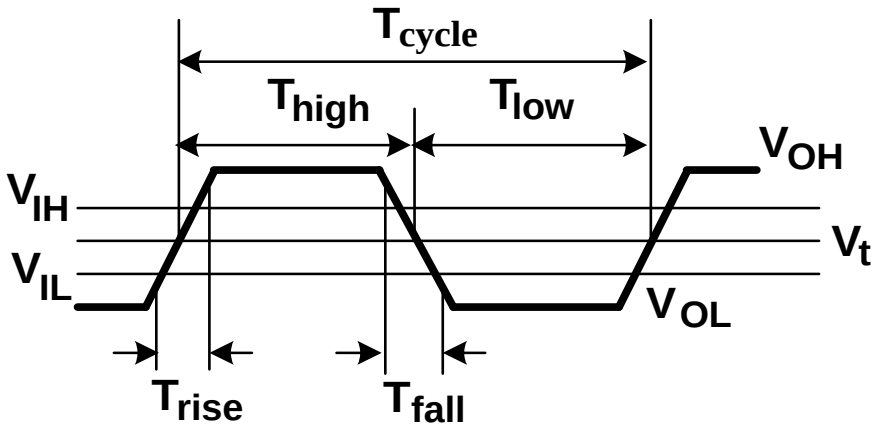


Figure 16. Output and Input Timing

7.2.4. Test Mode

The CM9882A does not support test mode or Automatic Test Equipment (ATE) mode.

7.3. Analog Performance

Standard Test Conditions

- $T_{ambient}$=25 °C, DVDD=3.3V ±5%, AVDD=5.0V±5%
- 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
- 10KΩ/50pF load; Test bench Characterization BW:10Hz~22kHz

Table 23. Analog Performance

Parameter	Min	Typical	Max	Units
Full-Scale Input Voltage All Inputs (Gain=0dB) to ADC	-	1.6	-	Vrms
Full-Scale Output Voltage (Gain=0dB)				
DAC	-	1.25	-	Vrms
Headphone Amplifier Output@32Ω Load	-	1.1	-	Vrms
Dynamic Range with –60dB Signal (A-Weight)				
ADC	-	104	-	dB FSA
DAC	-	108	-	dB FSA
Headphone Amplifier Output@32Ω Load	-	105	-	dB FSA
THD+N with –3dB Signal (No A-Weight)				
ADC from LINE1 and MIC2	-	-85	-	dB FS
ADC from Other Port Except LINE1 and MIC2	-	-90	-	dB FS
DAC to All Port	-	-90	-	dB FS
Headphone Amplifier Output@32Ω Load	-	-90	-	dB FS
Magnitude Response (10KΩ load)				
All DAC @Fs=48KHz (FR=±0.05dB)	0	-	21,792	Hz
All DAC @Fs=96KHz (FR=±0.05dB)	0	-	43,584	Hz
All DAC @Fs=192KHz (FR=±0.05dB)	0	-	87,168	Hz
All ADC @Fs=48KHz (FR=±0.04dB)	0	-	19,200	Hz
All ADC @Fs=96KHz (FR=±0.04dB)	0	-	38,400	Hz
All ADC @Fs=192KHz (FR=±0.04dB)	0	-	76,800	Hz
Power Supply Rejection (Measured at 1kHz Point)	-	-70	-	dB
Amplifier Gain Step	-	1.0	-	dB
Channel Separation (Crosstalk)	-	-80	-	dB
Input Impedance (Gain=0dB)	12	-	16	KΩ
Output Impedance				
Amplified Output	-	2	-	Ω
Non-Amplified Output	-	200	-	Ω
Digital Power Supply Current (Normal/DVD-Audio) DVDD=3.3V	-	17/40	-	mA
Digital Power Supply Current (D2) DVDD=3.3V	-	-	2000	μA
Analog Power Supply Current (Normal Operation) AVDD=5.0V	-	75	-	mA
Analog Power Supply Current (D2) AVDD=5.0V	-	500	-	μA
VREFOUTx Output Voltage	-	0.5*AVDD	0.8*AVDD	V
VREFOUTx Output Current	-	5	-	mA

8. Application Circuits

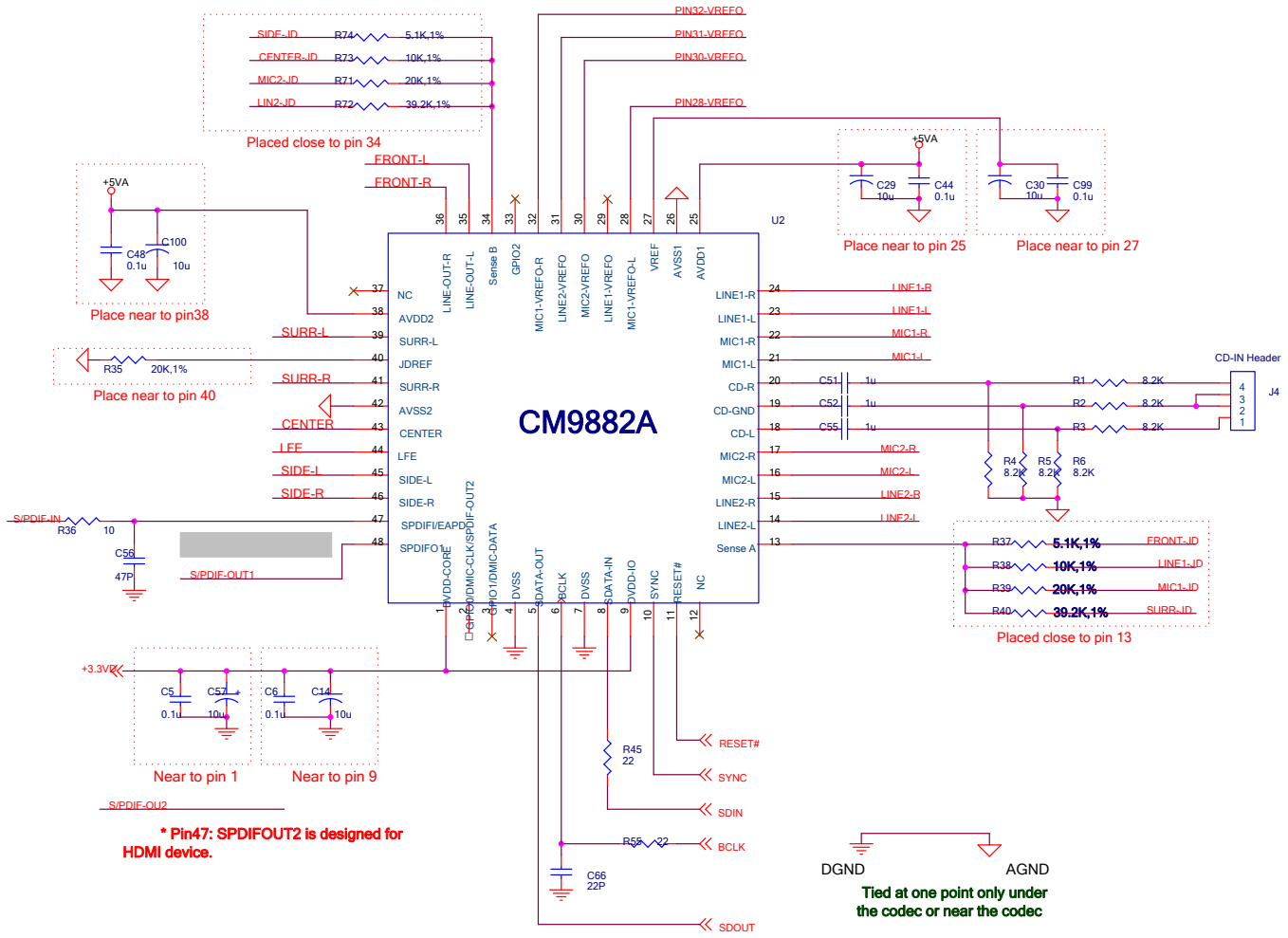
To get the best compatibility in hardware design and software driver, any modification should be confirmed with Cmedia.

8.1. Desktop System

This following pages show an example of a 7.1 channel output desktop system with three analog jacks on the rear panel, and with two re-tasking analog jacks on the front panel.

Table 24. Desktop System

Analog Port	Pin	Location	Function Description
FRONT	35, 36	Rear Panel	Front Channel Line Output and Amplified Output
SURR	39, 41	Rear Panel	Surround Channel Line Output
CENTER/LFE	43, 44	Rear Panel	Center and Low Frequency (Sub-Woofer) Channel Line Output
SIDE	45, 46	Rear Panel	Side Surround Channel Line Output
MIC1	21, 22	Rear Panel	Analog Microphone Input
LINE1	23, 24	Rear Panel	Analog Line Input
LINE2	14, 15	Front Panel	Re-Tasking Jack Supports Headphone Out (Default), Microphone Input, and Line Input
MIC2	16, 17	Front Panel	Re-Tasking Jack Supports Microphone Input (Default), Line Input, and Headphone Output


CM9882A
U2
SIDE-JD
CENTER-JD
MIC2-JD
LIN2-JD
R74 5.1K,1%
R73 10K,1%
R71 20K,1%
R72 39.2K,1%
Placed close to pin 34
PIN32-VREFO
PIN31-VREFO
PIN30-VREFO
PIN28-VREFO
FRONT-L
FRONT-R
+5VA
C48 0.1u
C100 10u
Place near to pin38
R35 20K,1%
Place near to pin 40
SURR-L
SURR-R
CENTER
LFE
SIDE-L
SIDE-R
S/PDIF-IN
R36 10
C56 47P
S/PDIF-OUT1
S/PDIF-OU2
* Pin47: SPDIFOUT2 is designed for HDMI device.
+3.3VD
C5 0.1u
C57 10u
C6 0.1u
C14 10u
Near to pin 1
Near to pin 9
C29 10u
C44 0.1u
C30 10u
C99 0.1u
Place near to pin 25
Place near to pin 27
LINE1-R
LINE1-L
MIC1-R
MIC1-L
CD-R
CD-GND
CD-L
MIC2-R
MIC2-L
LINE2-R
LINE2-L
Sense A
C51 1u
C52 1u
C55 1u
CD-IN Header
J4
R1 8.2K
R2 8.2K
R3 8.2K
R4 8.2K
R5 8.2K
R6 8.2K
R37 5.1K,1%
R38 10K,1%
R39 20K,1%
R40 39.2K,1%
FRONT-JD
LINE1-JD
MIC1-JD
SURR-JD
Placed close to pin 13
R45 22
R55 22
C66 22P
RESET#
SYNC
SDIN
BCLK
SDOUT
DGND
AGND
Tied at one point only under the codec or near the codec

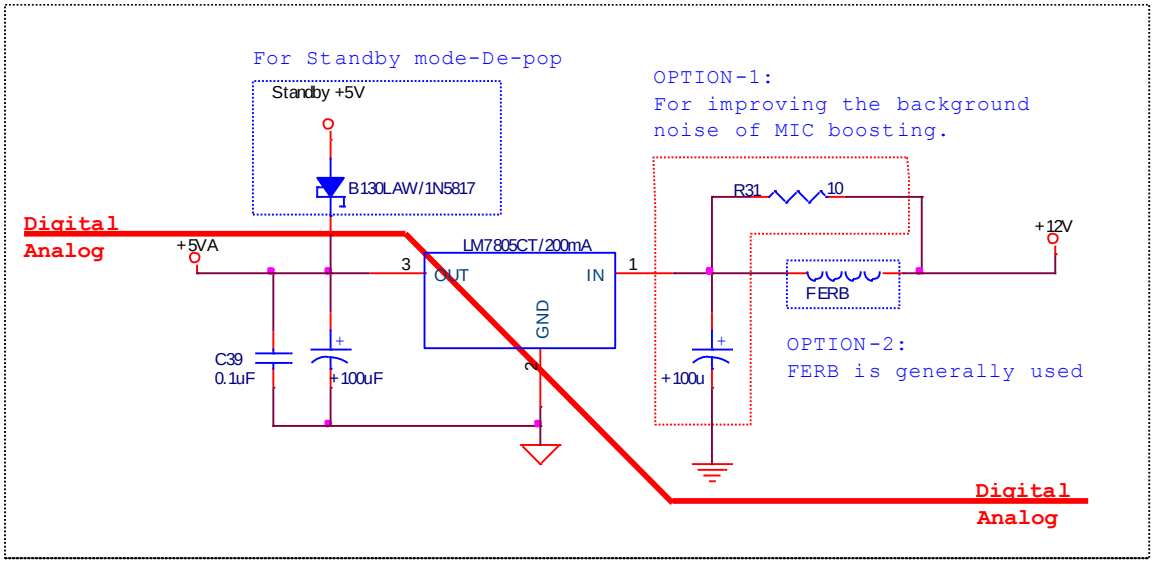
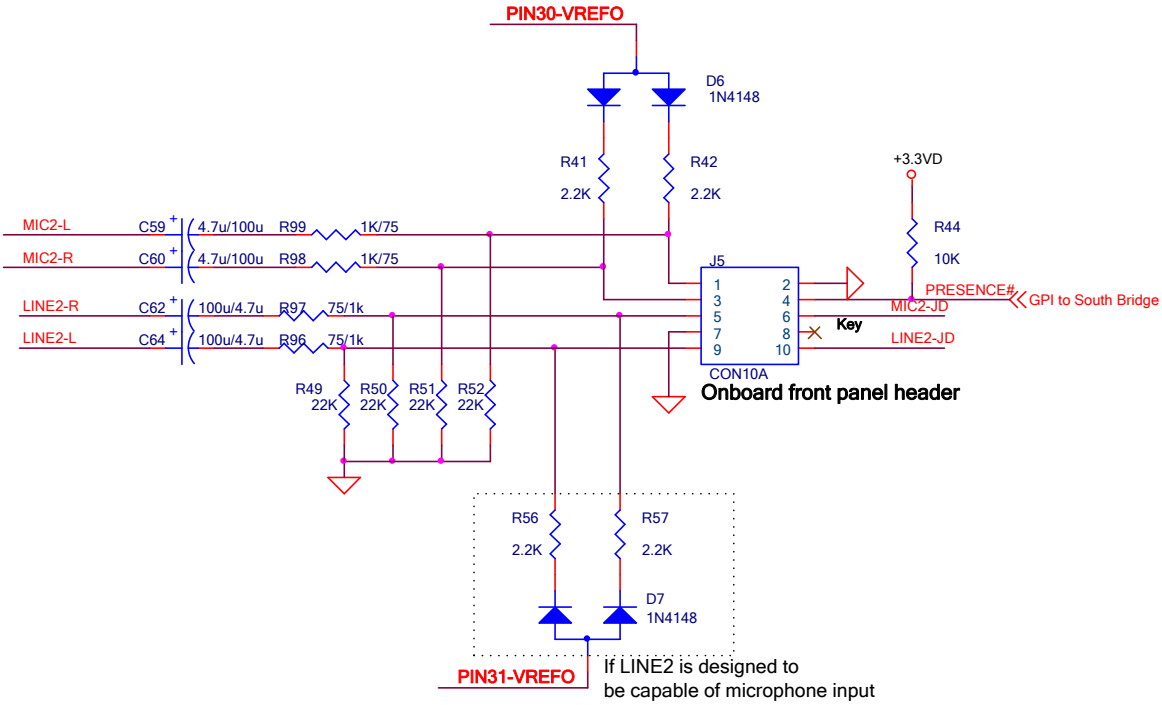


Figure 17. Filter Connection



To pass Vista requirement in low frequency band:

-If MIC2 is designed to be microphone input only, please put the 4.7u/X5R (C59/60) and 1k (R98/99).

-If LINE2 is designed to be line input only, please put the 4.7u/X5R (C62/64) and 1k (R96/97).
-If LINE2 and MIC2 are designed to support re-tasking funcion, please put non-polarity 100u cap (C59/C60/C62/C64) and 75 ohm (R98/R99/R96/R97).
-Add 22K pull-down resistors (R49/R50/R51/R52) to reduce pop noise when (C59/60/62/64) are polarity caps.

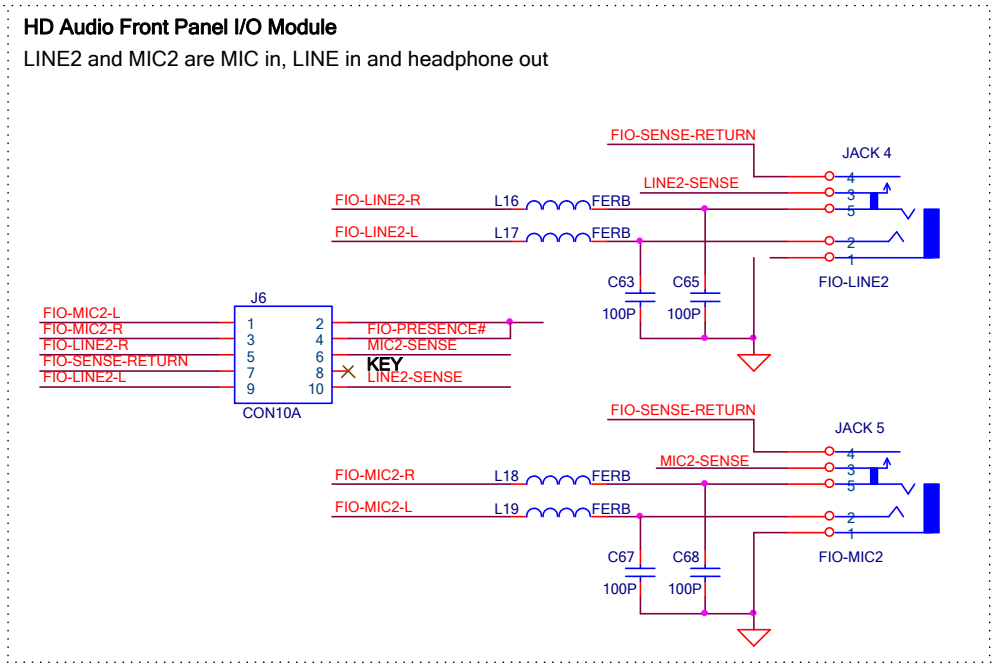
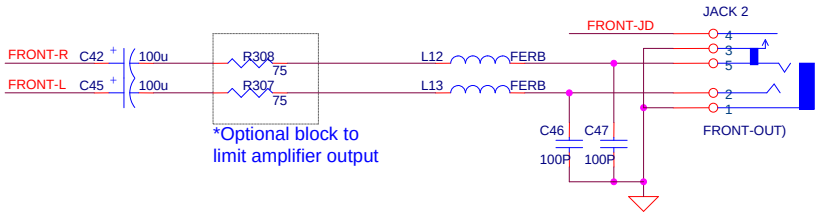
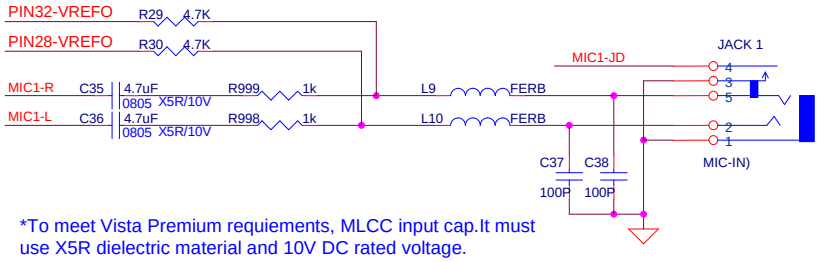


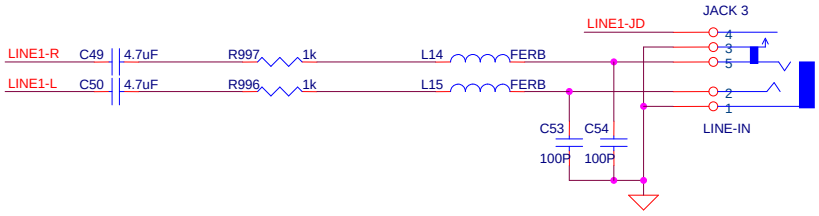
Figure 18. Front Panel Header and Front Panel Module Connection

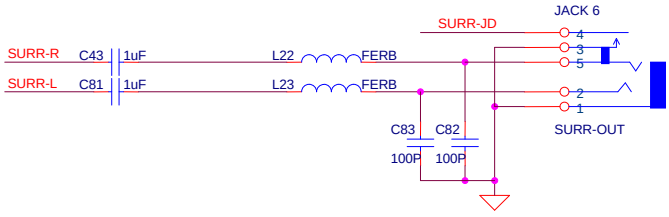


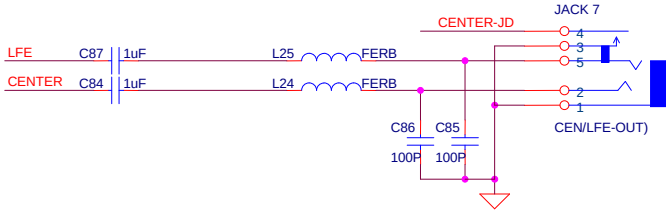


*To meet Vista Premium requiements, MLCC input cap.It must use X5R dielectric material and 10V DC rated voltage.

*Place R999/R998/R997/R996 to 1k£[for enhancing ESD ability.







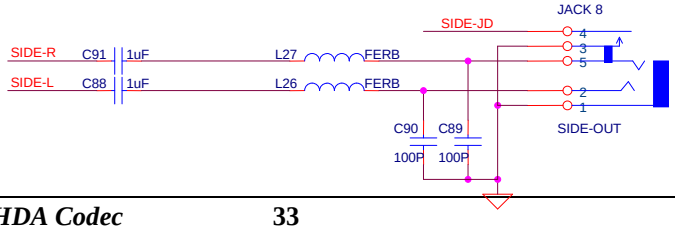
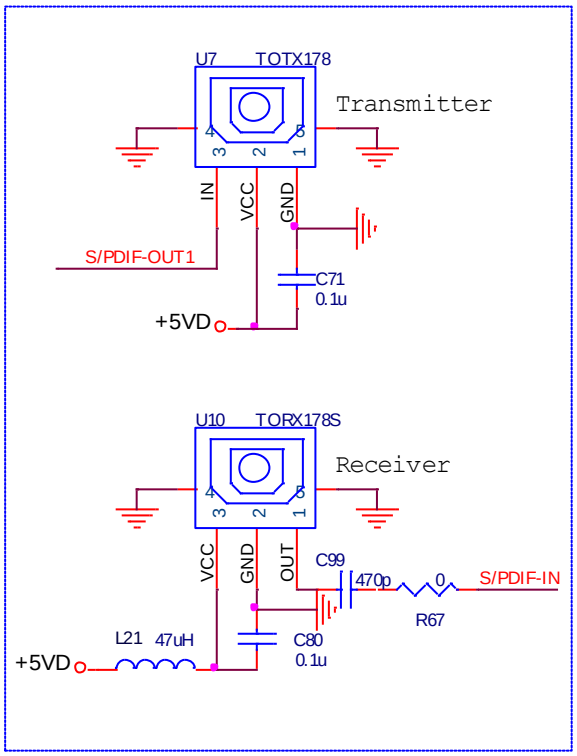
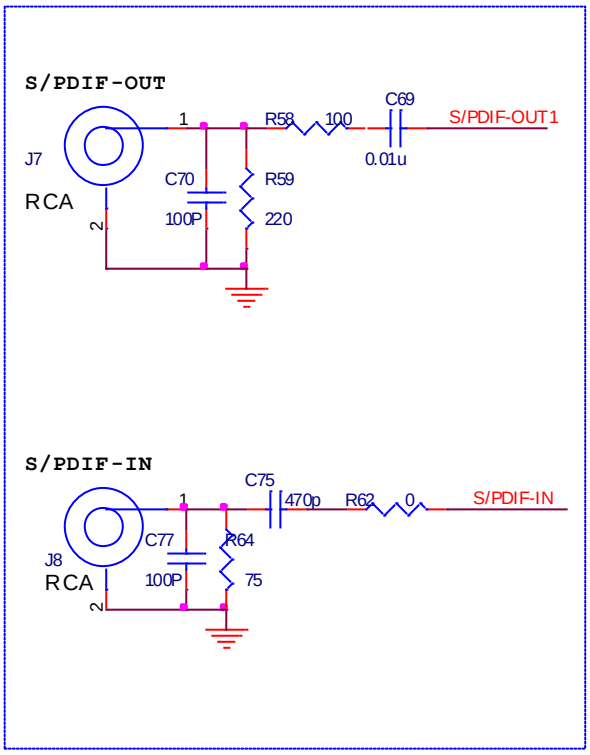


Figure 19. Jack Connection at Rear Panel

S/PDIF module option 1: Optical



S/PDIF option 2: RCA only



S/PDIF option 3: Optical & RCA

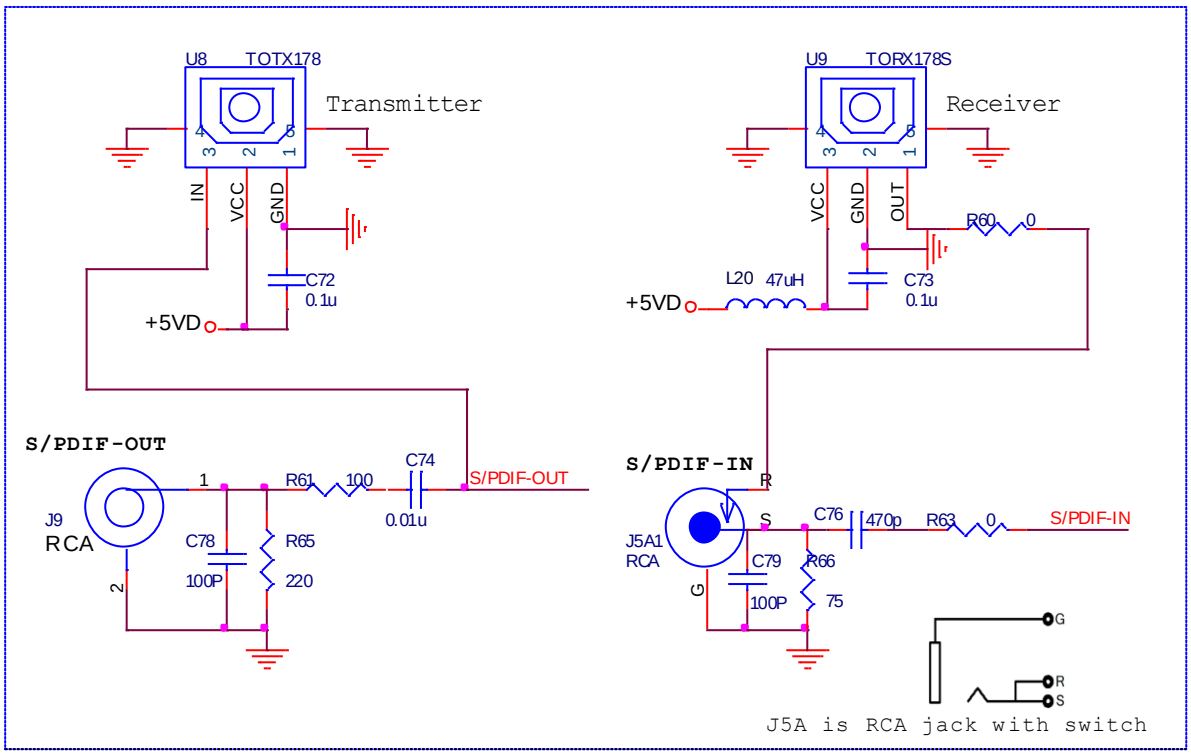


Figure 20. SPDIF Input/Output Connection

9. Application Supplements

9.1. Standby Mode

In standby mode the CM9882A turns on DC bias on all analog input and output ports. This is a special application to avoid 'Pop' noise while system is in power on and power off transition stages.

Table 25 shows the DC bias state when Standby mode is enabled.

Table 25. Standby Mode

+3.3V on DVDD (Pin-1)	+5VA on AVDD	Operation Mode
No (<2.0V)	No	Shut Down
No (<2.0V)	Yes	Standby Mode
Yes (>2.0V)	No	Normal
Yes (>2.0V)	Yes	Normal

9.2. Digital Microphone Implementation

This section describes the CM9882A digital microphone implementation. There is one Clock output pin and 1 Data input pin in the CM9882A. The CM9882A provides the clock signal to the digital microphone. When the digital microphone receives the external sound input, it converts the analog signals to digital in a 1-bit format. The 1-bit data is delivered to the codec though the data input pin. The Digital Filter in the audio codec converts the 1-bit data stream into Pulse Code Modulation (PCM) data. The PCM data is sent to the HDA controller through the HDA link.

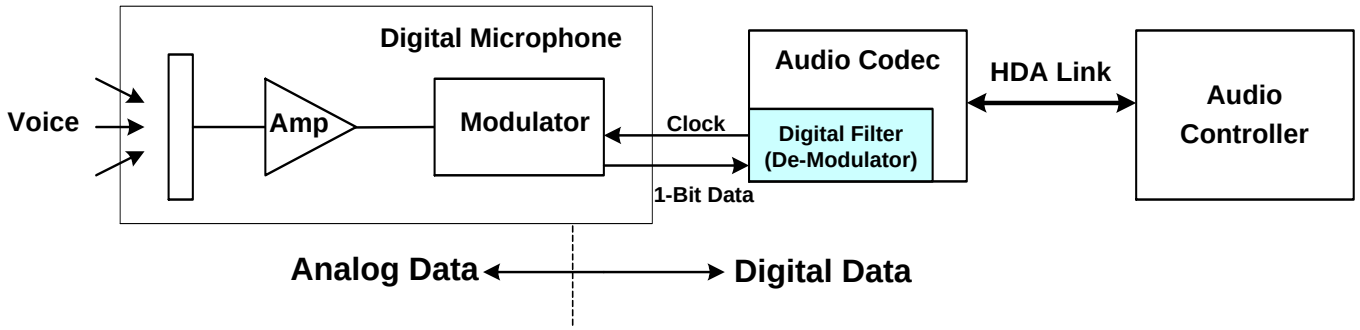


Figure 21. Digital Microphone Implementation

The CM9882A supports a two-wire interface for the digital microphone and operates in single-channel (mono type) or stereo-channel mode. One pin is clock output to the digital microphone, and the other is a serial pin. The default clock output is 2.048MHz.

The CM9882A uses one data pin to support stereo inputs from various digital microphones and microphone module. Popular digital microphones provided from Fortemedia, Akustica, Knowles, and Hosiden are supported. Please contact Cmedia and your digital microphone vendor to get the best compatibility between the CM9882A and various digital microphones.

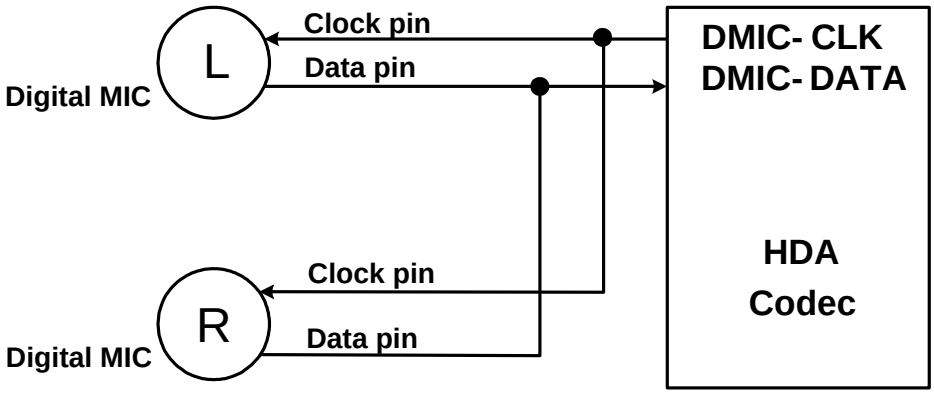
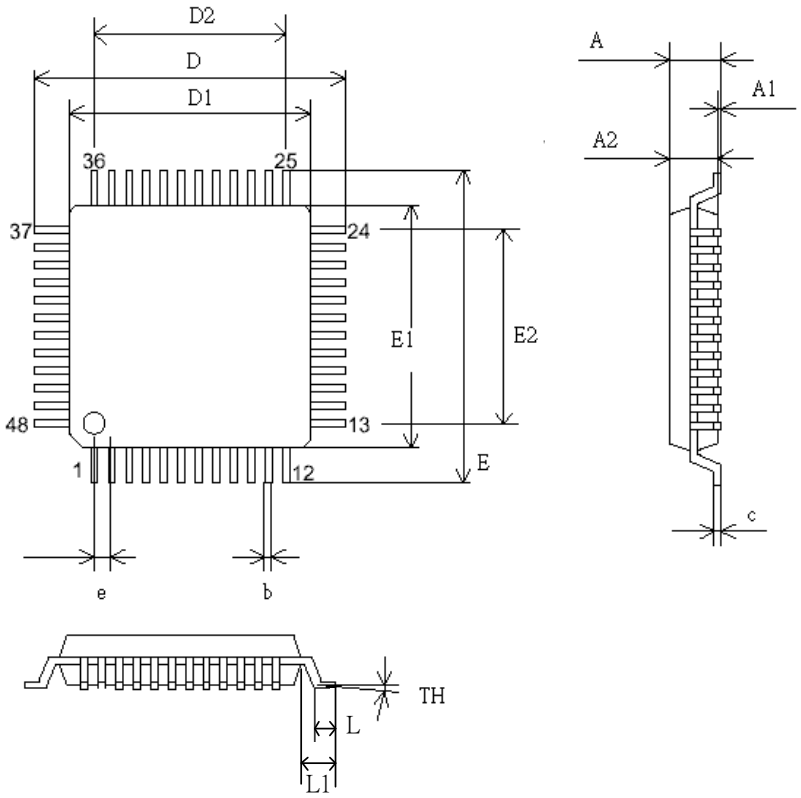


Figure 22. Stereo Digital Microphone Connection

10. Mechanical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN	TYP	MAX	MIN	TYP	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09	-	0.20	0.004	-	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0196 BSC		
TH	0^o	3.5^o	7^o	0^o	3.5^o	7^o
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1	-	1.00	-	-	0.0393	-

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