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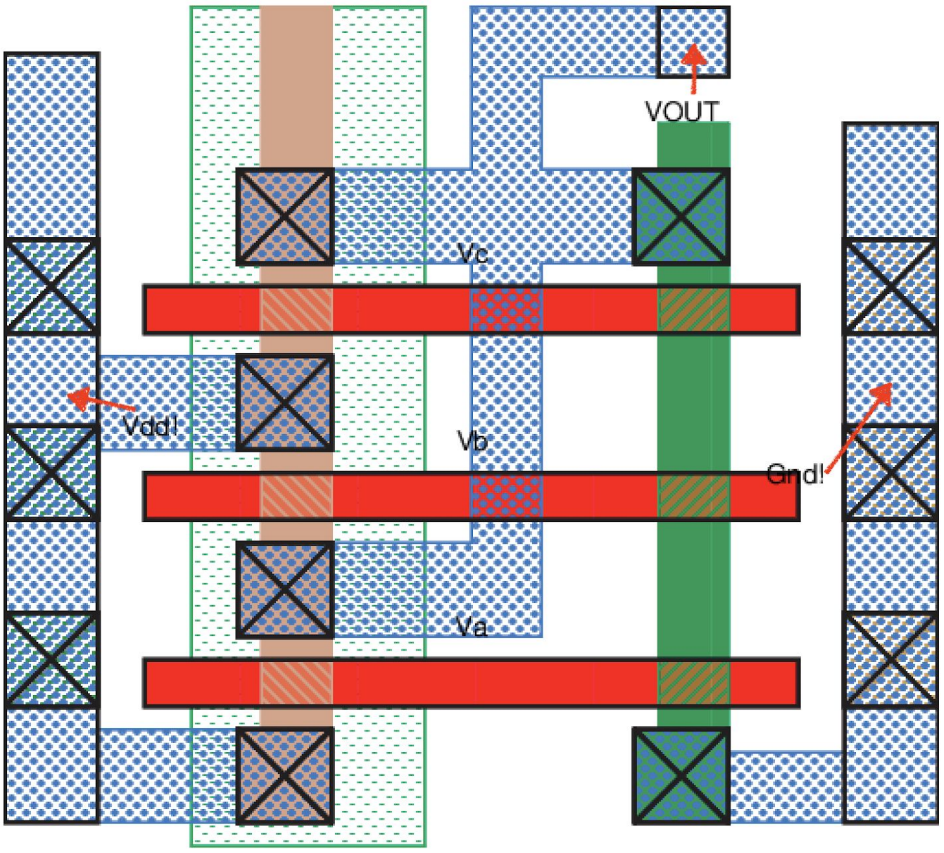
ELEC311 LAB

Introduction

In this assignment you are going to use “Magic VLSI ” which open software and can be downloaded from the website http://www.opencircuitdesign.com

Assignment-1

1. Please read Prof. James Stine's tutorial, IC Layout Using Magic and tutorial in http://opencircuitdesign.com/magic/tutorials/ Especially read Magic Tutorial #1: Getting Started and Magic Tutorial #2: Basic Painting and Selection. Please carefully read "Step-by-Step Example" in Prof. Stine's tutorial to create the layout for an inverter.
2. Use magic to create a layout of a 3-input CMOS NAND gate. All transistors in the NAND gate should be sized 3 lambda wide by two lambda long. Inputs should feed the NAND gate from the left on polysilicon (red) or metail1 (blue) wires, and the output should feed to the right of the cell on a metal1 wire. Power supply connections should be labelled Vdd! and Gnd! and should feed from left to right at the top and bottom of the layout. Save your layout using the command "save nor"; this will create a layout file named nand.mag.
3. Plot your layout using the magic command ":plot postscript nand.ps" after selecting the entire cell. Exit magic and print this file using the command "lpr nand.ps". Hand in this plot to the instructor before you leave.



You can find above my Nand gate implementation. Also I added a nand.ps document in zip.

Assignment-2

1. Use the "magic" layout editor to create a layout of the AOI-22 gate. Make sure to follow the Layout Guidelines given below.
2. Measure the area of your circuit by selecting the entire cell and typing "b" (this macro reports the current dimensions of the Magic "box", which after selection is the bounding box of your cell). Be sure to note the dimensions and overall area of your cell in your lab report.

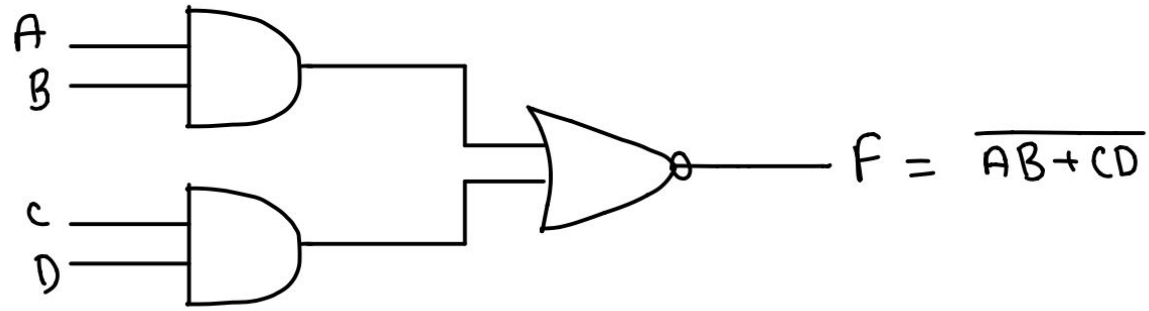
Report for assignment 2

For your lab report, hand in the following items:
1. A short "Technical Memorandum" which describes
(a) your approach to creating your AOI gate layout, (b) the characteristics of your layout, including dimensions and area, (c) any difficulties you encountered, and (d) suggestions for improving this lab in the future, if any.
2. Your schematic diagram of an AOI-22 gate and truth table. 3. Your stick diagram of your planned layout. 4. A plot of your magic layout of the AOI-22 gate.

Lab Report

AND-OR-invert logic gate is a complicated logic function developed by use of AND gate combination accompanied by a NOR gate. This logic function performs several AND operations followed by the OR operation then an inversion. This series accelerates the system's overall speed, minimizes power usage, creates smaller spaces, and potentially declines the cost of fabrication. For the development of this gate, I have utilized both the NMOS and PMOS transistors. All the dimensions I have made have been mentioned in this paper, under the magic layout screenshot. The size of the PMOS is bigger than that of NMOS. First, I tried to figure out how to build a single NAND gate, and then after looking at the schematics, I started developing the AO122 gate. Inputs used were named a, b, c, and d. Additionally, all the connections made to adhere to n/p, metal, and polysilicon rules. I ensured that there were several contacts for the proper functioning of the system. I made the layout and labeled outputs, inputs, and VDD as used in the universal symbol. Earlier I had no clue about gate development, but by reading the sources and watching several tutorials, the procedure was now clear in my head, and now I proudly enjoy making gates. During gate construction, I came across several problems, but after reading the mistakes, I got all the rules correctly. This program gives an insight into faster, error-fixing. Personally, the most challenging task is the installation of Magic VLSI. Currently, I have a Mac, and I have terminal challenges. In my research, I have discovered that installing Magic on Linux is more comfortable. I have downloaded Oracle Virtual Box Machine then Ubuntu Server. It was easy to download Magic with a terminal. For lab improvement, we can find more integrable software instead of Magic. I enjoyed this activity despite being faced with problems of rules and Ubuntu installation. I learned through reading and analyzing errors.

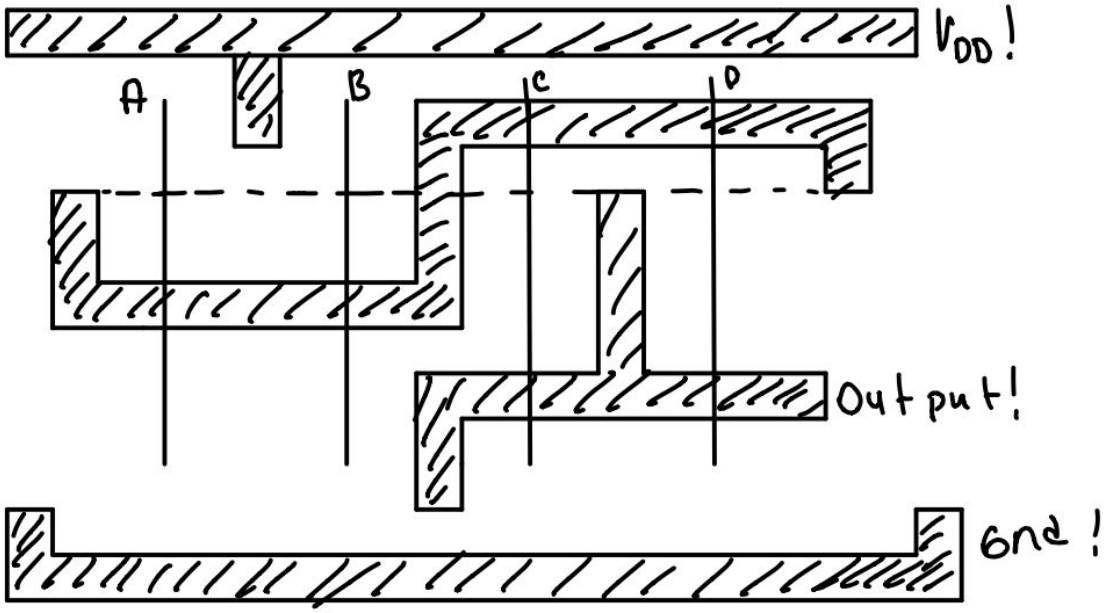
Schematics



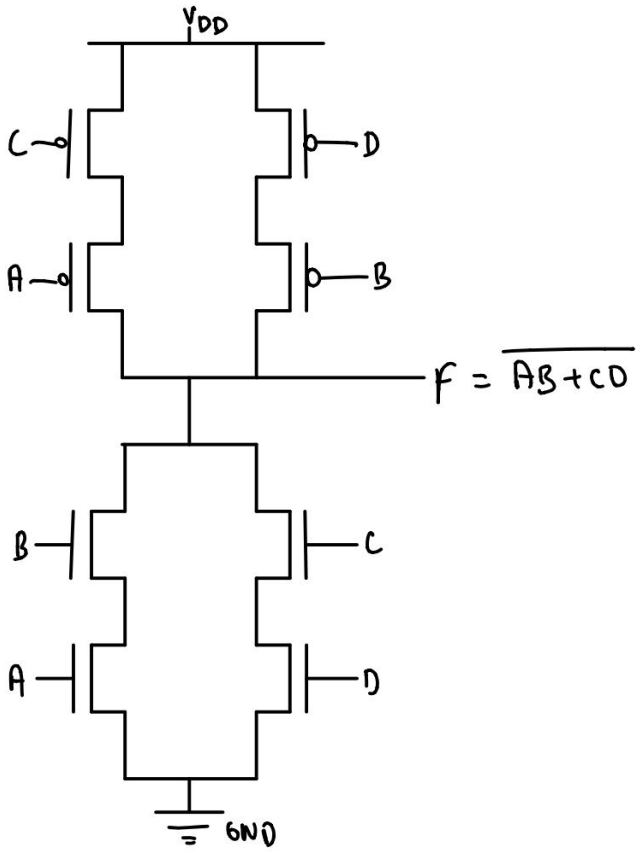
Truth Table:

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

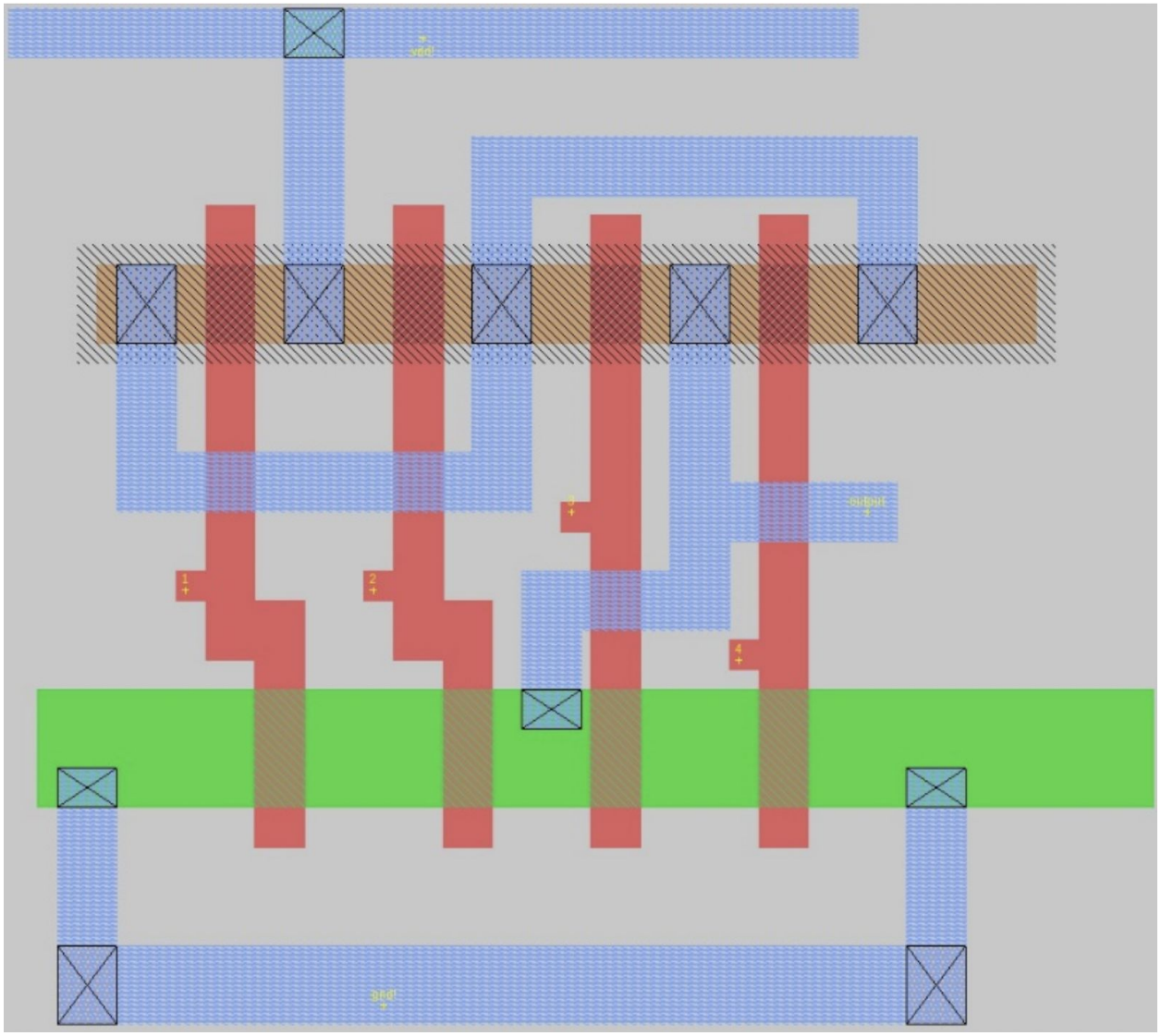
Stick Diagram:



CMOS schematics



Magic Plot:



Size:

```
Root cell box:
          width x height  (   llx,  lly  ), (   urx,  ury  )  area (units^2)

microns:  116.00 x 103.00  (-39.00, -85.00), ( 77.00,  18.00)  11948.00
lambda:     116 x 103      (   -39, -85    ), (    77,  18    )  11948
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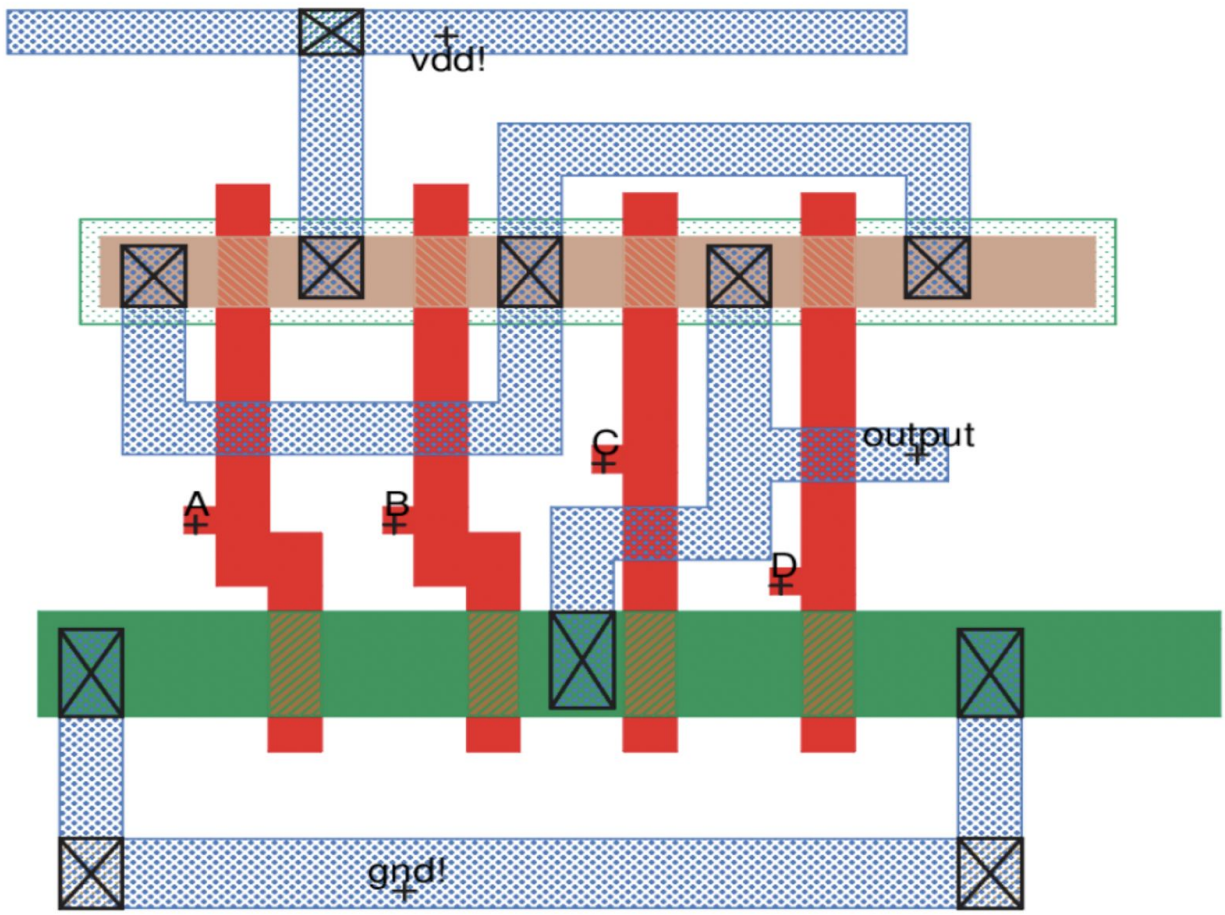
vdd!
output
C
A
B
D
gnd!