Practical PCB Design and Manufacture

Lab-15 Report: Good-bad switching noise board

Objective / Purpose of the Lab:

- The purpose of this lab is to provide hands-on experience with reducing switching noise in electronic circuits by emphasizing two design principles: maintaining a continuous return path under signal traces and using low inductance decoupling capacitors near IC power pins. Through analysing and measuring switching noise on a pre-built board featuring both well and poorly designed hex inverter circuits, we will gain insights into effective circuit design and layout practices.

Component Listing:

- 5V power supply
- Testing board
- 10x Probes with spring ground tips
- Oscilloscope

Board Design:

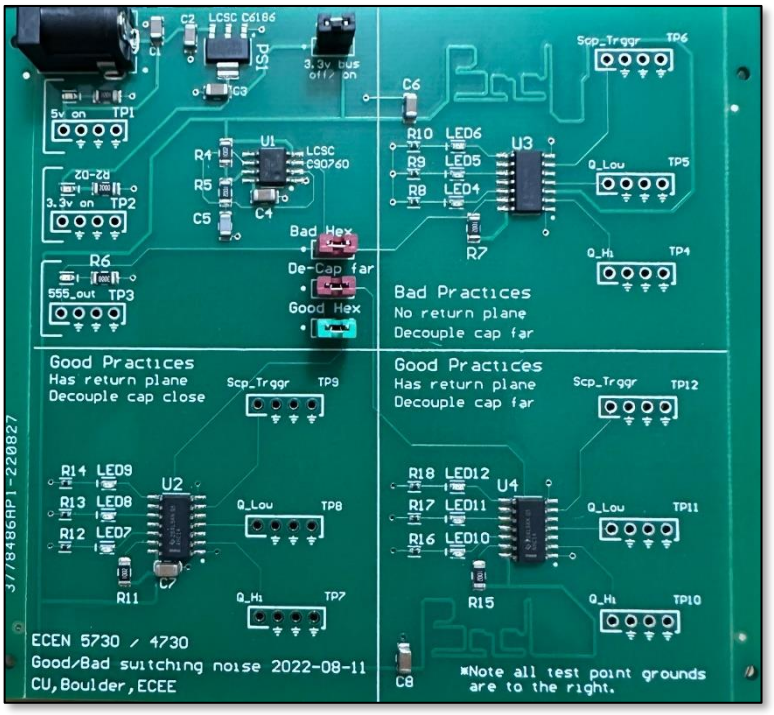

Fig – 1: Board layout

- The test board features a dual-layer design hosting three unique hex inverter circuits and employs a 555 timer as the clock source.
- The 'excellent' hex inverter circuit, located in the lower left quadrant, adheres to optimal design standards with a continuous return path and a decoupling capacitor positioned near the IC power pins. In contrast, the 'good decent' circuit, found in the lower right quadrant, maintains a continuous ground plane but places the decoupling capacitor far from the IC power pins.
- The 'poor' hex inverter circuit, situated in the upper right quadrant, neglects both essential design principles, leading to switching noise generated by the inverters.

- Within each circuit, four inverters are engaged by switching signals, with one triggering the oscilloscope and the others driving LEDs. The remaining two inverters, labelled 'quiet HIGH' and 'quiet LOW,' are utilized for switching noise assessment, displaying no voltage changes.

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Scope Shots with Analysis:

Fig – 2: Noise when connected between 3.3V and the 555 timer output

Fig – 3: 3.3V rise time for 555 output

As we can see from the above figures, the rise time for the 555 timer is around 31ns when connected to a 3.3V power from the board.

Part 1: Bad layout: no return plane and decoupling capacitor far away.

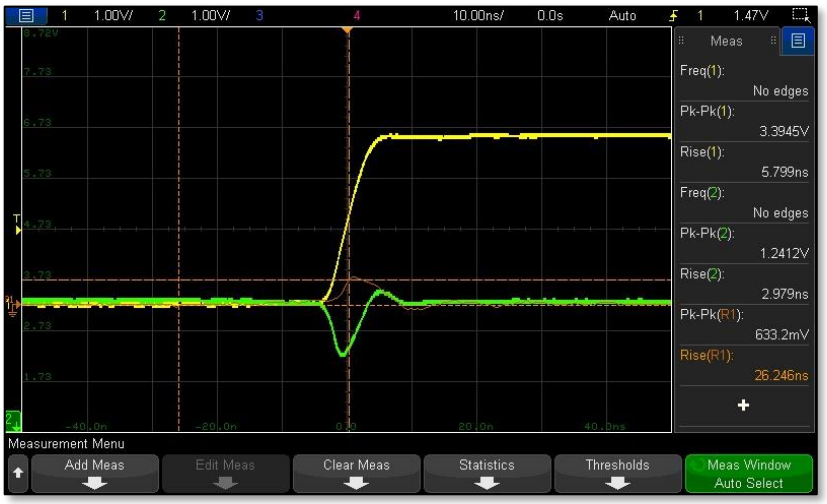

Fig – 4: Noise difference between quiet LOW and quiet HIGH (Bad 1)

- The Fig 5 which is shown analyses the difference in noise when the measurements are taken at the quiet LOW and the quiet HIGH test point of the bad layout board.
- The quiet low has a peak-to-peak voltage of around 633.2mV and for quiet HIGH, it is around 1.24V.
- There is also a difference in the rise times of quiet LOW and quiet HIGH outputs.
- Increased loop area leads to more noise emission and reception. Capacitor's effectiveness is reduced due to increased inductance from longer traces.
- This approach is highly prone to noise, probable malfunction, and instant vulnerability, especially in sensitive circuits.

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Part 2: Bad layout: has return plane but decoupling capacitor is far away.

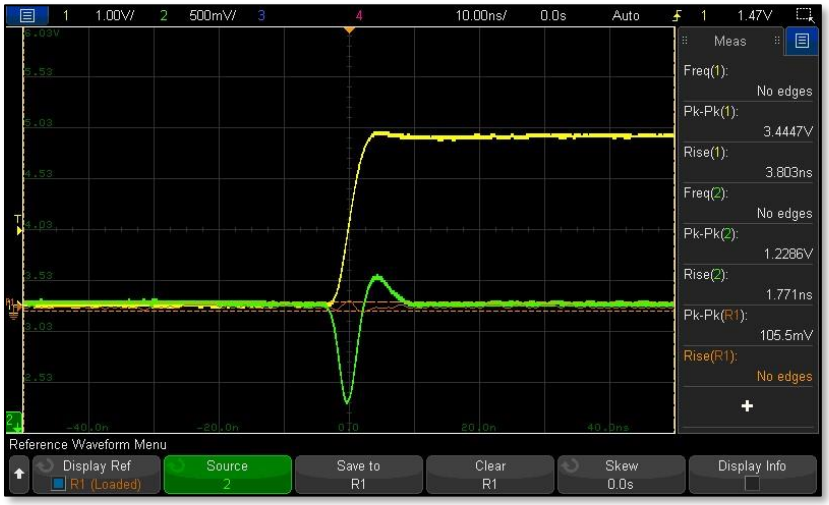

Fig – 5: Noise difference between quiet LOW and quiet HIGH (Bad 2)

- The Fig 5 which is shown analyses the difference in noise when the measurements are taken at the quiet LOW and quiet HIGH test point of another bad layout of the board.
- The quiet low has a peak-to-peak voltage of around 105.5mV and for quiet HIGH, it is around 1.23V.
- Introducing a return plane helps in reducing the loop area and noise emission but the capacitor's distance still introduces inductance, thus reducing its filtering effectiveness.
- This approach improves performance but not much and may still create issues for high-speed components.

Part 3: Good layout: has return plane and decoupling capacitor is close.

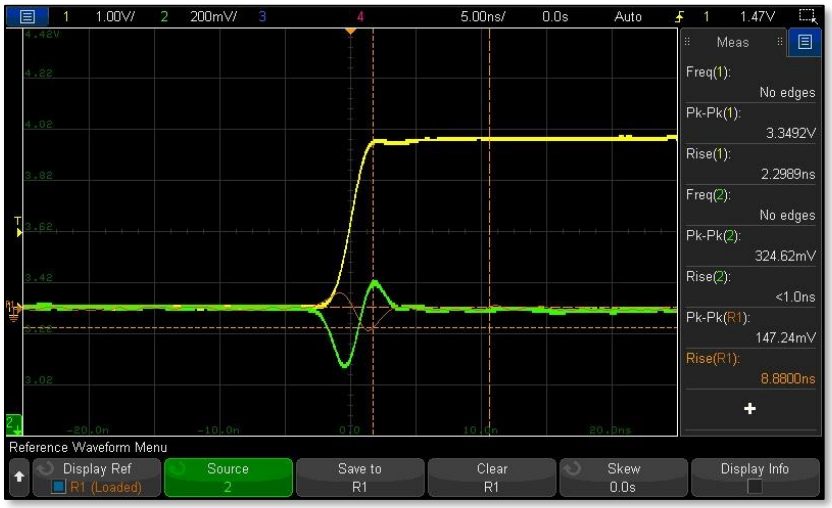

Fig – 6: Noise difference between quiet LOW and quiet HIGH (Good)

- The Fig 6 which is shown analyses the difference in noise when the measurements are taken at the quiet LOW and the quiet HIGH test point of good layout of the board.
- The quiet low has a peak-to-peak voltage of around 147.24mV and for quiet HIGH, it is very less too, around 324.62mV.
- Minimized loop area and close capacitor placement ensures quick response to power demands and effective high-frequency noise filtering.
- This system has highest level of system stability and performance, ideal for sensitive and critical applications.

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Fig – 7: Comparison between Good and Bad 1 layout

- Figure 7 presents a clear comparison in noise levels. The green trace illustrates the relatively high noise associated with a well-designed layout, where the decoupling capacitor is positioned close to the IC and is supported by a return plane. Conversely, the blue trace shows the noise level for a poorly designed layout, with no return plane and the decoupling capacitor placed at a distance from the IC.

Fig – 8: Comparison between Good and Bad 2 layout

- A clear difference in noise levels is shown in Figure 7. With a return plane and a decoupling capacitor next to the integrated circuit (IC), the improved configuration with the green trace represents a greater noise level. Conversely, the blue trace indicates the noise level corresponding to a less-than-ideal architecture, in which the return plane is absent and the decoupling capacitor is placed distant from the IC.

Conclusion / Inference:

- The bad layout will be a better choice if the decoupling capacitor is removed from the good layout because it still exists even if it is far away.
- Good hex inverters have superior performance because of proximal decoupling capacitors and designed return pathways, which efficiently reduce switching noise.
- Future designs will place a higher priority on circuit robustness and noise reduction, with a focus on carefully placing decoupling capacitors and low-pass filters.
- Improvements will also include schematic sectioning for easier reading and cost effectiveness, as well as isolation switches and pull-up resistors to guarantee stability.