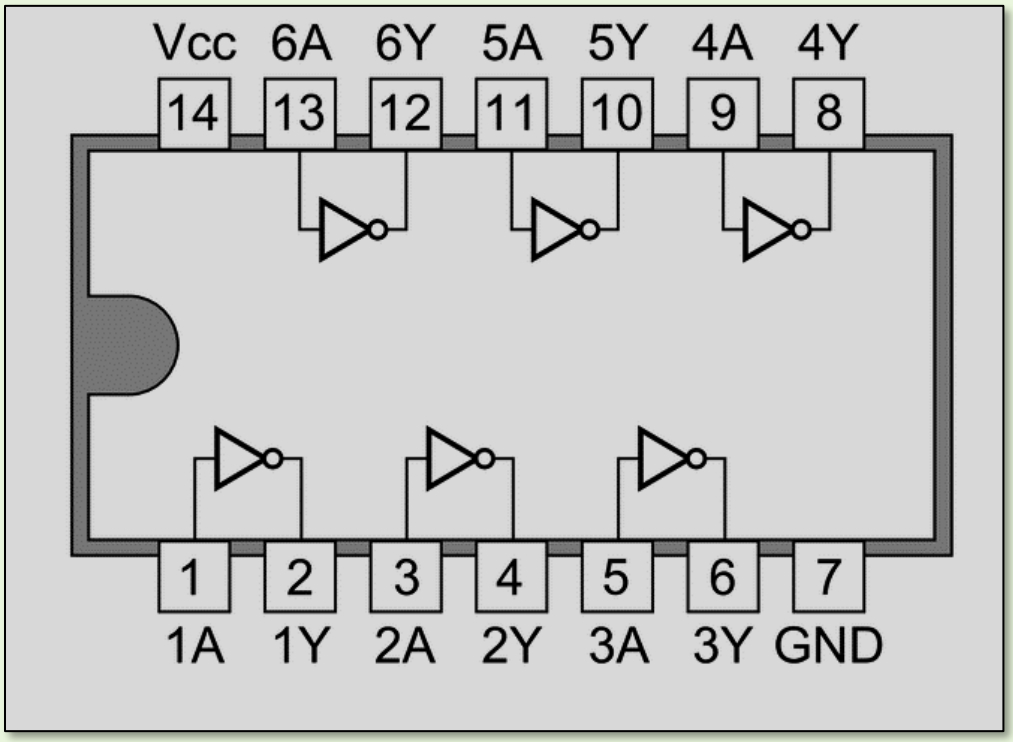
Practical PCB Design and Manufacture

Switching Noise with Good and Bad Layout
BOARD 2
PCB Design



Practical PCB Design and Manufacture

TABLE OF CONTENTS

Practical PCB Design and Manufacture

☞ *INTRODUCTION*

The primary objective of this laboratory exercise is to deepen the understanding of electronic circuits through hands-on experience with building and analyzing them. Specifically, the lab focuses on the construction of a circuit incorporating a hex inverter and familiarizes us with its operational characteristics and applications. An integral component of this circuit is the 555 timer IC, which is utilized to generate a 500 Hz signal. This signal serves as the input for the hex inverter, allowing us to observe and measure the switching noise produced by the hex inverter integrated circuit (IC) under operational conditions.

Furthermore, this lab introduces a comparative study designed to highlight the importance of good engineering and design practices. To this end, we have constructed two identical circuits on a single platform, referred to as board 2. These circuits are differentiated solely by their adherence to design principles: one circuit will be assembled following best design practices, while its counterpart will be built in a manner reminiscent of engineers unfamiliar with such practices. This juxtaposition aims to underscore the impact of design choices on circuit performance and reliability.

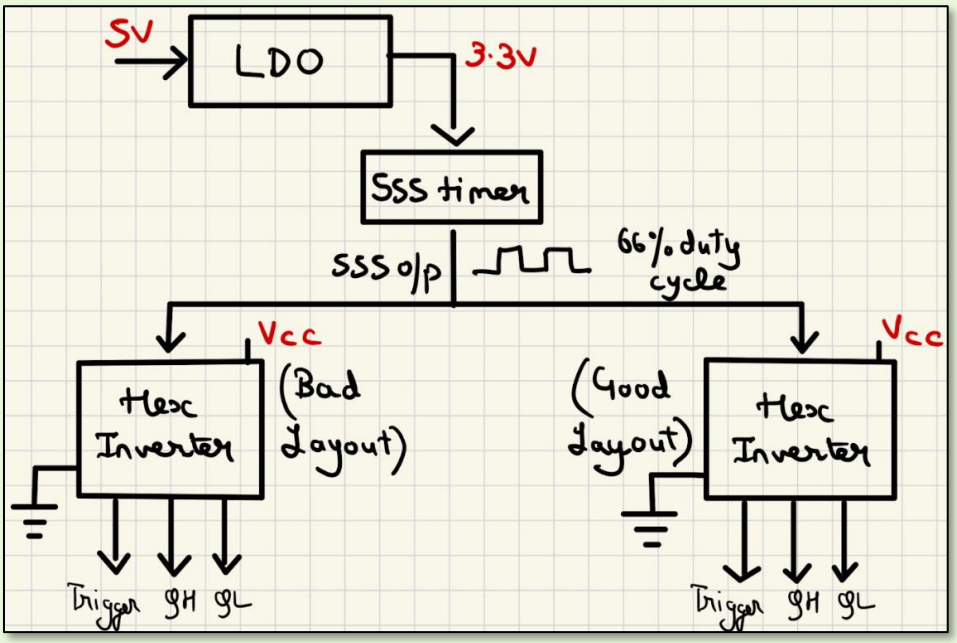
☞ *PLAN OF RECORD*

The plan of record for building my Board 2 is as follows:

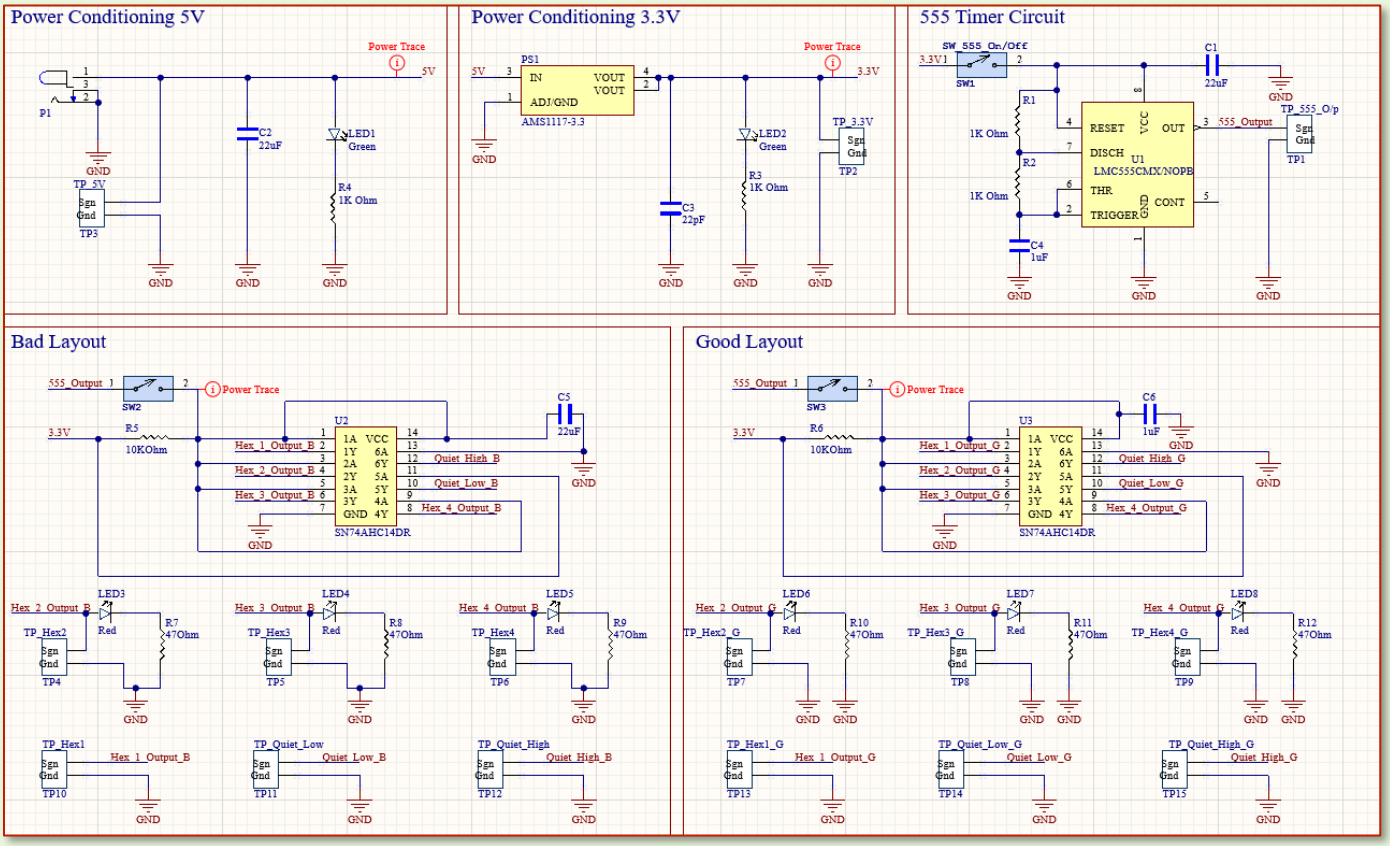
1. An LDO was used to convert 5V to 3.3V; voltages at test points were verified.
2. A 555 timer was set up for a 500 Hz output with a 66% duty cycle.
3. Circuit layouts were compared using four inputs on two hex inverters, highlighting good versus poor practices.
4. Switches employed to alternate the 555-timer output between hex inverters, demonstrating both layout qualities. It was ensured that all unselected inputs were held HIGH to prevent switching.
5. Red LEDs and 47-ohm resistors were utilized as indicators for three hex inverter outputs, lighting up upon activation.
6. The output from the fourth hex inverter pin was used as an oscilloscope trigger for detailed analysis.
7. One output from each hex inverter was maintained at a steady HIGH and another at a steady LOW to observe switching noise effects.
8. The board was designed with a clear distinction: one side followed best practices, including a ground plane, while the other exhibited a poor layout, with far-placed decoupling capacitors from Vcc.
9. The better-designed side included a ground plane for improved performance.

Practical PCB Design and Manufacture

ROUGH SKETCH OF SKEMATIC

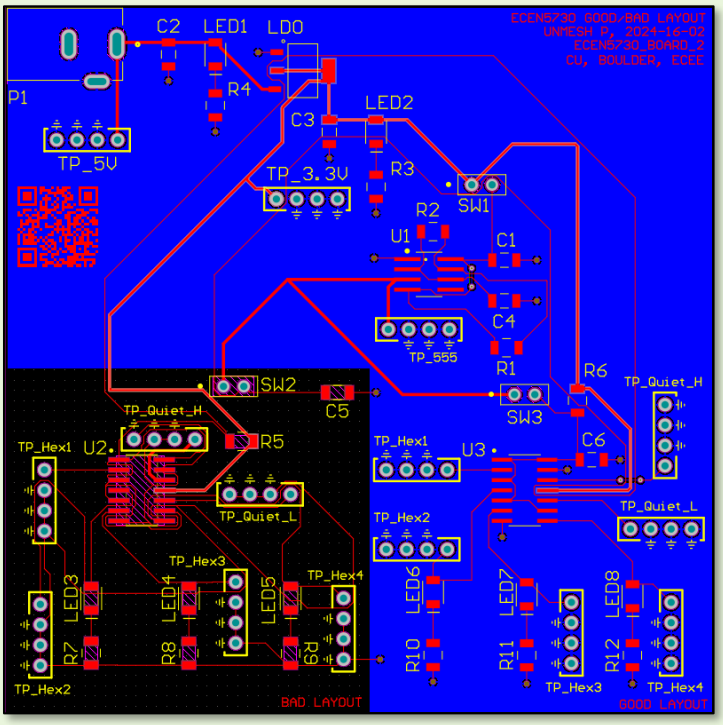


SKEMATIC CAPTURE ON ALTIUM

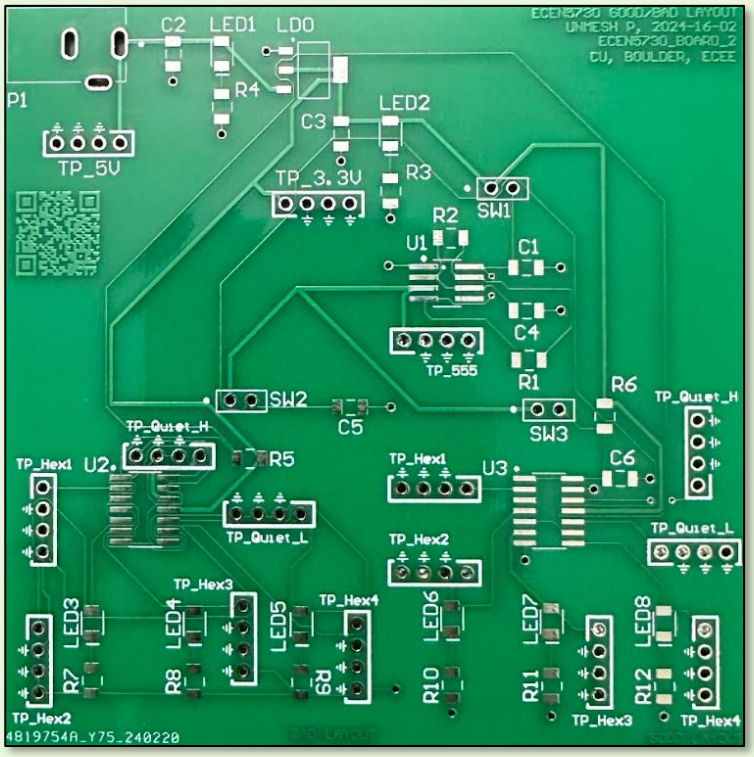


Practical PCB Design and Manufacture

☞ *BOARD LAYOUT ON ALTIUM*

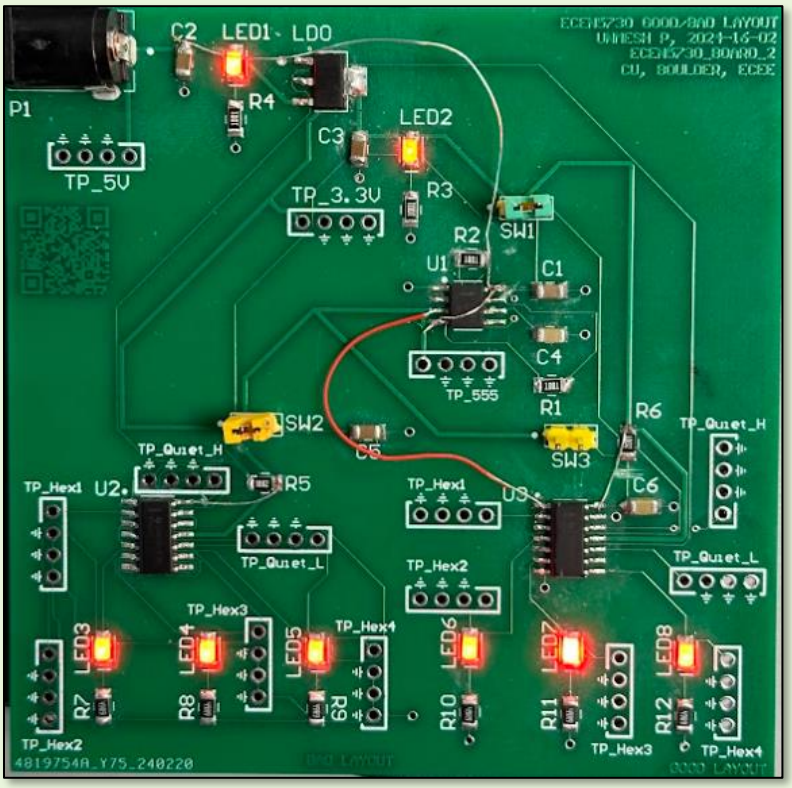


☞ *UNASSEMBLED BOARD PICTURE*



Practical PCB Design and Manufacture

☞ *ASSEMBLED WORKING BOARD*



☞ *CALCULATIONS*

Time High (T_1) = $0.693 \times (R_1 + R_2) \times C_1$
= 1.386 ms

Time Low (T_2) = $0.693 \times R_2 \times C_1$
= 0.693 ms

Time Period (T) = $0.693 \times (R_1 + 2R_2) \times C_1$
= 2.079 ms

Frequency (F) = $\frac{1.44}{(R_1 + 2R_2) \times C_1}$ = 481 Hz

Duty cycle = $\frac{R_1 + R_2}{(R_1 + 2R_2)} \times 100$ = 66.67 %

Practical PCB Design and Manufacture

☞ *WHAT WORKED*

1. The LED1 turned ON and a voltage of 5V was seen at the 5V rail test point to conclude that the board was in a working state.

2. The LED2 turned ON at 3.3V which was used to confirm that the LDO had properly converted the 5V to 3.3V.

3. After checking the output of the 555-timer circuit, a proper square wave was observed with a duty cycle of approximately 66%.

   The figures given below show the output of the 555-timer circuit with a Peak-to-Peak voltage of around 5.3V and a frequency of 500+ Hz.

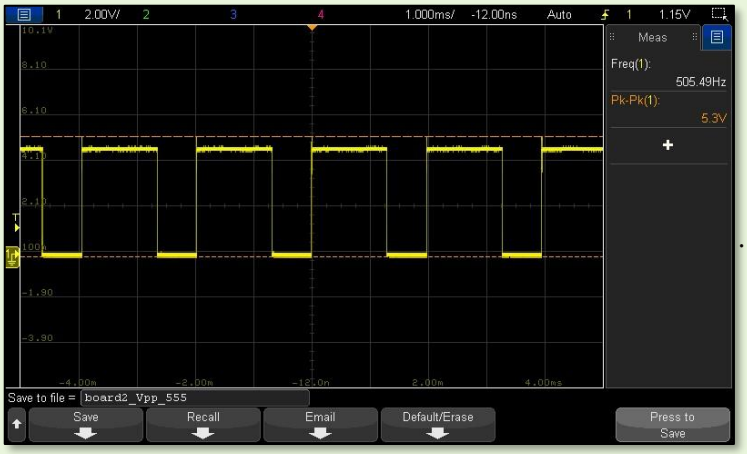


Fig 1: 555 timer output

Fig 2: 555 Output Rise Time

- The 555 timer IC is renowned for its versatility in generating precise time delays and oscillations. In astable mode, it can produce a continuous square wave output, the frequency of which is determined by external resistors and a capacitor.
- This frequency can be mathematically calculated, allowing for a wide range of applications. The duty cycle of the output wave can also be adjusted, but without additional components, it typically cannot go below 50%.
- The rise and fall times of the output wave are generally fast, making it suitable for digital circuits. However, these times can vary based on the specific 555 timer version and the external load it drives.
- We can see in the above figure a rise time of about 82ns which matches the value mentioned in the datasheet of the Slow Timer IC NE555DR.

Practical PCB Design and Manufacture

☞ *SCOPE ANALYSIS*

For the good layout, we can see the peak-to-peak Voltage of around 55.28mV for **quiet low noise** due to the hex inverter.

Fig 3: Hex Good Quiet Low

- Implementing a quiet, low-noise PCB layout is crucial for optimal performance, especially in sensitive electronic circuits.
- Placing decoupling capacitors close to the hex inverter significantly reduces noise. This proximity minimizes loop area and inductance, leading to improved noise suppression.
- Decoupling capacitors act as local energy reservoirs for the hex inverter, providing stable power supply and reducing transient voltage spikes.
- A well-thought-out layout with strategically placed decoupling capacitors enhances signal integrity and overall circuit reliability.

For the good layout, we can see the peak-to-peak Voltage of around 259.3mV for **quiet high noise** due to the hex inverter.

Fig 4: Hex Good Quiet High

Practical PCB Design and Manufacture

- Managing high noise in PCB layouts requires strategic planning and design, especially when interfacing with components like hex inverters.
- In environments with inherently high noise, decoupling capacitors should still be placed as close to the hex inverter as possible. This helps in mitigating noise at the source.
- The use of multiple decoupling capacitors with different values can target a broader range of noise frequencies, from low to high.
- Incorporating ground planes and shielding techniques can further isolate sensitive components from high noise sources, enhancing circuit robustness.
- While high noise can be challenging, a combination of close-placed decoupling capacitors and advanced noise reduction techniques ensures stable operation and minimizes interference.

For the bad layout, we can see the peak-to-peak Voltage of around 62.94mV for **quiet low noise** due to the hex inverter.

Fig 5: Hex Bad Quiet Low

- Quiet low noise in PCB design is critical for optimal performance, especially in sensitive applications.
- A common design oversight is placing decoupling capacitors far from their corresponding ICs, such as a hex inverter, which can introduce noise due to longer trace lengths.
- The absence of a dedicated return plane further exacerbates noise issues by increasing ground loop area and impedance, leading to inefficient noise suppression.
- This layout can result in increased electromagnetic interference (EMI), reduced signal integrity, and potential operational instability in circuits.
- To mitigate these issues, it's essential to place decoupling capacitors close to their ICs and incorporate a well-designed return plane for effective noise management and improved circuit performance.

Practical PCB Design and Manufacture

For the bad layout, we can see the peak-to-peak Voltage of around 723.6mV for **quiet high noise** due to the hex inverter.

Fig 6: Hex Bad Quiet High

- Achieving quiet high performance in PCB design demands meticulous layout considerations, particularly for high-speed or high-frequency circuits.
- A notable layout flaw is the improper placement of components, such as positioning high-speed signal lines too close to sensitive analog areas, leading to crosstalk and unwanted interference.
- Additionally, neglecting the integration of impedance matching techniques can result in signal reflections and loss, further degrading performance.
- The absence of a strategic ground plane arrangement, or poorly implemented ground planes, can lead to ineffective shielding and increased susceptibility to external noise sources.
- Ignoring the necessity for differential pairs or controlled impedance traces in high-speed designs can exacerbate signal integrity issues.
- To circumvent these problems, careful planning of trace routing, component placement, and ground plane design is crucial for minimizing noise and ensuring reliable, high-performance operation of the PCB.

Thus, a good PCB layout features a ground plane and closely placed decoupling capacitors to the ICs, ensuring minimal noise, optimal signal integrity, and reduced electromagnetic interference (EMI). This design facilitates efficient power delivery and grounding, enhancing overall circuit performance. In contrast, a bad layout lacks a ground plane and places decoupling capacitors far from ICs, leading to increased noise, potential operational instability, and greater susceptibility to EMI, compromising the circuit's reliability and performance.

Practical PCB Design and Manufacture

☞ *HEX OUTPUT*

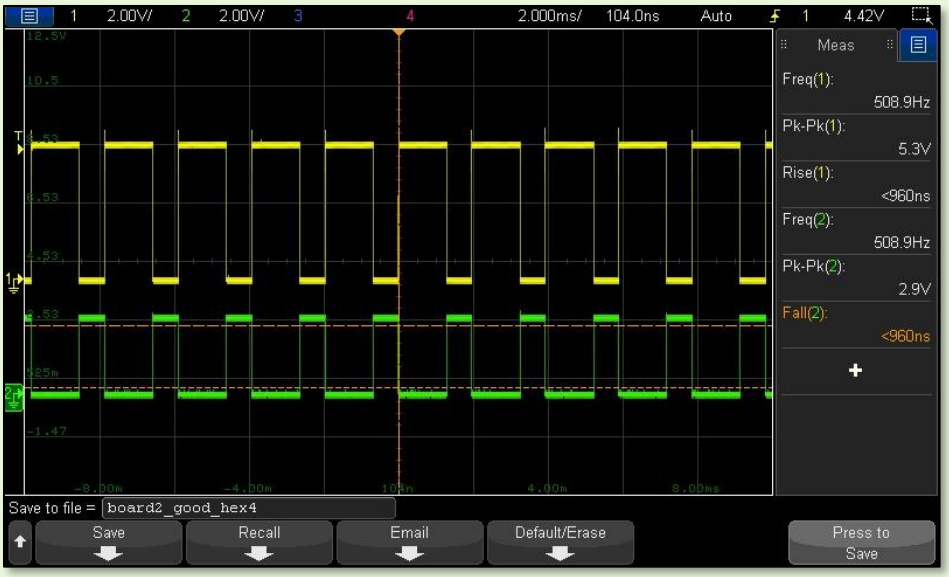
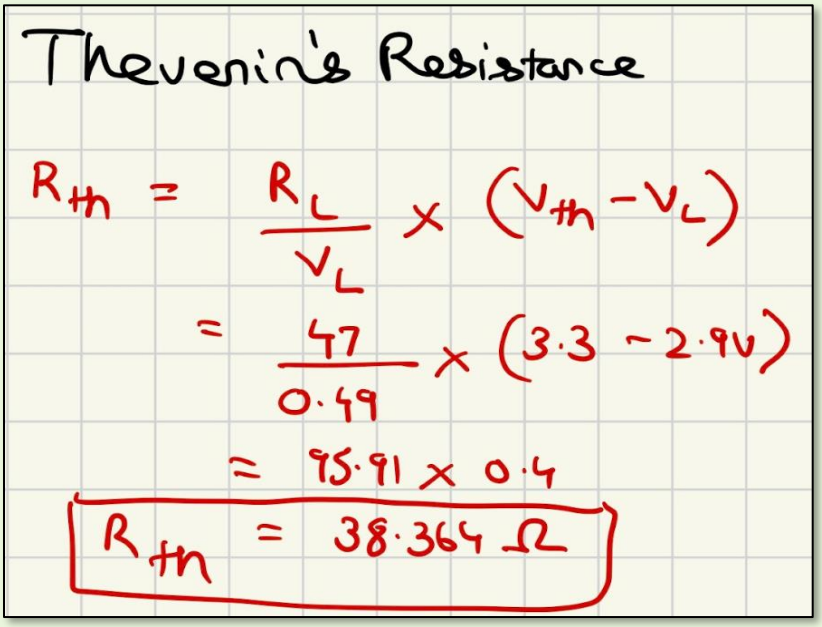


Fig 7: Hex Output Inverted

We see the inverted waveform at the output of the hex inverter test point I have added in my board layout.

☞ *THEVENIN'S RESISTANCE*



Practical PCB Design and Manufacture

☞ BEST DESIGN PRACTICES

In my PCB design, which contrasts effective and ineffective strategies, I have incorporated numerous advanced techniques to boost both its performance and reliability:

- **Clean Power Supply:** I ensured the power supply was meticulously regulated to mitigate voltage variations, ensuring a stable energy flow.
- **Noise Filtering Capacitor:** I placed a 1 µF ceramic capacitor adjacent to the 555 timer's VCC and GND pins, acting as a filter for any electrical noise.
- **Optimized Trace Layout:** By designing the PCB with minimized trace lengths between essential components, I effectively reduced noise and electromagnetic interference.
- **Integrated Ground Plane:** A ground plane was incorporated to diminish ground loop interference and improve signal integrity, providing a stable reference point.
- **Accessible Test Points:** I strategically positioned test points for critical signals, including the output and power supply, to facilitate easy diagnostics and testing.
- **Strategic Component Placement:** I arranged components with sufficient spacing to prevent short circuits and to allow for thermal expansion, ensuring long-term stability.

☞ MEASURED VALUES

Layout	Rise Time	Quiet Low Noise	Quiet High Noise
Good Hex layout	1.6ns	55.28mV	259.3mV
Bad Hex Layout	5.6ns	62.94mV	723.6mV

☞ MISTAKES MADE

In the rush to submit the design files for the board, I accidently printed my name and QR code on the top layer of the board instead of the top -overlay layer.

I encountered a few hard errors on the board. As shown in the part of the schematic below, I found out that the power supply to the hex inverter was being pulled up by the resistor which was supposed to go through the hex inverter inputs. The main logic was to directly give 3.3V to the Vcc pin of the hex inverter.

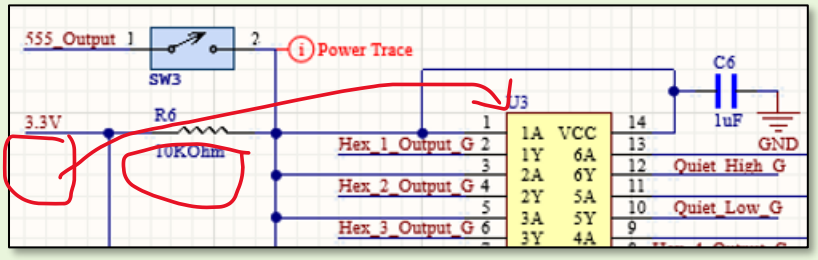


Fig 8: Schematic snippet

Practical PCB Design and Manufacture

I solved this problem by cutting out the trace as shown in Fig 9 and Fig 10 below and directly giving 3.3V supply using wires.

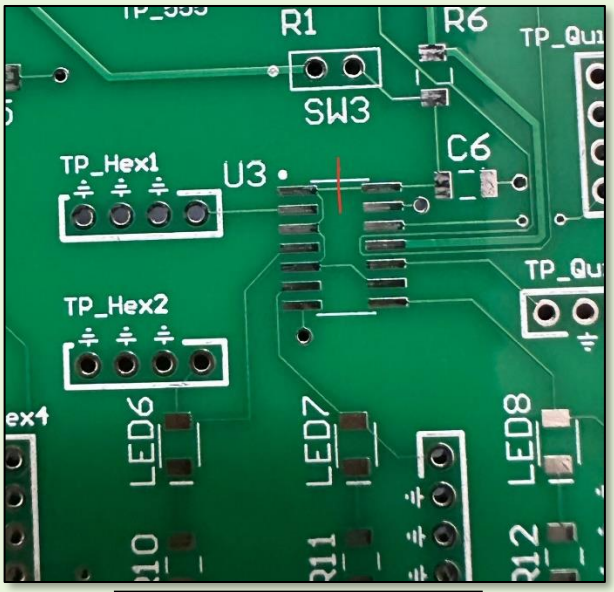


Fig 9: Good layout

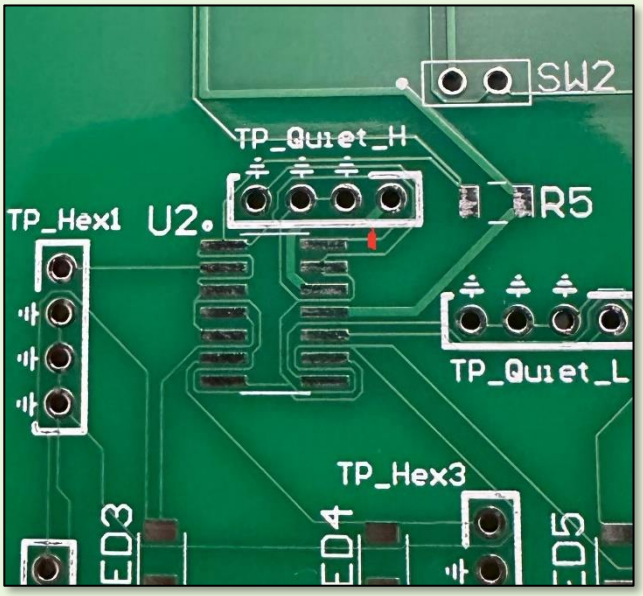


Fig 10: Bad layout

I was lucky not to face any soft errors as well and my outputs matched my calculations as shown in the table given above.

☞ ANALYSIS AND EFFECTIVE LEARNINGS

1. Every component of the circuit functioned after solving the hard errors.
2. Reviewing the design is important before submitting and rushing to submit the design files caused hard errors which took time to debug.
3. The decoupling capacitor is positioned near the integrated circuit (IC) to minimize loop inductance and prevent crosstalk.
4. The observed increase in rise time is attributed to the choice of a slower 555 timer.
5. The NPN transistor facilitates rapid switching on the falling edge.
6. The LED circuit is estimated to draw a current of approximately 1.9mA.

☞ CONCLUSION

Ground bounce occurs when changing return currents navigate through the high inductance of a narrow, shared return path, leading to noise. Similarly, power rail collapse happens due to the inductance between IC power pins and decoupling capacitors. Reducing these effects involves strategic design, such as placing decoupling capacitors close to ICs, utilizing ground planes, adding well-named test points, and incorporating isolation switches, indicator LEDs, and spring probe tips to minimize noise and facilitate debugging.