CPE 301 – Embedded Systems Design Lab

Lab # 03 – Memory

Spring 2022

Objectives:

1. To combine multiple RAM chips to expand word size and/or the number of words.
2. To become familiar with the basic signals and controls used in RAM memory circuits.

Required Equipment:

1. Laboratory Oscilloscope
2. Laboratory Power Supply
3. DIP Bar Graph LED
4. DIP 10-position switch array
5. DIP Push-button
6. 330Ω SIP Resistor (for LEDs)
7. 1K-4.7KΩ SIP Resistor (for switches)
8. 1K-10KΩ Axial Resistor (for buttons)
9. DIP 74LS04
10. DIP 74LS189
11. Solderless Breadboard
12. Jumper Kit

BEFORE THE LAB: Find the datasheets for the 74LS139 and the 74LS04 and read their functional descriptions on the first few pages. Then read the below background information on RAM chips and memory circuits.

Background:

Memory devices are used in digital systems to store digital information. A specific storage location in memory is identified with a unique binary value called an address. Accessing data stored at a specified address is referred to as a read operation. Storing new data at a specified address is referred to as a write operation.

Static vs Dynamic RAM

Random access memory (RAM) is the term used frequently for memory that can be read from or written into with equal ease (actually RWM). Ordinary semiconductor RAM devices are said to be "volatile" because the information stored in the device is lost if the electrical power for the memory is removed. Semiconductor RAM may be either static, which does not need the stored data to be periodically refreshed, or dynamic, which does require the data to be periodically rewritten into the memory cells.

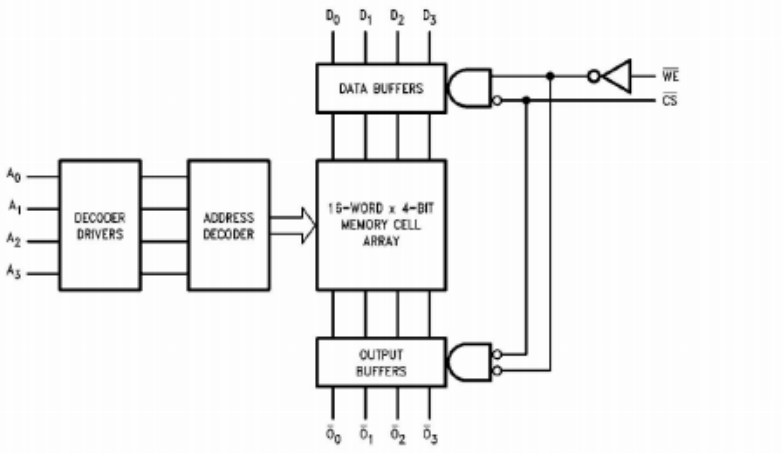
RAM Controls & Signals

Static RAM memory chips have the following types of pins:

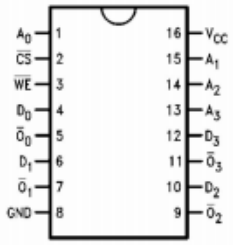
1. Address pins that are used to select a specific memory location2
2. Data pins that are used to input the data into and/or output the data from the addressed memory location
3. A chip select pin to enable a specific chip (or set of chips) in a memory system
4. A Read/Write pin to control the chip's read or write function (read = 1 and write = 0).

The block diagram for an example static RAM chip containing 16 4-bit words (16X4) is shown in the Block Diagram Connection Diagram below.

Block Diagram



Connection Diagram



Memory Organization

Many different memory devices (with different part numbers) are available that differ in word size and memory capacity. The memory chip's word size is the number of bits that are accessed simultaneously in the chip with a given address. The memory capacity for a chip is the total number of words (2n , where n = number of address bits) that can be addressed on the chip. Several memory chips can be interconnected to expand the total system memory. This expansion can be in word size, total number of addressable words, or both.

Tristate Bus Drivers

In addition to high and low output levels, a tri-state output device also has a high impedance output condition. This type of output structure is normally used to connect several possible sources of digital information to a common bus, such as a data bus in a memory system. Only one source of information will be enabled at a time and allowed to place data on the bus. Most memory chips today have built-in tri-state output buffers for the data pins that are enabled when the chip is selected and a read operation is performed. The source of data for a write operation must also be tristated from the data bus when a write operation is not being performed. Separate tri-state buffer or bus driver chips are available to accomplish this task. The 74LS244 is an example of a tri-state buffer. It contains a total of eight buffers in one chip. NOTE: The 74189 chip has built in tri-state output buffers as shown in the Function Table below.

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Function Table

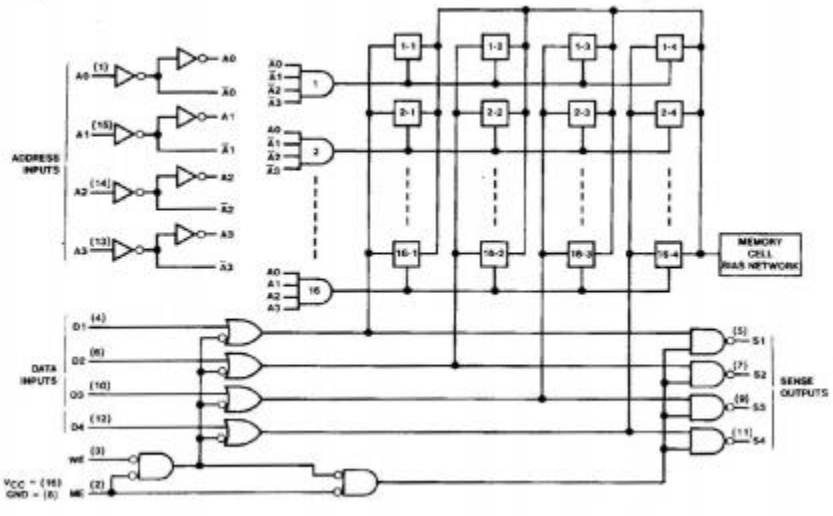
Inputs		Operation	Condition of Outputs
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Storing the Complement

The data outputs are the complements of the data inputs stored in the chip as shown in the Logic Diagram below. In actual use you would need to invert the input data bus with a chip such as a 7404 before connecting it to the 74189. To simplify your breadboard wiring for this lab we will be satisfied that you read the compliments of the inputs and translate them by inverting what you read on the scope when you write your lab report.

Logic Diagram



Procedure:

Complete each part of the lab, answer the questions and include them in your lab report. Be sure to label your answers with respect to their relevant lab part and question number (ex. Part 1 #4c). Find the schematics for both circuits on WebCampus. Any handwritten drawings should be scanned and included alongside the text of your lab report.

Part 1

Construct a 16x8 memory circuit using two 74-189s. The 189 is a 64-bit RAM chip that is arranged in an array that has 16 addresses, with each location being 4 bits wide. A set of switches should be used to select the address location, and a set of LEDs should be used to show the contents of the memory. Use a push-button for the read-write signal. For full credit, include images of your circuit showing the data in the table below stored at the appropriate address. Be sure to take the pictures such that the LEDs and the switches are both visible, and such that the LSB is on the right.

Address	0x00	0x05	0x07	0x0F
Data	0x72	0x22	0x55	0x33

Part 2

Construct a 32x4 memory circuit using two 74-189's. Follow the same data input / output controls as above, however use the CS line of the memory chips as the 5th address bit. This will require decoding, through the use of a 74LS04 inverter. Again, for full credit, include pictures of the following data stored at the corresponding address.

Address	0x00	0x02	0x13	0x1F
Data	0x0A	0x0C	0x03	0x0F

Questions

1. Describe the difference between the circuits in part 1 and part 2. Is the amount of data stored different?
2. Describe the function of the CS pin in Part 2, especially with respect to how it is used to decode the address.
3. Why must the RAM chip be capable of tri-stated output when there is more than one device on a bus?