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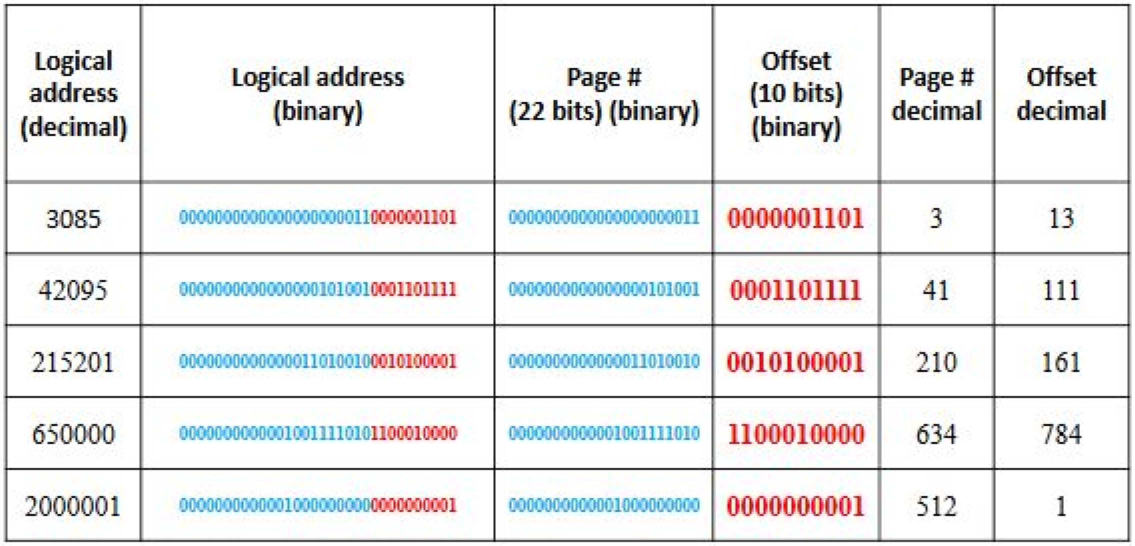
Operating System Concepts

Chapter 8 - Practice Exercises

8.20 Assuming a 1-KB page size, what are the page numbers and offsets for the following address references (provided as decimal numbers):

a. 3085
b. 42095
c. 215201
d. 650000
e. 2000001

Tamaño de página = 2^n = 1024 B = 2^{10} B
# de bits en la parte de Offset(n) = 10
Solución pasos:
1. Convertir la dirección lógica: decimal a binario
2. Divida la dirección binaria en 2 partes (número de página, Offset), Offset: n dígitos
3. Convierte Offset y número de página: binario
 a decimal.



Logical address (decimal)	Logical address (binary)	Page # (22 bits) (binary)	Offset (10 bits) (binary)	Page # decimal	Offset decimal
3085	00000000000000000000110000001101	0000000000000000000011	0000001101	3	13
42095	00000000000000001010010001101111	0000000000000000101001	0001101111	41	111
215201	00000000000000110100100010100001	0000000000000011010010	0010100001	210	161
650000	00000000000010011110101100010000	0000000000001001111010	1100010000	634	784
2000001	00000000000010000000000000000001	0000000000001000000000	0000000001	512	1

8.21 The BTV operating system has a 21-bit virtual address, yet on certain embedded devices, it has only a 16-bit physical address. It also has a 2-KB page size. How many entries are there in each of the following?
a. A conventional, single-level page table
b. An inverted page table

La tabla de páginas convencionales de un solo nivel tendrá 2 entradas.
La tabla de páginas invertidas tendrá 2
S = 32 entradas
10 = 1024

8.22 What is the maximum amount of physical memory?

2_{16} = 65536 (or 64-KB.)

8.23 Consider a logical address space of 256 pages with a 4-KB page size, mapped onto a physical memory of 64 frames.
a. How many bits are required in the logical address?

12+8=20bits

b. How many bits are required in the physical address?

12+6=18bits

8.24 Consider a computer system with a 32-bit logical address and 4-KB page size. The system supports up to 512 MB of physical memory. How many entries are there in each of the following?

220 entradas
512K K/4K = 128K entradas

8.25 Consider a paging system with the page table stored in memory.
a. If a memory reference takes 50 nanoseconds, how long does a paged memory reference take?

400 nanosegundos: 200 nanosegundos de accesso a la tabla de páginas y 200 nanosegundos a la palabra en memoria

b. If we add TLBs, and 75 percent of all page-table references are found in the TLBs, what is the effective memory reference time? (Assume that finding a page-table entry in the TLBs takes 2 nanoseconds, if the entry is present.)

Tiempo efectivo de acceso: 0,75x200nanosegunods +0,25 x400nanosegunods = 250 nanosegundos

8.26 Why are segmentation and paging sometimes combined into one scheme?

8.27 Explain why sharing a reentrant module is easier when segmentation is used than when pure paging is used.

8.28 Consider the following segment table: Segment Base Length
0 219 600
1 2300 14
2 90 100
3 1327 580
4 1952 96
What are the physical addresses for the following logical addresses?
a. 0,430
b. 1,10
c. 2,500
d. 3,400
e. 4,112

0,430	219+430=649
1,10	2300+10=2310
2,500	Invalid
3,400	1327+400=1727
4,112	Invalid

8.29 What is the purpose of paging the page tables?

8.30 Consider the hierarchical paging scheme used by the VAX architecture.How many memory operations are performed when a user program executes a memory-load operation?

8.31 Compare the segmented paging scheme with the hashed page table scheme for handling large address spaces. Under what circumstances is one scheme preferable to the other?

8.32 Consider the Intel address-translation scheme shown in Figure 8.22.
a. Describe all the steps taken by the Intel Pentium in translating a logical address into a physical address.
b. What are the advantages to the operating system of hardware that provides such complicated memory translation?