[1 mark] Which of the following unsigned 8-bit binary to decimal conversions are CORRECT?   
  
i. 111111112 = 25510  
ii. 001111012 = 6010  
iii. 100000012 = 12910

i and iii

i and ii

ii and iii

i only

iii only

[1 mark] This exam has one too many questions   
  
i. oopsie daisy  
ii. oopsie  
iii. oops

i and iii

i and ii

ii and iii

i only

iii only

[1 mark] Which of the following conversions are CORRECT? All binary values are unsigned integer values.  
  
i. 11010012 = 1518  
ii. C316 = 110000112  
iii. 111012 = 1D16

i, ii, and iii

ii and iii

i, and iii

i only

iii only

[1 mark] Which of the following calculations are CORRECT? All binary values are in unsigned integer values.  
  
i. 1012 + 0112 = 10002  
ii. 1102 – 1012 = 1012  
iii. 100002 – 1112 = 10012

i and iii

i only

ii only

ii and iii

iii only

[1 mark] Which of the following statements are CORRECT?  
  
i. Left shifting an unsigned binary value by 2 is equivalent to multiplying the value by 2.  
ii. We need 10 bits to represent 1024 different values.  
iii. An unsigned binary value, 10.101 is equivalent to in decimal.

ii, iii

i and ii

i, ii, and iii

ii only

i only

[1 mark] Which of the following decimal to 7-bit signed binary conversions are CORRECT?  
  
i. -2110 = 11010102 (signed magnitude)  
ii. -2110 = 11010112 (one’s complement)  
iii. -2110 = 11010112 (two’s complement)

iii only

i only

ii only

i and ii

ii and iii

[1 mark] Which of the following conversions are CORRECT? All the hexadecimal values are in textbook floating point format.  
  
i. 3210 = 400616  
ii. 404916 = 51310  
iii. The textbook floating point format consists of 16 bits, 1 bit for the sign of mantissa, 9 bits for the mantissa, 1 bit for the sign of exponent, and 5 bits for the exponent.

i and iii

i only

ii only

ii and iii

i, ii, and iii

[1 mark] Which of the following statements are CORRECT about compression?  
  
i. A compression ratio is 2 if the original message size has been reduced from 20 characters to 10 characters.  
ii. Run-length encoding (RLE) is generally useful for compressing text messages.  
iii. A compression ratio of less than 1 indicates that compression has not been achieved.  
iv. Due to the limitations of human perception, lossy compression is well-suited for audio and graphics data.

i, iii, iv

i only

i and iii

ii and iv

i, ii, iii, and iv

|  |  |
| --- | --- |
| **Letter** | **Code** |
| e | 000 |
| a | 010 |
| space | 111 |
| n | 0010 |
| t | 0110 |
| m | 0111 |
| i | 1000 |
| h | 1010 |
| s | 1011 |
| f | 1101 |
| o | 00110 |
| u | 00111 |
| x | 10010 |
| p | 10011 |
| r | 11000 |
| l | 11001 |

[1 mark] Which of the following Huffman encodings are CORRECT given the Huffman table above?   
  
i. 0000100110 is the Huffman encoding for "eat".  
ii. 1101001101011 is the Huffman encoding for "fox".  
iii. 010100011000 is the Huffman encoding for "air".

i and iii

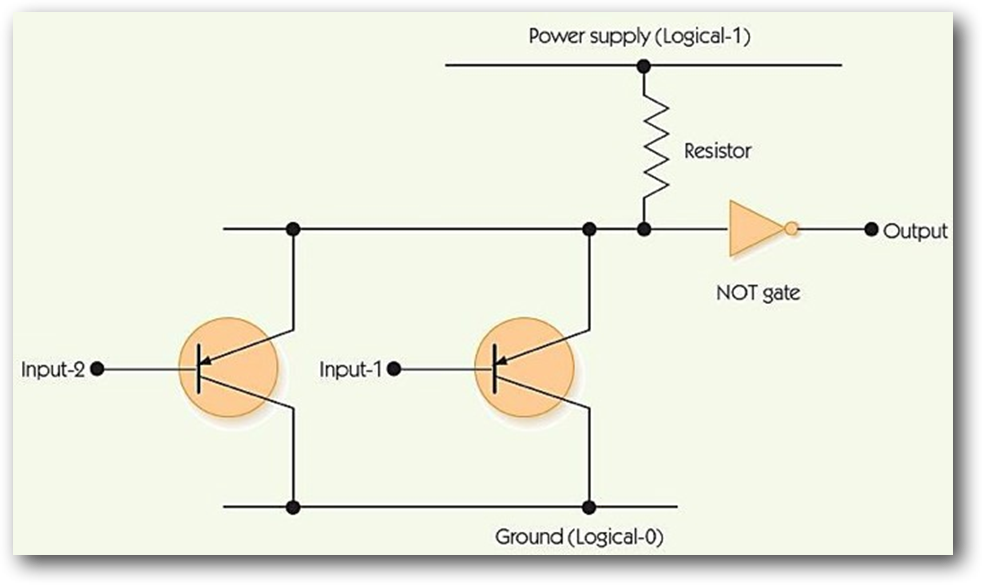
i, ii, and iii

ii and iii

ii only

i only

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Output** |
| **0** | **0** |  |
| **0** | **1** |  |
| **1** | **0** |  |
| **1** | **1** |  |



[1 mark] Which logical gate does the above circuit represent? You may use the truth table to work out the outputs.  
  
i. AND gate  
ii. NAND gate  
iii. OR gate  
iv. NOR gate

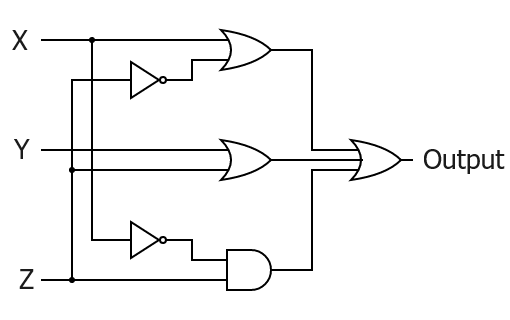
iii

i

ii

iv

None of the options

[1 mark] Which of the following Boolean expressions matches the circuit below?  
  
i.   
ii.   
iii.   
iv.

iv

ii

iii

i

None of the options

[1 mark] Which of the following Boolean expressions would give the truth table below?  
A row of numbers and digits

Description automatically generated with medium confidence  
  
i.   
ii.   
iii.   
iv.

iv

iii

i

ii

None of the options

[1 mark] Which of the following Boolean expressions are logically equivalent?  
  
i.   
ii.   
iii.   
iv.

i, iii, and iv

i and ii

i, ii, and iii

ii and iii

None of the options

[1 mark] Which of the following statements are CORRECT?  
  
i. An output of 1 from a Compare-for-equality (CE) circuit indicates that two values are not equal.  
ii. An n-bit adder can be constructed from n number of 1-bit adders.  
iii. A 1-bit adder takes three inputs (ai, bi, ci) and produces two outputs (si, ci+1).  
iv. Construction of n-bit subtraction circuit is not related to an n-bit adder.

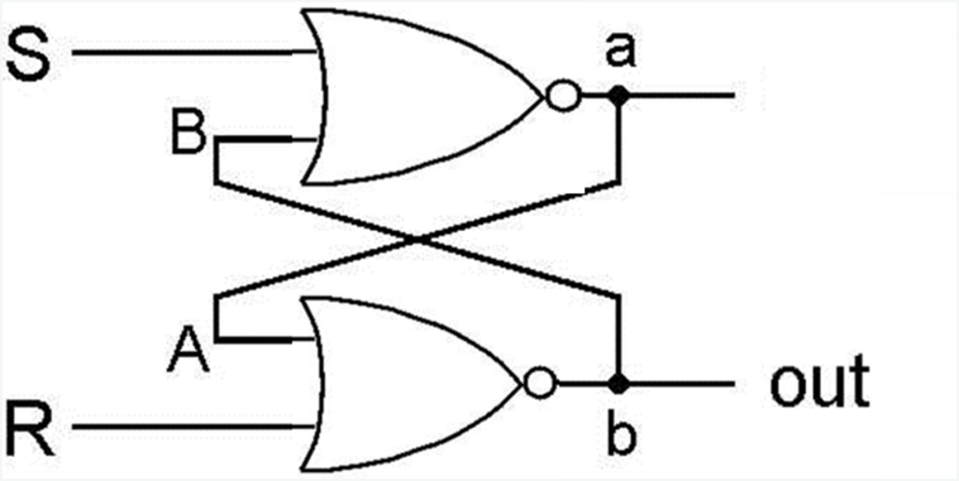
ii and iii

ii only

i, ii, iii, and iv

i, and iii

ii, iii, and iv



[1 mark] Which of the following statements about the NOR SR latches are CORRECT?  
  
i. If S = 0 and R = 0, the output has to be 0.  
ii. If S = 0 and R = 1, the output will be 0.  
iii. If S = 1 and R = 0, the output will be 1.  
iv. If S = 1 and R = 1, this SR latch breaks.

ii, iii, and iv

i, ii, iii, and iv

i, ii and iii

ii and iii

iii and iv

[1 mark] Consider a machine where its memory is organized using a two-dimensional grid, with the same number of rows and columns. The memory row and column decoders each accept 3 bits of input. Which of the following statements about this machine are CORRECT?  
  
i. The Memory Address Register (MAR) is 6 bits in size.  
ii. The largest possible memory address is 63.  
iii. The two-dimension grid approach yields 16 output lines, compared to 64 in the one-dimension approach.

i, ii, and iii

i and ii

i and iii

i only

iii only

[1 mark] What is the output produced by the following assembly language program?  
A white sheet with black text

Description automatically generated

40

10

30

20

80

Here is an assembly language program using the textbook language. Use this program to answer the next two questions. Assume that the first instruction is stored at address 0.

|  |  |  |  |
| --- | --- | --- | --- |
|  | .BEGIN |  | -- line 1 |
|  | IN | NUM1 | -- line 2 |
|  | IN | NUM2 | -- line 3 |
| LOOP: | LOAD | ZERO | -- line 4 |
|  | COMPARE | NUM2 | -- line 5 |
|  | JUMPLT | END | -- line 6 |
|  | LOAD | RESULT | -- line 7 |
|  | ADD | NUM1 | -- line 8 |
|  | STORE | RESULT | -- line 9 |
|  |  |  |  |
|  | INCREMENT | NUM1 | -- line 10 |
|  | DECREMENT | NUM2 | -- line 11 |
|  | JUMP | LOOP | -- line 12 |
| END: | OUT | RESULT | -- line 13 |
|  | HALT |  | -- line 14 |
| ZERO: | .DATA | 0 | -- line 15 |
| NUM1: | .DATA | 0 | -- line 16 |
| NUM2: | .DATA | 0 | -- line 17 |
| RESULT: | .DATA | 0 | -- line 18 |
|  | .END |  | -- line 19 |

[1 mark] Which of the following statements are CORRECT?  
  
i. The output when this program runs with inputs of 10 and 1 (in that order) is 21.  
ii. The output when this program runs with inputs of 100 and 0 (in that order) is 100.  
iii. Regardless of the input, whenever the program ends, the EQ condition code is set to 1, while the GT and LT condition codes are set to 0.

i and ii

ii and iii

i, ii, and iii

ii only

i only

[1 mark] Which of the following statements are CORRECT?   
i. The machine code in hexadecimal for the instruction at line 2 is D01016.  
ii. The machine code in hexadecimal for the instruction at line 14 is F00016.  
iii. .DATA pseudo-ops are stored as 16-bit 2’s complement value.

ii and iii

i and iii

ii only

i only

i, ii, and iii

Here is a machine code program using the textbook assembly language. Assume that the first instruction is stored at address 0.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1101 | 0000 | 0000 | 1100 | -- line 1 |
| 0000 | 0000 | 0000 | 1011 | -- line 2 |
| 0111 | 0000 | 0000 | 1101 | -- line 3 |
| 1010 | 0000 | 0000 | 1001 | -- line 4 |
| 0000 | 0000 | 0000 | 1111 | -- line 5 |
| 0101 | 0000 | 0000 | 1100 | -- line 6 |
| 0001 | 0000 | 0000 | 1111 | -- line 7 |
| 0100 | 0000 | 0000 | 1101 | -- line 8 |
| 1000 | 0000 | 0000 | 0001 | -- line 9 |
| 1110 | 0000 | 0000 | 1111 | -- line 10 |
| 1111 | 0000 | 0000 | 0000 | -- line 11 |
| 0000 | 0000 | 0000 | 0000 | -- line 12 |
| 1111 | 1111 | 1111 | 1111 | -- line 13 |
| 0000 | 0000 | 0000 | 0000 | -- line 14 |
| 1111 | 1111 | 1111 | 1111 | -- line 15 |
| 0000 | 0000 | 0000 | 0000 | -- line 16 |

[1 mark] Which of the following statements are CORRECT?  
i. The assembly language instruction for line 13 is HALT.  
ii. The code contains five .DATA pseudo-ops, three instances of 0 and two instances of -1.  
iii. The assembly language instruction for line 5 is LOAD 15

ii and iii

i and ii

i and iii

ii only

iii only

**get num1**

**get num2**

**get stop**

**if stop = 0 then**

**print num1**

**else**

**count ← 0**

**while count < stop**

**print num1**

**print ","**

**temp ← num1 + num2**

**num1 ← num2**

**num2 ← temp**

**count ← count + 1**

**end while**

**end if**

[1 mark] Which of the following statements are CORRECT given the pseudocode algorithm above?  
  
i. The output when this algorithm runs with inputs of 0, 1, and 4 (in that order) is 0,1,1,2,3,  
ii. The output when this algorithm runs with inputs of 0, 1, and 4 (in that order) is 0,1,1,2,  
iii. The three basic pseudocode constructs are sequential, conditional, and loop constructs.

ii and iii

i and ii

i only

iii only

i and iii