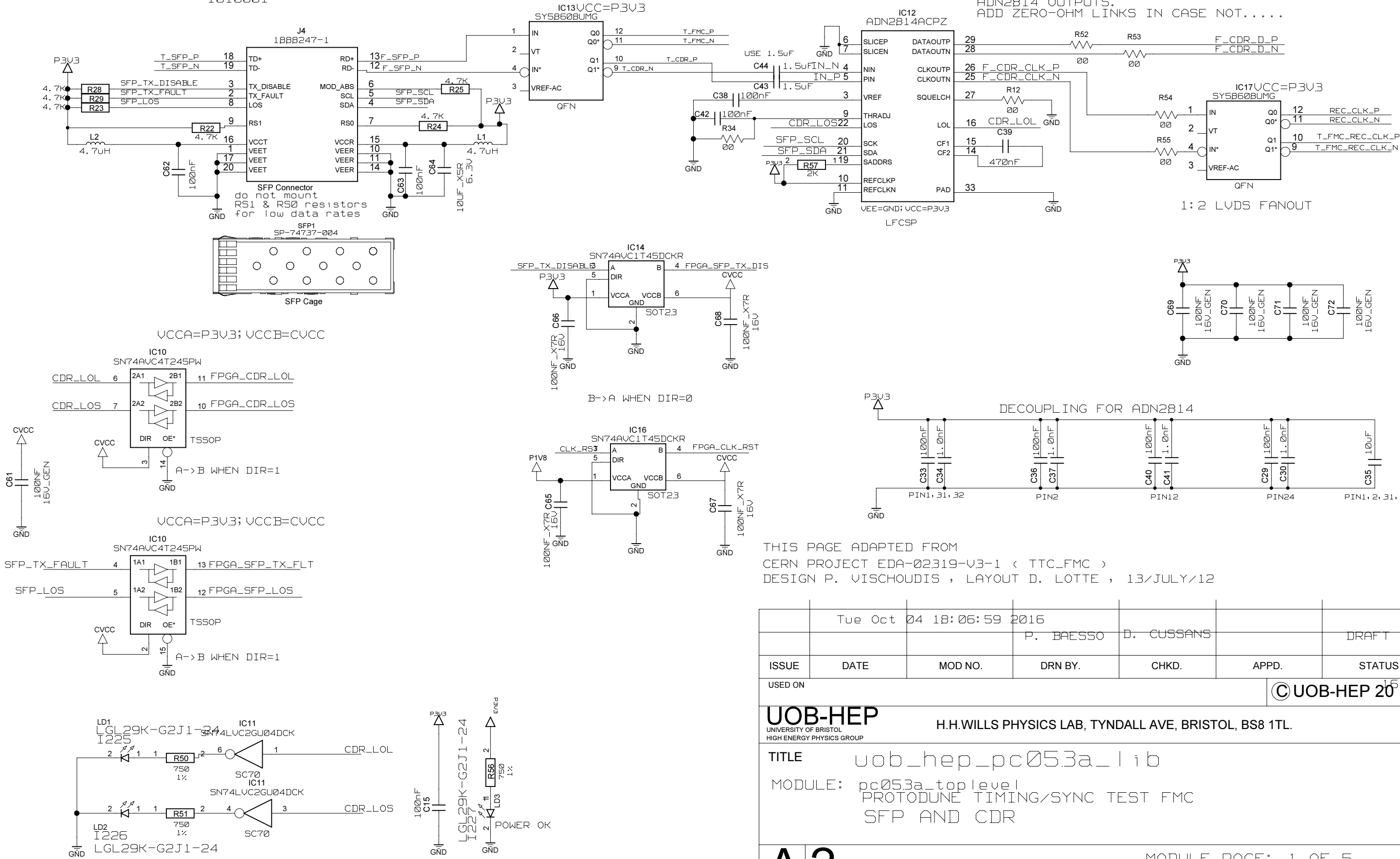


SFP I2C ADDRESSES:  
1010000 AND  
1010001

CLOCK AND DATA RECOVERY (CDR)

CDR I2C ADDRESS:  
1100000 (SADDRS=1)

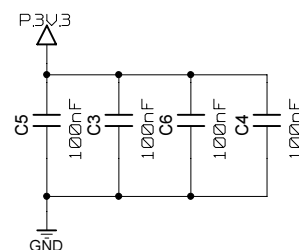
SHOULD BE ABLE TO DC COUPLE  
ADN2814 OUTPUTS.  
ADD ZERO-OHM LINKS IN CASE NOT.....



THIS PAGE ADAPTED FROM  
CERN PROJECT EDA-02319-V3-1 ( TTC\_FMC )  
DESIGN P. VISCHOU DIS , LAYOUT D. LOTTE , 13/JULY/12

	Tue Oct 04 18:06:59 2016					
	P. BAESSO	D. CUSSANS			DRAFT	
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
USED ON					© UOB-HEP 2016	
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TITLE		uob_hep_pc053a_lib				
MODULE:		pc053a_top level PROTODUNE TIMING/SYNC TEST FMC SFP AND CDR				
A2		MODULE PAGE: 1 OF 5 OVERALL PAGE: 1 OF 5				
		TOTAL NO. OF SHEETS				





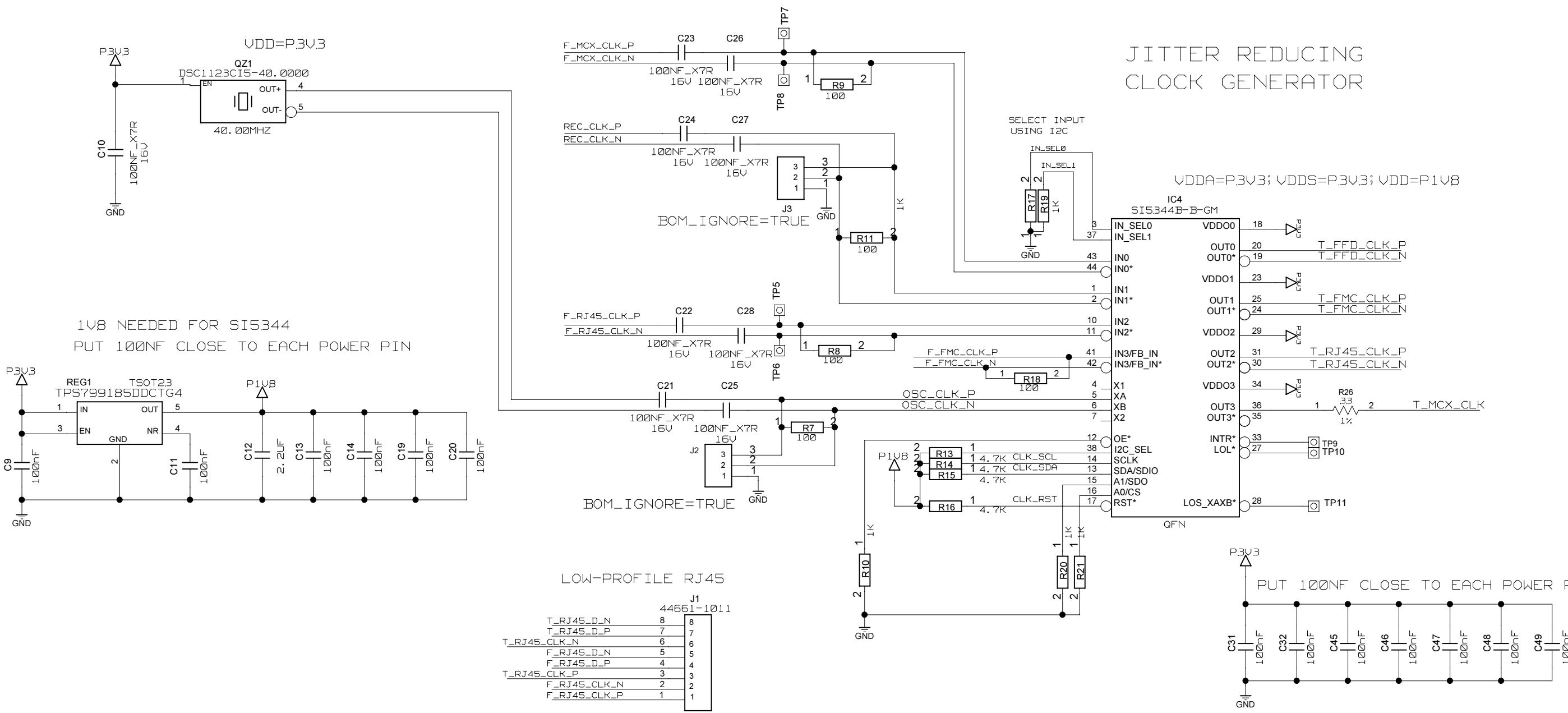
A	2
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A

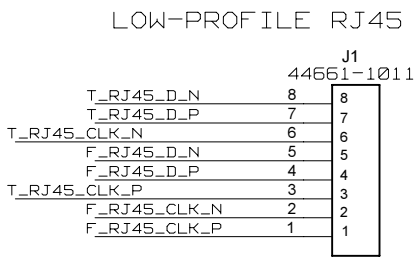
B

C

A 2



JITTER REDUCING  
CLOCK GENERATOR



	Tue Oct 04 18:07:00 2016				
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TITLE		uob_hep_pc05.3a_lib			
MODULE:		pc05.3a_toplevel			
		PROTODUNE TIMING/SYNC TEST FMC			
		CLOCK GENERATOR , RJ45 CONNECTORS			
A	2	MODULE PAGE: 4 OF 5			
		OVERALL PAGE: 4 OF 5			
		TOTAL NO. OF SHEETS			

DIODE VF ~ 2.2V  
--> DROP ACROSS RESISTOR = 3.3 - 2.2 = 1.1V  
WANT < 25MA --> R > 1.1V/0.025A = 44 OHMS

