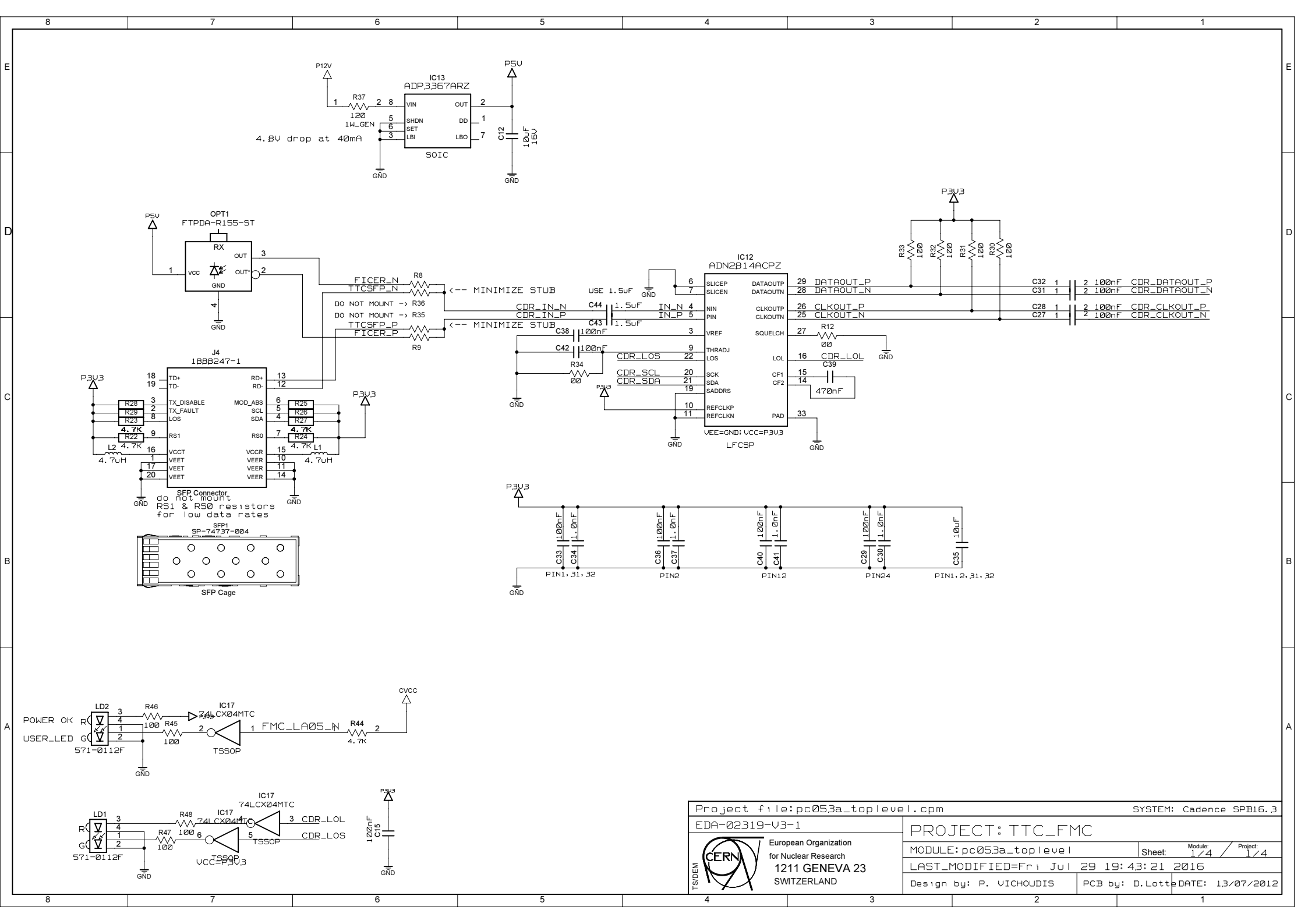
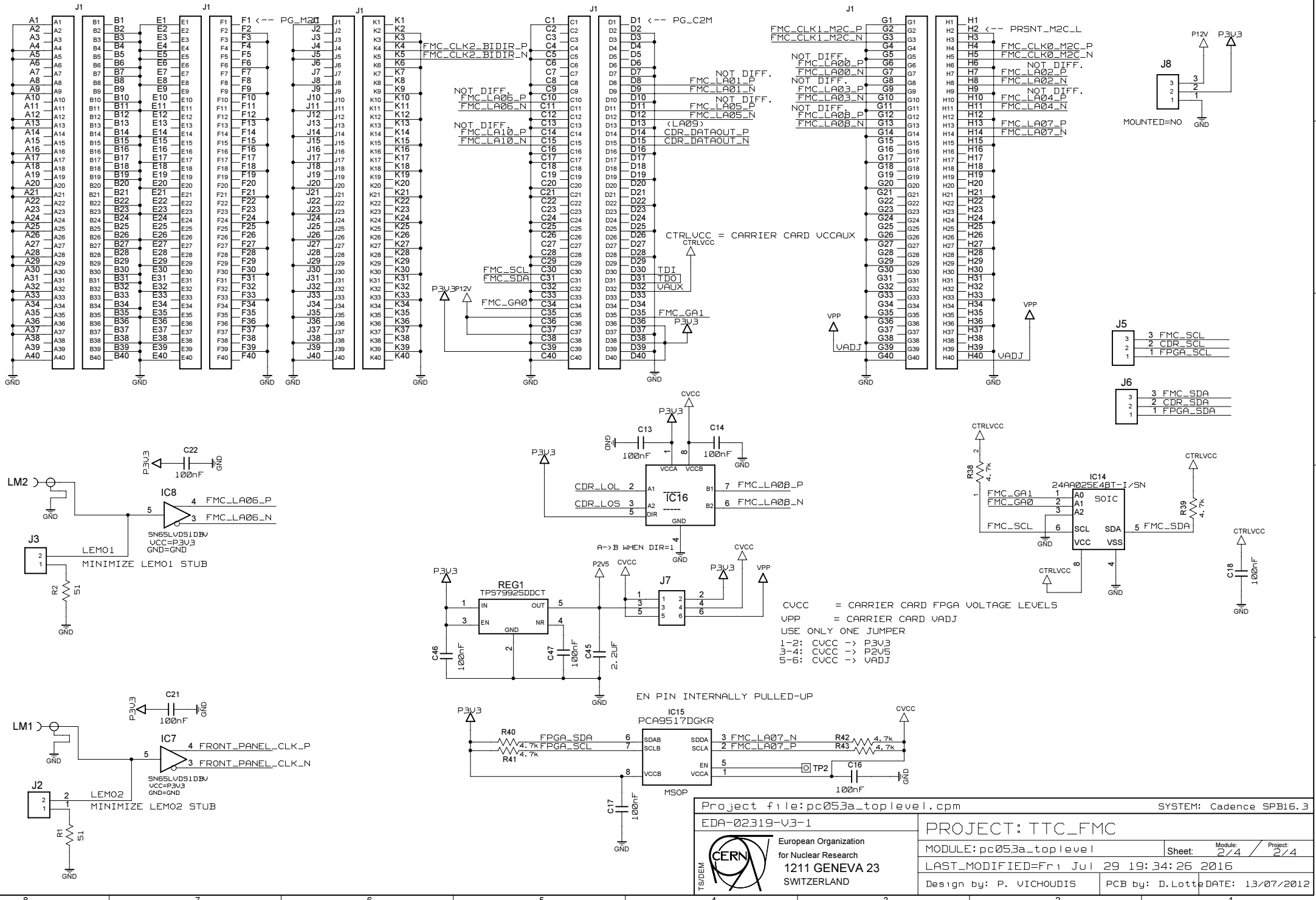


Project file: pc053a_toplevel.cpm		SYSTEM: Cadence SPB16.3
EDA-02319-V3-1	PROJECT: TTC_FMC	
TS/DEM CERN European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE: pc053a_toplevel	Sheet: Module: 1/4 Project: 1/4
	LAST_MODIFIED=Fri Jul 29 19:43:21 2016	
	Design by: P. VICHOUDIS	PCB by: D.Lotte DATE: 13/07/2012



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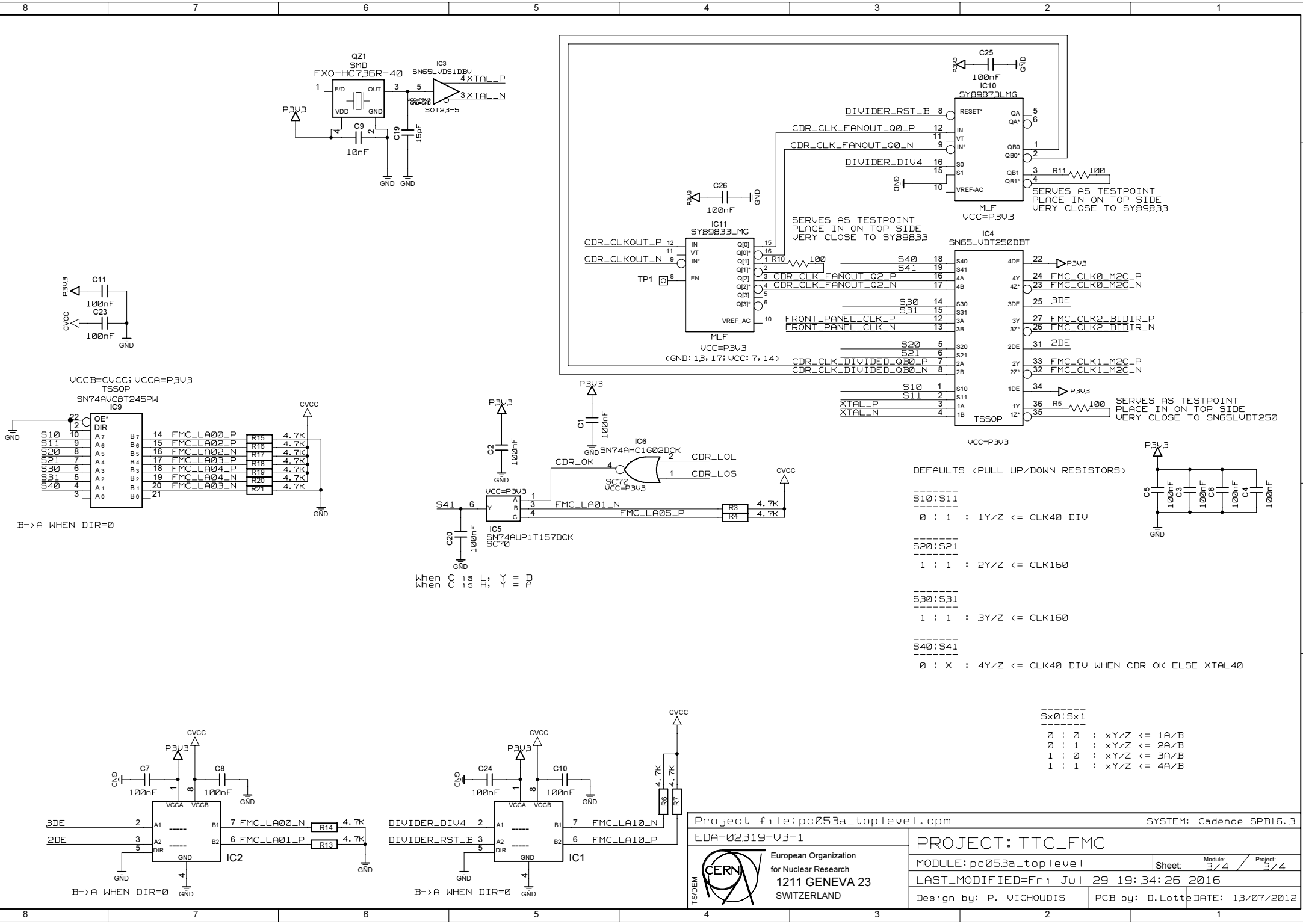
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	MODULE: pc053a_toplevel — Sheet: Module: 2/4 / Project: 2/4
TS/DEM	LAST_MODIFIED=Fri Jul 29 19:34:26 2016
Design by: P. VICHOUDIS	PCB by: D.Lotte — DATE: 13/07/2012


QZ1
SMD
FXO-HC7.36R-40
IC3
SN65LVDS1DBV
SOT23-5
XTAL_P
XTAL_N
P3V3
C9
10nF
C19
15pF
GND
IC10
SY89873LMG
DIVIDER_RST_B
CDR_CLK_FANOUT_Q0_P
CDR_CLK_FANOUT_Q0_N
DIVIDER_DIV4
VREF-AC
C25
100nF
C26
100nF
R11
100
SERVES AS TESTPOINT
PLACE IN ON TOP SIDE
VERY CLOSE TO SY89833
MLF
VCC=P3V3
IC11
SY89833LMG
CDR_CLKOUT_P
CDR_CLKOUT_N
TP1
R10
100
VREF_AC
MLF
VCC=P3V3
(GND: 13, 17; VCC: 7, 14)
IC4
SN65LVDT250DBT
S40
S41
S30
S31
S20
S21
S10
S11
FRONT_PANEL_CLK_P
FRONT_PANEL_CLK_N
CDR_CLK_DIVIDED_QB0_P
CDR_CLK_DIVIDED_QB0_N
XTAL_P
XTAL_N
FMC_CLK0_M2C_P
FMC_CLK0_M2C_N
FMC_CLK2_BIDIR_P
FMC_CLK2_BIDIR_N
FMC_CLK1_M2C_P
FMC_CLK1_M2C_N
R5
100
TSSOP
VCC=P3V3
C11
100nF
C23
100nF
CVCC
VCCB=CVCC; VCCA=P3V3
TSSOP
SN74AVCBT245PW
IC9
FMC_LA00_P
FMC_LA02_P
FMC_LA02_N
FMC_LA03_P
FMC_LA04_P
FMC_LA04_N
FMC_LA03_N
R15
R16
R17
R18
R19
R20
R21
4.7K
B->A WHEN DIR=0
C1
100nF
C2
100nF
IC6
SN74AHC1G02DCK
SC70
VCC=P3V3
CDR_OK
CDR_LOL
CDR_LOS
IC5
SN74AUP1T157DCK
SC70
C20
100nF
FMC_LA01_N
FMC_LA05_P
R3
R4
When C is L, Y = B
When C is H, Y = A
C5
C3
C6
C4
100nF
DEFAULTS (PULL UP/DOWN RESISTORS)
S10:S11
0 : 1 : 1Y/Z <= CLK40 DIV
S20:S21
1 : 1 : 2Y/Z <= CLK160
S30:S31
1 : 1 : 3Y/Z <= CLK160
S40:S41
0 : X : 4Y/Z <= CLK40 DIV WHEN CDR OK ELSE XTAL40
Sx0:Sx1
0 : 0 : xY/Z <= 1A/B
0 : 1 : xY/Z <= 2A/B
1 : 0 : xY/Z <= 3A/B
1 : 1 : xY/Z <= 4A/B
C7
C8
100nF
IC2
3DE
2DE
FMC_LA00_N
FMC_LA01_P
R14
R13
B->A WHEN DIR=0
C24
C10
IC1
DIVIDER_DIV4
DIVIDER_RST_B
FMC_LA10_N
FMC_LA10_P
R6
R7
B->A WHEN DIR=0
Project file:pc053a_toplevel.cpm
SYSTEM: Cadence SPB16.3
EDA-02319-V3-1
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TS/DEM
PROJECT: TTC_FMC
MODULE:pc053a_toplevel
Sheet: 3/4
Module: 3/4
Project: 3/4
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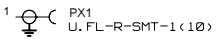
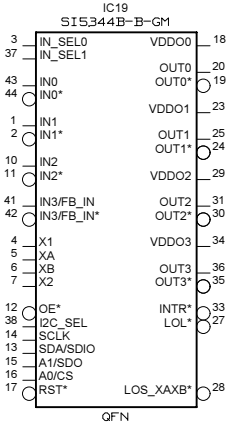
DATE: 13/07/2012

U/FL FOR TEST-POINTS





CLOCK GENERATOR WILL REPLACE CLOCK FANOUT/DIVIDER IC10 , IC11

	Fri Jul 29 19:51:58 2016					
ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS

USED ON

UOB-HEP
UNIVERSITY OF BRISTOL
HIGH ENERGY PHYSICS GROUP

H.H.WILLS PHYSICS LAB, TYNDALL AVE, BRISTOL, BS8 1TL.

TITLE uob_hep_pc053a_lib

MODULE: pc053a_toplevel

A2

MODULE PAGE: 4 OF 4
OVERALL PAGE: 4 OF 4

TOTAL NO. OF SHEETS