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3V3_MB_FILT	3V3 filtered from MIB (MB)	
3V3_MB	3V3_VCCO	3V3 from MIB (MB) Above switched to VCCO
2V5_MB	2V5_VCCO	2V5 from MIB (MB) Above switched to VCCO
1V8	1V8 for VCCAUX	
1V2	1V2 for MGTAVTT	
1V0	1V0 for Core + MGTAVCC	
GND	System GND/0V rail	

DRAFTER	DATE	<div><div>UNIVERSITY OF OXFORD</div><div>Department of Physics, Central Electronics Group Denys Wilkinson Building Keble Road Oxford OX1 3RH United Kingdom</div></div>			
Peter Hastings	06/02/23				
CHECKER	DATE	TITLE			
Roy Wastie, David Cussans	xx/xx/xx	MIB_FPGA_Module			
ENGINEER	DATE				
Peter Hastings	06/02/23				
APPROVAL	DATE	A3		SIZE	DRAWING NUMBER
TBD	xx/xx/xx				PPP/DUN/DAQ/004
APPROVAL	DATE			Top Sheet	
TBD	xx/xx/xx				
		DATE 31/03/2023:07:51			SHEET 1 OF 8

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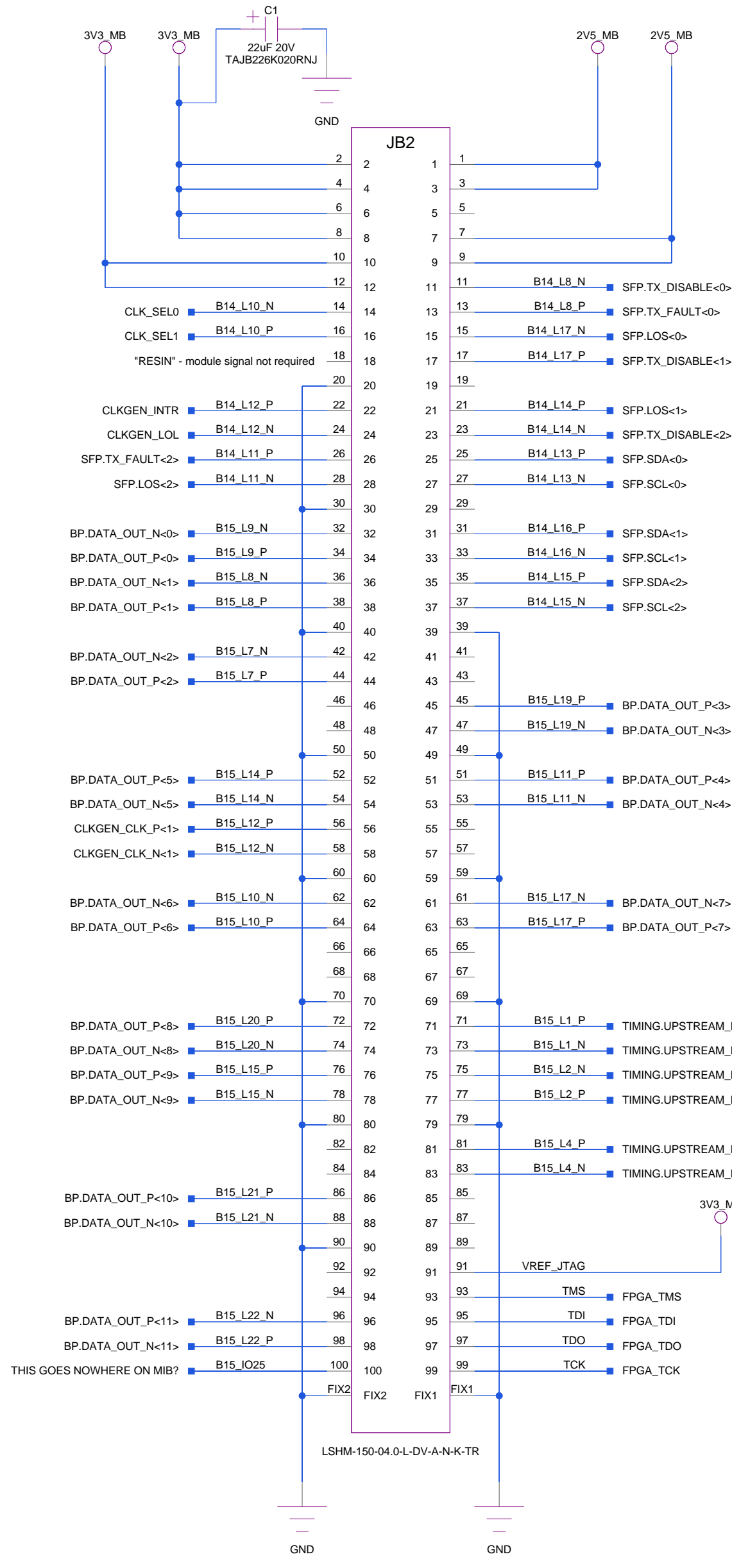
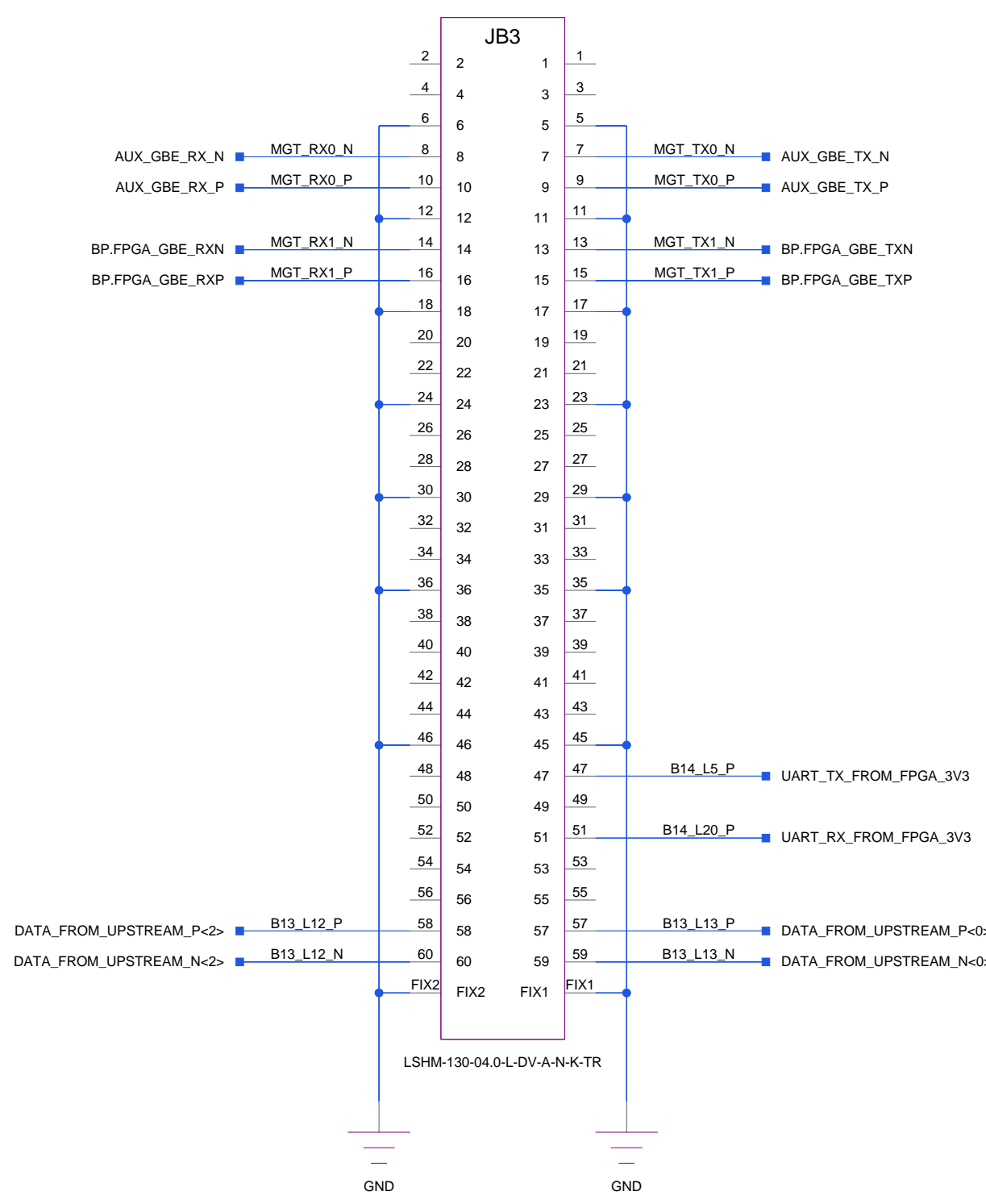
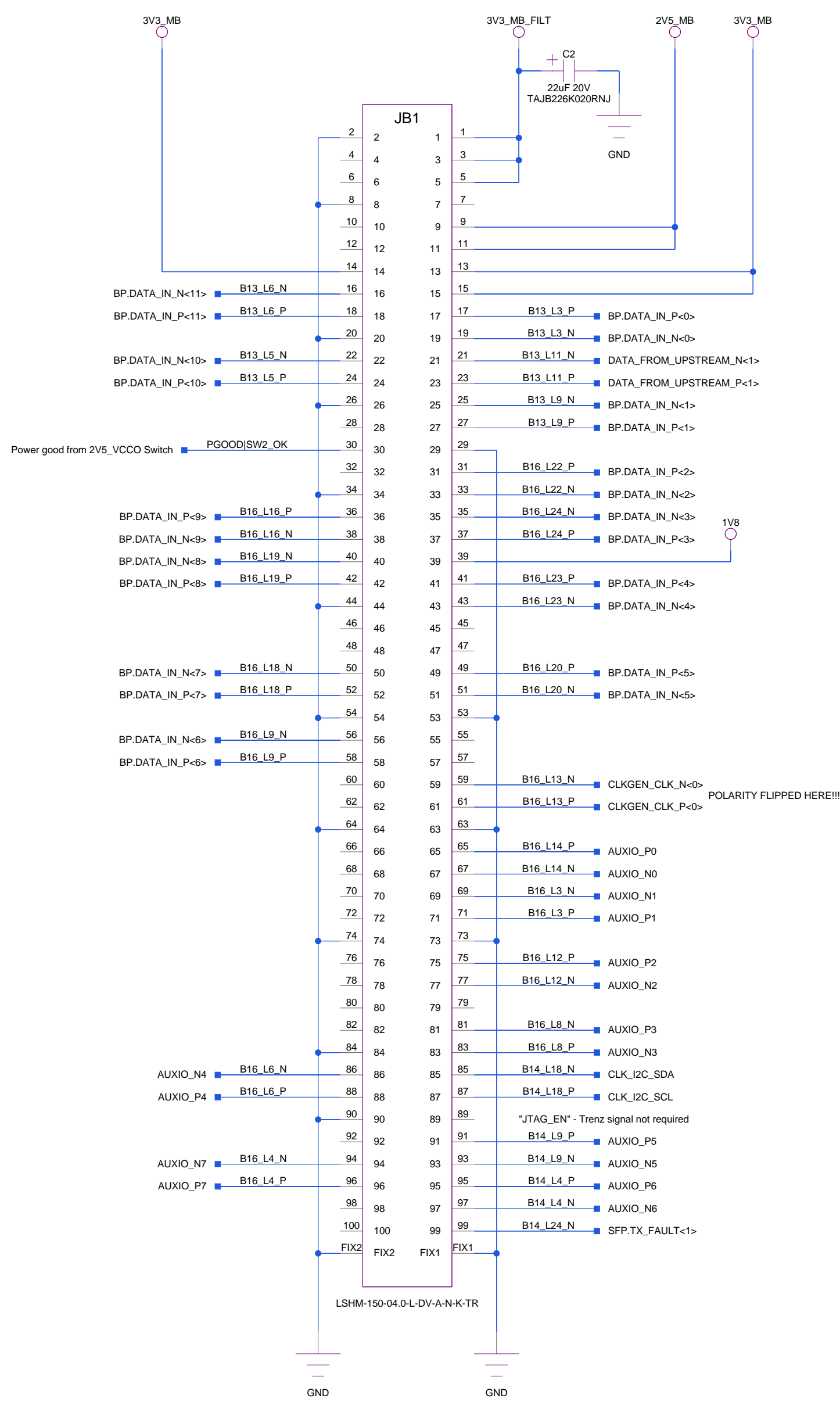
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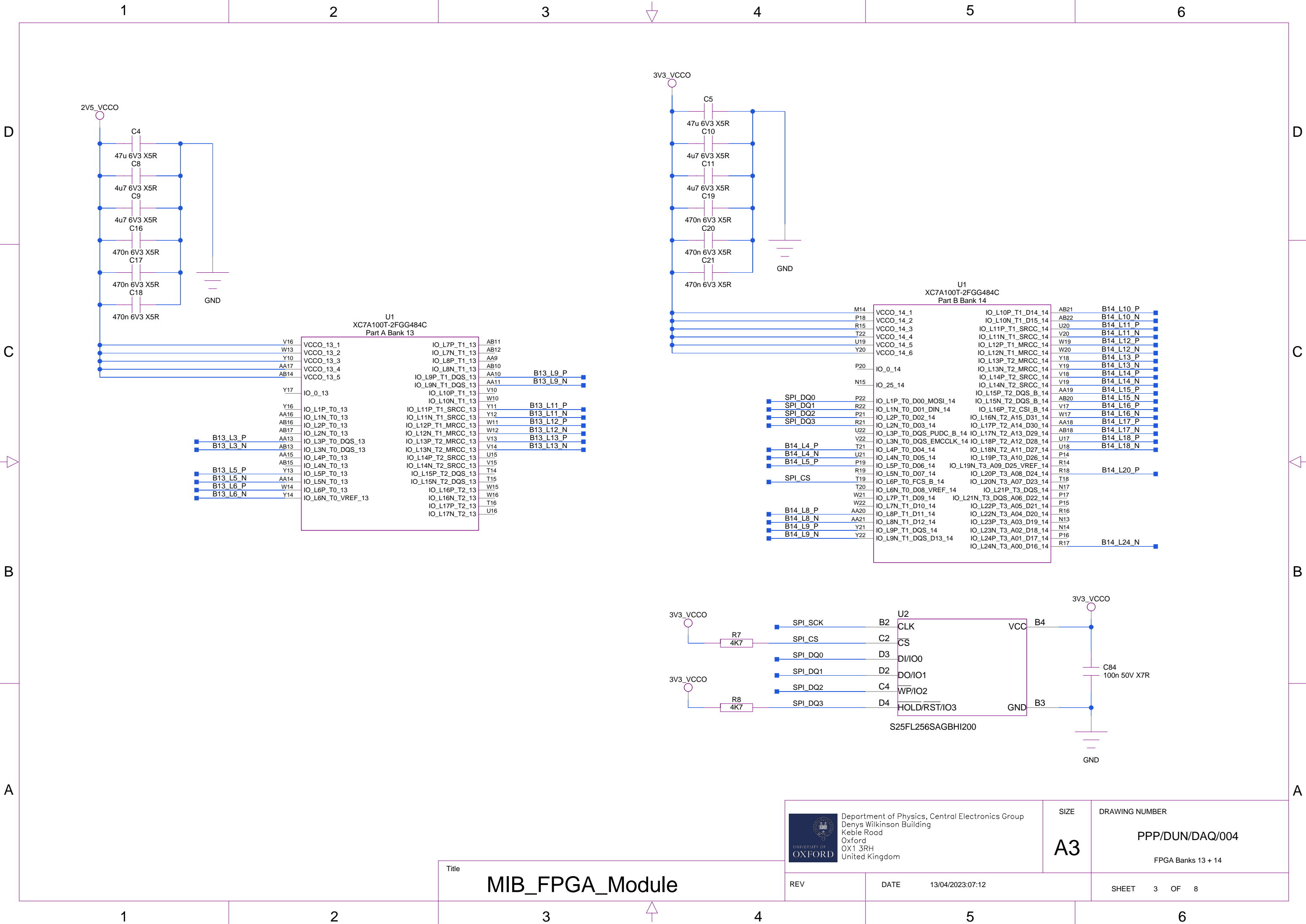
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TITLE

MIB\_FPGA\_Module

 <div>Department of Physics, Central Electronics Group Denys Wilkinson Building Keble Road Oxford OX1 3RH United Kingdom</div>	SIZE	DRAWING NUMBER	
		PPP/DUN/DAQ/004	
REV	DATE	Hermaphroditic Mezzanine Connectors	
		SHEET	2 OF 8



MIB\_FPGA\_Module



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SIZE  
A3

DRAWING NUMBER  
PPP/DUN/DAQ/004

FPGA Banks 13 + 14

REV

DATE 13/04/2023:07:12

SHEET 3 OF 8

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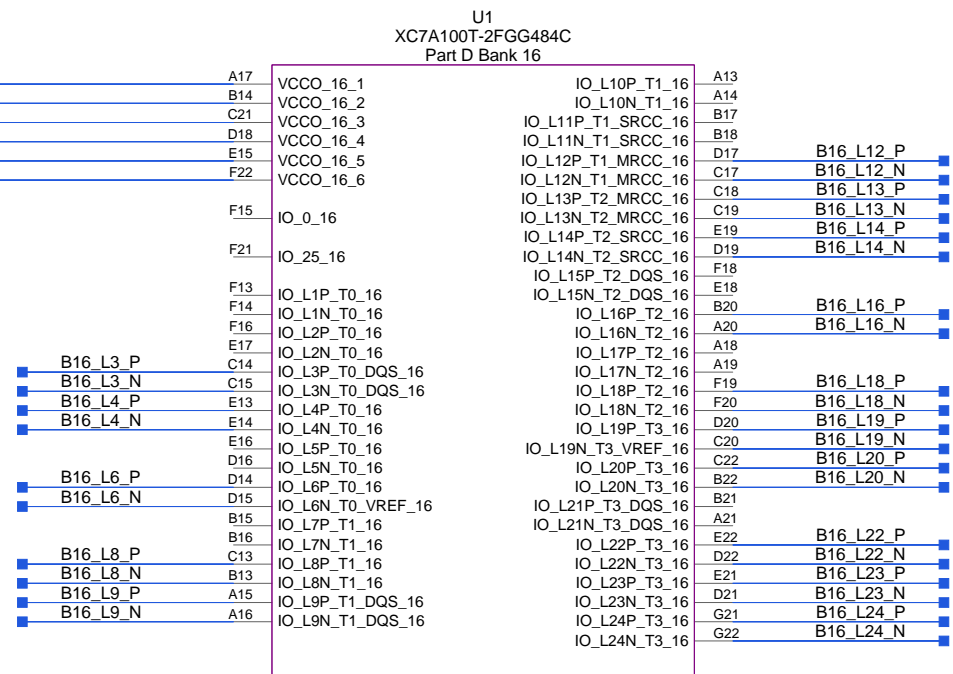
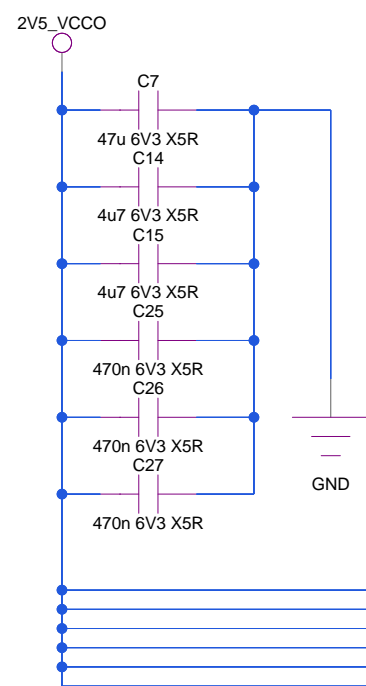
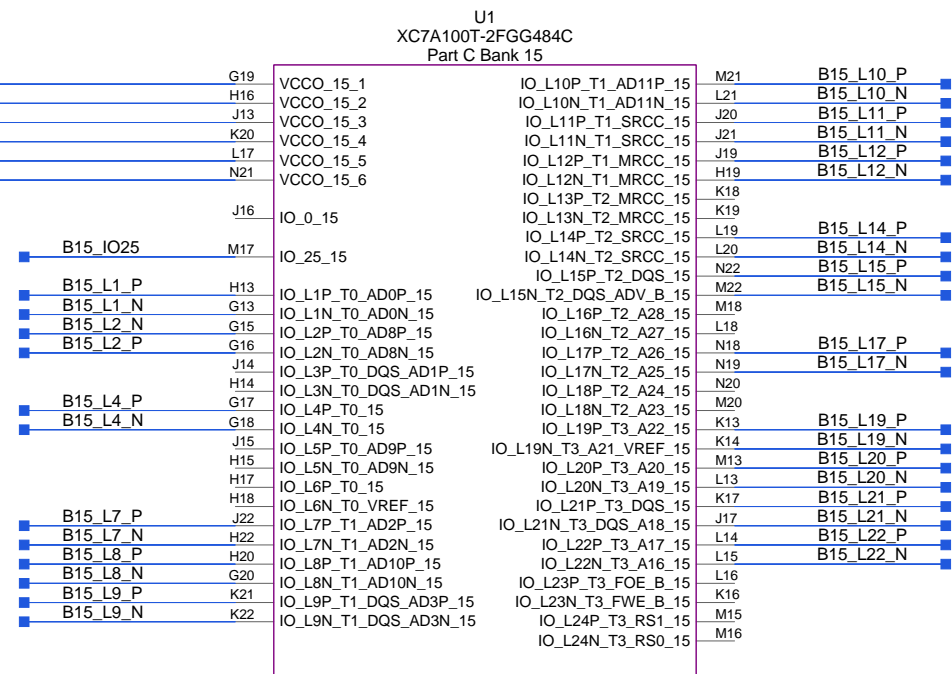
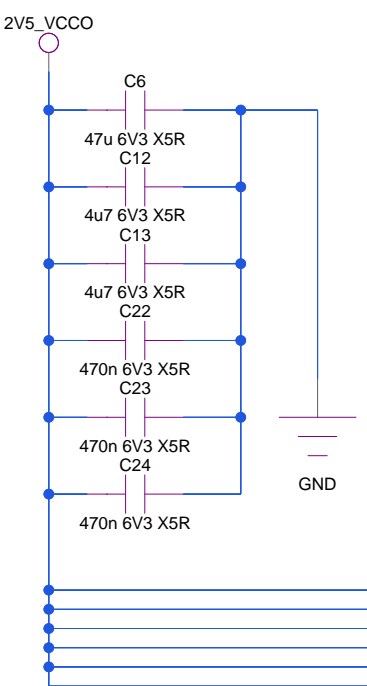
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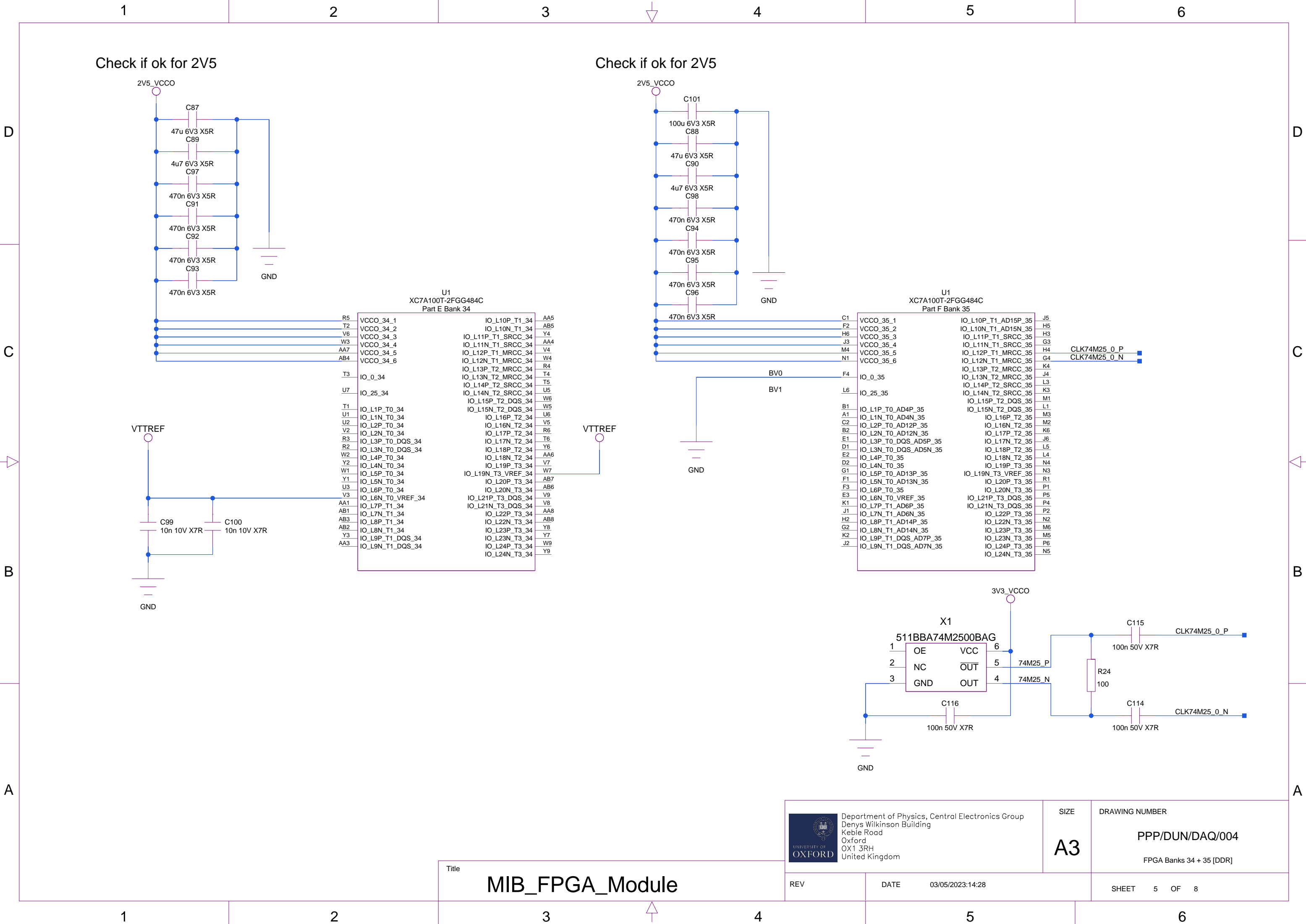
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FPGA Banks 34 + 35 [DDR]

Title

MIB\_FPGA\_Module

REV

DATE

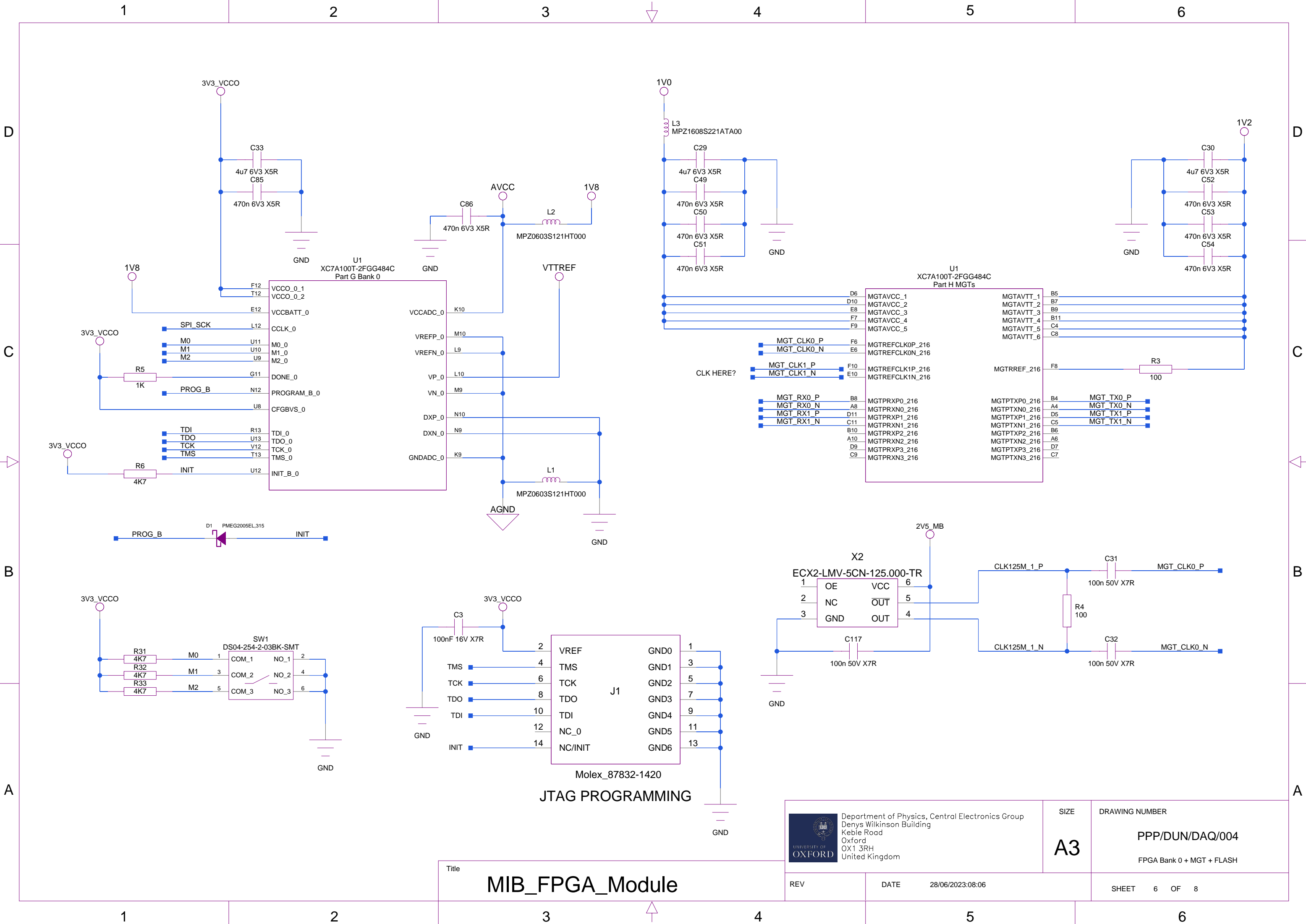
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SHEET

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OF

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MIB\_FPGA\_Module



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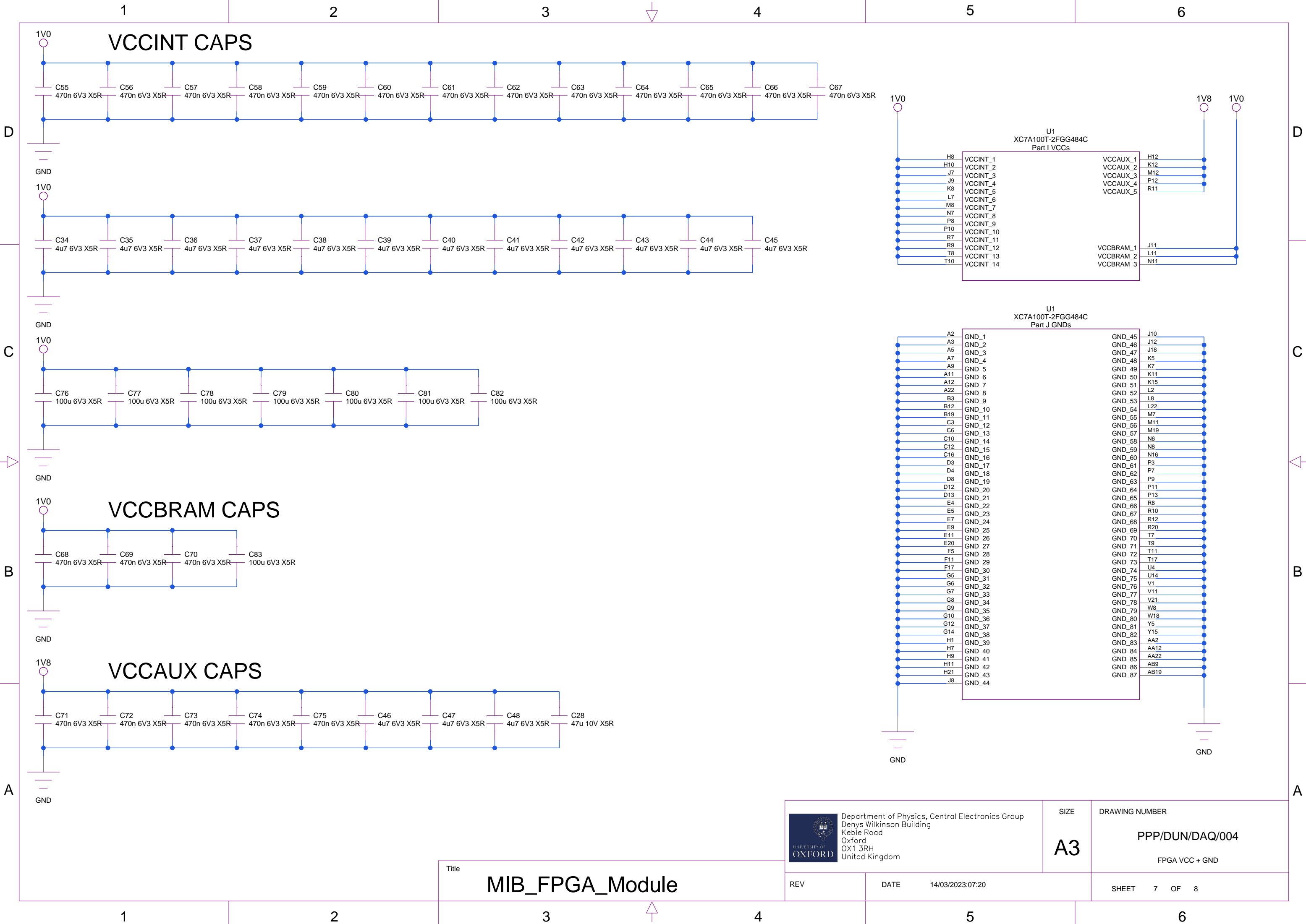
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DRAWING NUMBER  
**PPP/DUN/DAQ/004**


FPGA Bank 0 + MGT + FLASH

REV  
DATE  
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SHEET  
6 OF 8

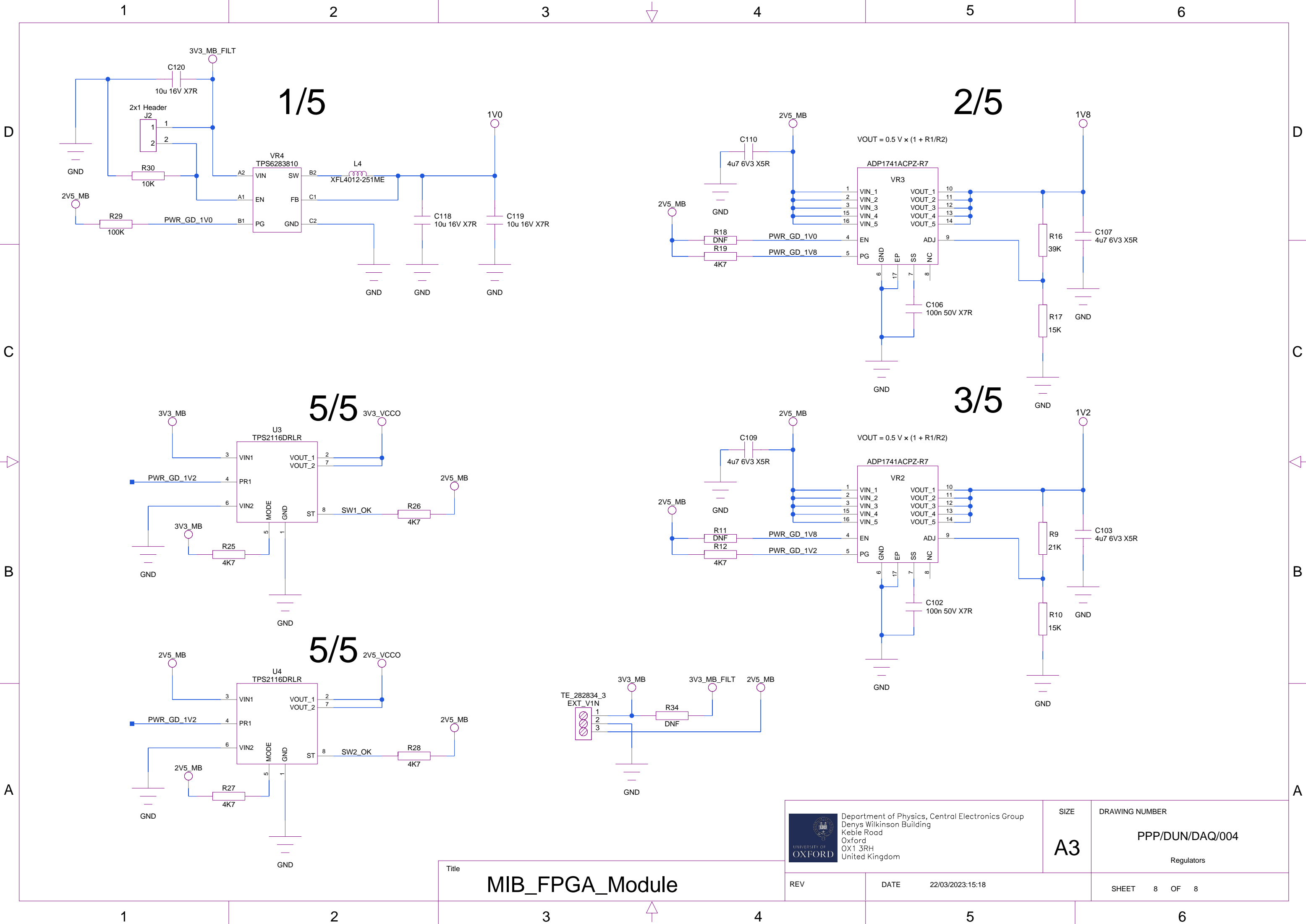


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**MIB\_FPGA\_Module**


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SIZE	DRAWING NUMBER
A3	PPP/DUN/DAQ/004
FPGA VCC + GND	
REV	DATE 14/03/2023:07:20
SHEET 7	OF 8





Title  
**MIB\_FPGA\_Module**

 Department of Physics, Central Electronics Group Denys Wilkinson Building Keble Road Oxford OX1 3RH United Kingdom		SIZE <b>A3</b>	DRAWING NUMBER <b>PPP/DUN/DAQ/004</b> Regulators
REV	DATE 22/03/2023:15:18	SHEET 8 OF 8	