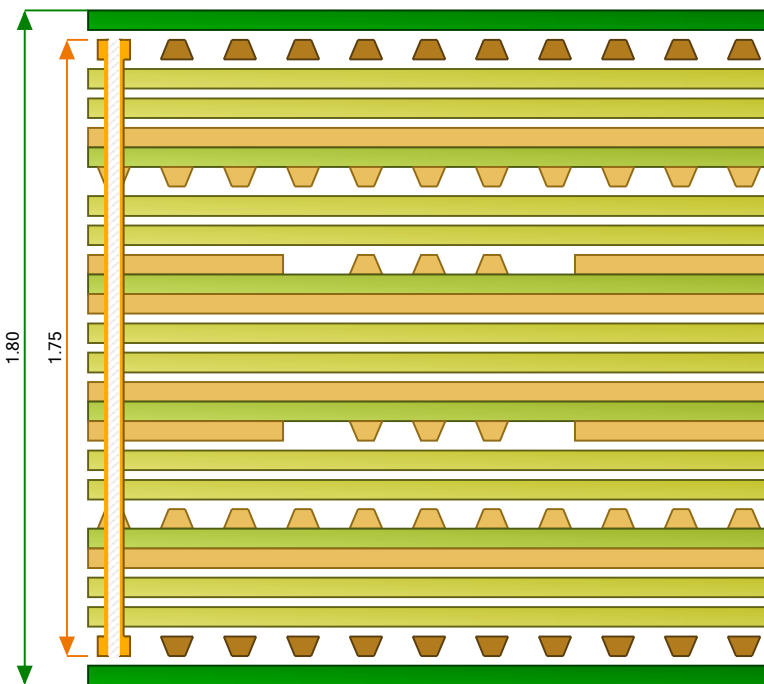





Units: Millimetres











Layer	Stack up	Supplier Description	εr	Tg	Mask Thickness	Isolation Distance	Finish Thickness	
1		SM/001	4.000		0.025			
		FO/001					0.035	
2		VT-48PP HR	4.200	150.000		0.060	0.060	
		VT-48PP HR	4.200	150.000		0.060	0.060	
3		VT 48	4.200	150.000		0.200	0.200	
							0.035	
4		VT-48PP HR	4.200	150.000		0.060	0.060	
		VT-48PP HR	4.200	150.000		0.060	0.060	
5		VT 48	4.200	150.000		0.200	0.200	
							0.035	
6		VT-48PP HR	4.200	150.000		0.060	0.060	
		VT-48PP HR	4.200	150.000		0.060	0.060	
7		VT 48	4.200	150.000		0.200	0.200	
							0.035	
8		VT-48PP HR	4.200	150.000		0.060	0.060	
		VT-48PP HR	4.200	150.000		0.060	0.060	
9		VT 48	4.200	150.000		0.200	0.200	
							0.035	
10		VT-48PP HR	4.200	150.000		0.060	0.060	
		VT-48PP HR	4.200	150.000		0.060	0.060	
		FO/001					0.035	
		SM/001	4.000		0.025			


Copper Thickness = 0.350 | Dielectric Thickness = 1.400 | Solder Mask Thickness = 0.050 |
Stack Up Thickness = 1.750 | Stack Up Thickness with Soldermask = 1.800

Structure Image	Impedance ID	Impedance Signal Layer	Structure Name	Lower Trace Width (W1)	Upper Trace Width (W2)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)	Coating Above Trace (C2)	Coating Above Substrate (C1)	Coating Between Traces (C3)	Error %	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Trace Separation (S1)
	1	1	Edge Coupled Coated Microstrip 1B	0.160	0.160	0.000	101.060	100.000	10.000	0.025	0.025	0.025	1.1	2	0	0.330
	2	1	Coated Microstrip 1B	0.190	0.190	0.000	49.700	50.000	10.000	0.025	0.025	0.000	0.6	2	0	0.000

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Author:							
Department:							
Site:							

Units: Millimetres

Structure Image	Impedance ID	Impedance Signal Layer	Structure Name	Lower Trace Width (W1)	Upper Trace Width (W2)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)	Coating Above Trace (C2)	Coating Above Substrate (C1)	Coating Between Traces (C3)	Error %	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Trace Separation (S1)	
	3	3	Edge Coupled Offset Stripline 1B1A	0.100	0.100	0.000	99.880	100.000	10.000	0.000	0.000	0.000	0.1	2	4	0.527	
	4	3	Offset Stripline 1B1A	0.100	0.100	0.000	50.140	50.000	10.000	0.000	0.000	0.000	0.3	2	4	0.000	
	5	4	Edge Coupled Offset Stripline 1B1A	0.160	0.160	0.000	100.150	100.000	10.000	0.000	0.000	0.000	0.2	2	5	0.330	
	6	4	Offset Stripline 1B1A	0.199	0.199	0.000	49.550	50.000	10.000	0.000	0.000	0.000	0.9	2	5	0.000	
	7	7	Edge Coupled Offset Stripline 1B1A	0.160	0.160	0.000	100.150	100.000	10.000	0.000	0.000	0.000	0.2	6	9	0.330	
	8	7	Offset Stripline 1B1A	0.199	0.199	0.000	49.550	50.000	10.000	0.000	0.000	0.000	0.9	6	9	0.000	
	9	8	Edge Coupled Offset Stripline 1B1A	0.100	0.100	0.000	98.960	100.000	10.000	0.000	0.000	0.000	1.0	7	9	0.400	
	10	8	Offset Stripline 1B1A	0.100	0.100	0.000	50.140	50.000	10.000	0.000	0.000	0.000	0.3	7	9	0.000	
	11	10	Edge Coupled Coated Microstrip 1B	0.160	0.160	0.000	101.060	100.000	10.000	0.025	0.025	0.025	1.1	9	0	0.330	
	12	10	Coated Microstrip 1B	0.190	0.190	0.000	49.700	50.000	10.000	0.025	0.025	0.000	0.6	9	0	0.000	

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Drill Image	1st Layer	2nd Layer	Column Position	Drill Type	
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110Mechanical PTH

Notes

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