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8	Regulators

3V3_MB_FILT	3V3 filtered from MIB (MB)	
3V3_MB	3V3_VCCO	3V3 from MIB (MB) Above switched to VCCO
2V5_MB	2V5_VCCO	2V5 from MIB (MB) Above switched to VCCO
1V8	1V8 for VCCAUX	
1V2	1V2 for MGTAVTT	
1V0	1V0 for Core + MGTAVCC	
GND	System GND/0V rail	

DRAFTER	Peter Hastings	DATE	06/02/23
CHECKER	Roy Wastie, David Cussans	DATE	xx/xx/xx
ENGINEER	Peter Hastings	DATE	06/02/23
APPROVAL	TBD	DATE	xx/xx/xx
APPROVAL	TBD	DATE	xx/xx/xx

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TITLE

MIB_FPGA_Module

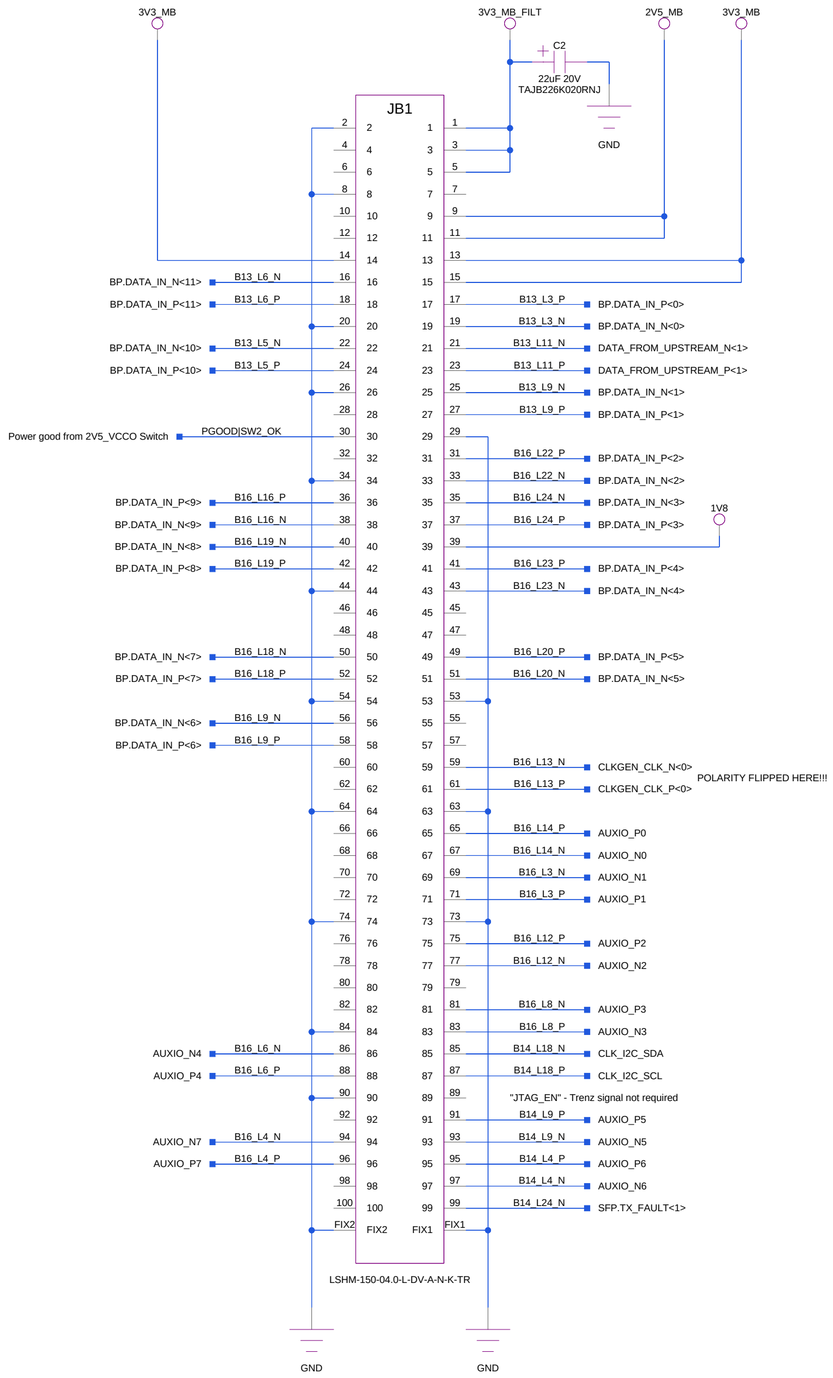
SIZE A3

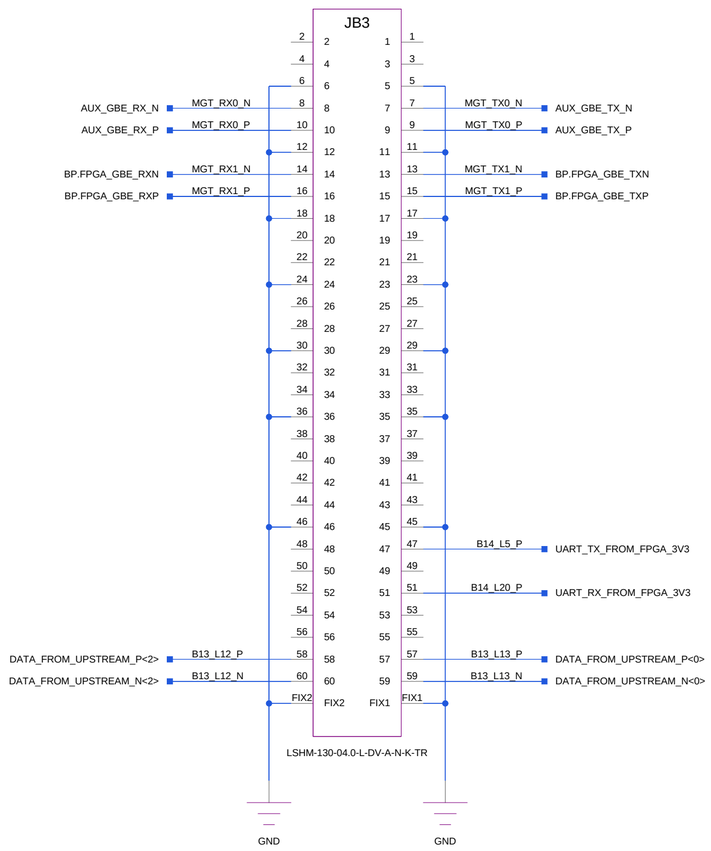
DRAWING NUMBER PPP/DUN/DAQ/004

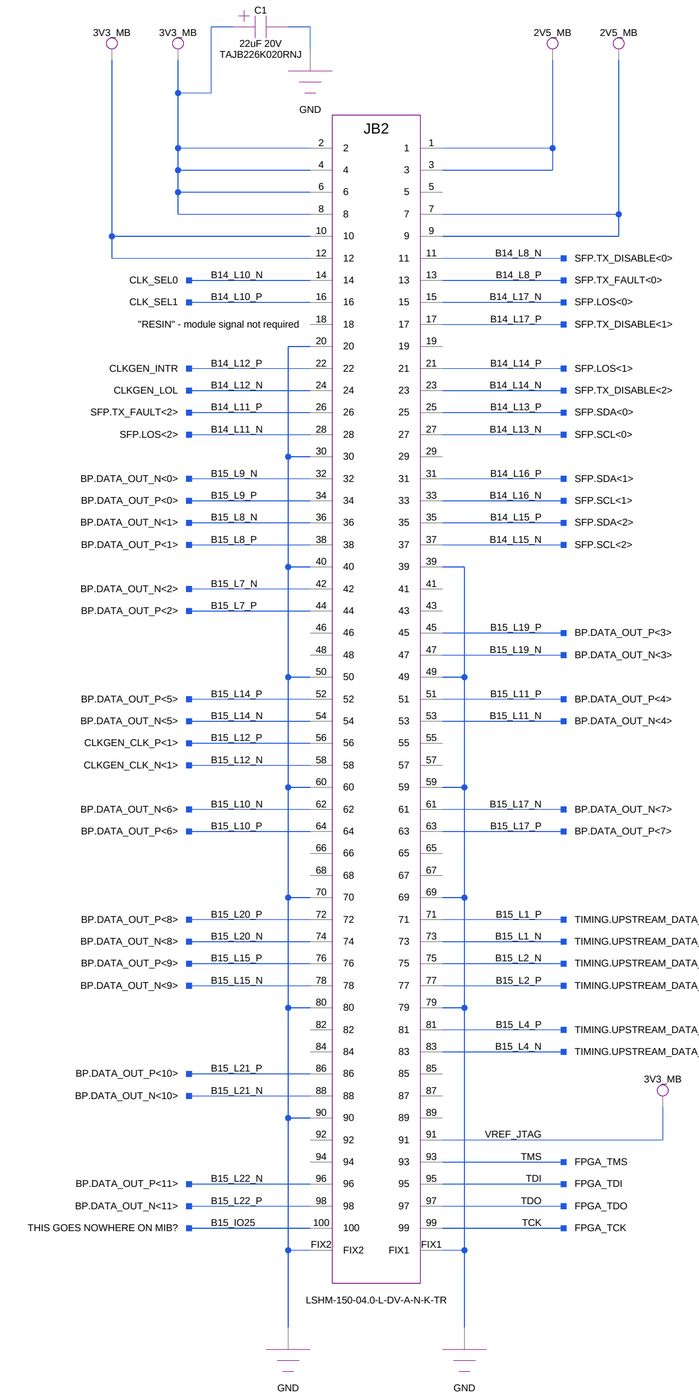
Top Sheet

DATE 31/03/2023:07:51

SHEET 1 OF 8







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SIZE A2

DRAWING NUMBER PPP/DUN/DAQ/004

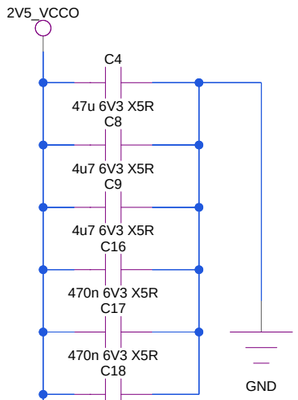
Hermaphroditic Mezzanine Connectors

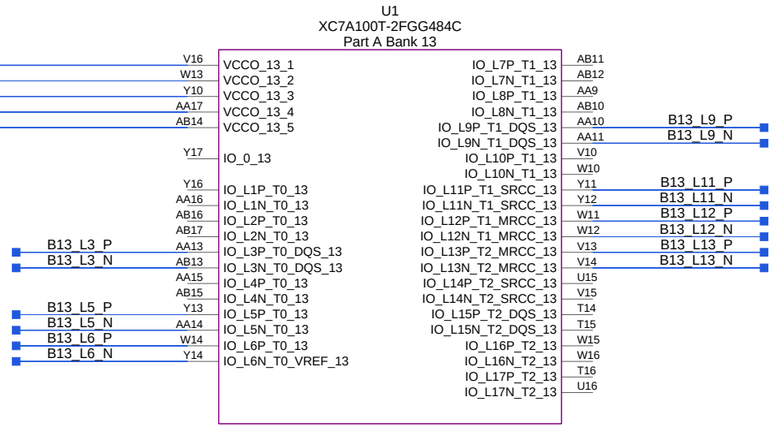
TITLE MIB_FPGA_Module

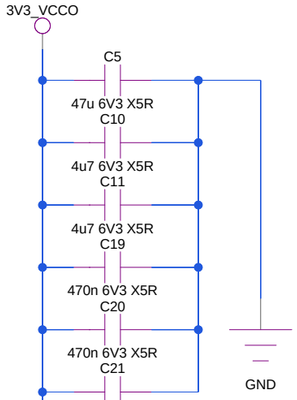
REV

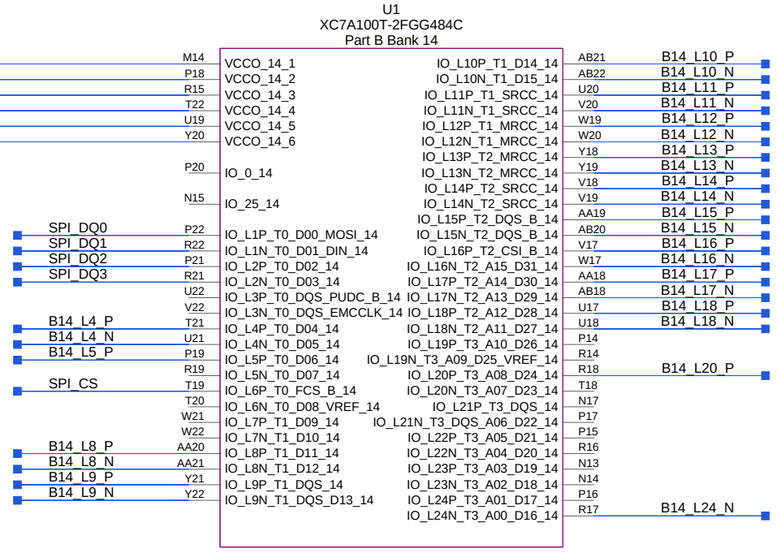
DATE 04/04/2023:15:09

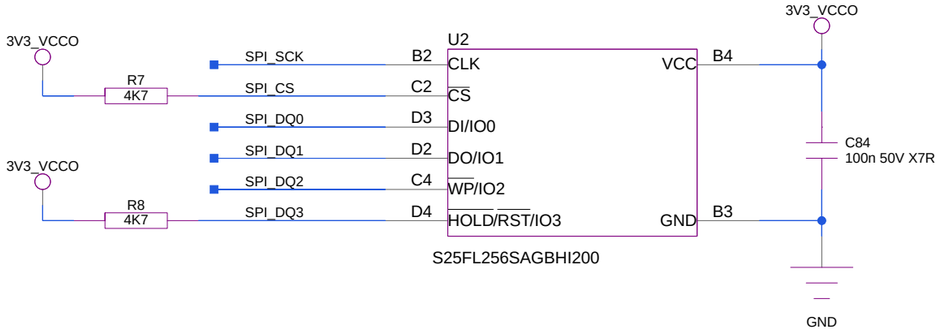
SHEET 2 OF 8











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SIZE A3

DRAWING NUMBER PPP/DUN/DAQ/004

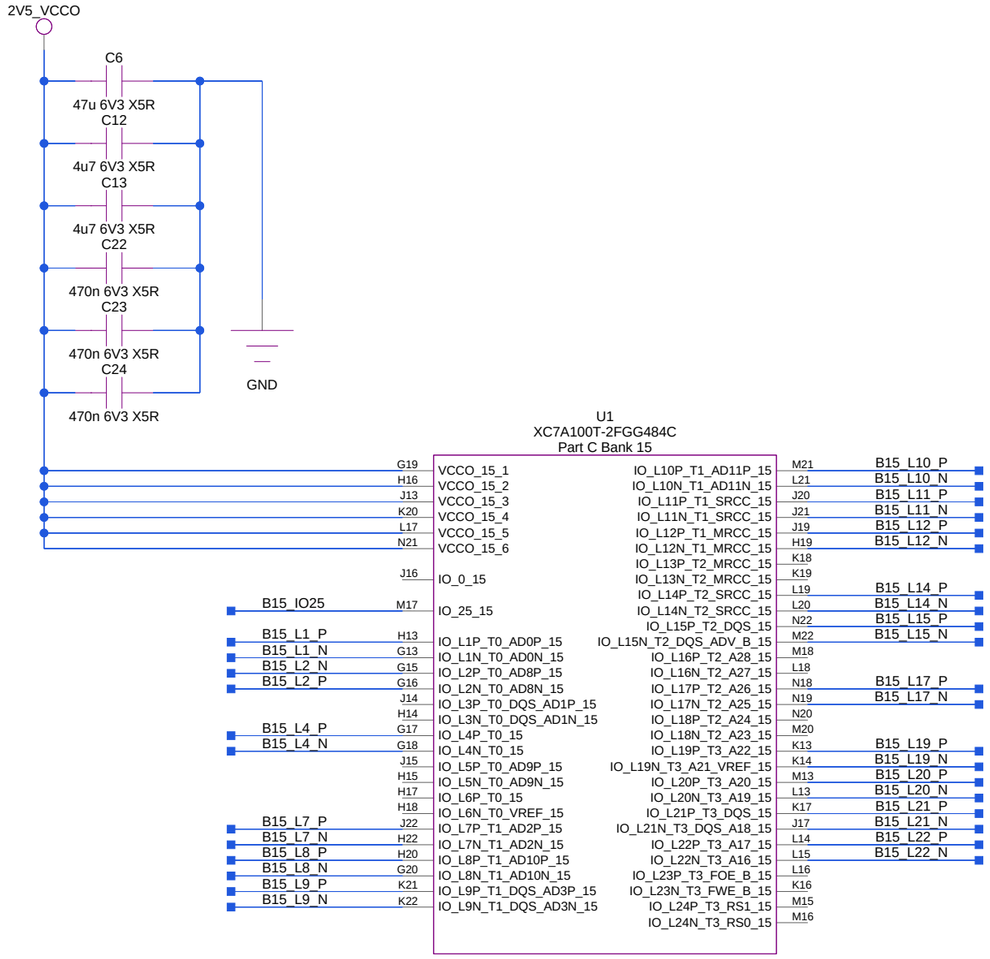
FPGA Banks 13 + 14

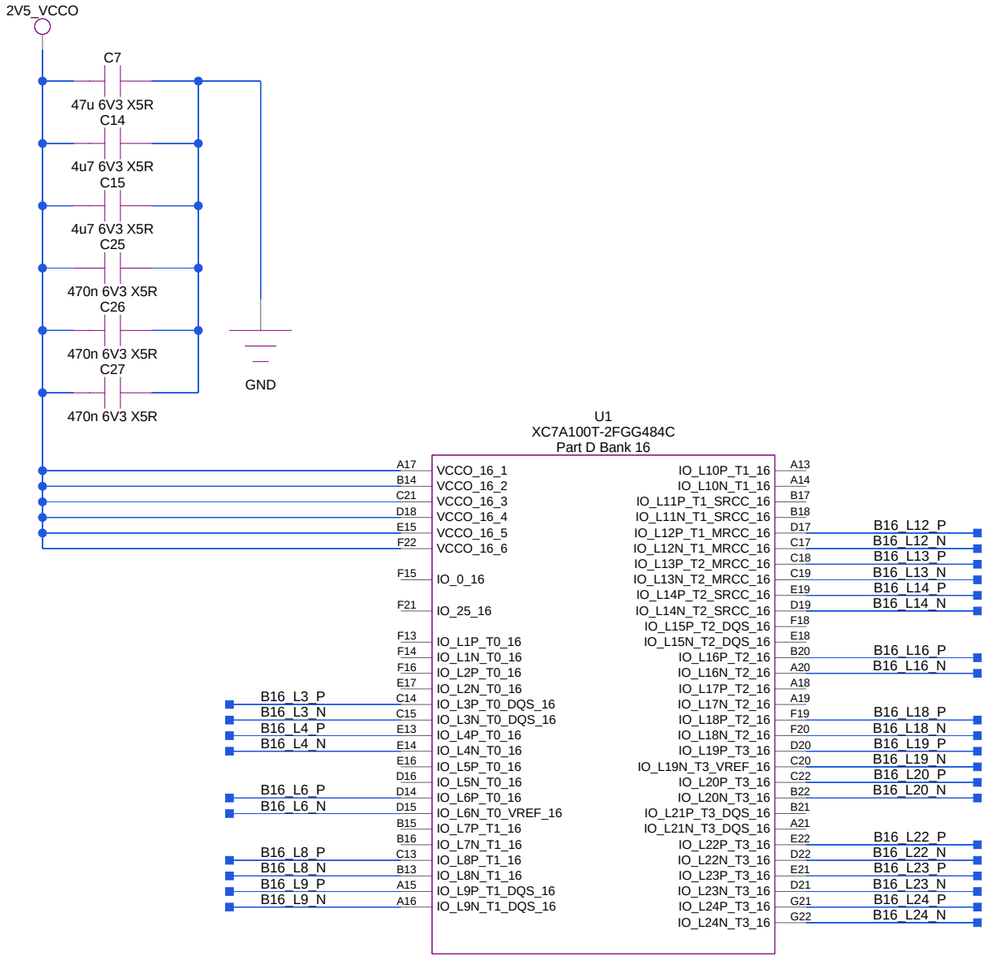
Title MIB_FPGA_Module

REV

DATE 13/04/2023:07:12

SHEET 3 OF 8





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SIZE A3

DRAWING NUMBER PPP/DUN/DAQ/004

FPGA Banks 15 + 16

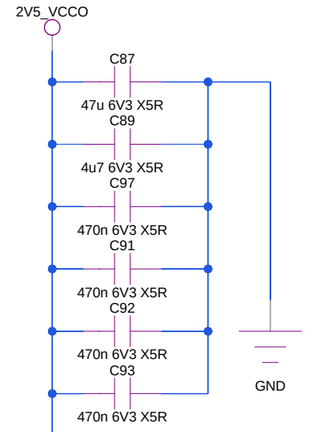
Title MIB_FPGA_Module

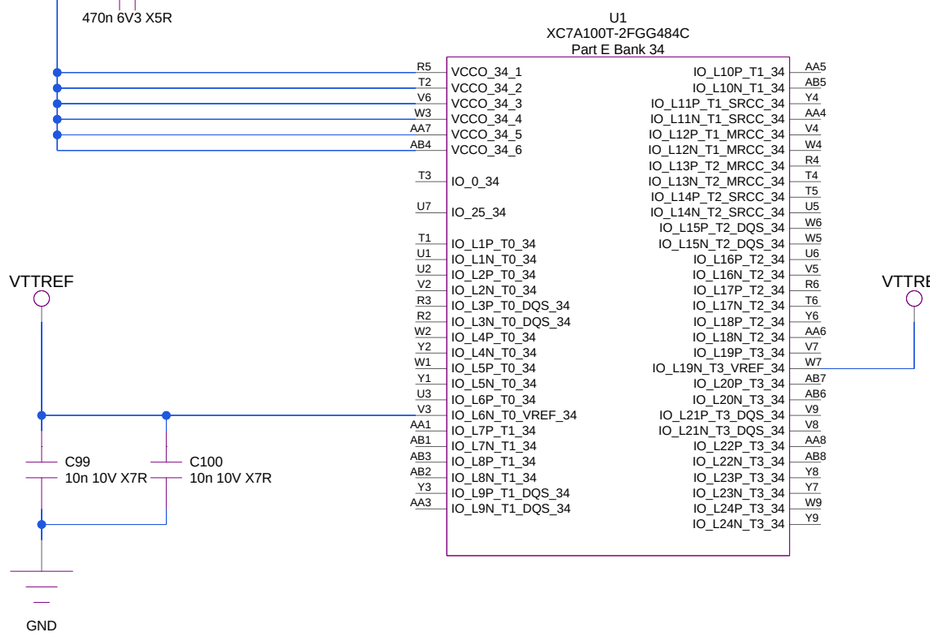
REV

DATE 04/04/2023:14:41

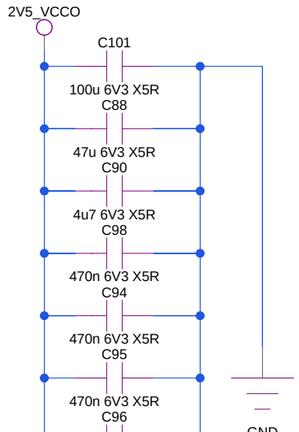
SHEET 4 OF 8

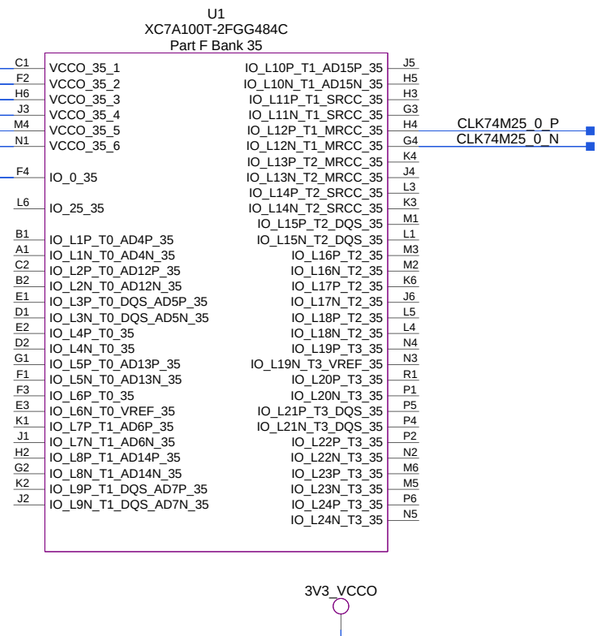
Check if ok for 2V5

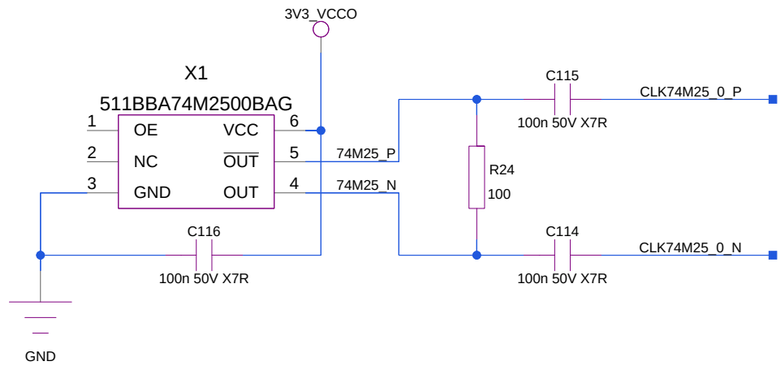




Check if ok for 2V5







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SIZE A3

DRAWING NUMBER PPP/DUN/DAQ/004

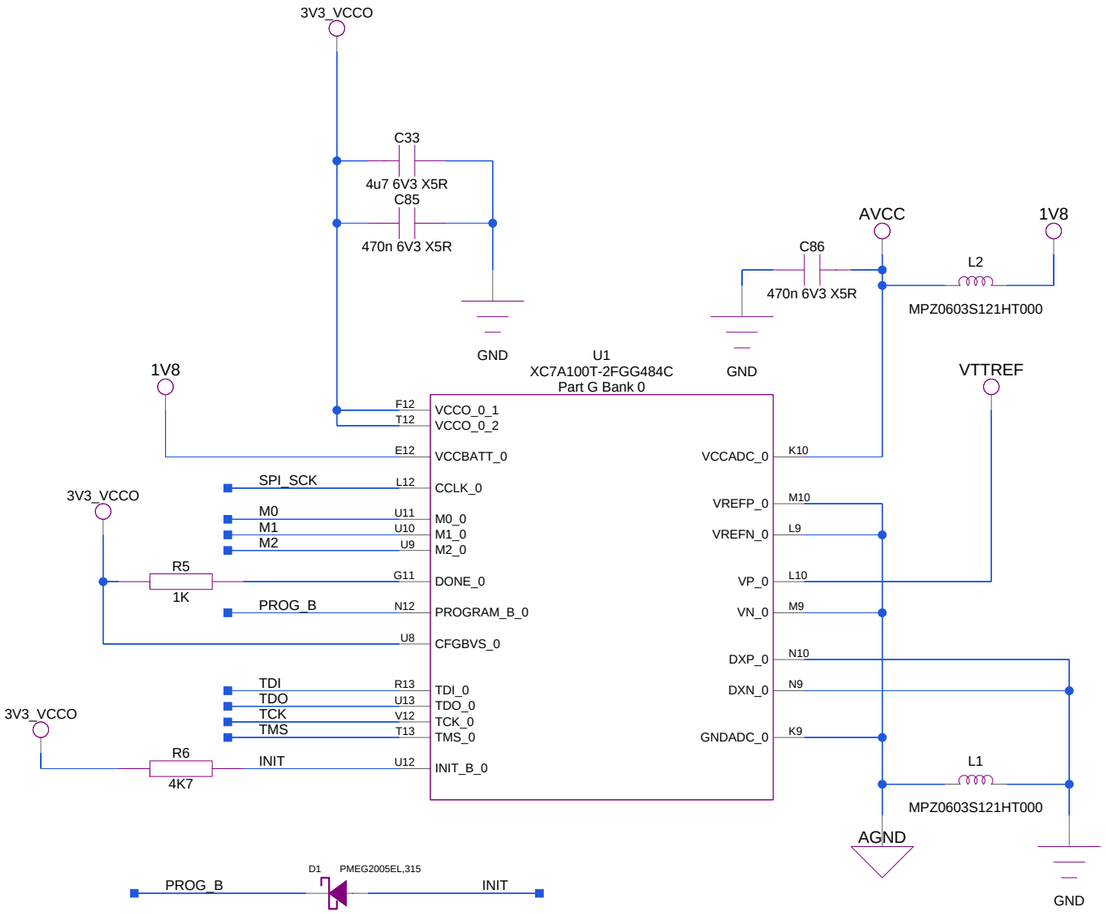
FPGA Banks 34 + 35 [DDR]

Title MIB_FPGA_Module

REV

DATE 03/05/2023:14:28

SHEET 5 OF 8

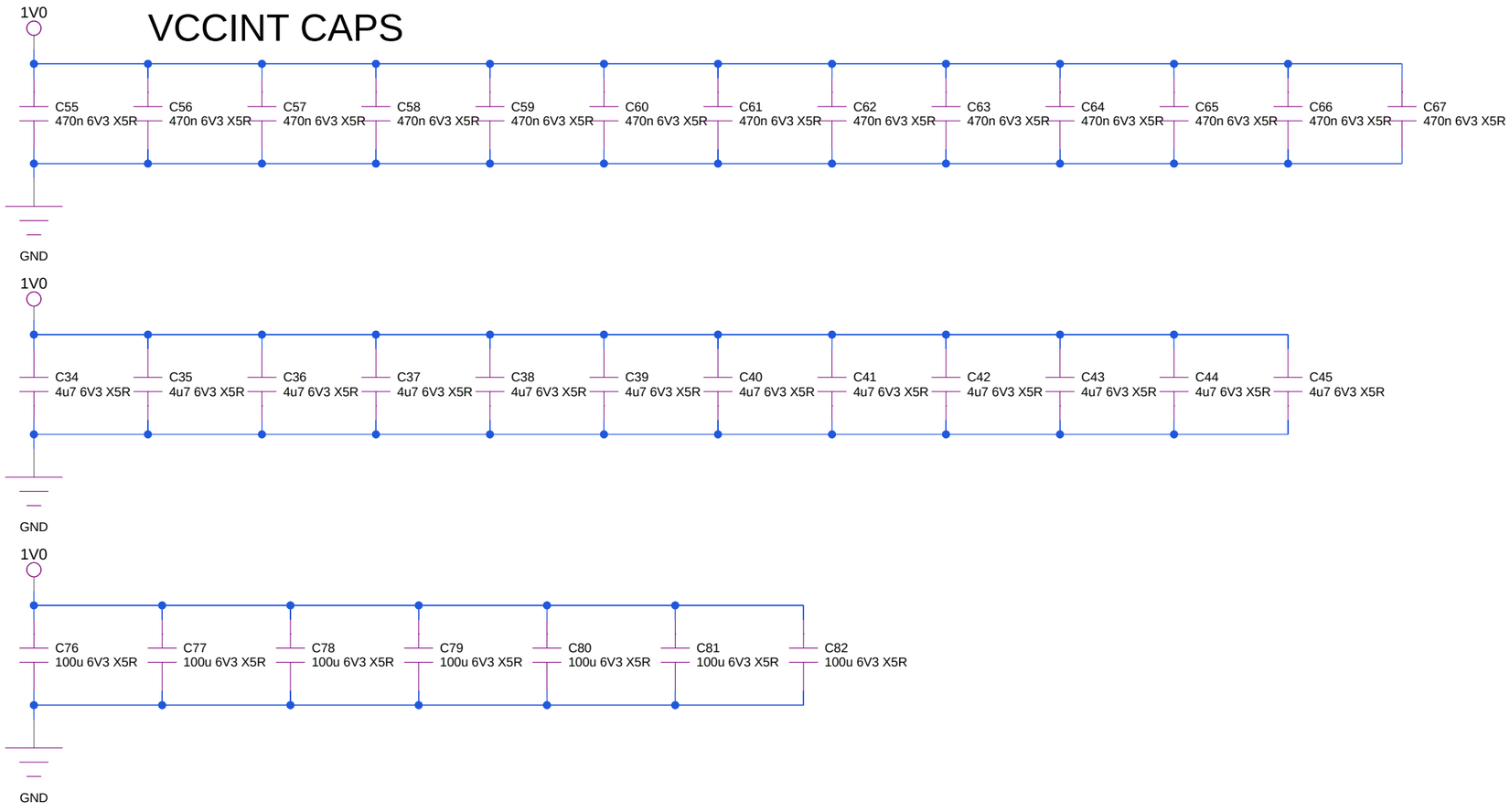


Department of Physics, Central Electronics Group Denys Wilkinson Building Keble Road Oxford OX1 3RH United Kingdom	SIZE A3	DRAWING NUMBER PPP/DUN/DAQ/004 FPGA Bank 0 + MGT + FLASH	
REV	DATE 15/06/2023:13:57	SHEET 6 OF 8	

Title

MIB_FPGA_Module

VCCINT CAPS



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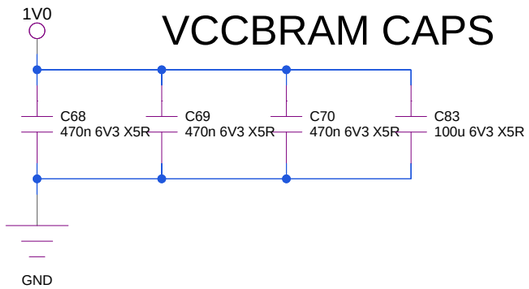
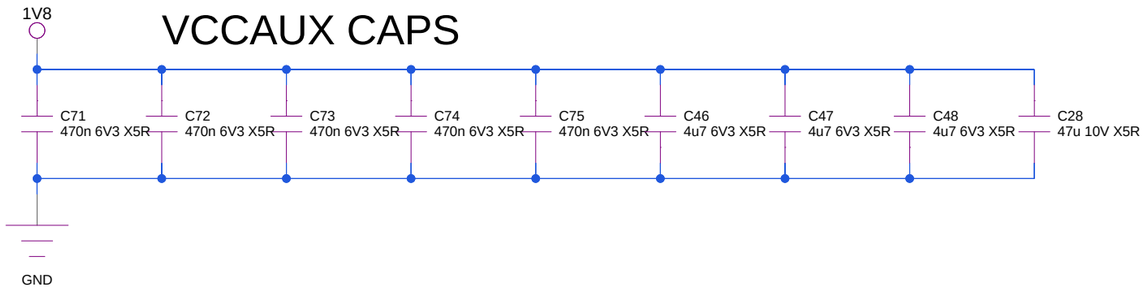
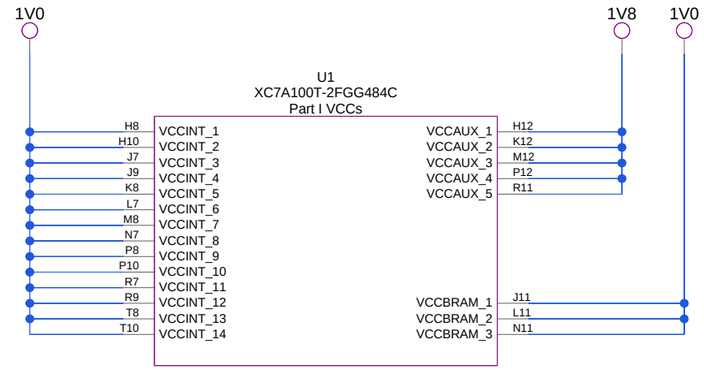
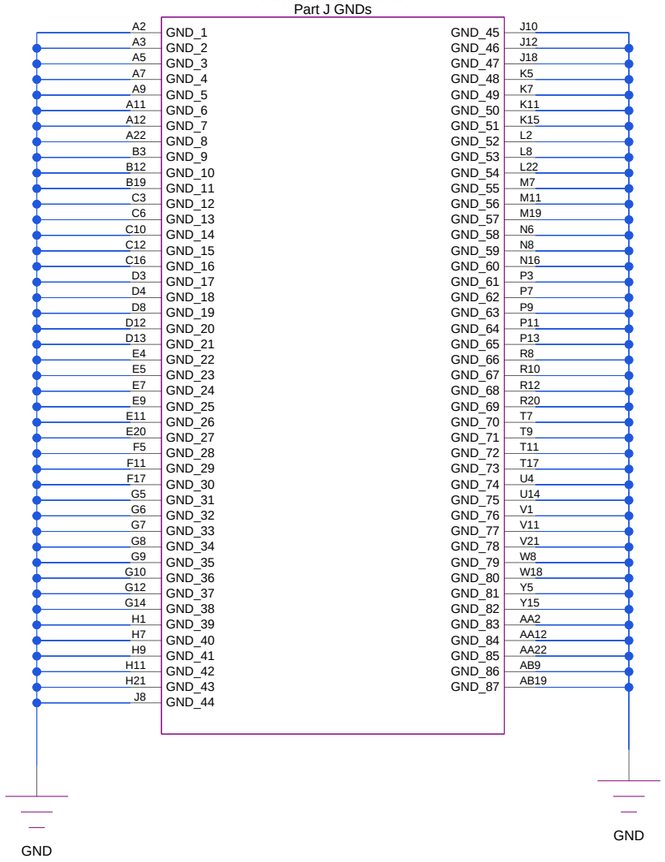


VCCAUX CAPS







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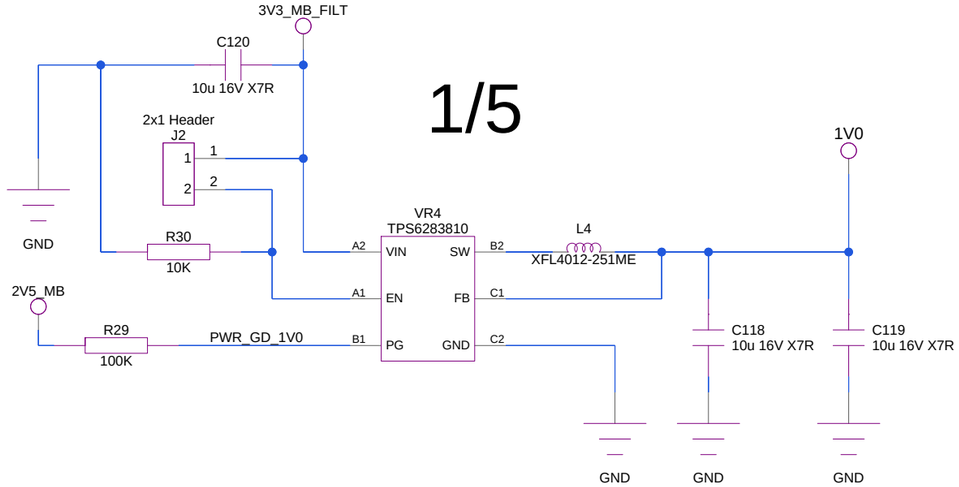
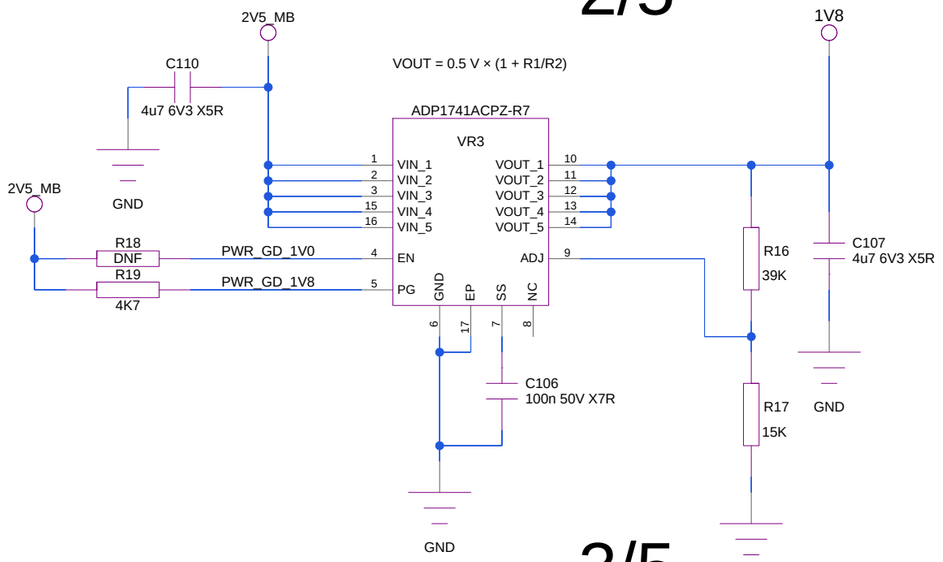
Title: MIB_FPGA_Module	SIZE: A3	DRAWING NUMBER: PPP/DUN/DAQ/004	
REV	DATE 14/03/2023:07:20	FPGA VCC + GND	SHEET 7 OF 8

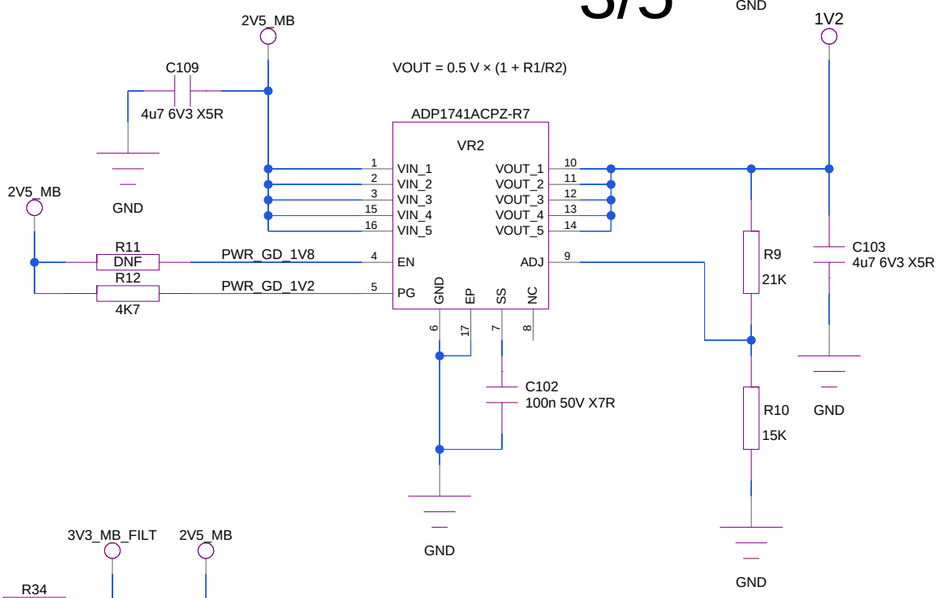
1/5



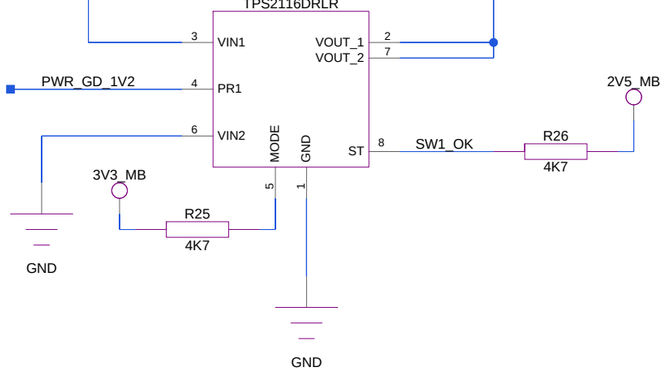
2/5



3/5



5/5



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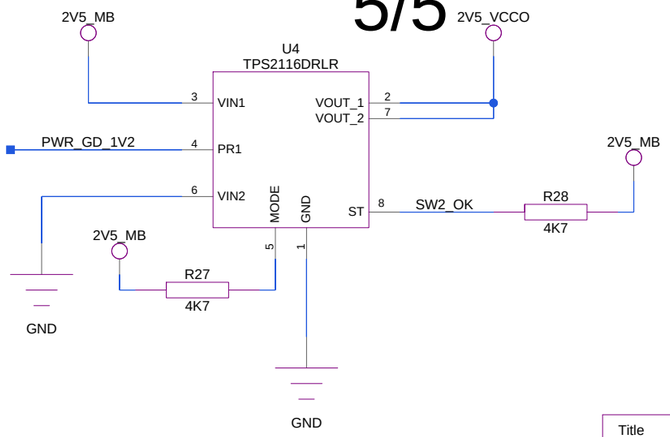

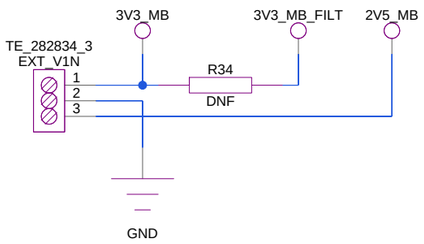

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SIZE A3

DRAWING NUMBER PPP/DUN/DAQ/004

Regulators

Title MIB_FPGA_Module

REV

DATE 22/03/2023:15:18

SHEET 8 OF 8