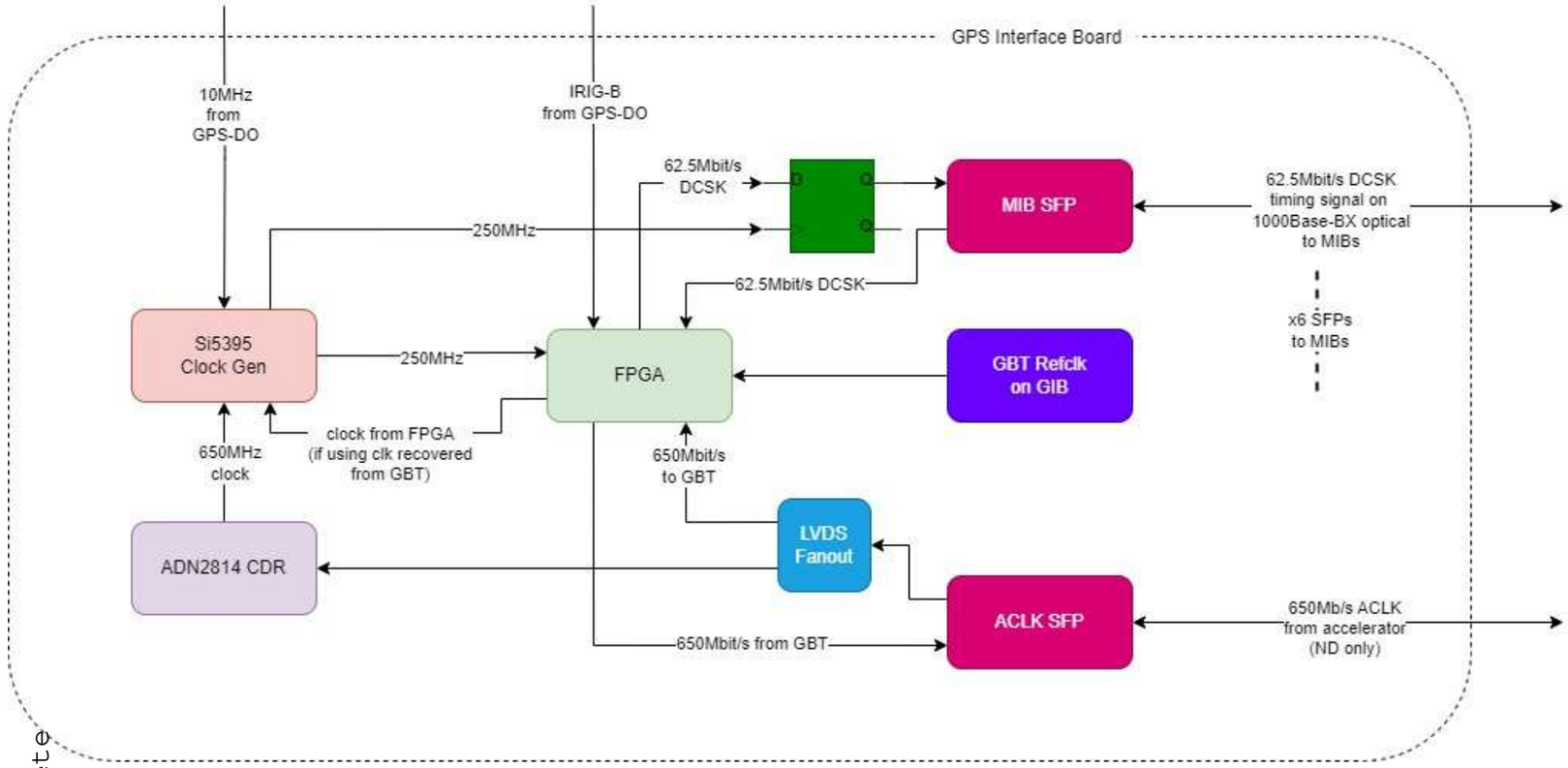

Part	I2C Address
ACLK SFP	0x50
ACLK CDR	0x40
SFP 1	0x50
SFP 2	
SFP 3	
SFP 4	
SFP 5	
SFP 6	

Part	I2C Address
Board ID EEPROM	0x50
SI5395 Clock Gen.	0x68
I2C Extender 1	0x74
I2C Extender 2	0x75
VCC5V Power Monitor	0x67
VCC3V3 Power Monitor	0x6A
VCC2V5 Power Monitor	0x69
I2C Switch	0x70
Temperature Monitor	0x48

This power consumption table is obsolete
Update/Remove

Power Estimate			Max Current (mA)				
Part	Description	Occurence	VCC5V	VCC3V3	VCC2V5	VCC1V8	12V Main PWR
LTC6957-2	Sine Wave to LVDS	1		72			
MAX9371	Low Jitter 5V TTL to LVDS	2	16				
SN74avc2t45	5V <--> 3.3V	1	100	100			
SN74avc2t45	3.3V <--> 2.5V	5		100	100		
SI5395	Clock Generator	1		302		300	
LTC2945	Power Monitor	4	1.2				
24AA025E48T	Board ID EEPROM	1		3			
LEDs		13		20			
NB7V52M	Diff. Flip-Flop	6			90		
ADN2814	CDR	6		145			
SFP		6		280			
SN74lvc1g32	OR Gate	12		100			
PCA9539	I2C Extender	2		160			
TCA9548A	I2C Switch	1			100		
LM75A	Temp Monitor	1		20			
NC7SZ08	AND Gate	1		50			
SN65LVDM176	LVDS Transceiver	2		15			
TXB0104(6)	Level Translator	2		100	100		
	Totals	Current (A)	0.14	5.41	1.14	0.30	
		Power (W)	0.68	17.84	3.76	0.54	22.83
	Max Power Supply	Current (A)	2	8			4
		Power (W)	11	28			48

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Design Title: GPS Interface Board
Schematic Title: 00. GIB Top
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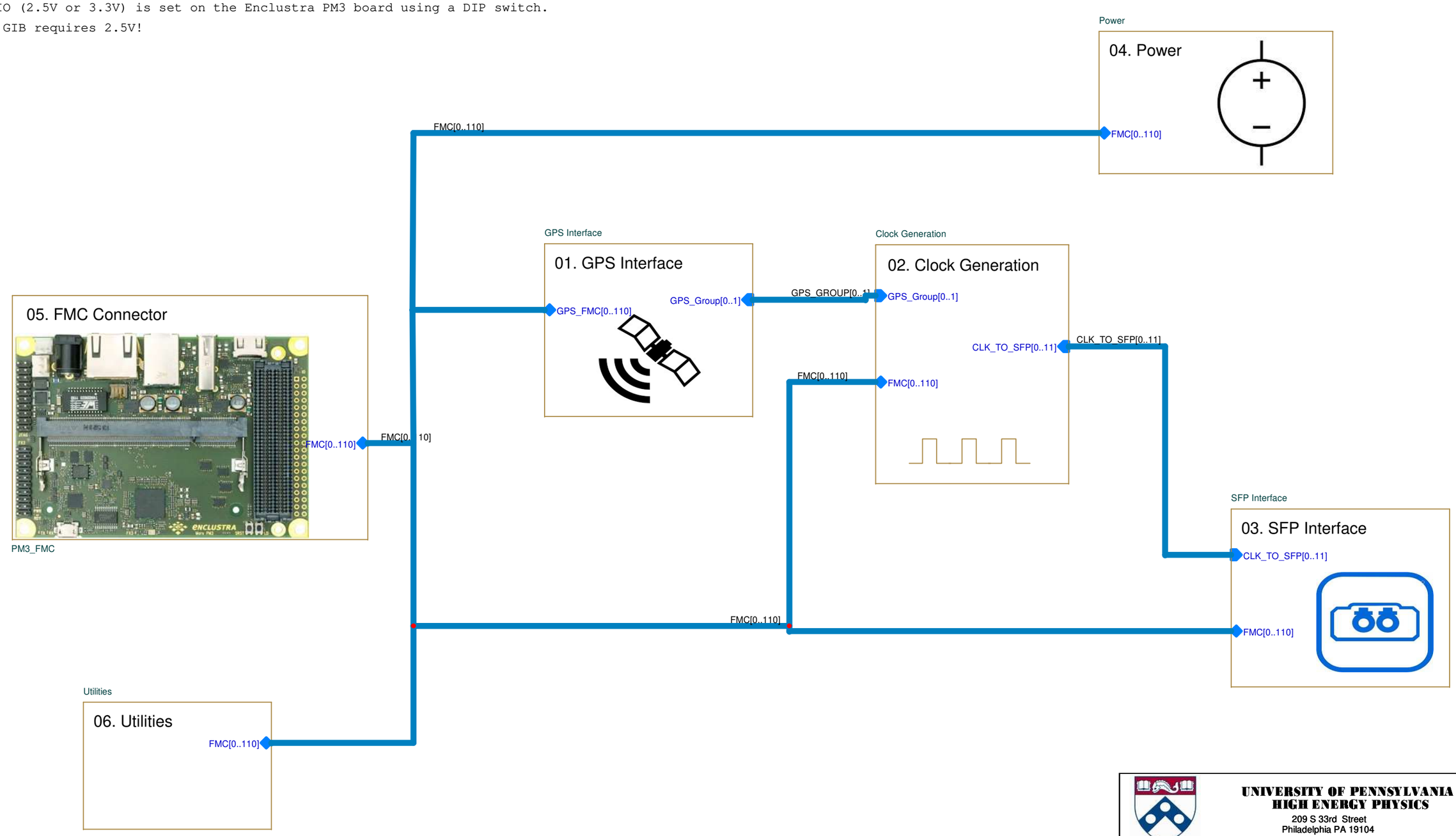
VCCIO (2.5V or 3.3V) is set on the Enclustra PM3 board using a DIP switch.
The GIB requires 2.5V!



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Design Title:	GPS Interface Board
Schematic Title:	00. GIB Top
Page Title:	02. Top Level

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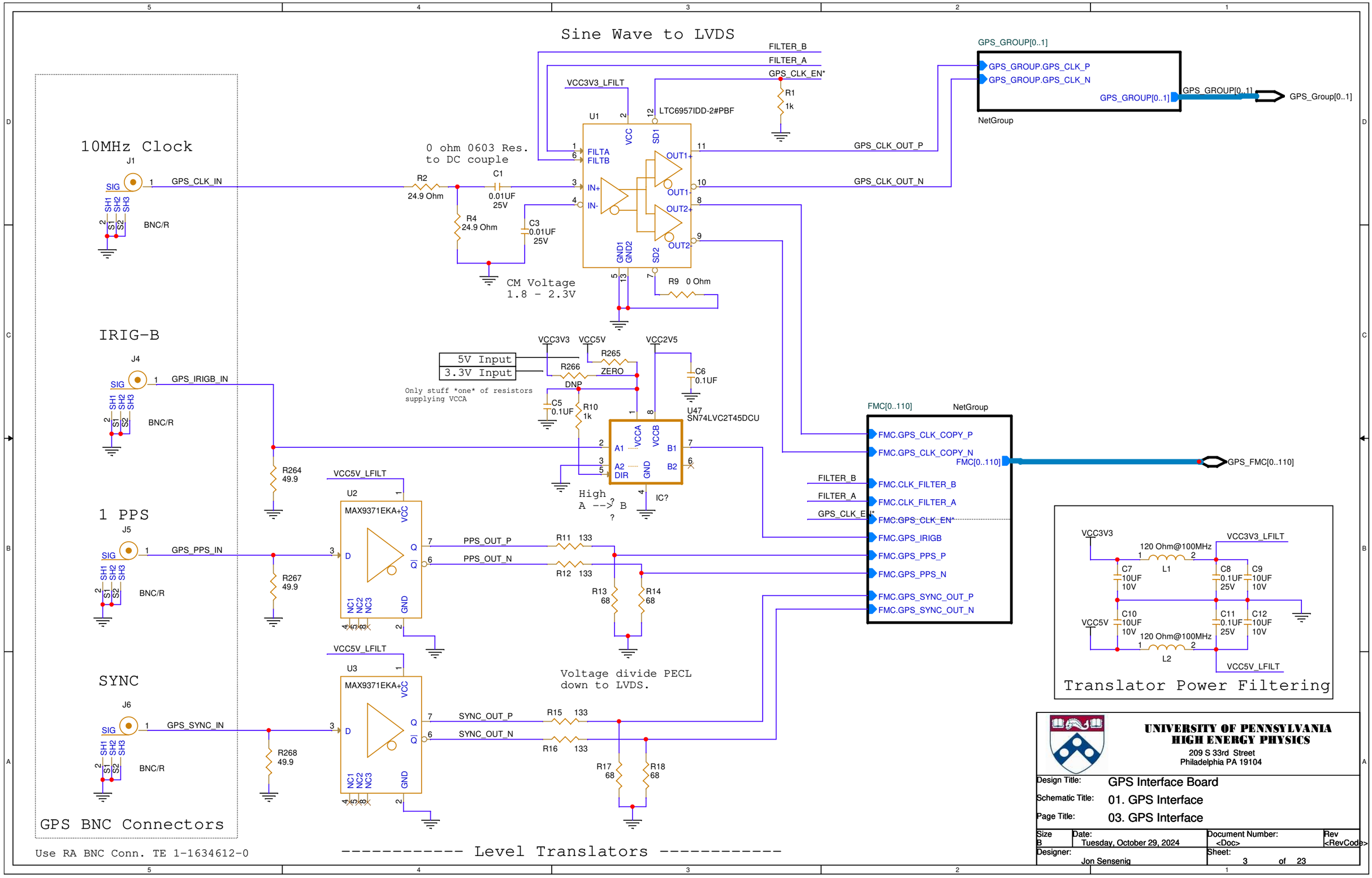
Sine Wave to LVDS
10MHz Clock
J1
SIG
GPS_CLK_IN
BNC/R
0 ohm 0603 Res.
to DC couple
R2
24.9 Ohm
C1
0.01UF
25V
R4
24.9 Ohm
C3
0.01UF
25V
CM Voltage
1.8 - 2.3V
U1
LTC6957IDD-2#PBF
FILTA
FILTB
IN+
IN-
OUT1+
OUT1-
OUT2+
OUT2-
VCC
SD1
GND1
GND2
SD2
VCC3V3_LFILT
FILTER_B
FILTER_A
GPS_CLK_EN*
R1
1k
GPS_CLK_OUT_P
GPS_CLK_OUT_N
R9 0 Ohm
GPS_GROUP[0..1]
GPS_GROUP.GPS_CLK_P
GPS_GROUP.GPS_CLK_N
NetGroup
GPS_Group[0..1]
IRIG-B
J4
GPS_IRIGB_IN
5V Input
3.3V Input
Only stuff *one* of resistors
supplying VCCA
VCC3V3
VCC5V
VCC2V5
R265
R266
ZERO
DNP
C5
0.1UF
R10
1k
C6
0.1UF
U47
SN74LVC2T45DCU
VCCA
VCCB
A1
A2
DIR
GND
B1
B2
High
A --> B
IC?
R264
49.9
1 PPS
J5
GPS_PPS_IN
R267
49.9
VCC5V_LFILT
U2
MAX9371EKA+
VCC
D
Q
Q|
NC1
NC2
NC3
GND
PPS_OUT_P
PPS_OUT_N
R11 133
R12 133
R13
68
R14
68
SYNC
J6
GPS_SYNC_IN
R268
49.9
U3
SYNC_OUT_P
SYNC_OUT_N
R15 133
R16 133
R17
68
R18
68
Voltage divide PECL
down to LVDS.
GPS BNC Connectors
Use RA BNC Conn. TE 1-1634612-0
---------- Level Translators ----------
FMC[0..110]
NetGroup
FMC.GPS_CLK_COPY_P
FMC.GPS_CLK_COPY_N
FMC.CLK_FILTER_B
FMC.CLK_FILTER_A
FMC.GPS_CLK_EN*
FMC.GPS_IRIGB
FMC.GPS_PPS_P
FMC.GPS_PPS_N
FMC.GPS_SYNC_OUT_P
FMC.GPS_SYNC_OUT_N
GPS_FMC[0..110]
VCC3V3
VCC3V3_LFILT
120 Ohm@100MHz
L1
C7
10UF
10V
C8
0.1UF
25V
C9
10UF
10V
VCC5V
C10
10UF
10V
C11
0.1UF
25V
C12
10UF
10V
L2
VCC5V_LFILT
Translator Power Filtering
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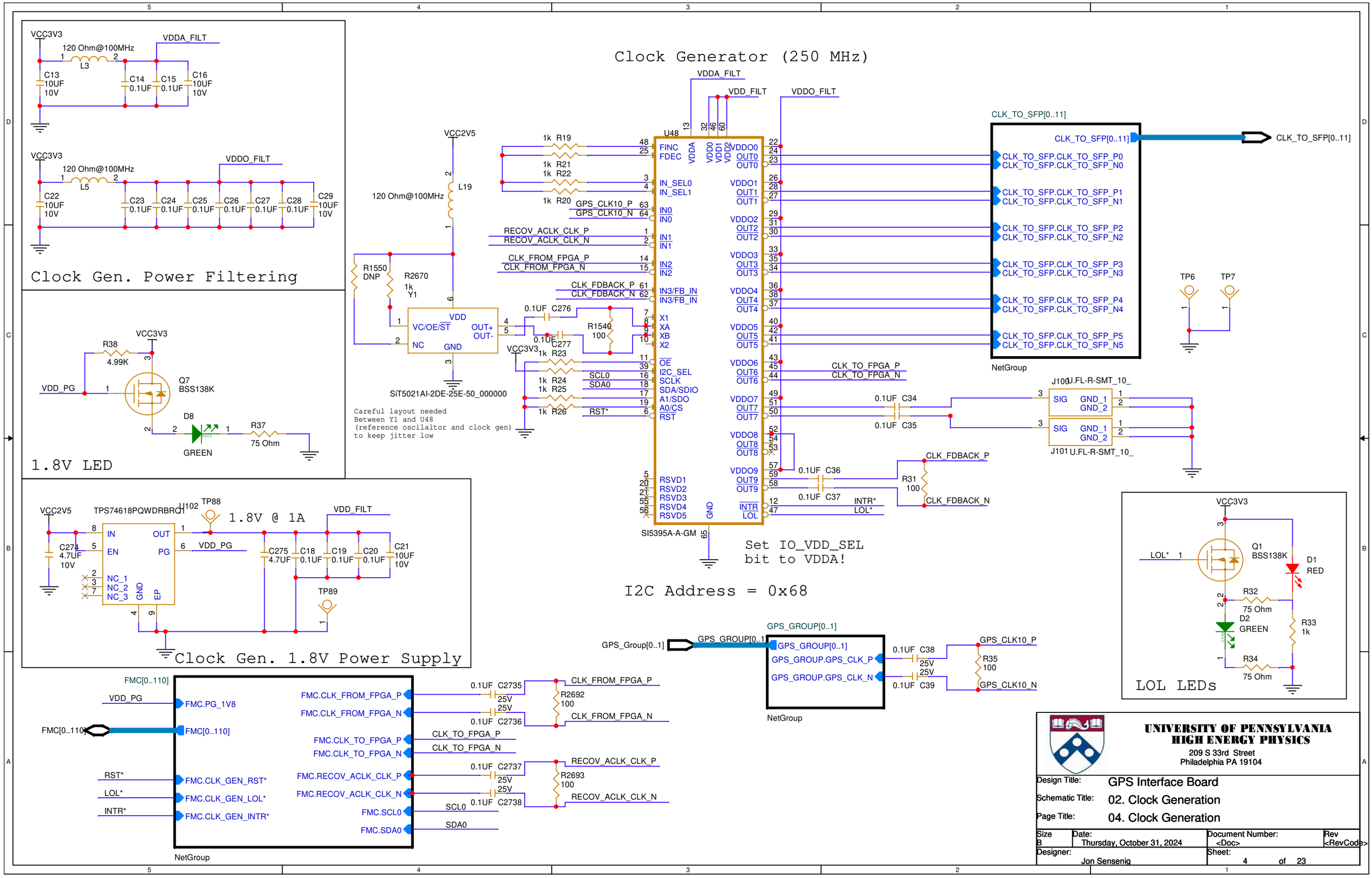
Clock Generator (250 MHz)
Clock Gen. Power Filtering
VCC3V3
120 Ohm@100MHz
L3
VDDA_FILT
C13 10UF 10V
C14 0.1UF
C15 0.1UF
C16 10UF 10V
L5
VDDO_FILT
C22 10UF 10V
C23 0.1UF
C24 0.1UF
C25 0.1UF
C26 0.1UF
C27 0.1UF
C28 0.1UF
C29 10UF 10V
1.8V LED
R38 4.99K
VDD_PG
Q7 BSS138K
D8 GREEN
R37 75 Ohm
Clock Gen. 1.8V Power Supply
VCC2V5
TPS74618PQWDRBRQ1
U102
TP88
1.8V @ 1A
VDD_FILT
C274 4.7UF 10V
C275 4.7UF
C18 0.1UF
C19 0.1UF
C20 0.1UF
C21 10UF 10V
TP89
IN
OUT
EN
PG
NC_1
NC_2
NC_3
GND
EP
VDD_PG
L19
120 Ohm@100MHz
R1550 DNP
R2670 1k
Y1
VDD
VC/OE/ST
OUT+
OUT-
NC
GND
SiT5021AI-2DE-25E-50_000000
Careful layout needed
Between Y1 and U48
(reference oscilaltor and clock gen)
to keep jitter low
U48
SI5395A-A-GM
FINC
FDEC
IN_SEL0
IN_SEL1
IN0
IN1
IN2
IN3/FB_IN
X1
XA
XB
X2
OE
I2C_SEL
SCLK
SDA/SDIO
A1/SDO
A0/CS
RST
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
VDDA
VDD0
VDD1
VDD2
VDDO0
OUT0
VDDO1
OUT1
VDDO2
OUT2
VDDO3
OUT3
VDDO4
OUT4
VDDO5
OUT5
VDDO6
OUT6
VDDO7
OUT7
VDDO8
OUT8
VDDO9
OUT9
INTR
LOL
VDD_FILT
VDDO_FILT
1k R19
1k R21
1k R22
1k R20
GPS_CLK10_P
GPS_CLK10_N
RECOV_ACLK_CLK_P
RECOV_ACLK_CLK_N
CLK_FROM_FPGA_P
CLK_FROM_FPGA_N
CLK_FDBACK_P
CLK_FDBACK_N
0.1UF C276
0.1UF C277
R1540 100
1k R23
1k R24
1k R25
1k R26
SCL0
SDA0
RST*
CLK_TO_SFP[0..11]
CLK_TO_SFP.CLK_TO_SFP_P0
CLK_TO_SFP.CLK_TO_SFP_N0
CLK_TO_SFP.CLK_TO_SFP_P1
CLK_TO_SFP.CLK_TO_SFP_N1
CLK_TO_SFP.CLK_TO_SFP_P2
CLK_TO_SFP.CLK_TO_SFP_N2
CLK_TO_SFP.CLK_TO_SFP_P3
CLK_TO_SFP.CLK_TO_SFP_N3
CLK_TO_SFP.CLK_TO_SFP_P4
CLK_TO_SFP.CLK_TO_SFP_N4
CLK_TO_SFP.CLK_TO_SFP_P5
CLK_TO_SFP.CLK_TO_SFP_N5
NetGroup
TP6
TP7
CLK_TO_FPGA_P
CLK_TO_FPGA_N
0.1UF C34
0.1UF C35
J100 U.FL-R-SMT_10_
J101 U.FL-R-SMT_10_
SIG
GND_1
GND_2
0.1UF C36
0.1UF C37
R31 100
INTR*
LOL*
Set IO_VDD_SEL
bit to VDDA!
I2C Address = 0x68
GPS_Group[0..1]
GPS_GROUP[0..1]
GPS_GROUP.GPS_CLK_P
GPS_GROUP.GPS_CLK_N
0.1UF C38
0.1UF C39
25V
R35 100
GPS_CLK10_P
GPS_CLK10_N
NetGroup
LOL LEDs
Q1 BSS138K
D1 RED
D2 GREEN
R32 75 Ohm
R33 1k
R34 75 Ohm
FMC[0..110]
FMC.PG_1V8
FMC.CLK_GEN_RST*
FMC.CLK_GEN_LOL*
FMC.CLK_GEN_INTR*
FMC.CLK_FROM_FPGA_P
FMC.CLK_FROM_FPGA_N
FMC.CLK_TO_FPGA_P
FMC.CLK_TO_FPGA_N
FMC.RECOV_ACLK_CLK_P
FMC.RECOV_ACLK_CLK_N
FMC.SCL0
FMC.SDA0
0.1UF C2735
0.1UF C2736
0.1UF C2737
0.1UF C2738
R2692 100
R2693 100
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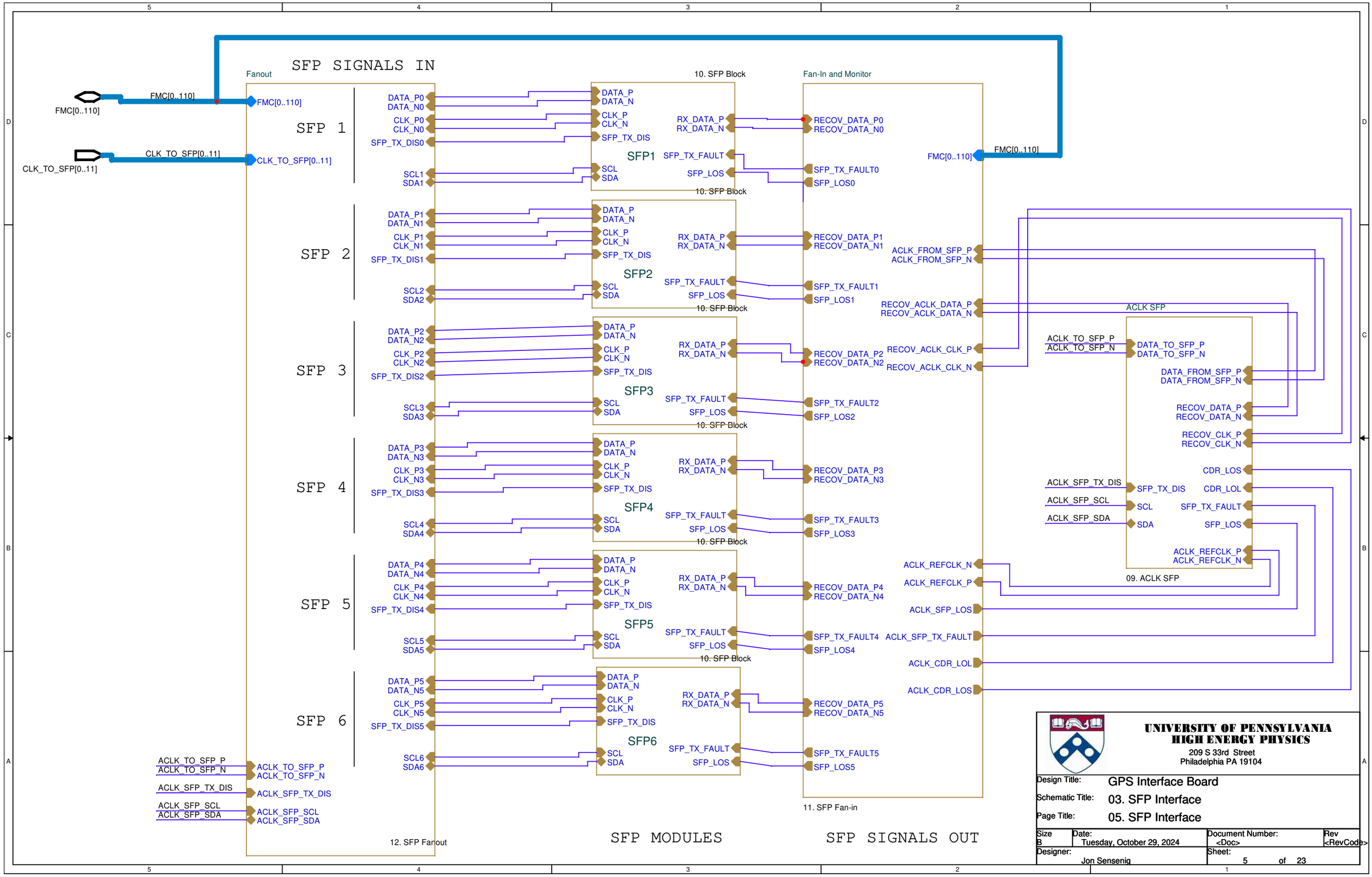

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Schematic Title:	03. SFP Interface
Page Title:	05. SFP Interface

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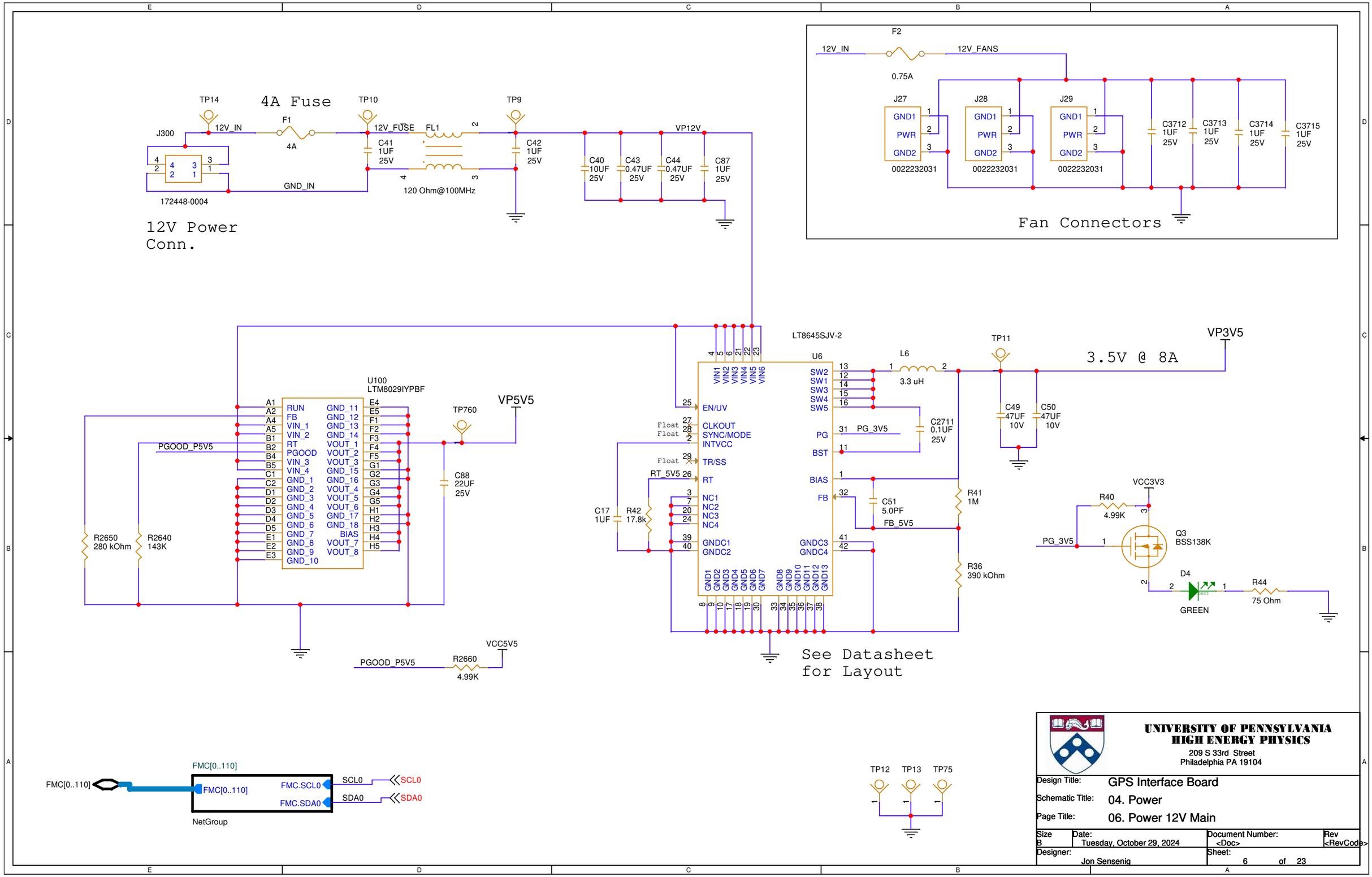

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Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	06. Power 12V Main
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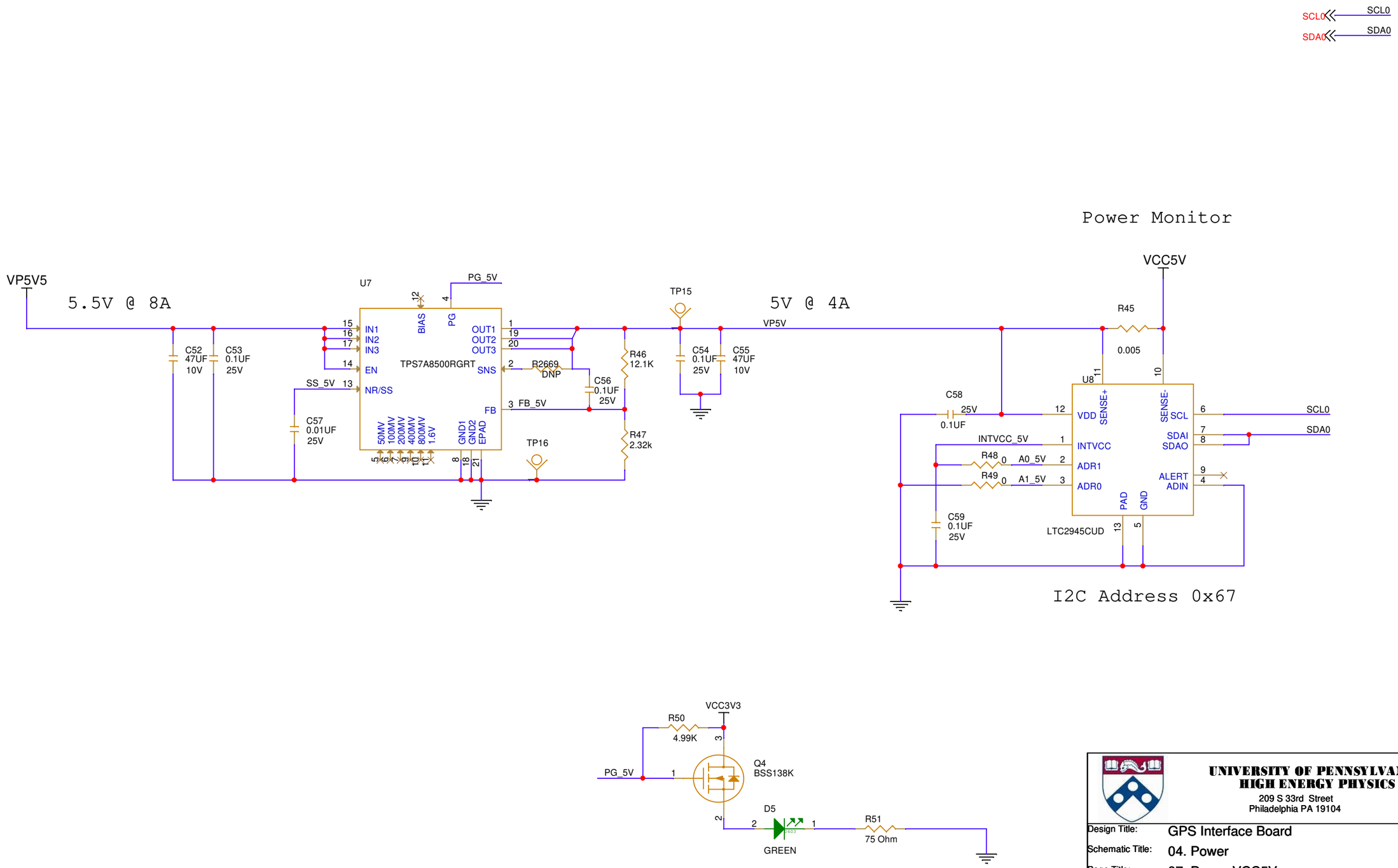

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Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	07. Power VCC5V

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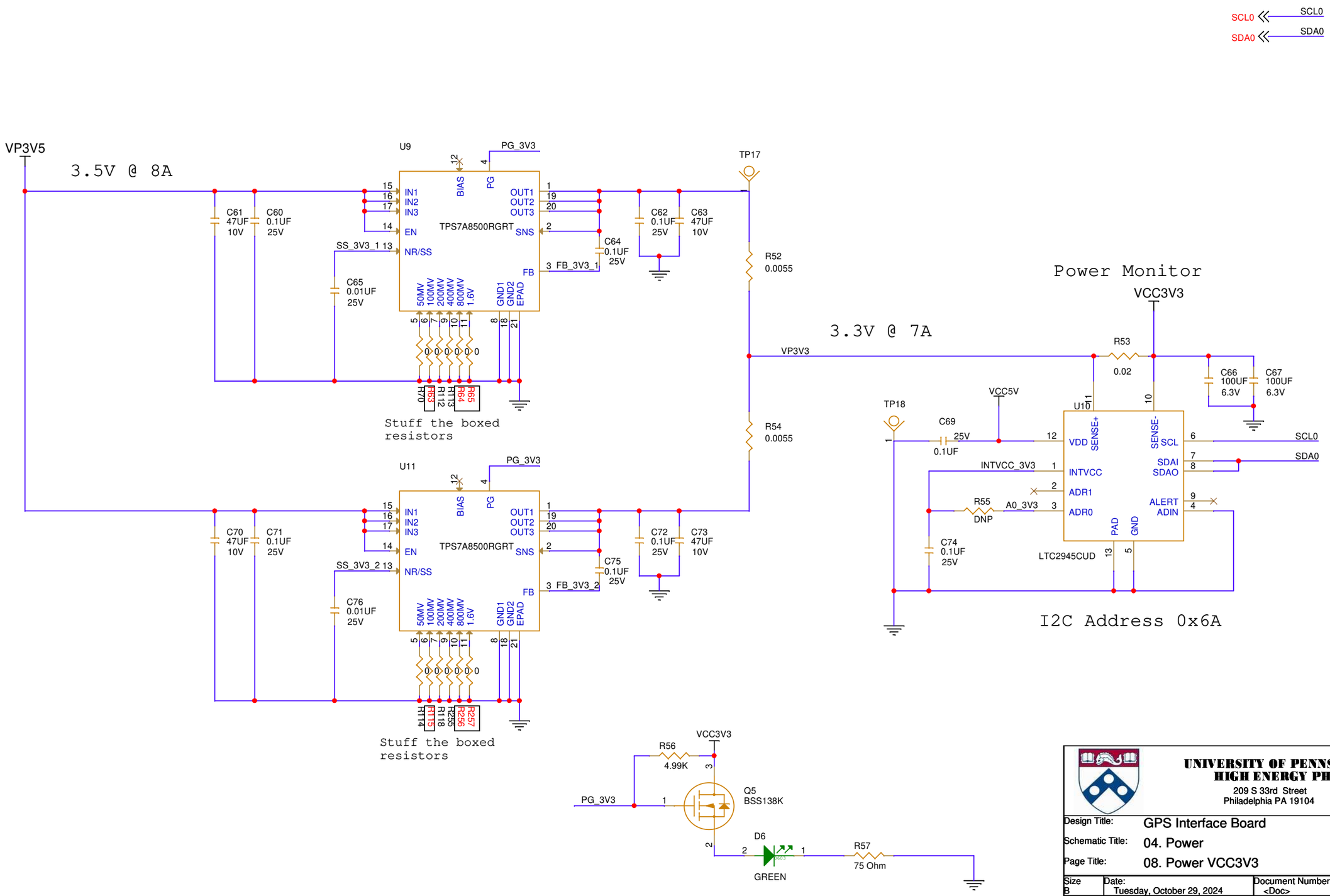
Designer: Jon Sensenig		Sheet: 7 of 23	



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Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	08. Power VCC3V3

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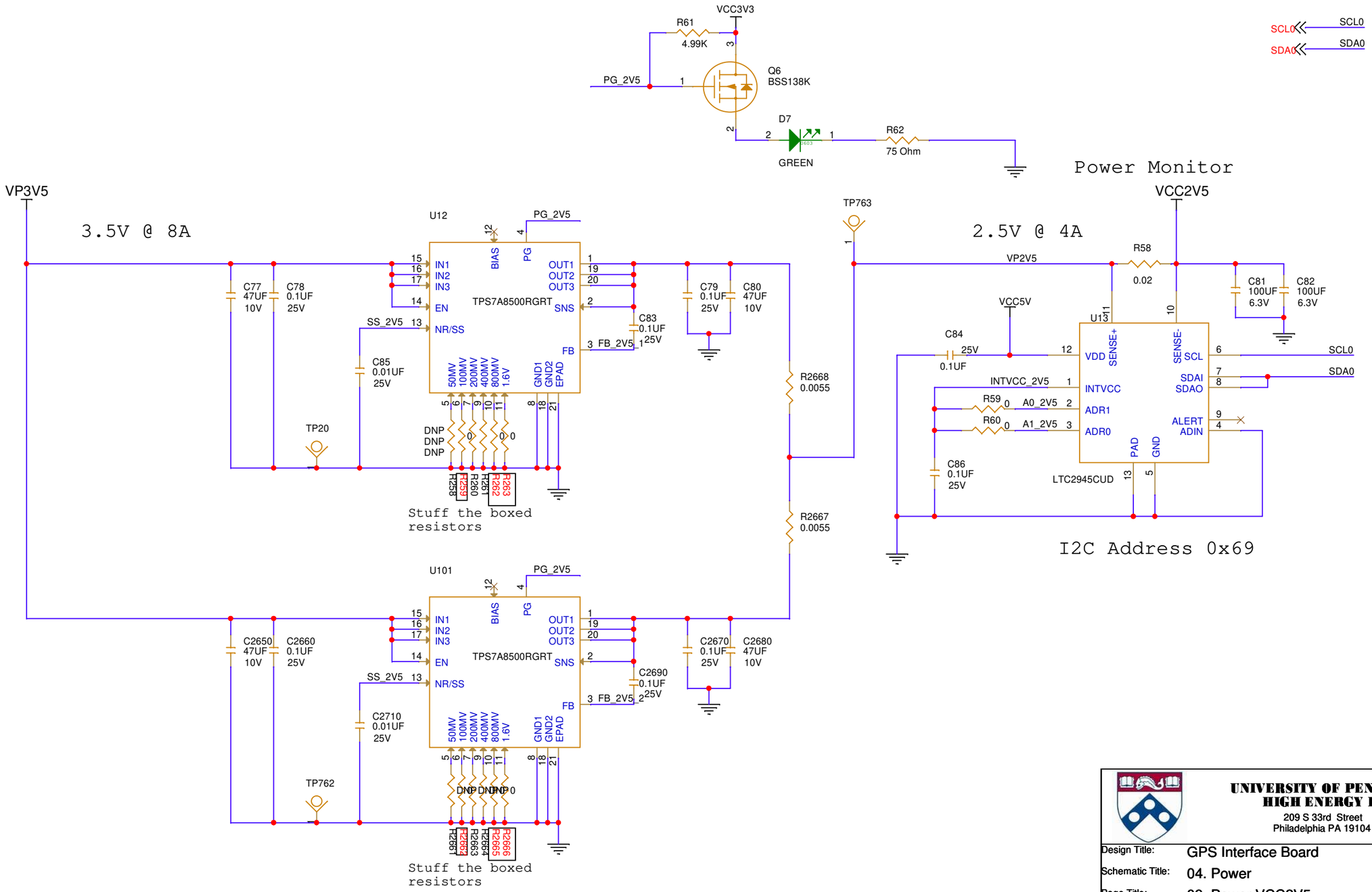

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Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	09. Power VCC2V5

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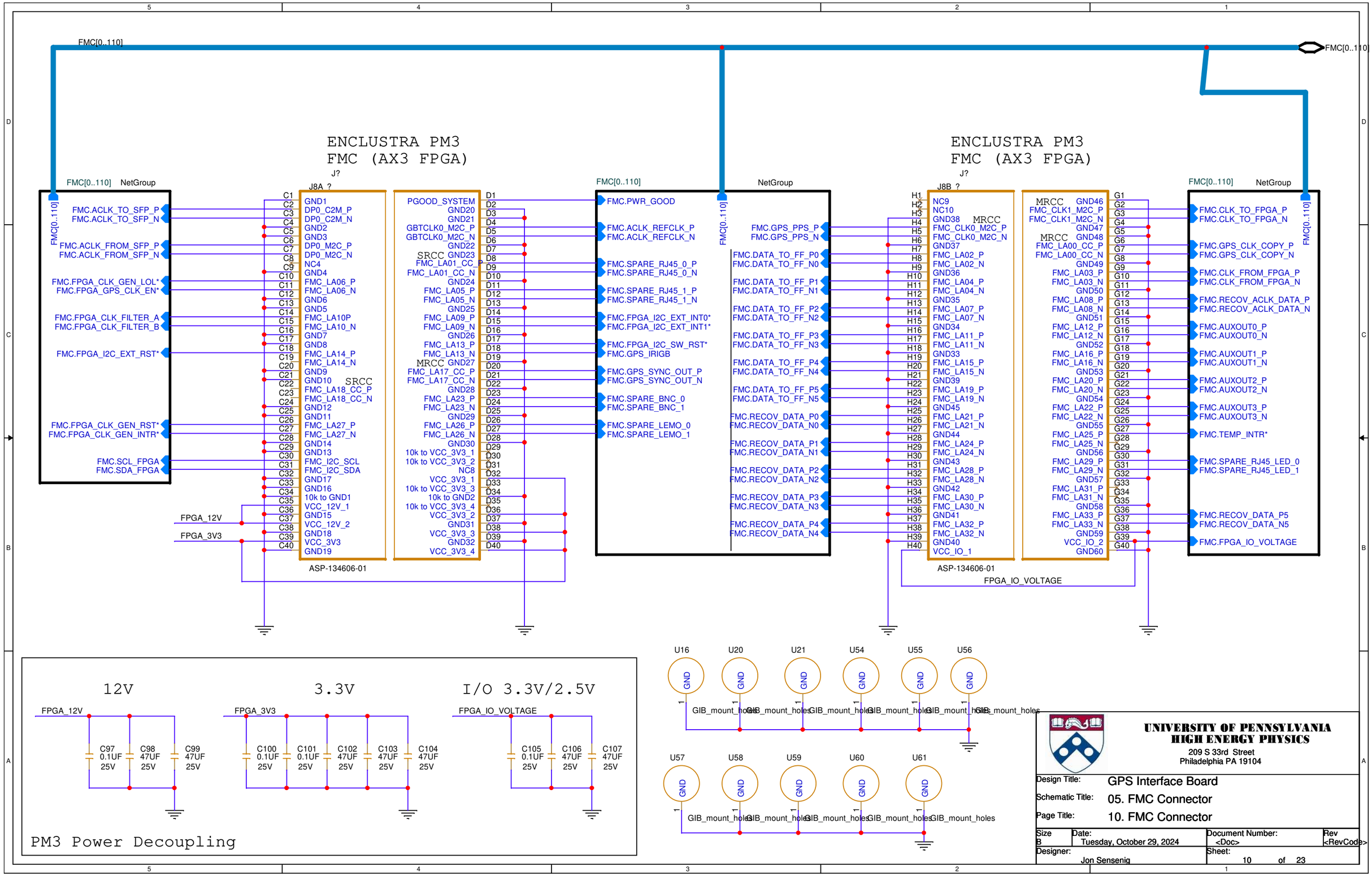
FMC[0..110]
ENCLUSTRA PM3
FMC (AX3 FPGA)
J?
J8A ?
J8B ?
NetGroup
FMC.ACLK_TO_SFP_P
FMC.ACLK_TO_SFP_N
FMC.ACLK_FROM_SFP_P
FMC.ACLK_FROM_SFP_N
FMC.FPGA_CLK_GEN_LOL*
FMC.FPGA_GPS_CLK_EN*
FMC.FPGA_CLK_FILTER_A
FMC.FPGA_CLK_FILTER_B
FMC.FPGA_I2C_EXT_RST*
FMC.FPGA_CLK_GEN_RST*
FMC.FPGA_CLK_GEN_INTR*
FMC.SCL_FPGA
FMC.SDA_FPGA
FMC.PWR_GOOD
FMC.ACLK_REFCLK_P
FMC.ACLK_REFCLK_N
FMC.SPARE_RJ45_0_P
FMC.SPARE_RJ45_0_N
FMC.SPARE_RJ45_1_P
FMC.SPARE_RJ45_1_N
FMC.FPGA_I2C_EXT_INT0*
FMC.FPGA_I2C_EXT_INT1*
FMC.FPGA_I2C_SW_RST*
FMC.GPS_IRIGB
FMC.GPS_SYNC_OUT_P
FMC.GPS_SYNC_OUT_N
FMC.SPARE_BNC_0
FMC.SPARE_BNC_1
FMC.SPARE_LEMO_0
FMC.SPARE_LEMO_1
FMC.GPS_PPS_P
FMC.GPS_PPS_N
FMC.DATA_TO_FF_P0
FMC.DATA_TO_FF_N0
FMC.DATA_TO_FF_P1
FMC.DATA_TO_FF_N1
FMC.DATA_TO_FF_P2
FMC.DATA_TO_FF_N2
FMC.DATA_TO_FF_P3
FMC.DATA_TO_FF_N3
FMC.DATA_TO_FF_P4
FMC.DATA_TO_FF_N4
FMC.DATA_TO_FF_P5
FMC.DATA_TO_FF_N5
FMC.RECOV_DATA_P0
FMC.RECOV_DATA_N0
FMC.RECOV_DATA_P1
FMC.RECOV_DATA_N1
FMC.RECOV_DATA_P2
FMC.RECOV_DATA_N2
FMC.RECOV_DATA_P3
FMC.RECOV_DATA_N3
FMC.RECOV_DATA_P4
FMC.RECOV_DATA_N4
FMC.CLK_TO_FPGA_P
FMC.CLK_TO_FPGA_N
FMC.GPS_CLK_COPY_P
FMC.GPS_CLK_COPY_N
FMC.CLK_FROM_FPGA_P
FMC.CLK_FROM_FPGA_N
FMC.RECOV_ACLK_DATA_P
FMC.RECOV_ACLK_DATA_N
FMC.AUXOUT0_P
FMC.AUXOUT0_N
FMC.AUXOUT1_P
FMC.AUXOUT1_N
FMC.AUXOUT2_P
FMC.AUXOUT2_N
FMC.AUXOUT3_P
FMC.AUXOUT3_N
FMC.TEMP_INTR*
FMC.SPARE_RJ45_LED_0
FMC.SPARE_RJ45_LED_1
FMC.RECOV_DATA_P5
FMC.RECOV_DATA_N5
FMC.FPGA_IO_VOLTAGE
FPGA_12V
FPGA_3V3
FPGA_IO_VOLTAGE
ASP-134606-01
12V
3.3V
I/O 3.3V/2.5V
C97 0.1UF 25V
C98 47UF 25V
C99 47UF 25V
C100 0.1UF 25V
C101 0.1UF 25V
C102 47UF 25V
C103 47UF 25V
C104 47UF 25V
C105 0.1UF 25V
C106 47UF 25V
C107 47UF 25V
PM3 Power Decoupling
U16
U20
U21
U54
U55
U56
U57
U58
U59
U60
U61
GND
GIB_mount_holes
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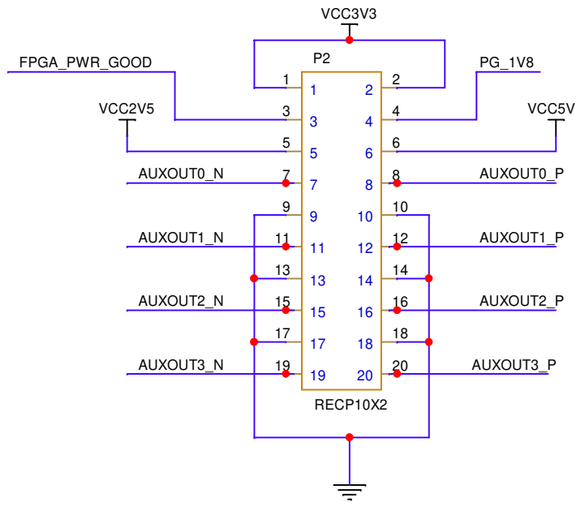
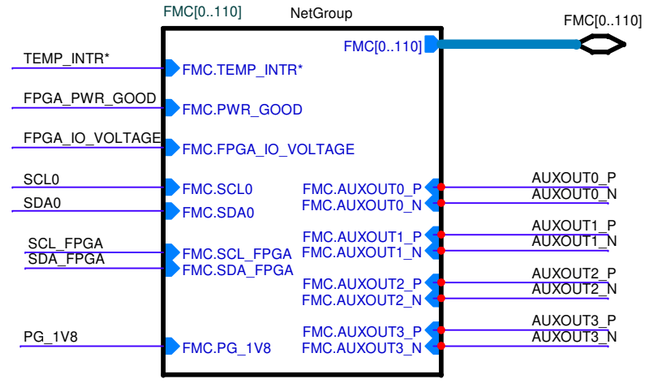
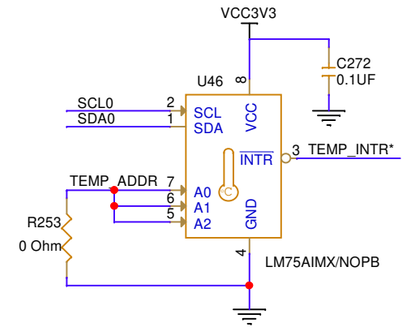


Connections to front panel LEDs / Auxilliary I/O





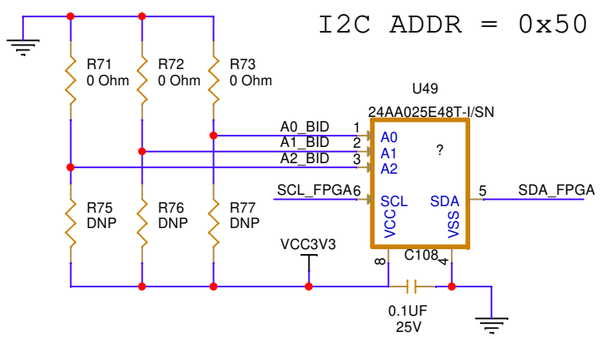
I2C ADDR = 0x48

Temp. Monitor

Note: Temperature measured from component's die.

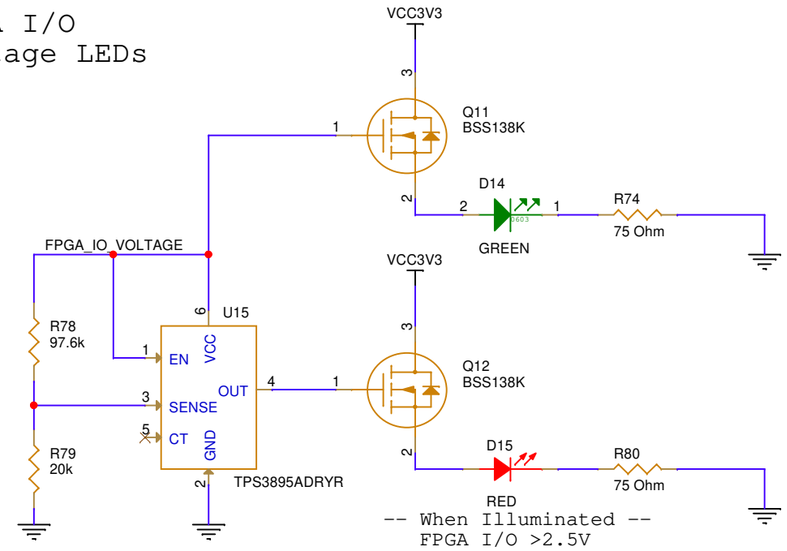
EEPROM

I2C ADDR = 0x50



Board ID

FPGA I/O
Voltage LEDs



-- When Illuminated --
FPGA I/O >2.5V
Change setting!

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Page Title:	13. Utilities

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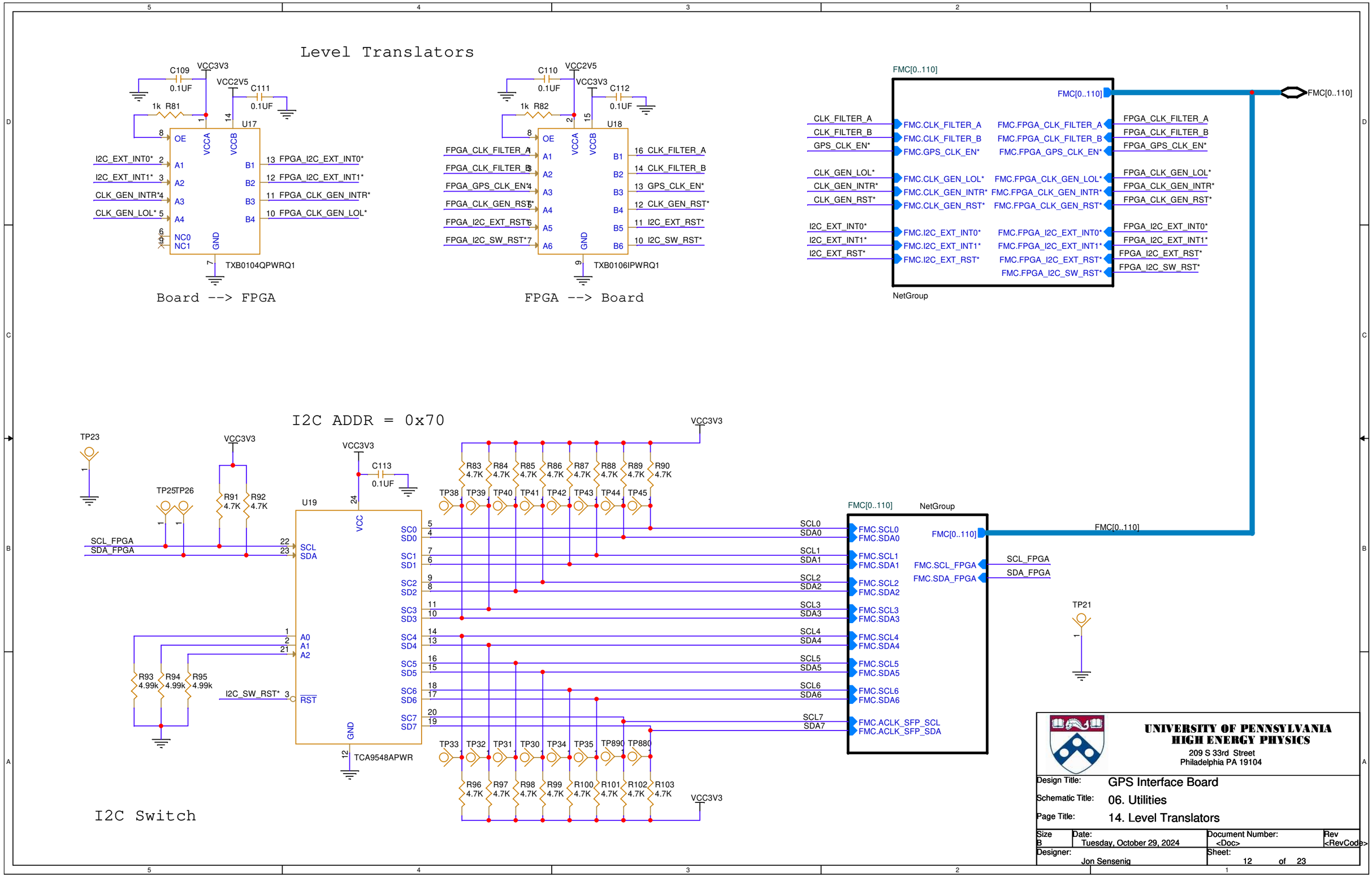

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Schematic Title:	06. Utilities
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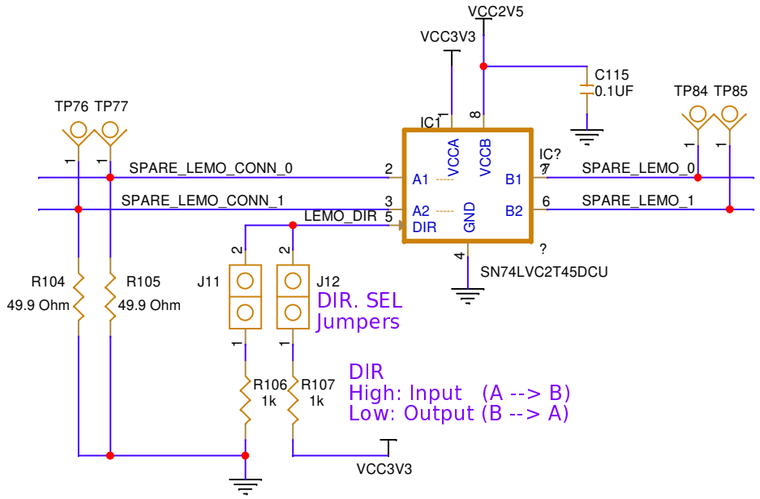
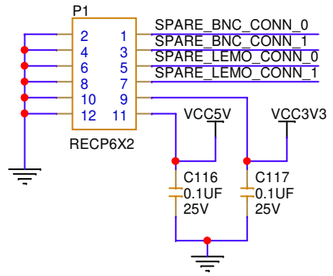
SPARE I/O
LEMO





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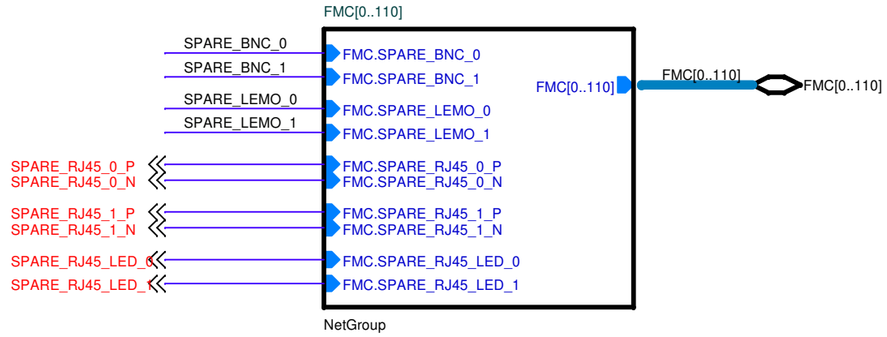

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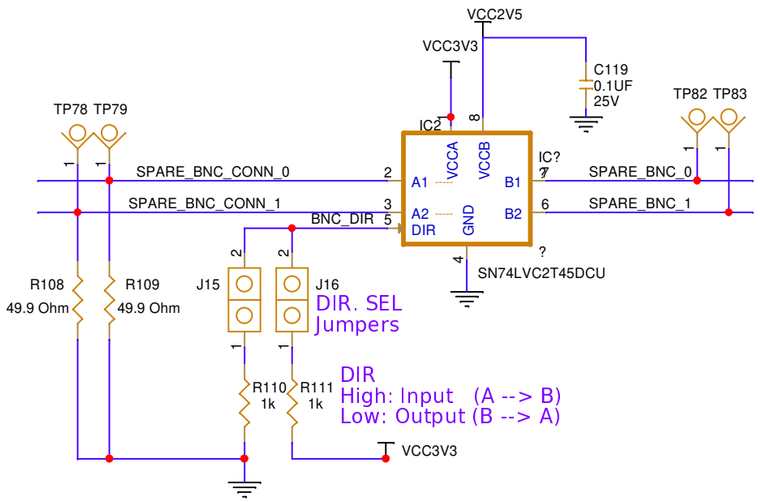

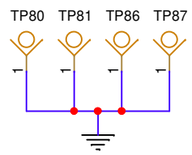

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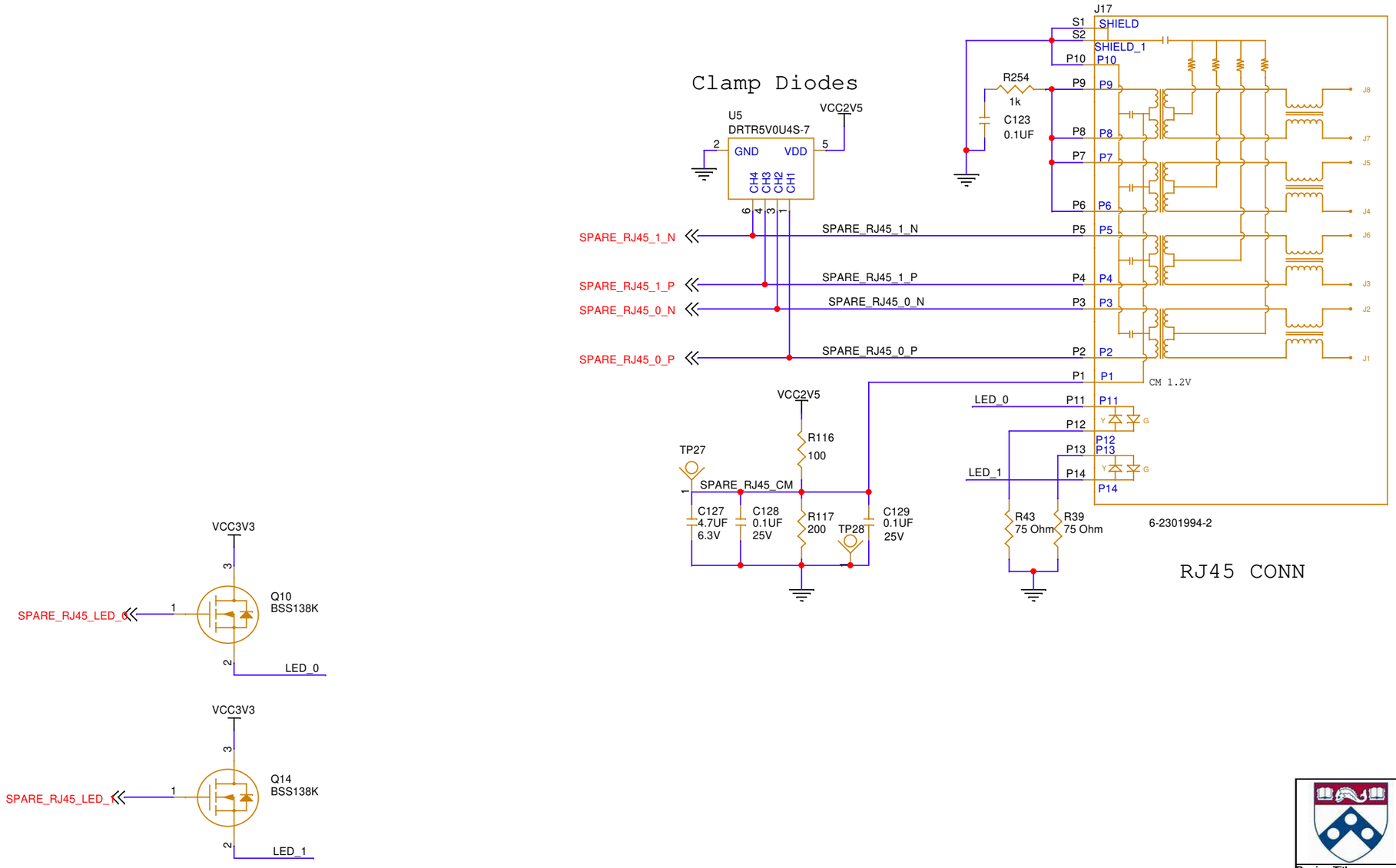

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Design Title:	GPS Interface Board
Schematic Title:	06. Utilities
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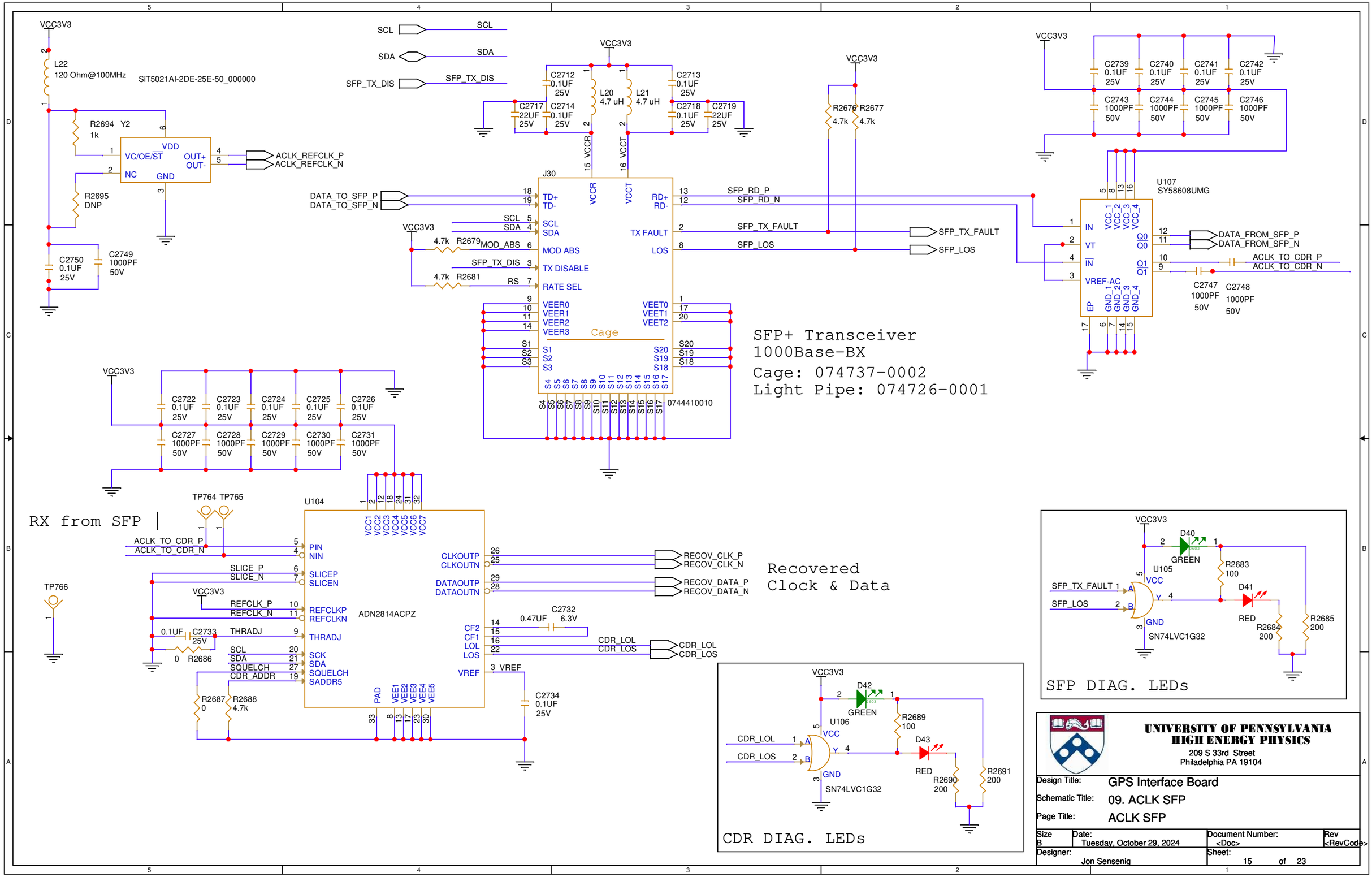
SFP+ Transceiver
1000Base-BX
Cage: 074737-0002
Light Pipe: 074726-0001
RX from SFP
Recovered
Clock & Data
SFP DIAG. LEDs
CDR DIAG. LEDs
SiT5021AI-2DE-25E-50_000000
J30
Cage
0744410010
U107
SY58608UMG
U104
ADN2814ACPZ
U105
U106
SN74LVC1G32
VCC3V3
SCL
SDA
SFP_TX_DIS
ACLK_REFCLK_P
ACLK_REFCLK_N
DATA_TO_SFP_P
DATA_TO_SFP_N
SFP_RD_P
SFP_RD_N
SFP_TX_FAULT
SFP_LOS
DATA_FROM_SFP_P
DATA_FROM_SFP_N
ACLK_TO_CDR_P
ACLK_TO_CDR_N
MOD_ABS
RS
RECOV_CLK_P
RECOV_CLK_N
RECOV_DATA_P
RECOV_DATA_N
CDR_LOL
CDR_LOS
SLICE_P
SLICE_N
REFCLK_P
REFCLK_N
THRADJ
SQUELCH
CDR_ADDR
TP764
TP765
TP766
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Schematic Title: 09. ACLK SFP
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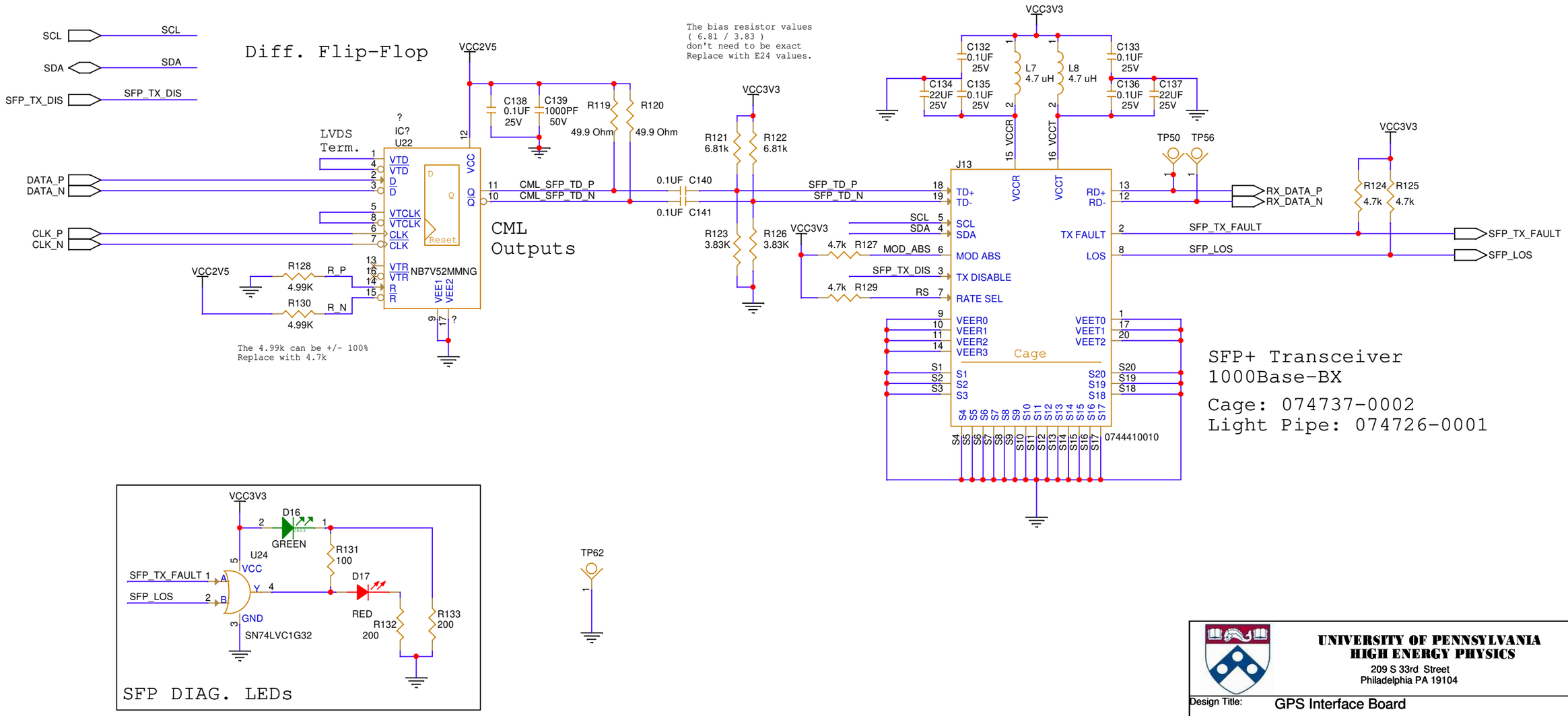

SFP DIAG. LEDs

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Schematic Title:	10. SFP Block
Page Title:	SFP

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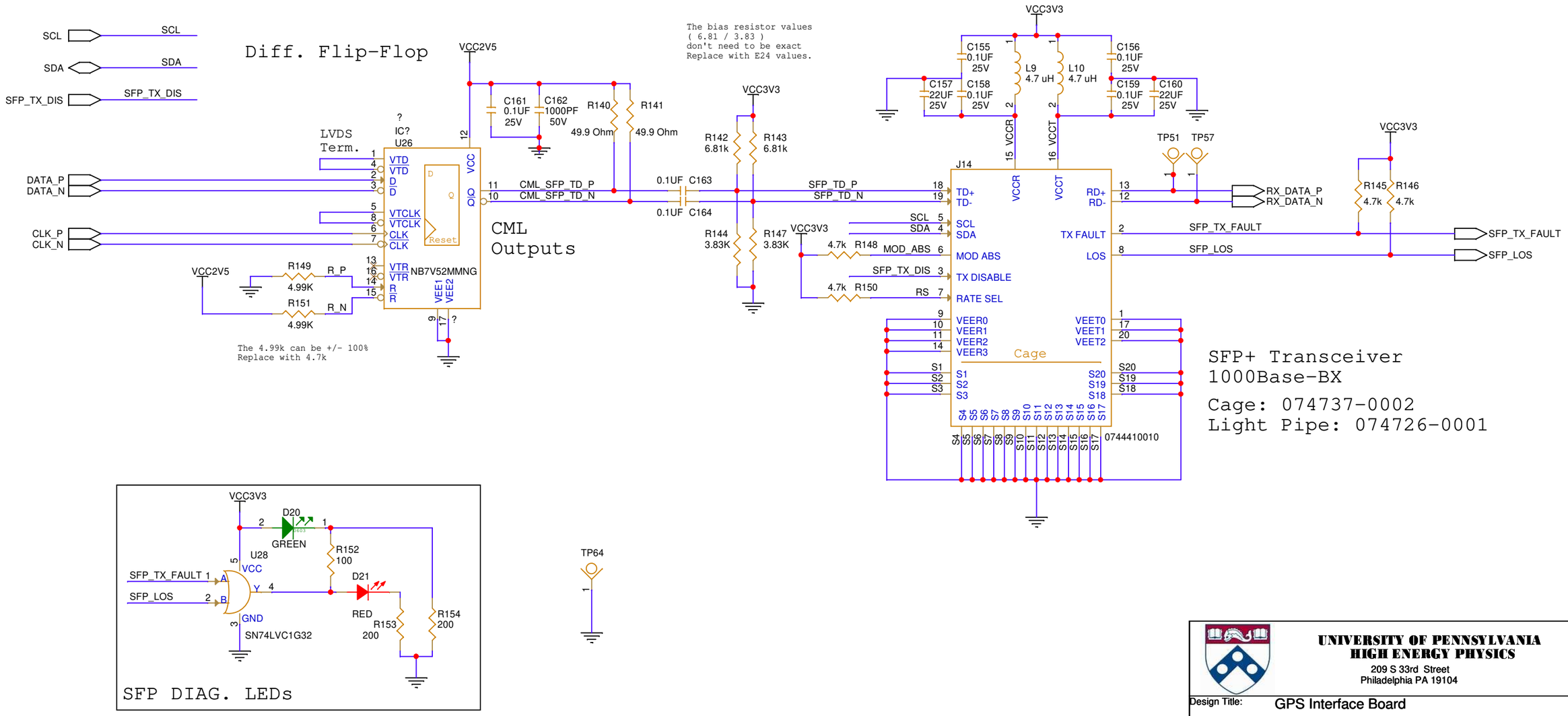

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Schematic Title:	10. SFP Block
Page Title:	SFP

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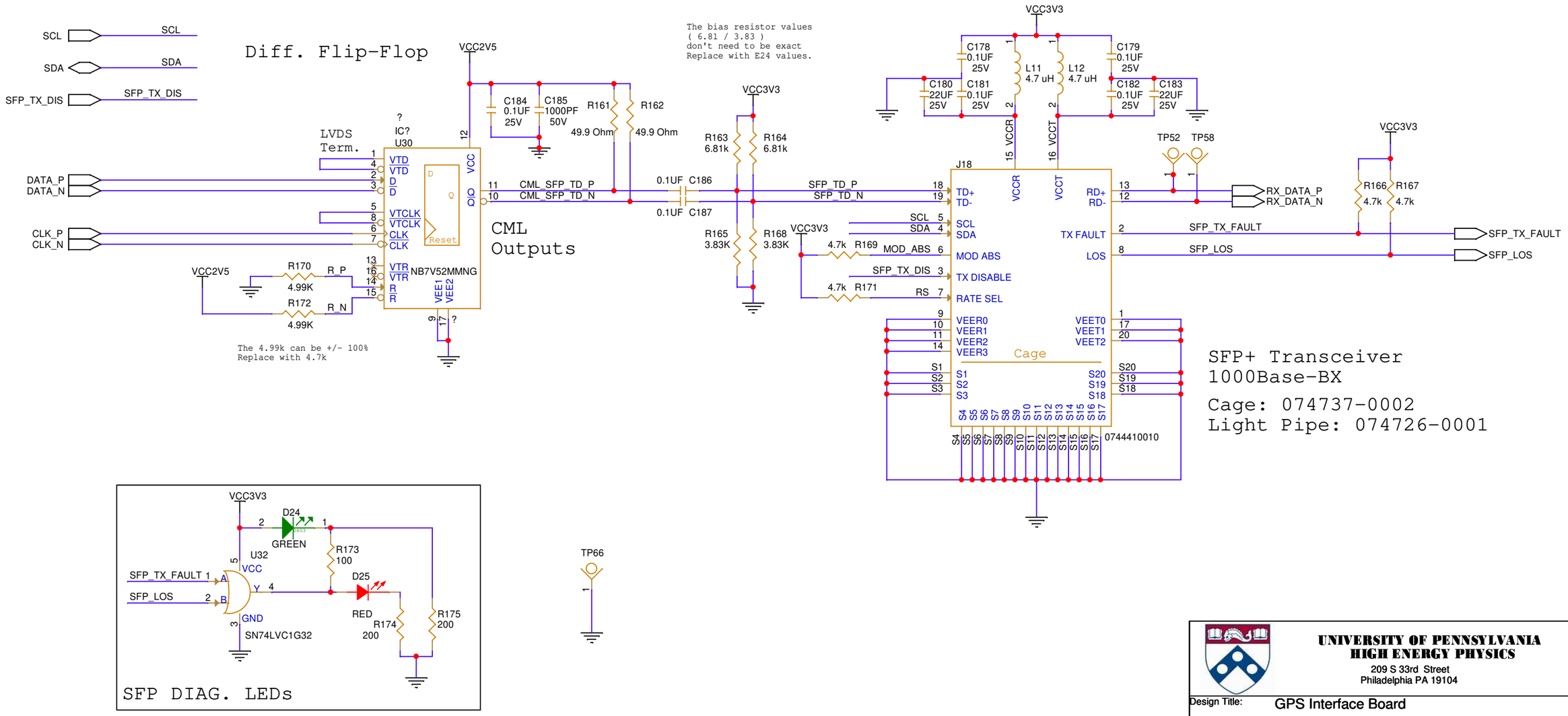

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Schematic Title:	10. SFP Block
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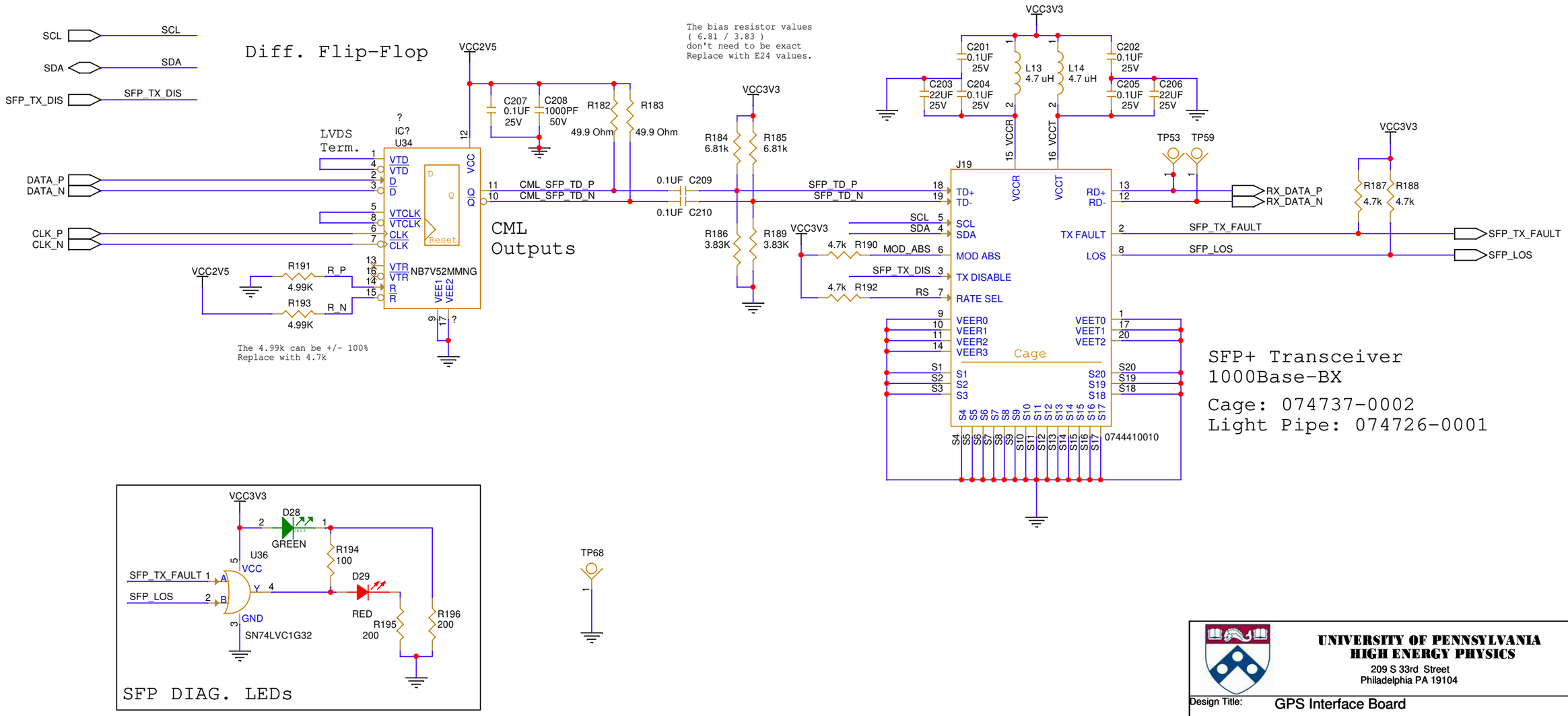

SFP DIAG. LEDs

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Schematic Title:	10. SFP Block
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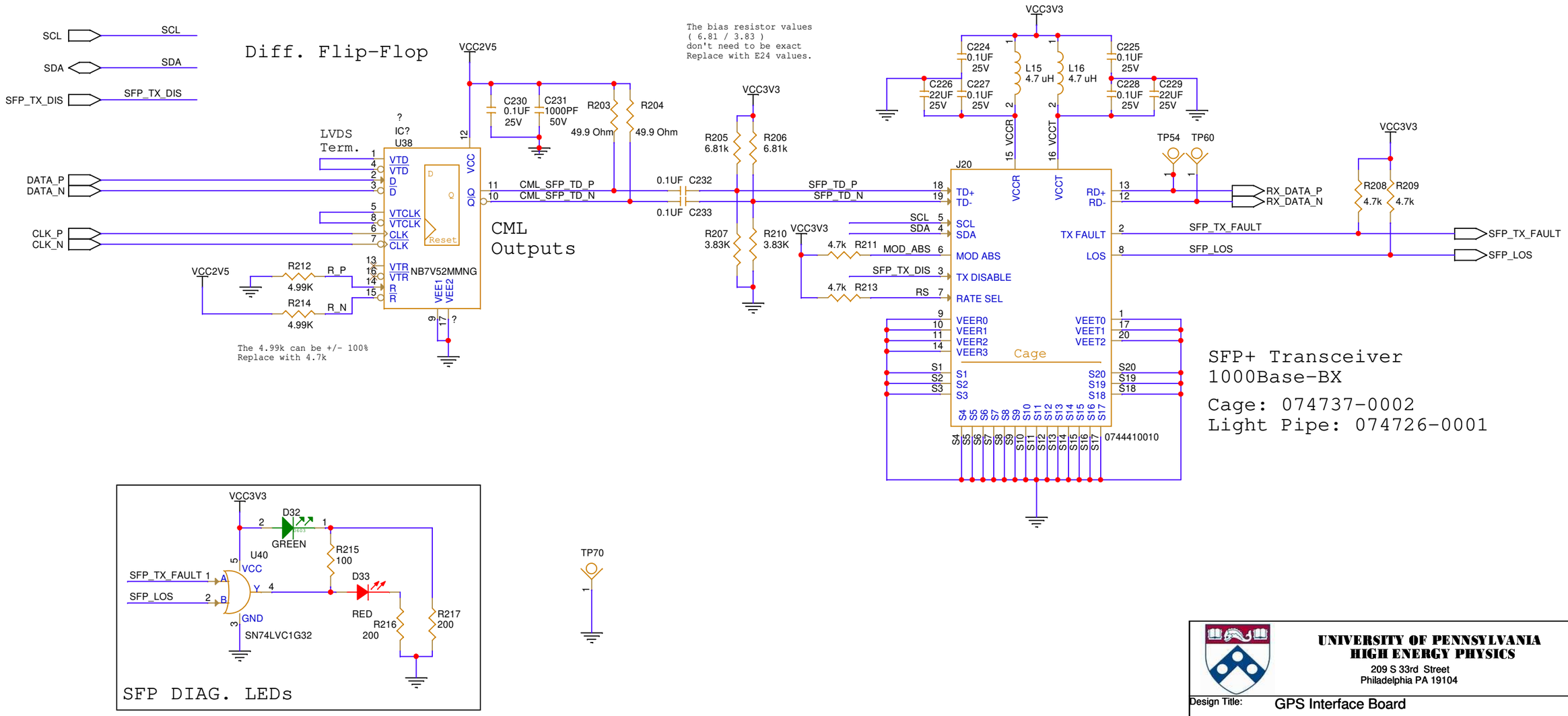

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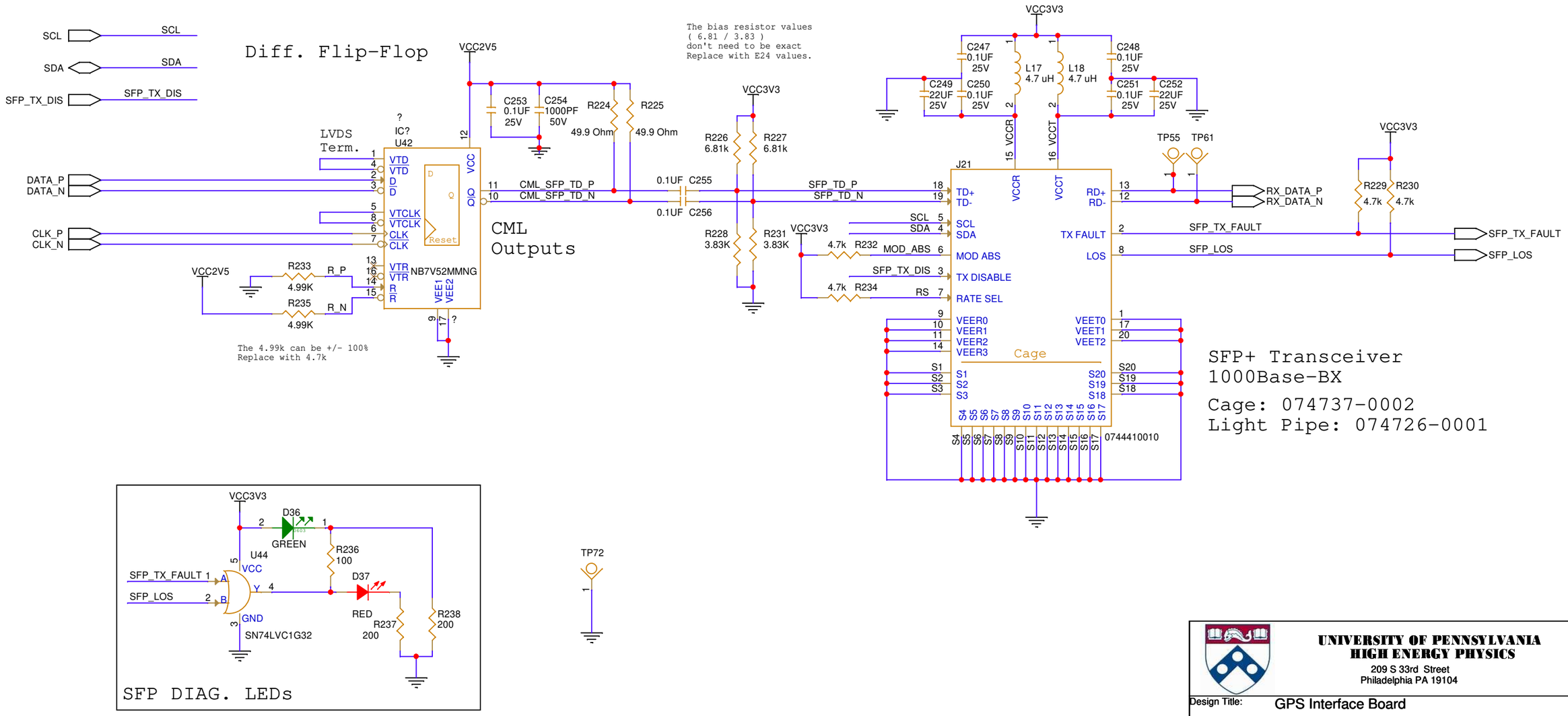

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Schematic Title:	10. SFP Block
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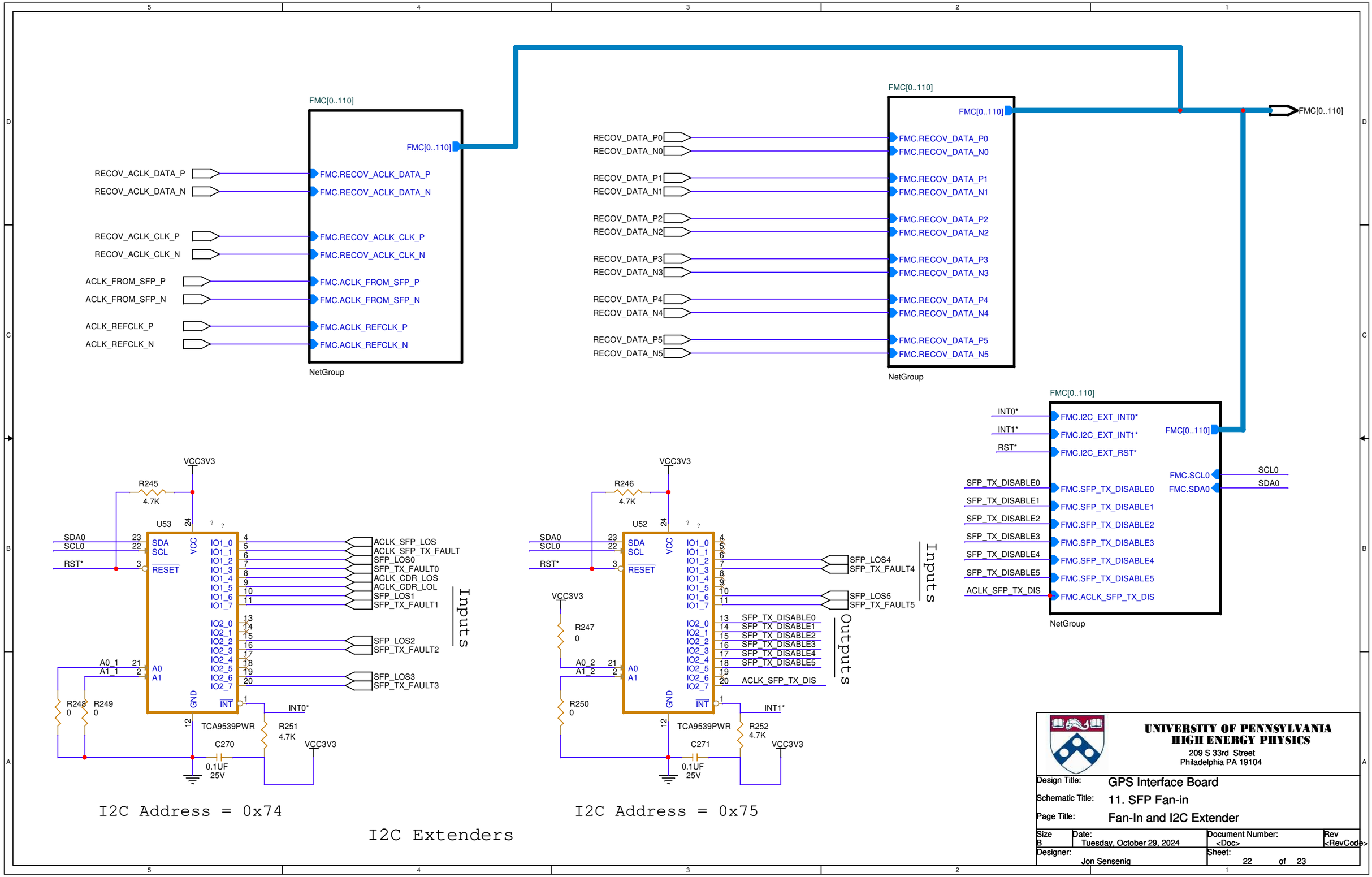

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Design Title:	GPS Interface Board
Schematic Title:	11. SFP Fan-in
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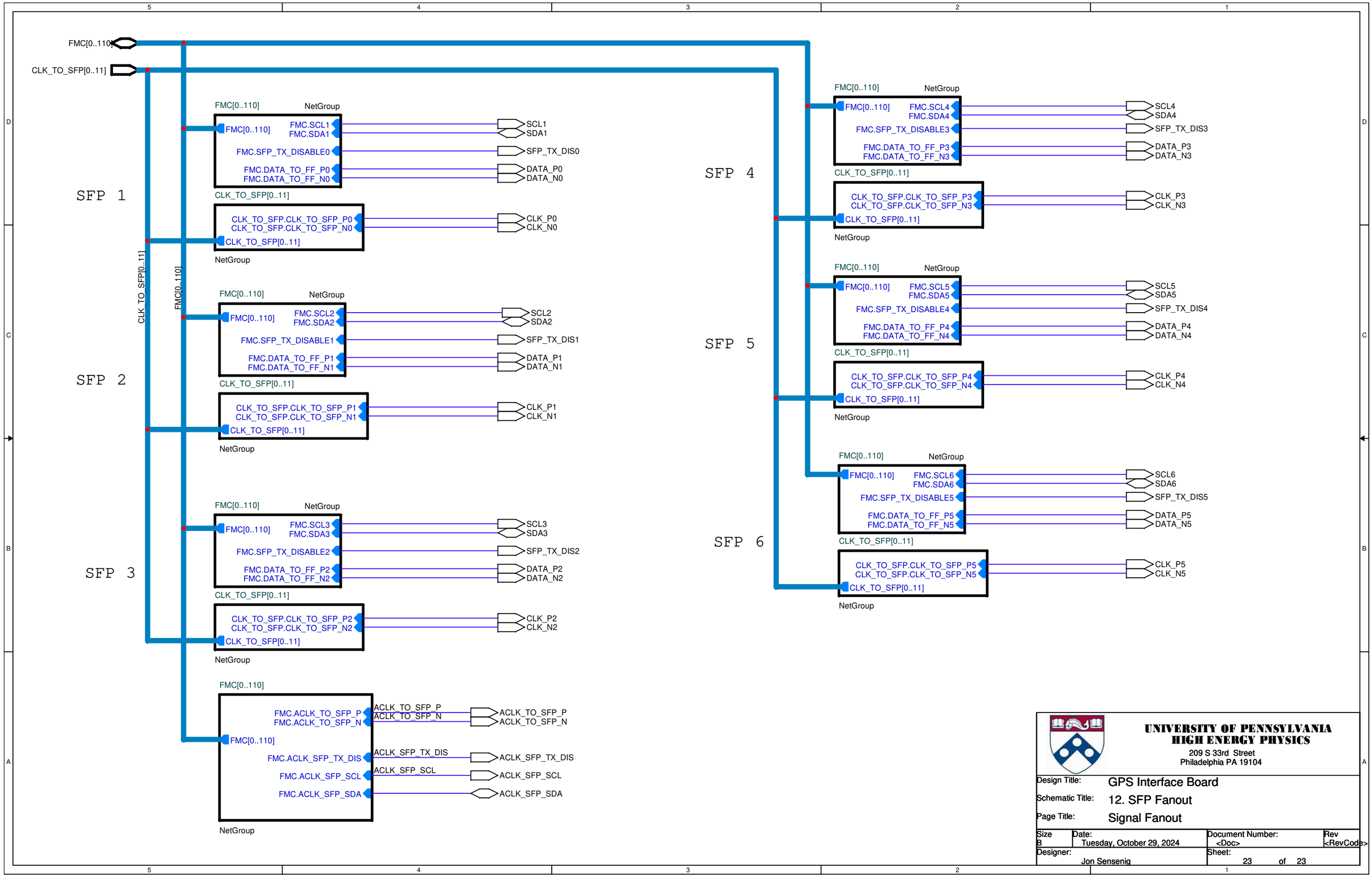
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CLK_TO_SFP[0..11]
SFP 1
FMC[0..110]
NetGroup
FMC[0..110]
FMC.SCL1
FMC.SDA1
FMC.SFP_TX_DISABLE0
FMC.DATA_TO_FF_P0
FMC.DATA_TO_FF_N0
CLK_TO_SFP[0..11]
SCL1
SDA1
SFP_TX_DIS0
DATA_P0
DATA_N0
CLK_TO_SFP.CLK_TO_SFP_P0
CLK_TO_SFP.CLK_TO_SFP_N0
CLK_TO_SFP[0..11]
NetGroup
CLK_P0
CLK_N0
SFP 2
FMC[0..110]
NetGroup
FMC[0..110]
FMC.SCL2
FMC.SDA2
FMC.SFP_TX_DISABLE1
FMC.DATA_TO_FF_P1
FMC.DATA_TO_FF_N1
CLK_TO_SFP[0..11]
SCL2
SDA2
SFP_TX_DIS1
DATA_P1
DATA_N1
CLK_TO_SFP.CLK_TO_SFP_P1
CLK_TO_SFP.CLK_TO_SFP_N1
CLK_TO_SFP[0..11]
NetGroup
CLK_P1
CLK_N1
SFP 3
FMC[0..110]
NetGroup
FMC[0..110]
FMC.SCL3
FMC.SDA3
FMC.SFP_TX_DISABLE2
FMC.DATA_TO_FF_P2
FMC.DATA_TO_FF_N2
CLK_TO_SFP[0..11]
SCL3
SDA3
SFP_TX_DIS2
DATA_P2
DATA_N2
CLK_TO_SFP.CLK_TO_SFP_P2
CLK_TO_SFP.CLK_TO_SFP_N2
CLK_TO_SFP[0..11]
NetGroup
CLK_P2
CLK_N2
FMC[0..110]
FMC.ACLK_TO_SFP_P
FMC.ACLK_TO_SFP_N
FMC[0..110]
FMC.ACLK_SFP_TX_DIS
FMC.ACLK_SFP_SCL
FMC.ACLK_SFP_SDA
ACLK_TO_SFP_P
ACLK_TO_SFP_N
ACLK_SFP_TX_DIS
ACLK_SFP_SCL
ACLK_TO_SFP_P
ACLK_TO_SFP_N
ACLK_SFP_TX_DIS
ACLK_SFP_SCL
ACLK_SFP_SDA
NetGroup
CLK_TO_SFP[0..11]
FMC[0..110]
SFP 4
FMC[0..110]
NetGroup
FMC[0..110]
FMC.SCL4
FMC.SDA4
FMC.SFP_TX_DISABLE3
FMC.DATA_TO_FF_P3
FMC.DATA_TO_FF_N3
CLK_TO_SFP[0..11]
SCL4
SDA4
SFP_TX_DIS3
DATA_P3
DATA_N3
CLK_TO_SFP.CLK_TO_SFP_P3
CLK_TO_SFP.CLK_TO_SFP_N3
CLK_TO_SFP[0..11]
NetGroup
CLK_P3
CLK_N3
SFP 5
FMC[0..110]
NetGroup
FMC[0..110]
FMC.SCL5
FMC.SDA5
FMC.SFP_TX_DISABLE4
FMC.DATA_TO_FF_P4
FMC.DATA_TO_FF_N4
CLK_TO_SFP[0..11]
SCL5
SDA5
SFP_TX_DIS4
DATA_P4
DATA_N4
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CLK_TO_SFP.CLK_TO_SFP_N4
CLK_TO_SFP[0..11]
NetGroup
CLK_P4
CLK_N4
SFP 6
FMC[0..110]
NetGroup
FMC[0..110]
FMC.SCL6
FMC.SDA6
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FMC.DATA_TO_FF_N5
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SDA6
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DATA_N5
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CLK_TO_SFP.CLK_TO_SFP_N5
CLK_TO_SFP[0..11]
NetGroup
CLK_P5
CLK_N5
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FMC[0..110]
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