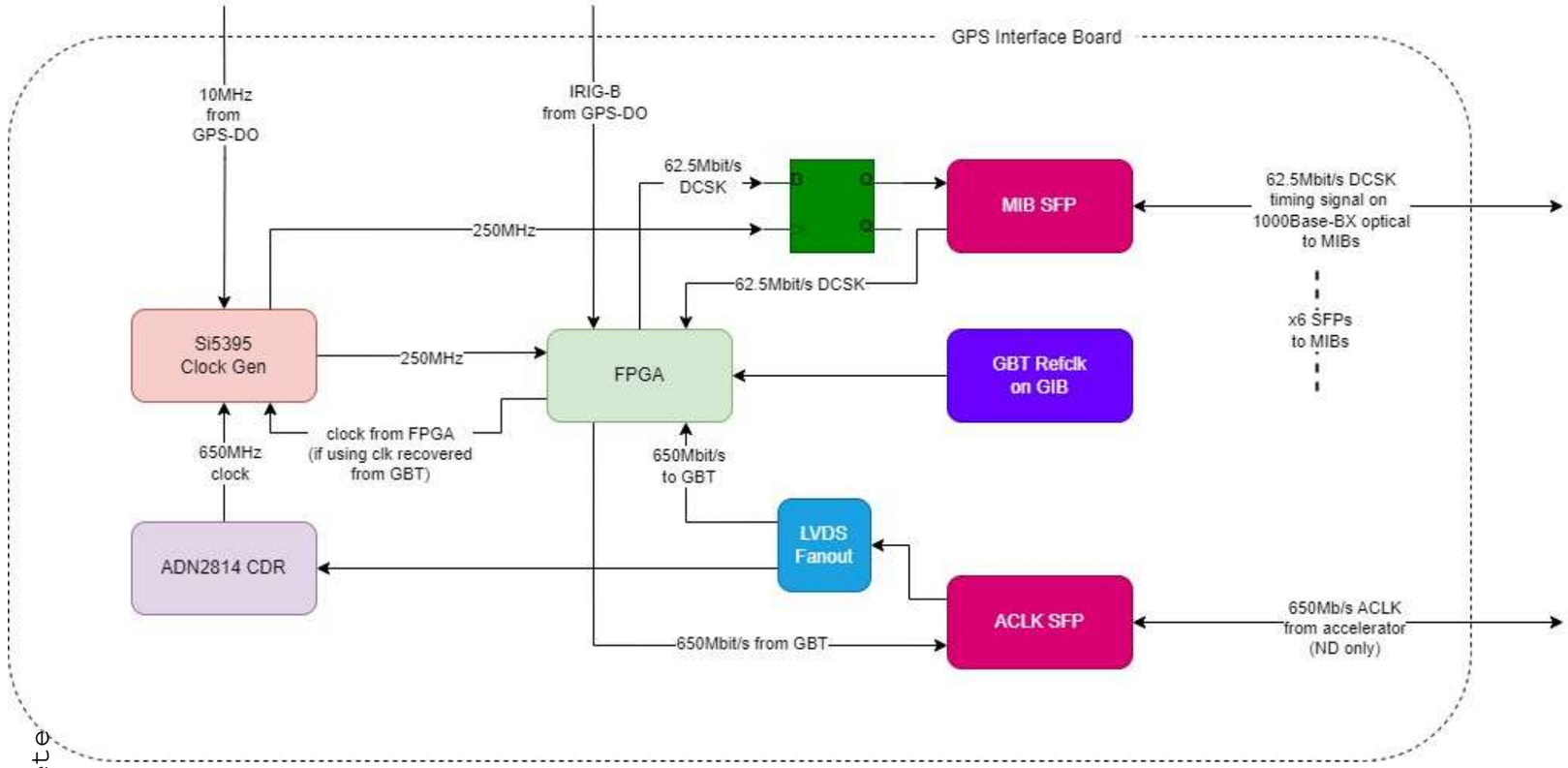

Part	I2C Address
ACLK SFP	0x50
ACLK CDR	0x40
SFP 1	0x50
SFP 2	
SFP 3	
SFP 4	
SFP 5	
SFP 6	

Part	I2C Address
Board ID EEPROM	0x54
SI5395 Clock Gen.	0x68
I2C Extender 1	0x74
I2C Extender 2	0x75
VCC5V Power Monitor	0x67
VCC3V3 Power Monitor	0x6A
VCC2V5 Power Monitor	0x69
I2C Switch	0x70
Temperature Monitor	0x48

This power consumption table is obsolete
Update/Remove

Power Estimate			Max Current (mA)				
Part	Description	Occurence	VCC5V	VCC3V3	VCC2V5	VCC1V8	12V Main PWR
LTC6957-2	Sine Wave to LVDS	1		72			
MAX9371	Low Jitter 5V TTL to LVDS	2	16				
SN74avc2t45	5V <--> 3.3V	1	100	100			
SN74avc2t45	3.3V <--> 2.5V	5		100	100		
SI5395	Clock Generator	1		302		300	
LTC2945	Power Monitor	4	1.2				
24AA025E48T	Board ID EEPROM	1		3			
LEDs		13		20			
NB7V52M	Diff. Flip-Flop	6			90		
ADN2814	CDR	6		145			
SFP		6		280			
SN74lvc1g32	OR Gate	12		100			
PCA9539	I2C Extender	2		160			
TCA9548A	I2C Switch	1			100		
LM75A	Temp Monitor	1		20			
NC7SZ08	AND Gate	1		50			
SN65LVDM176	LVDS Transceiver	2		15			
TXB0104(6)	Level Translator	2		100	100		
	Totals	Current (A)	0.14	5.41	1.14	0.30	
		Power (W)	0.68	17.84	3.76	0.54	22.83
	Max Power Supply	Current (A)	2	8			4
		Power (W)	11	28			48

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Design Title: GPS Interface Board
Schematic Title: 00. GIB Top
Page Title: 01. Address Table

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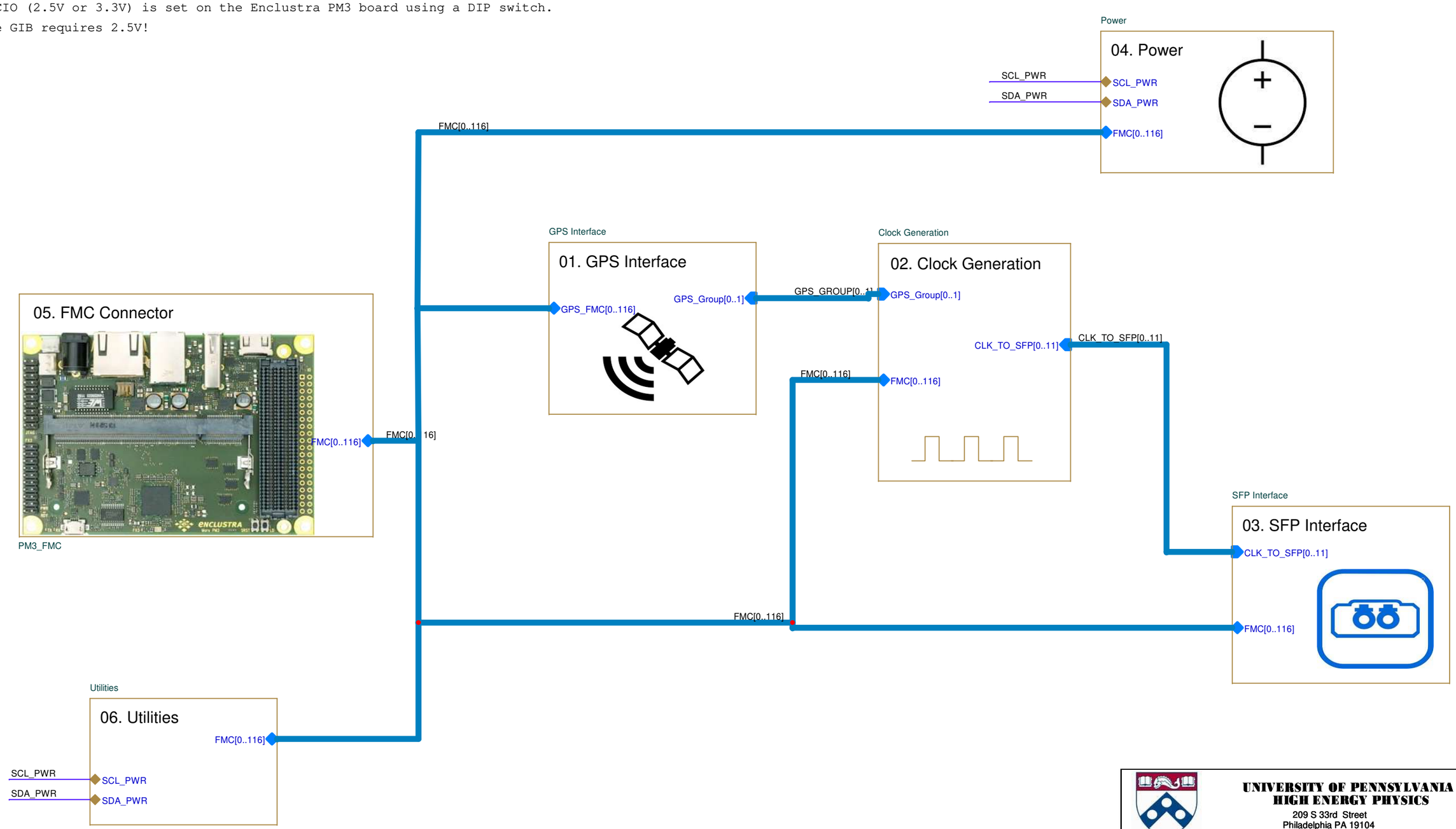
VCCIO (2.5V or 3.3V) is set on the Enclustra PM3 board using a DIP switch.
The GIB requires 2.5V!



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Design Title:	GPS Interface Board
Schematic Title:	00. GIB Top
Page Title:	02. Top Level

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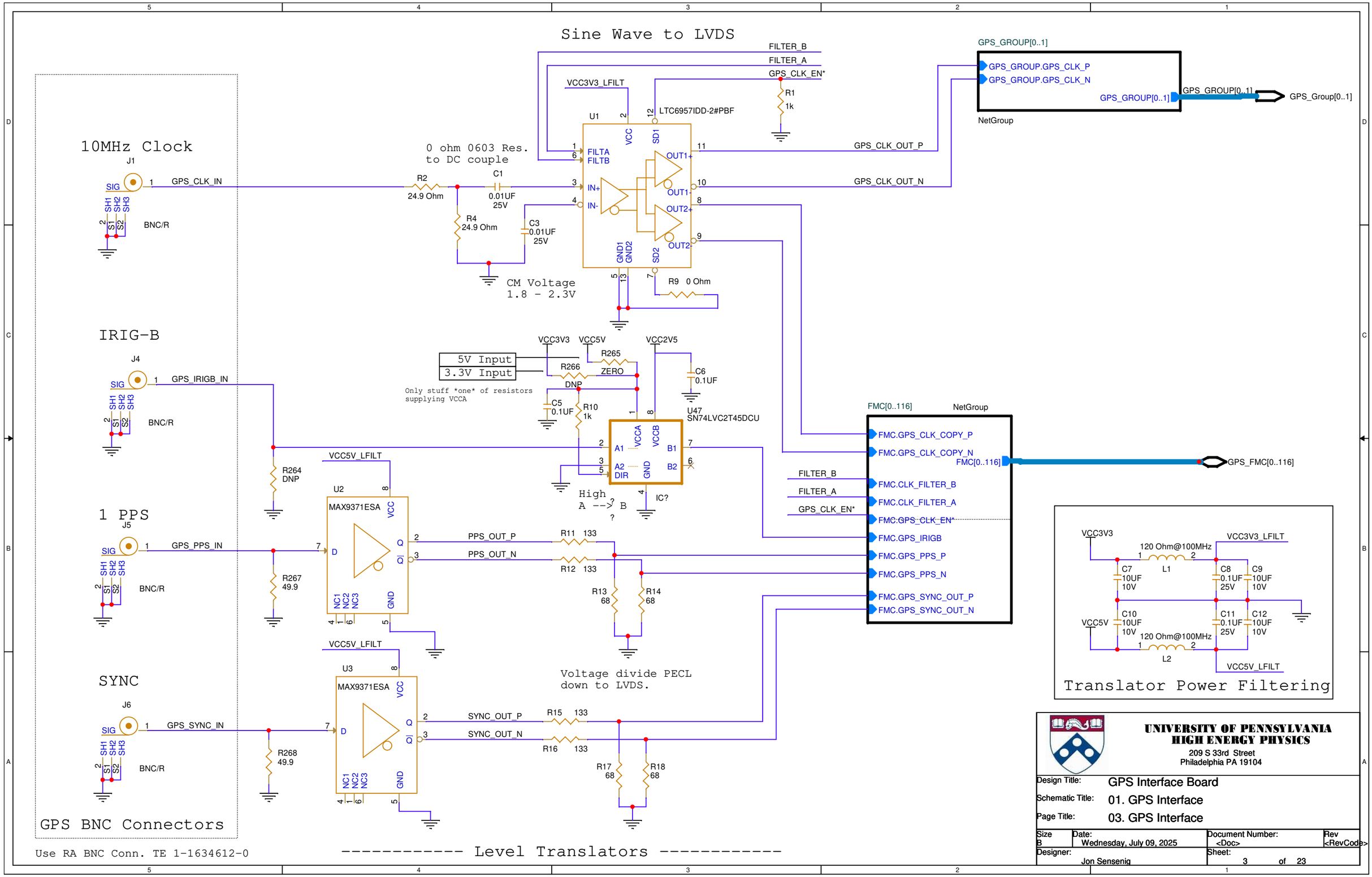
Designer: Jon Sensenig		Sheet: 2 of 23	


Sine Wave to LVDS
10MHz Clock
IRIG-B
1 PPS
SYNC
GPS BNC Connectors
Use RA BNC Conn. TE 1-1634612-0
0 ohm 0603 Res.
to DC couple
CM Voltage
1.8 - 2.3V
LTC6957IDD-2#PBF
5V Input
3.3V Input
Only stuff *one* of resistors
supplying VCCA
SN74LVC2T45DCU
MAX9371ESA
High
A --> B
Voltage divide PECL
down to LVDS.
Level Translators
GPS_GROUP[0..1]
GPS_Group[0..1]
NetGroup
FMC[0..116]
GPS_FMC[0..116]
Translator Power Filtering
120 Ohm@100MHz
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Design Title: GPS Interface Board
Schematic Title: 01. GPS Interface
Page Title: 03. GPS Interface
Size B
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Designer: Jon Sensenig
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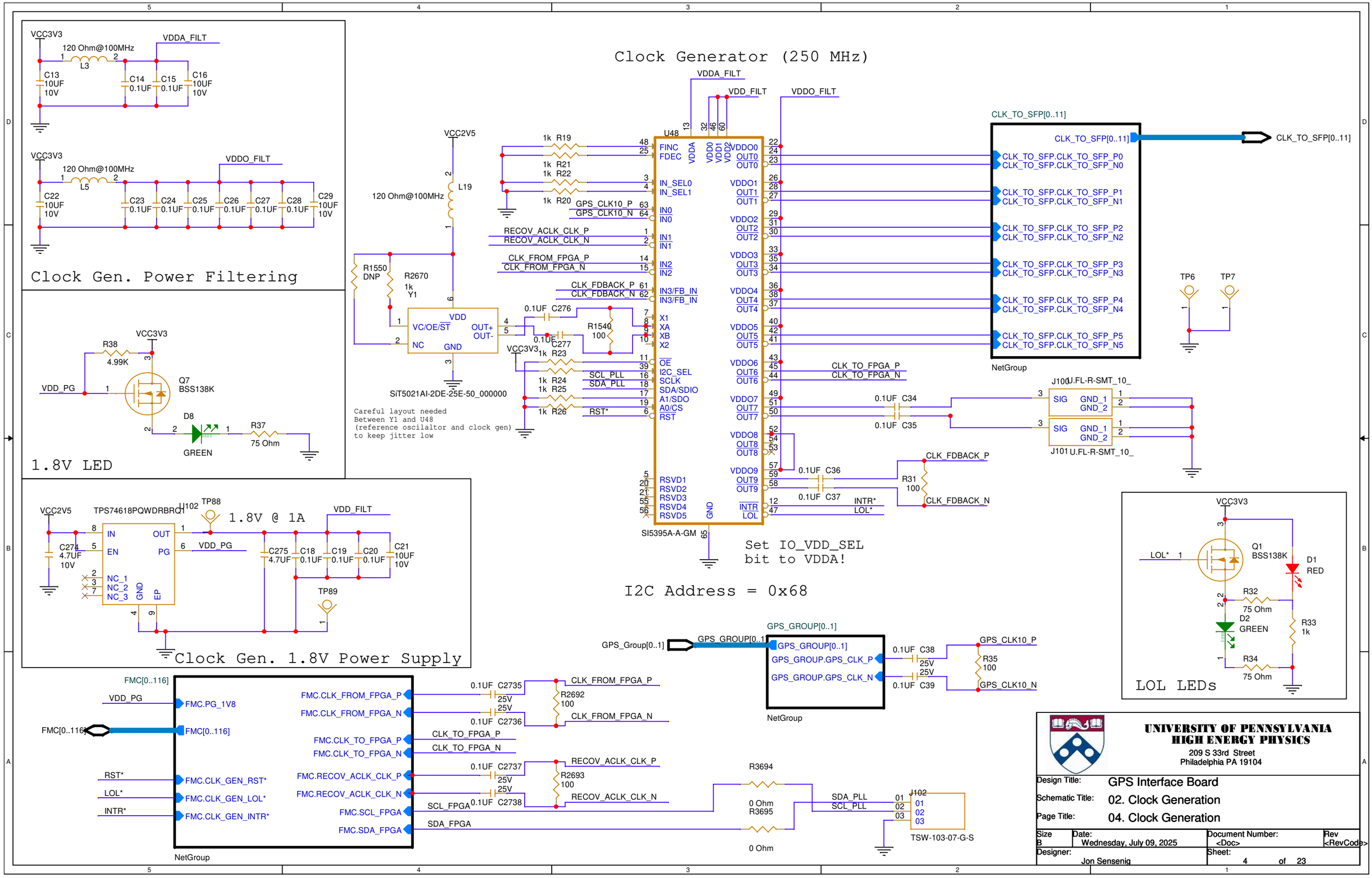
Clock Generator (250 MHz)
Clock Gen. Power Filtering
VCC3V3
120 Ohm@100MHz
L3
VDDA_FILT
C13 10UF 10V
C14 0.1UF
C15 0.1UF
C16 10UF 10V
L5
VDDO_FILT
C22 10UF 10V
C23 0.1UF
C24 0.1UF
C25 0.1UF
C26 0.1UF
C27 0.1UF
C28 0.1UF
C29 10UF 10V
1.8V LED
R38 4.99K
VDD_PG
Q7 BSS138K
D8 GREEN
R37 75 Ohm
Clock Gen. 1.8V Power Supply
VCC2V5
TPS74618PQWDRBRQ1
U102
TP88
1.8V @ 1A
VDD_FILT
C274 4.7UF 10V
C275 4.7UF
C18 0.1UF
C19 0.1UF
C20 0.1UF
C21 10UF 10V
TP89
IN
EN
OUT
PG
NC_1
NC_2
NC_3
GND
EP
VDD_PG
L19
R1550 DNP
R2670 1k
Y1
VDD
VC/OE/ST
OUT+
OUT-
NC
GND
SiT5021AI-2DE-25E-50_000000
Careful layout needed
Between Y1 and U48
(reference oscilaltor and clock gen)
to keep jitter low
U48
VDDA_FILT
VDD_FILT
VDDO_FILT
FINC
FDEC
VDDA
VDD0
VDD1
VDD2
IN_SEL0
IN_SEL1
IN0
IN1
IN2
IN3/FB_IN
X1
XA
XB
X2
OE
I2C_SEL
SCLK
SDA/SDIO
A1/SDO
A0/CS
RST
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
GND
SI5395A-A-GM
1k R19
1k R21
1k R22
1k R20
GPS_CLK10_P
GPS_CLK10_N
RECOV_ACLK_CLK_P
RECOV_ACLK_CLK_N
CLK_FROM_FPGA_P
CLK_FROM_FPGA_N
CLK_FDBACK_P
CLK_FDBACK_N
0.1UF C276
0.1UF C277
R1540 100
1k R23
1k R24
1k R25
1k R26
SCL_PLL
SDA_PLL
RST*
VDDO0
OUT0
VDDO1
OUT1
VDDO2
OUT2
VDDO3
OUT3
VDDO4
OUT4
VDDO5
OUT5
VDDO6
OUT6
VDDO7
OUT7
VDDO8
OUT8
VDDO9
OUT9
INTR
LOL
CLK_TO_FPGA_P
CLK_TO_FPGA_N
0.1UF C34
0.1UF C35
0.1UF C36
0.1UF C37
INTR*
LOL*
R31 100
CLK_TO_SFP[0..11]
CLK_TO_SFP.CLK_TO_SFP_P0
CLK_TO_SFP.CLK_TO_SFP_N0
CLK_TO_SFP.CLK_TO_SFP_P1
CLK_TO_SFP.CLK_TO_SFP_N1
CLK_TO_SFP.CLK_TO_SFP_P2
CLK_TO_SFP.CLK_TO_SFP_N2
CLK_TO_SFP.CLK_TO_SFP_P3
CLK_TO_SFP.CLK_TO_SFP_N3
CLK_TO_SFP.CLK_TO_SFP_P4
CLK_TO_SFP.CLK_TO_SFP_N4
CLK_TO_SFP.CLK_TO_SFP_P5
CLK_TO_SFP.CLK_TO_SFP_N5
NetGroup
TP6
TP7
J100 U.FL-R-SMT_10_
J101 U.FL-R-SMT_10_
SIG
GND_1
GND_2
Set IO_VDD_SEL
bit to VDDA!
I2C Address = 0x68
GPS_Group[0..1]
GPS_GROUP[0..1]
GPS_GROUP.GPS_CLK_P
GPS_GROUP.GPS_CLK_N
0.1UF C38
0.1UF C39
25V
R35 100
GPS_CLK10_P
GPS_CLK10_N
LOL LEDs
VCC3V3
LOL*
Q1 BSS138K
D1 RED
R32 75 Ohm
D2 GREEN
R33 1k
R34 75 Ohm
FMC[0..116]
VDD_PG
FMC.PG_1V8
FMC[0..116]
RST*
LOL*
INTR*
FMC.CLK_GEN_RST*
FMC.CLK_GEN_LOL*
FMC.CLK_GEN_INTR*
FMC.CLK_FROM_FPGA_P
FMC.CLK_FROM_FPGA_N
FMC.CLK_TO_FPGA_P
FMC.CLK_TO_FPGA_N
FMC.RECOV_ACLK_CLK_P
FMC.RECOV_ACLK_CLK_N
FMC.SCL_FPGA
FMC.SDA_FPGA
0.1UF C2735
0.1UF C2736
0.1UF C2737
0.1UF C2738
R2692 100
R2693 100
R3694 0 Ohm
R3695 0 Ohm
SCL_FPGA
SDA_FPGA
J102
TSW-103-07-G-S
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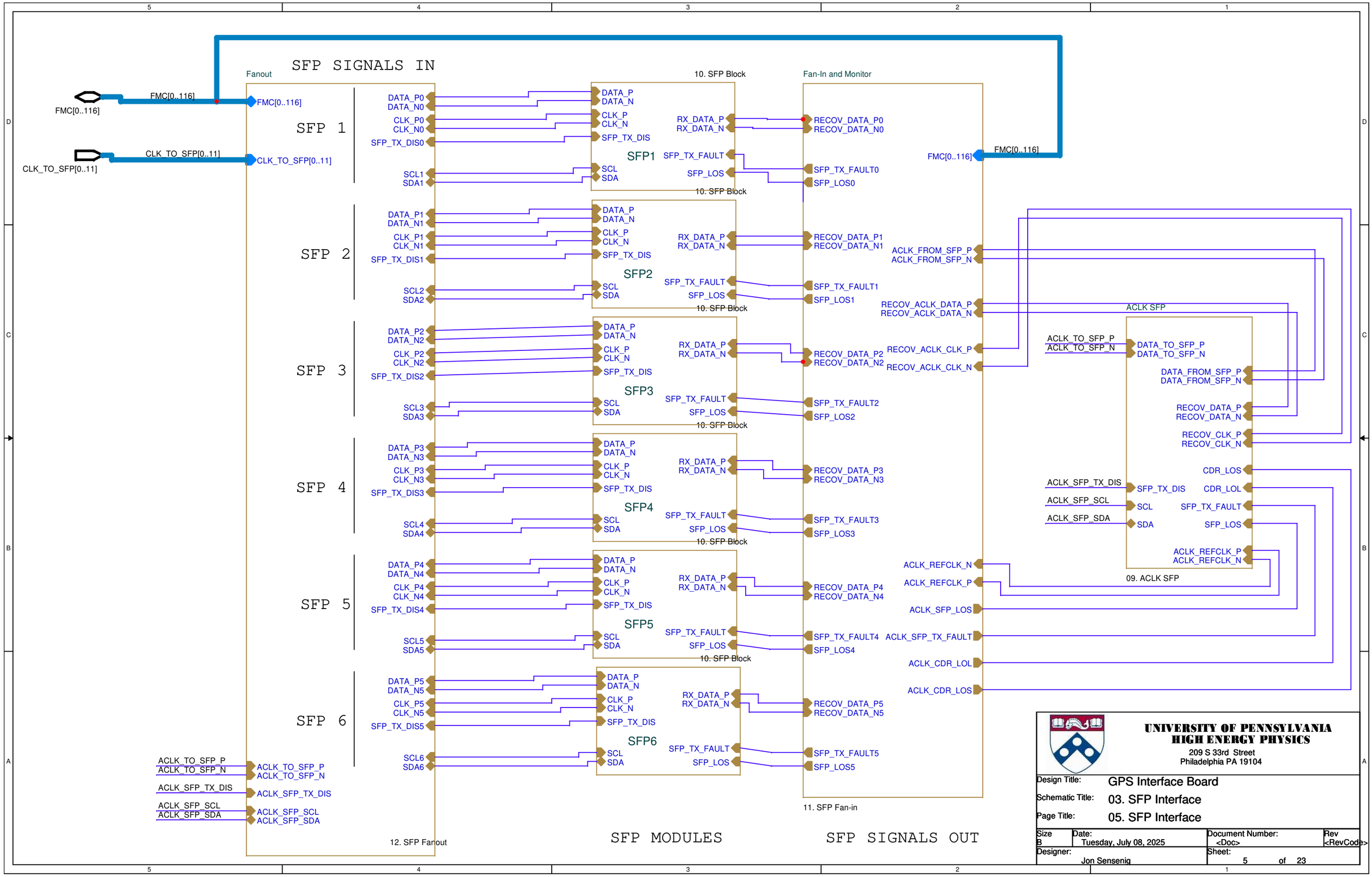
209 S 33rd Street
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 02. Clock Generation
Page Title: 04. Clock Generation
Size B
Date: Wednesday, July 09, 2025
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 4 of 23



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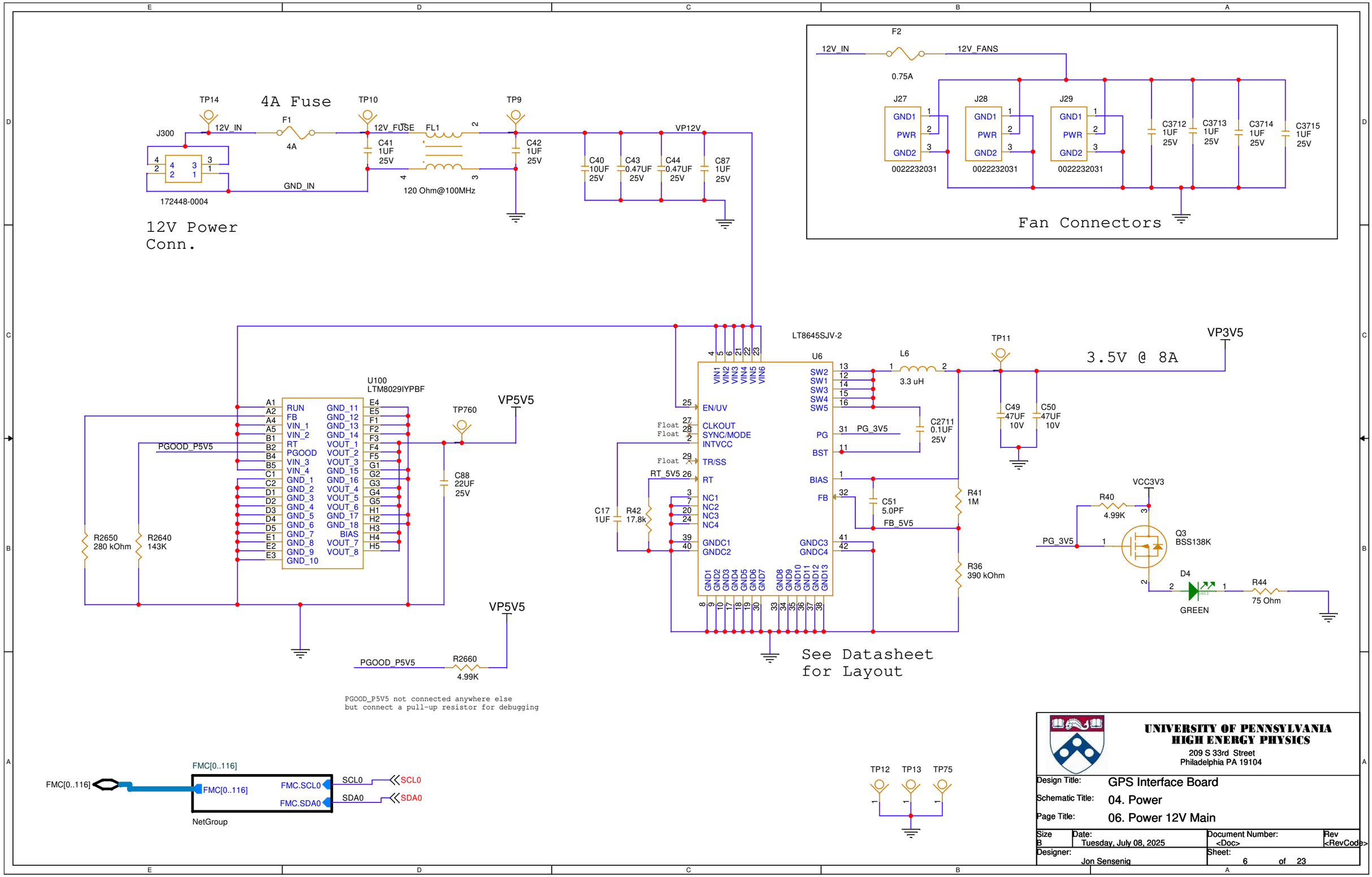
Design Title:	GPS Interface Board
Schematic Title:	03. SFP Interface
Page Title:	05. SFP Interface

Size	Date:	Document Number:	Rev
B	Tuesday, July 08, 2025	<Doc>	<RevCode>
Designer: Jon Sensenig		Sheet: 5 of 23	



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Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	06. Power 12V Main

Size	Date:	Document Number:	Rev
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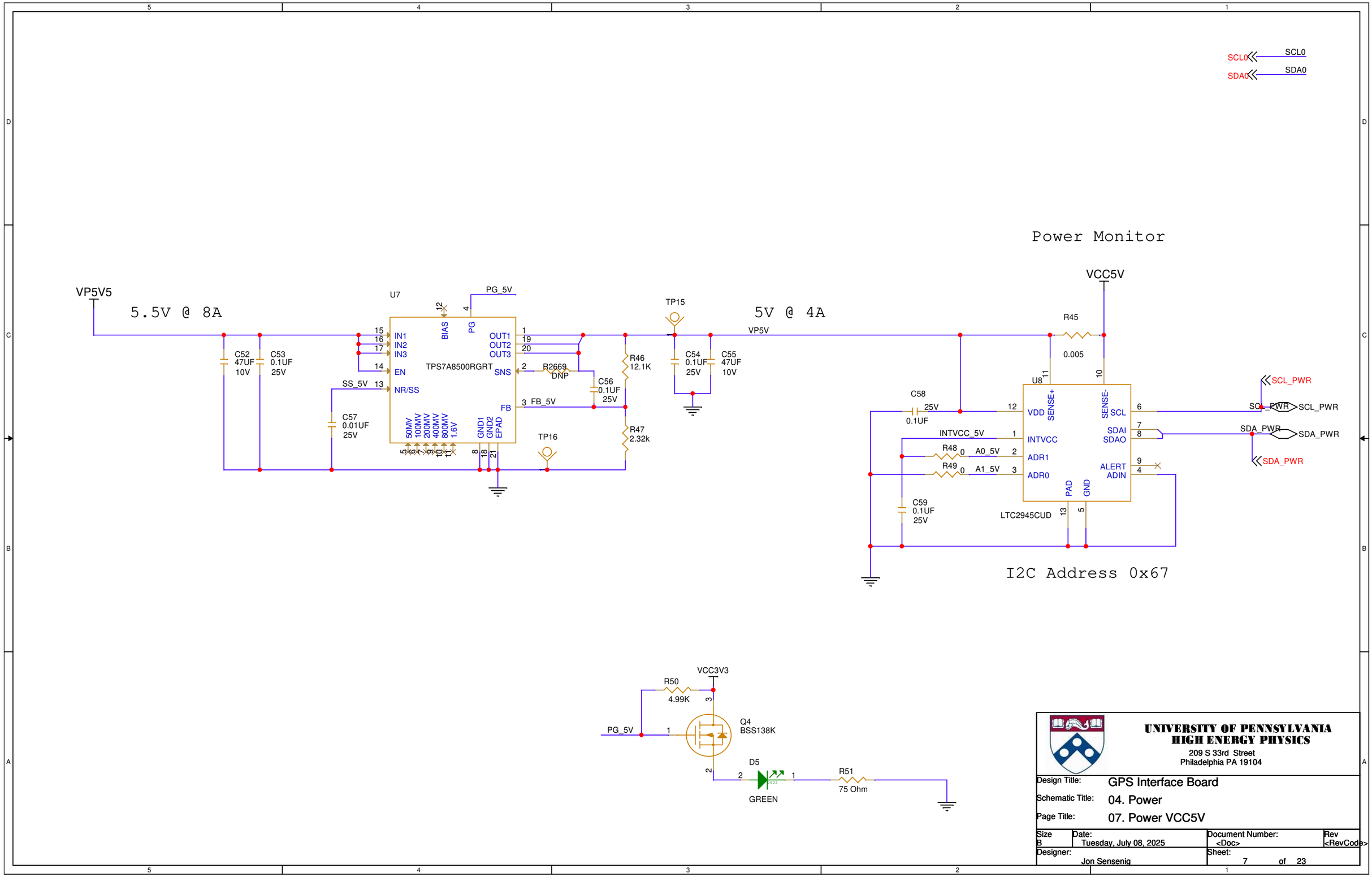
Designer: Jon Sensenig		Sheet: 6 of 23	



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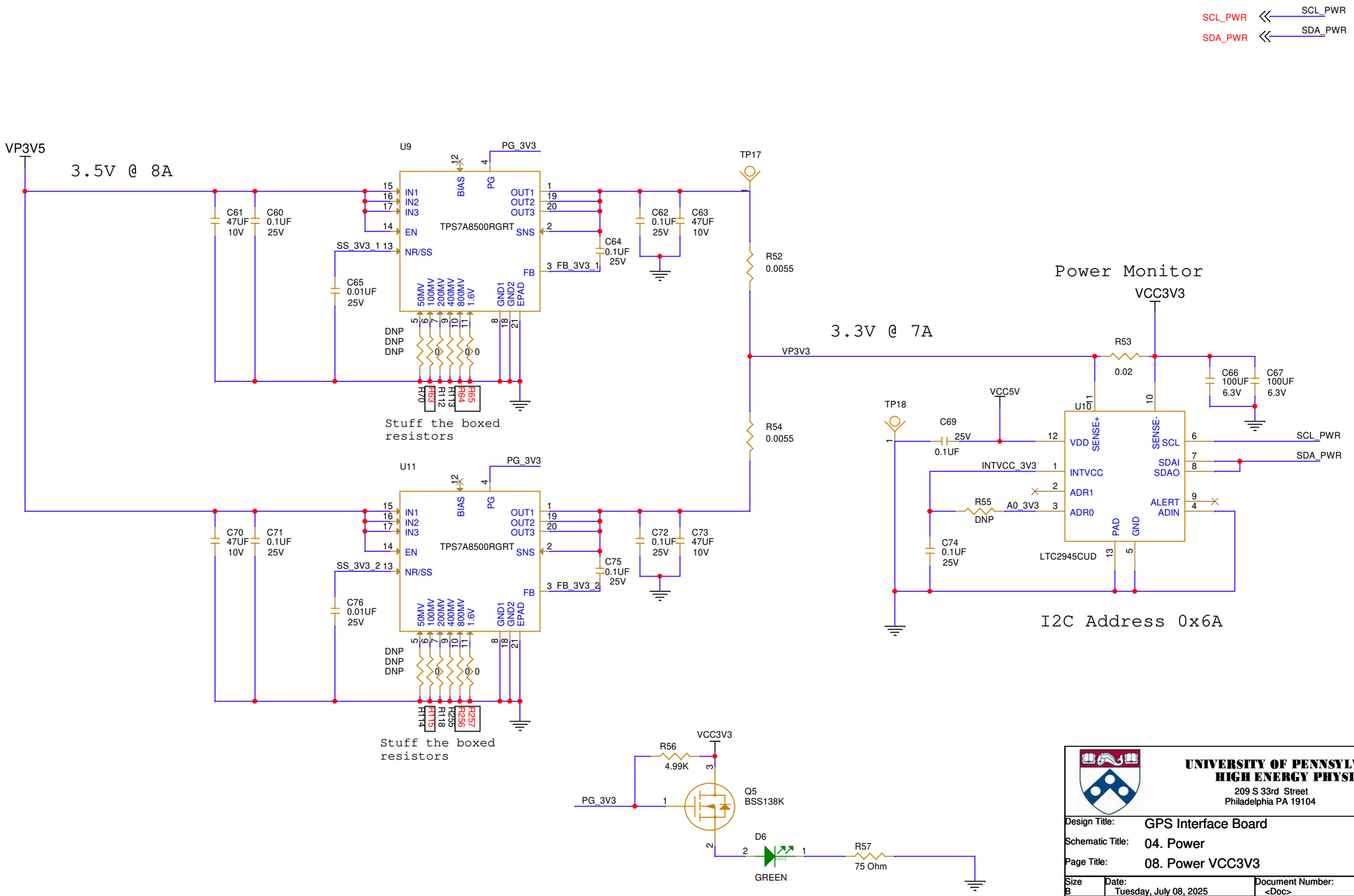
209 S 33rd Street
Philadelphia PA 19104

Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	07. Power VCC5V

Size	Date:	Document Number:	Rev
B	Tuesday, July 08, 2025	<Doc>	<RevCode>
Designer: Jon Sensenig		Sheet: 7 of 23	



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Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	08. Power VCC3V3

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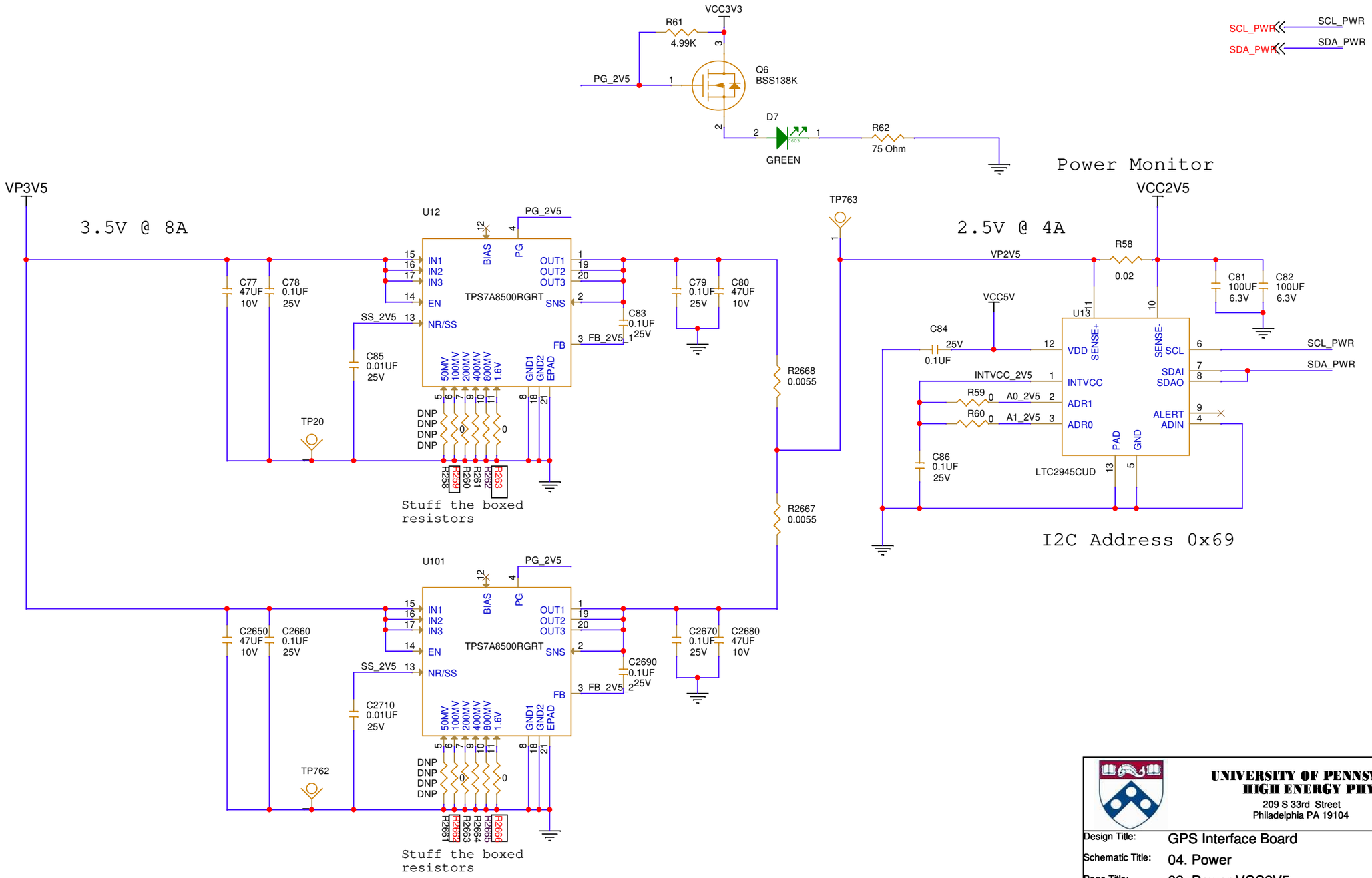
Designer: Jon Sensenig		Sheet: 8 of 23	



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Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	09. Power VCC2V5

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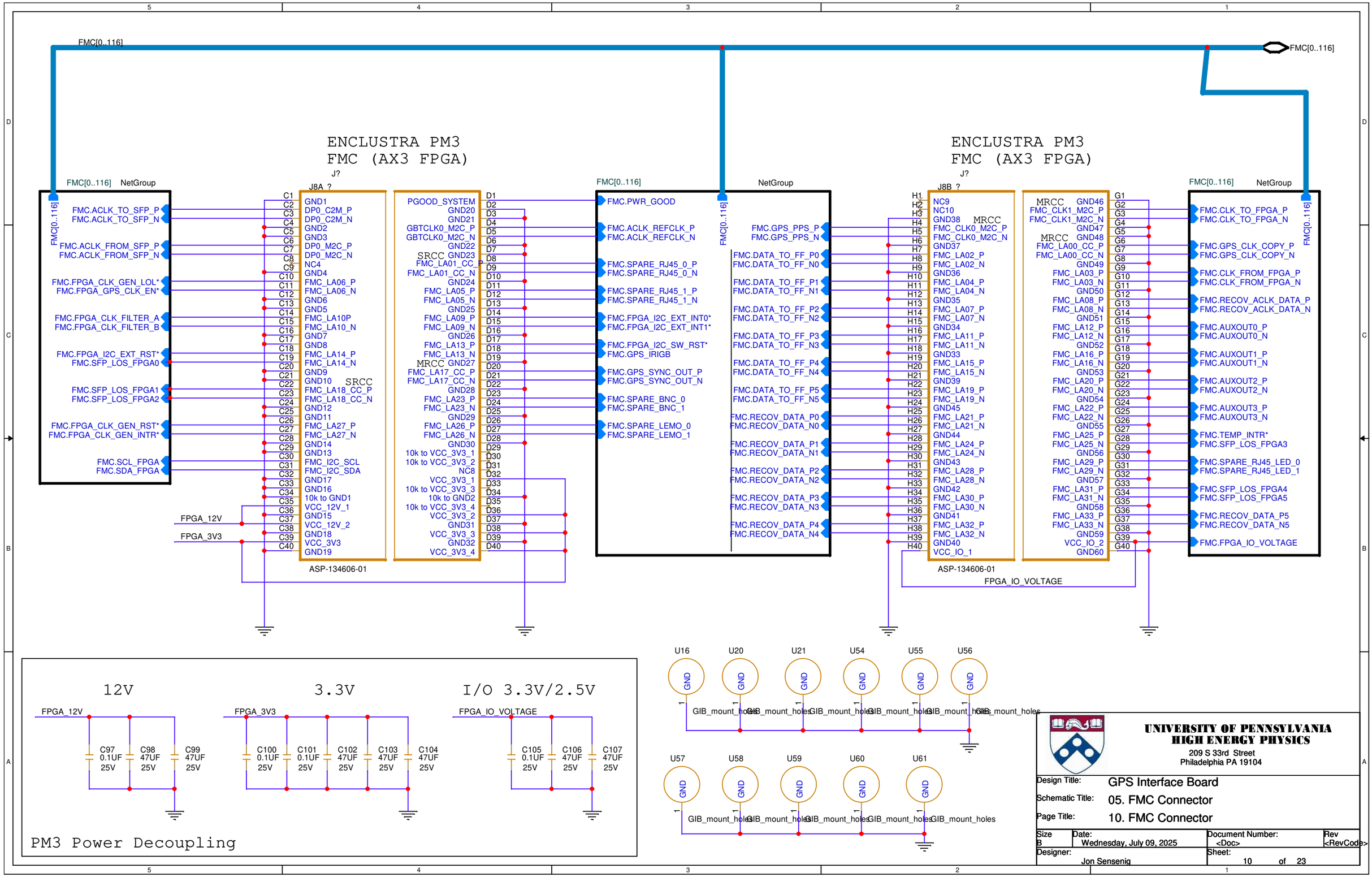
FMC[0..116]
ENCLUSTRA PM3
FMC (AX3 FPGA)
J?
J8A ?
NetGroup
FMC.ACLK_TO_SFP_P
FMC.ACLK_TO_SFP_N
FMC.ACLK_FROM_SFP_P
FMC.ACLK_FROM_SFP_N
FMC.FPGA_CLK_GEN_LOL*
FMC.FPGA_GPS_CLK_EN*
FMC.FPGA_CLK_FILTER_A
FMC.FPGA_CLK_FILTER_B
FMC.FPGA_I2C_EXT_RST*
FMC.SFP_LOS_FPGA0
FMC.SFP_LOS_FPGA1
FMC.SFP_LOS_FPGA2
FMC.FPGA_CLK_GEN_RST*
FMC.FPGA_CLK_GEN_INTR*
FMC.SCL_FPGA
FMC.SDA_FPGA
FPGA_12V
FPGA_3V3
ASP-134606-01
FMC.PWR_GOOD
FMC.ACLK_REFCLK_P
FMC.ACLK_REFCLK_N
FMC.SPARE_RJ45_0_P
FMC.SPARE_RJ45_0_N
FMC.SPARE_RJ45_1_P
FMC.SPARE_RJ45_1_N
FMC.FPGA_I2C_EXT_INT0*
FMC.FPGA_I2C_EXT_INT1*
FMC.FPGA_I2C_SW_RST*
FMC.GPS_IRIGB
FMC.GPS_SYNC_OUT_P
FMC.GPS_SYNC_OUT_N
FMC.SPARE_BNC_0
FMC.SPARE_BNC_1
FMC.SPARE_LEMO_0
FMC.SPARE_LEMO_1
ENCLUSTRA PM3
FMC (AX3 FPGA)
J8B ?
FMC.GPS_PPS_P
FMC.GPS_PPS_N
FMC.DATA_TO_FF_P0
FMC.DATA_TO_FF_N0
FMC.DATA_TO_FF_P1
FMC.DATA_TO_FF_N1
FMC.DATA_TO_FF_P2
FMC.DATA_TO_FF_N2
FMC.DATA_TO_FF_P3
FMC.DATA_TO_FF_N3
FMC.DATA_TO_FF_P4
FMC.DATA_TO_FF_N4
FMC.DATA_TO_FF_P5
FMC.DATA_TO_FF_N5
FMC.RECOV_DATA_P0
FMC.RECOV_DATA_N0
FMC.RECOV_DATA_P1
FMC.RECOV_DATA_N1
FMC.RECOV_DATA_P2
FMC.RECOV_DATA_N2
FMC.RECOV_DATA_P3
FMC.RECOV_DATA_N3
FMC.RECOV_DATA_P4
FMC.RECOV_DATA_N4
FMC.CLK_TO_FPGA_P
FMC.CLK_TO_FPGA_N
FMC.GPS_CLK_COPY_P
FMC.GPS_CLK_COPY_N
FMC.CLK_FROM_FPGA_P
FMC.CLK_FROM_FPGA_N
FMC.RECOV_ACLK_DATA_P
FMC.RECOV_ACLK_DATA_N
FMC.AUXOUT0_P
FMC.AUXOUT0_N
FMC.AUXOUT1_P
FMC.AUXOUT1_N
FMC.AUXOUT2_P
FMC.AUXOUT2_N
FMC.AUXOUT3_P
FMC.AUXOUT3_N
FMC.TEMP_INTR*
FMC.SFP_LOS_FPGA3
FMC.SPARE_RJ45_LED_0
FMC.SPARE_RJ45_LED_1
FMC.SFP_LOS_FPGA4
FMC.SFP_LOS_FPGA5
FMC.RECOV_DATA_P5
FMC.RECOV_DATA_N5
FMC.FPGA_IO_VOLTAGE
FPGA_IO_VOLTAGE
12V
3.3V
I/O 3.3V/2.5V
C97 0.1UF 25V
C98 47UF 25V
C99 47UF 25V
C100 0.1UF 25V
C101 0.1UF 25V
C102 47UF 25V
C103 47UF 25V
C104 47UF 25V
C105 0.1UF 25V
C106 47UF 25V
C107 47UF 25V
PM3 Power Decoupling
U16
U20
U21
U54
U55
U56
U57
U58
U59
U60
U61
GND
GIB_mount_holes
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Design Title: GPS Interface Board
Schematic Title: 05. FMC Connector
Page Title: 10. FMC Connector
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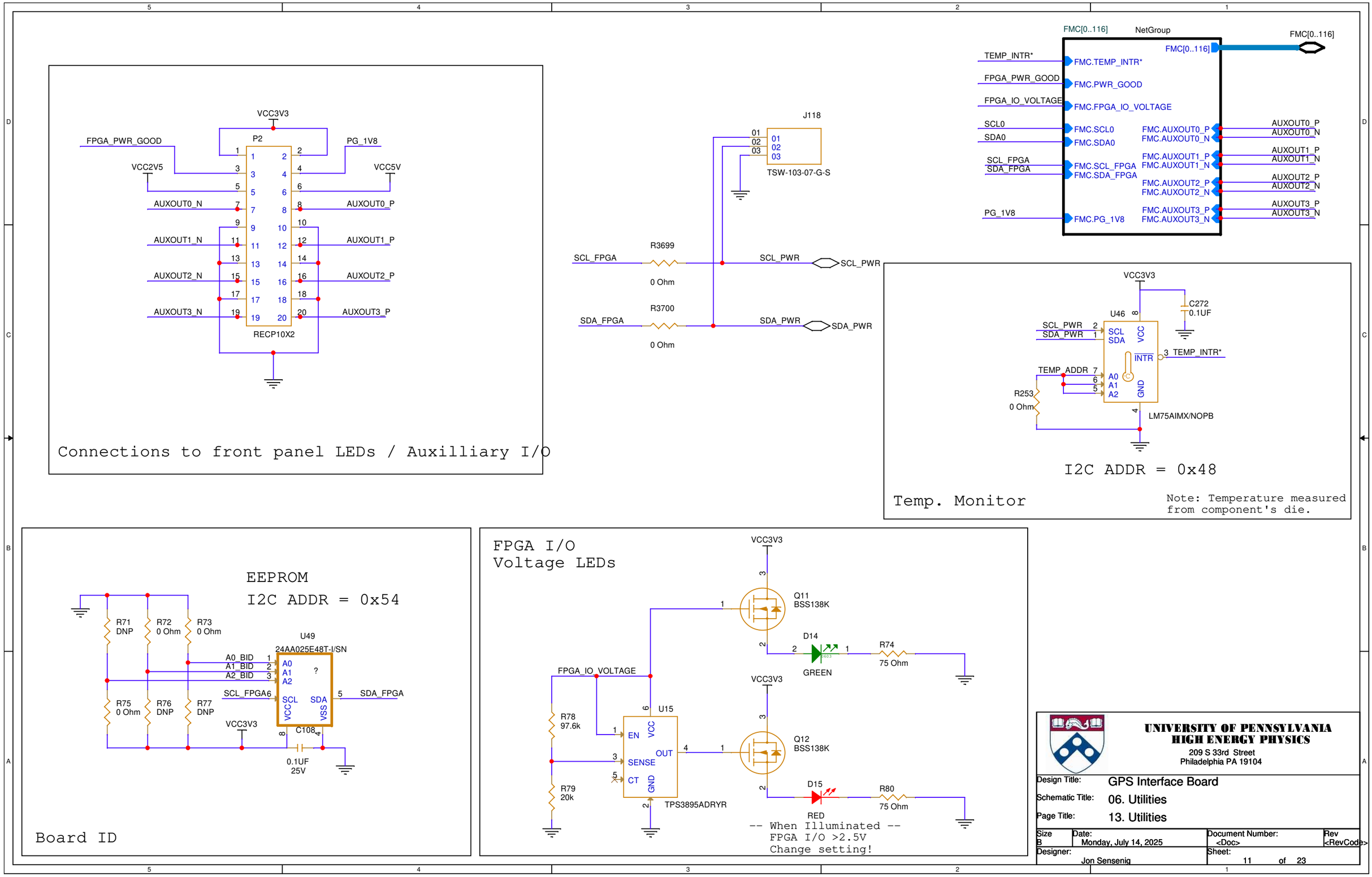
Connections to front panel LEDs / Auxilliary I/O
VCC3V3
P2
FPGA_PWR_GOOD
PG_1V8
VCC2V5
VCC5V
AUXOUT0_N
AUXOUT0_P
AUXOUT1_N
AUXOUT1_P
AUXOUT2_N
AUXOUT2_P
AUXOUT3_N
AUXOUT3_P
RECP10X2
J118
TSW-103-07-G-S
R3699
0 Ohm
SCL_FPGA
SCL_PWR
R3700
SDA_FPGA
SDA_PWR
FMC[0..116]
NetGroup
TEMP_INTR*
FPGA_PWR_GOOD
FPGA_IO_VOLTAGE
SCL0
SDA0
SCL_FPGA
SDA_FPGA
PG_1V8
FMC.TEMP_INTR*
FMC.PWR_GOOD
FMC.FPGA_IO_VOLTAGE
FMC.SCL0
FMC.SDA0
FMC.SCL_FPGA
FMC.SDA_FPGA
FMC.PG_1V8
FMC.AUXOUT0_P
FMC.AUXOUT0_N
FMC.AUXOUT1_P
FMC.AUXOUT1_N
FMC.AUXOUT2_P
FMC.AUXOUT2_N
FMC.AUXOUT3_P
FMC.AUXOUT3_N
Temp. Monitor
U46
C272
0.1UF
SCL
SDA
VCC
INTR
A0
A1
A2
GND
R253
0 Ohm
LM75AIMX/NOPB
I2C ADDR = 0x48
Note: Temperature measured from component's die.
EEPROM
I2C ADDR = 0x54
R71
DNP
R72
0 Ohm
R73
0 Ohm
R75
0 Ohm
R76
DNP
R77
DNP
U49
24AA025E48T-I/SN
A0_BID
A1_BID
A2_BID
SCL_FPGA6
SDA_FPGA
C108
0.1UF
25V
Board ID
FPGA I/O
Voltage LEDs
Q11
BSS138K
D14
GREEN
R74
75 Ohm
R78
97.6k
R79
20k
U15
EN
SENSE
CT
OUT
TPS3895ADRYR
Q12
BSS138K
D15
RED
R80
75 Ohm
-- When Illuminated --
FPGA I/O >2.5V
Change setting!
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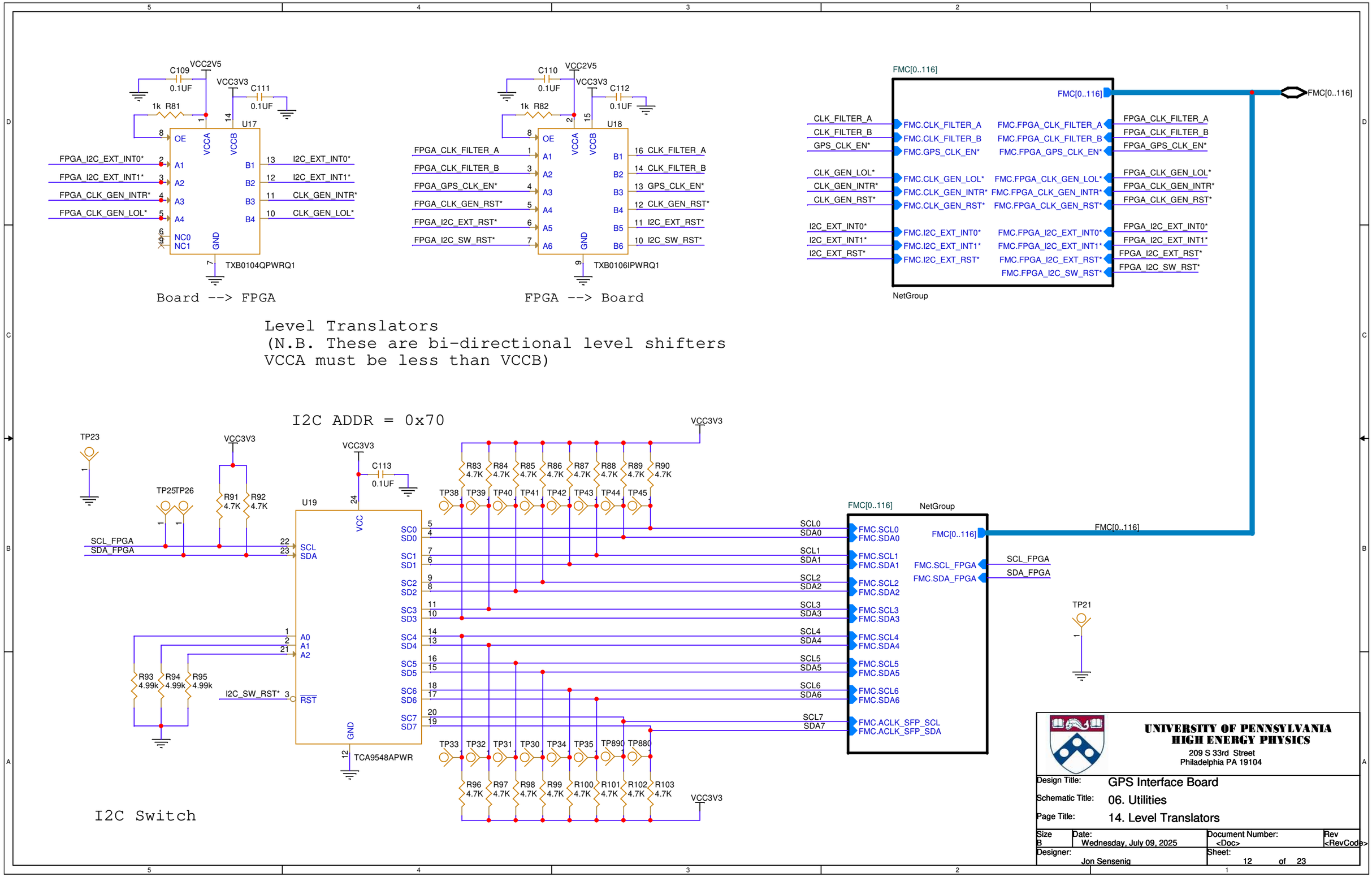
Philadelphia PA 19104
Design Title: GPS Interface Board
Schematic Title: 06. Utilities
Page Title: 13. Utilities
Size B
Date: Monday, July 14, 2025
Document Number: <Doc>
Rev <RevCode>
Designer: Jon Sensenig
Sheet: 11 of 23



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Design Title:	GPS Interface Board
Schematic Title:	06. Utilities
Page Title:	14. Level Translators

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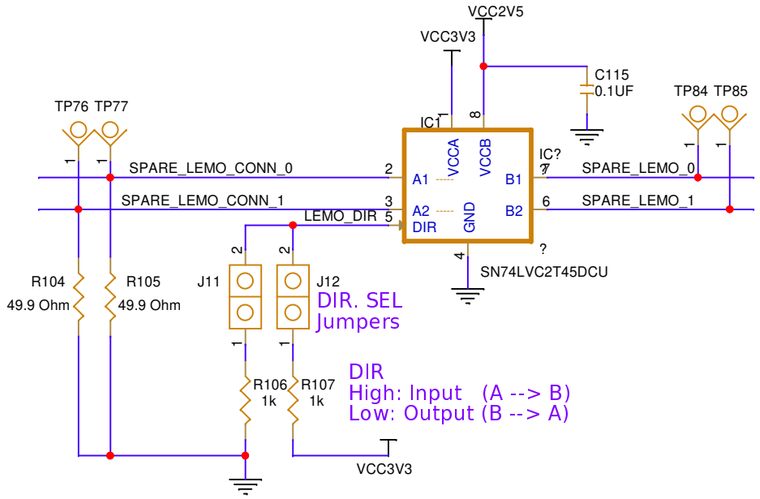
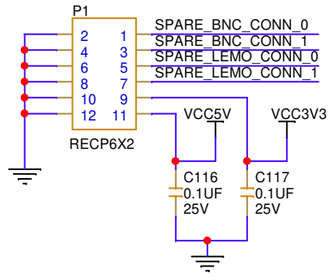
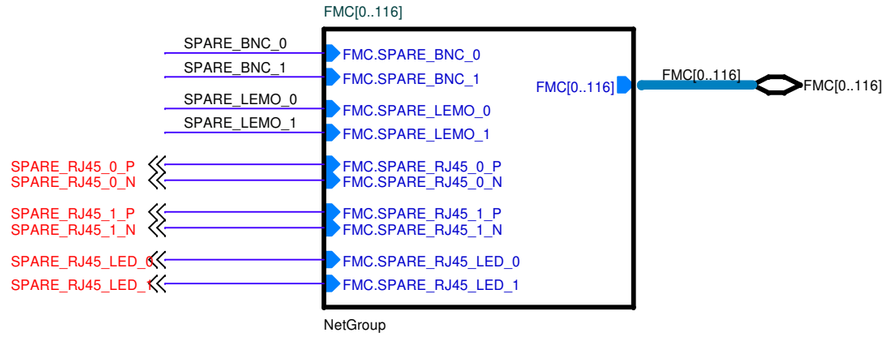
SPARE I/O
LEMO

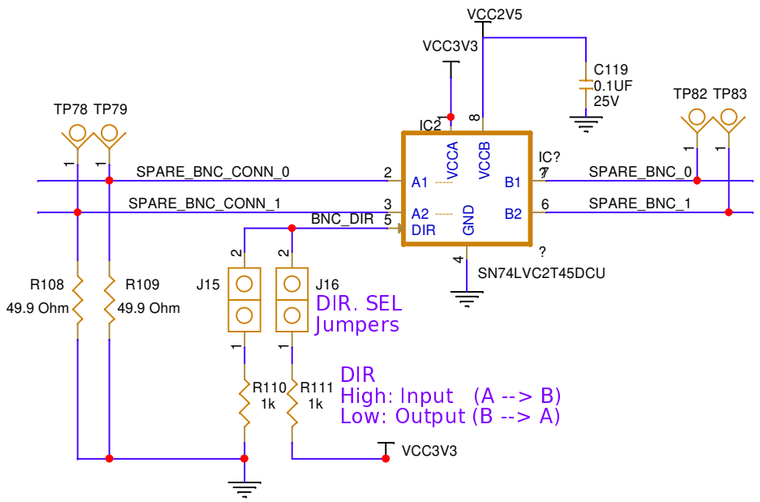


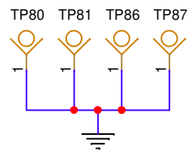


I/O Connector
to BNC & LEMO



SPARE I/O
BNC





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Schematic Title:	06. Utilities
Page Title:	15. Spare I/O BNC/LEMO

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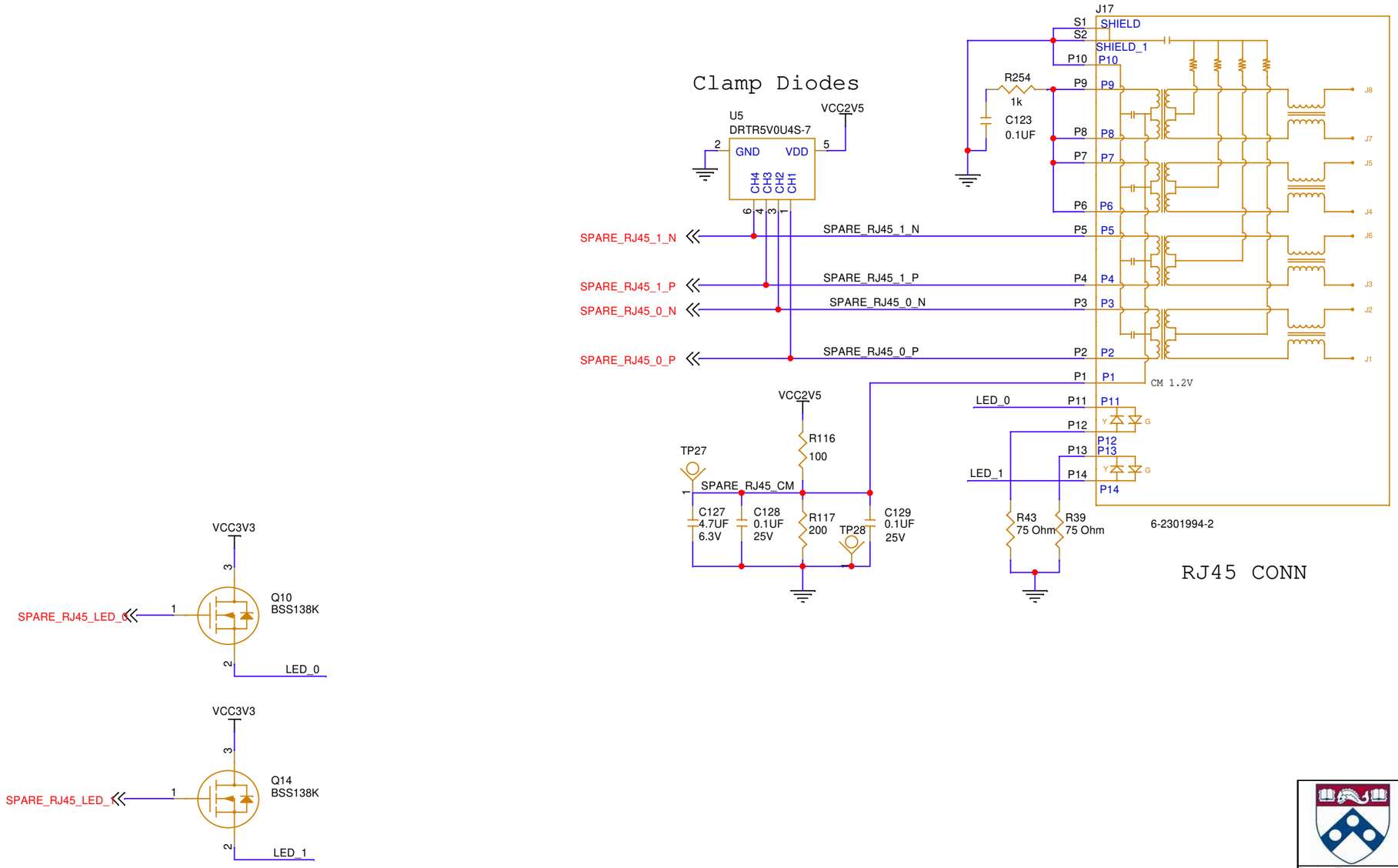

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Design Title:	GPS Interface Board
Schematic Title:	06. Utilities
Page Title:	16. Spare I/O RJ45

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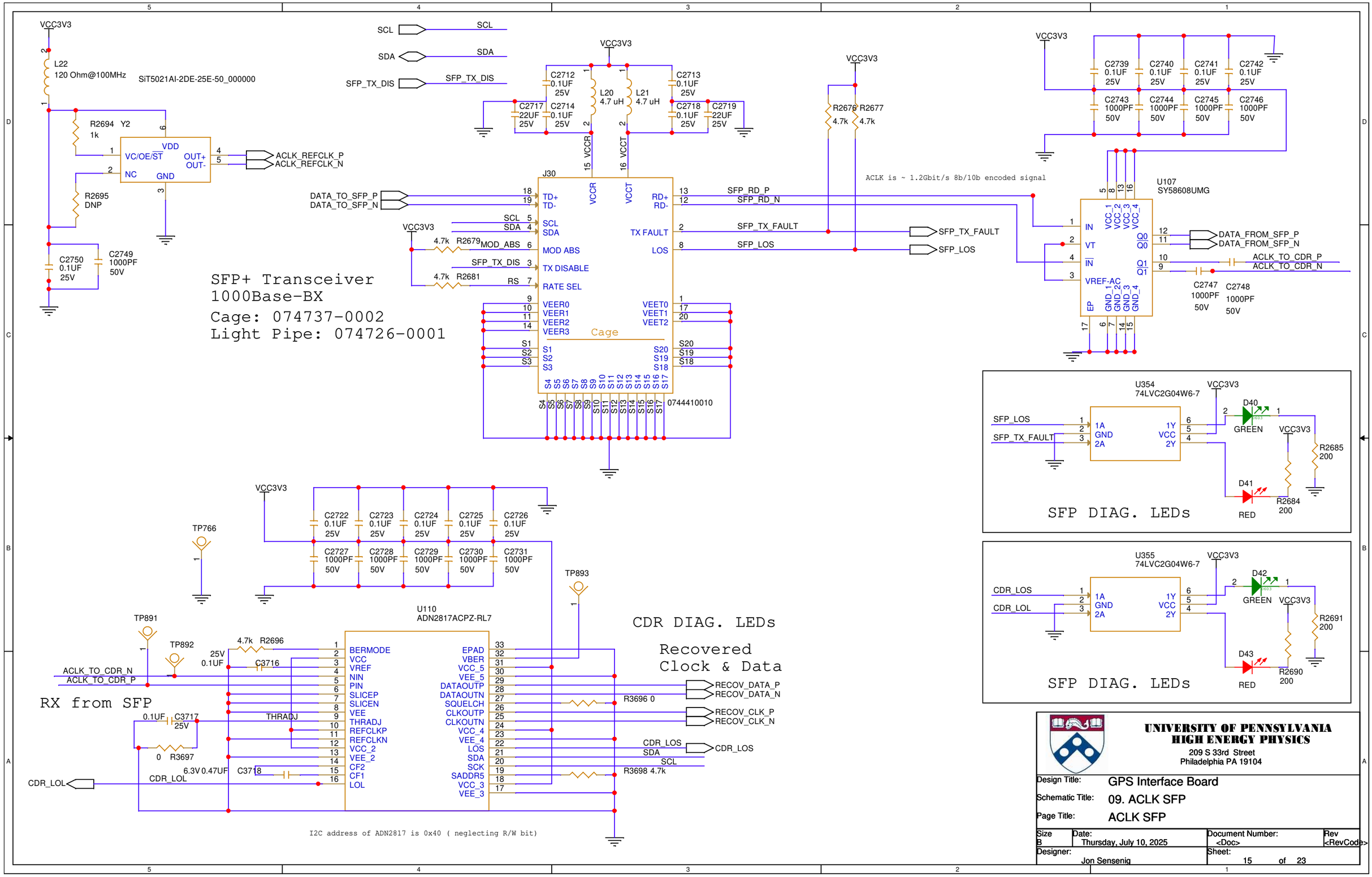
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Cage: 074737-0002
Light Pipe: 074726-0001
SiT5021AI-2DE-25E-50_000000
J30
Cage
0744410010
U107
SY58608UMG
ACLK is ~ 1.2Gbit/s 8b/10b encoded signal
U354
74LVC2G04W6-7
SFP DIAG. LEDs
U355
74LVC2G04W6-7
SFP DIAG. LEDs
U110
ADN2817ACPZ-RL7
RX from SFP
CDR DIAG. LEDs
Recovered
Clock & Data
I2C address of ADN2817 is 0x40 (neglecting R/W bit)
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Schematic Title: 09. ACLK SFP
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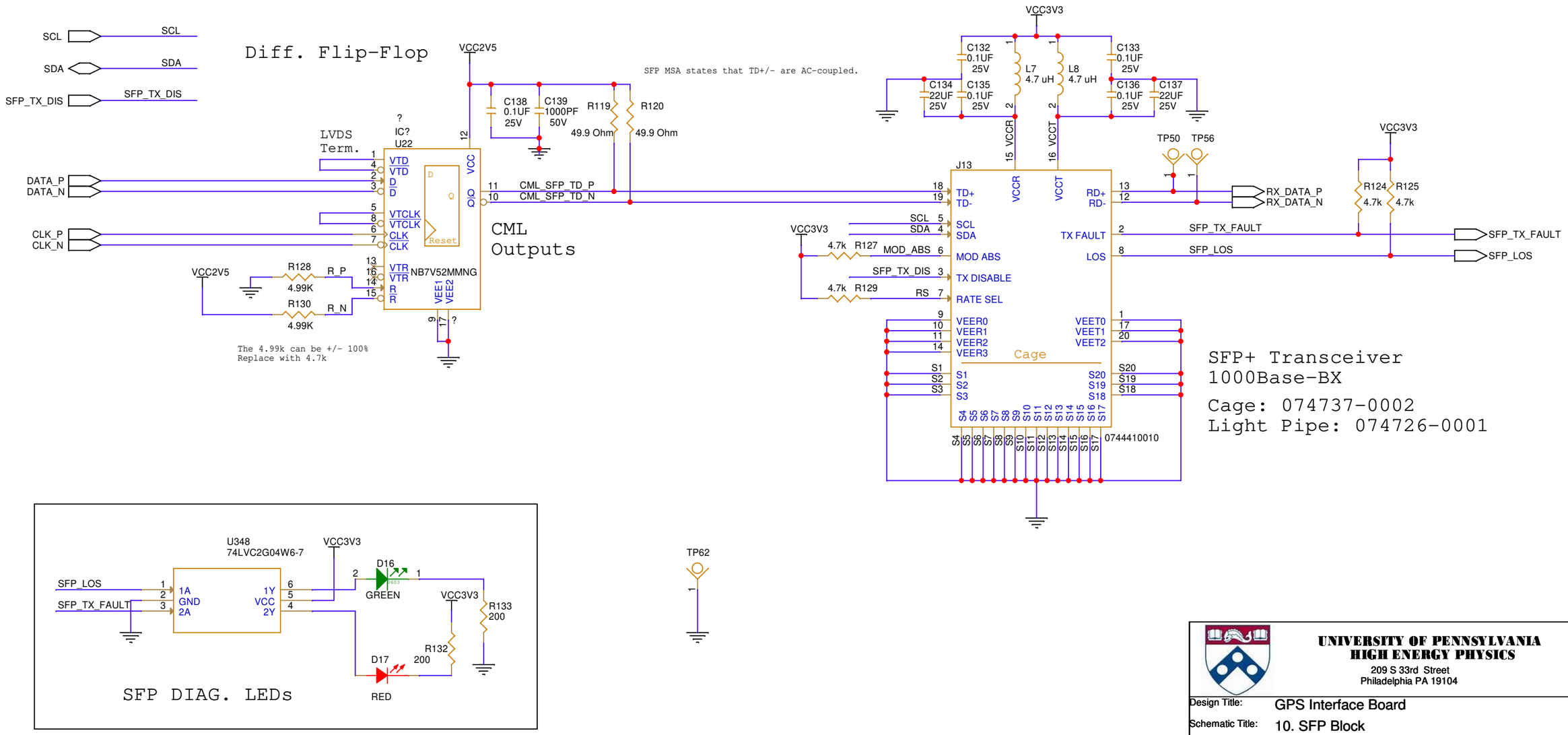

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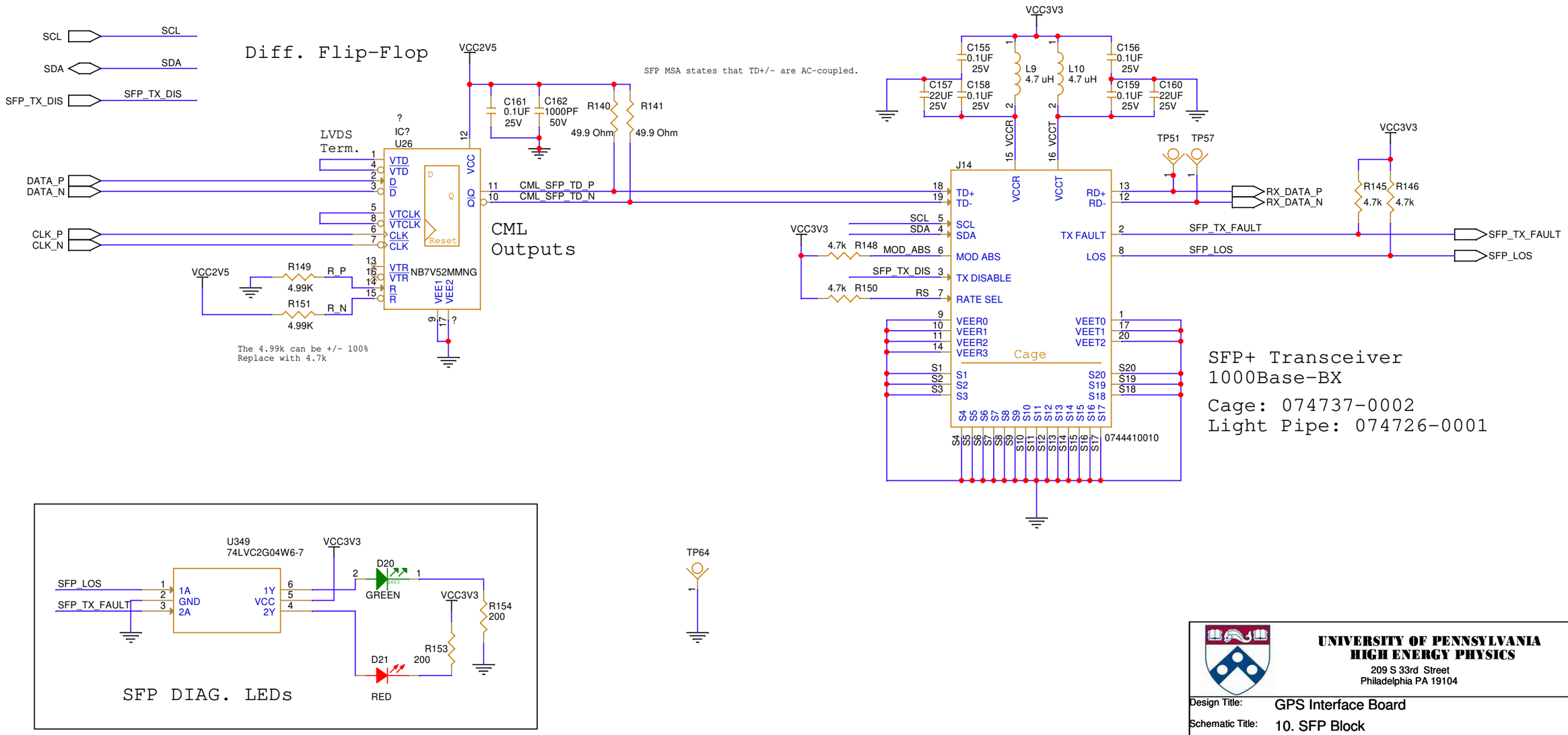

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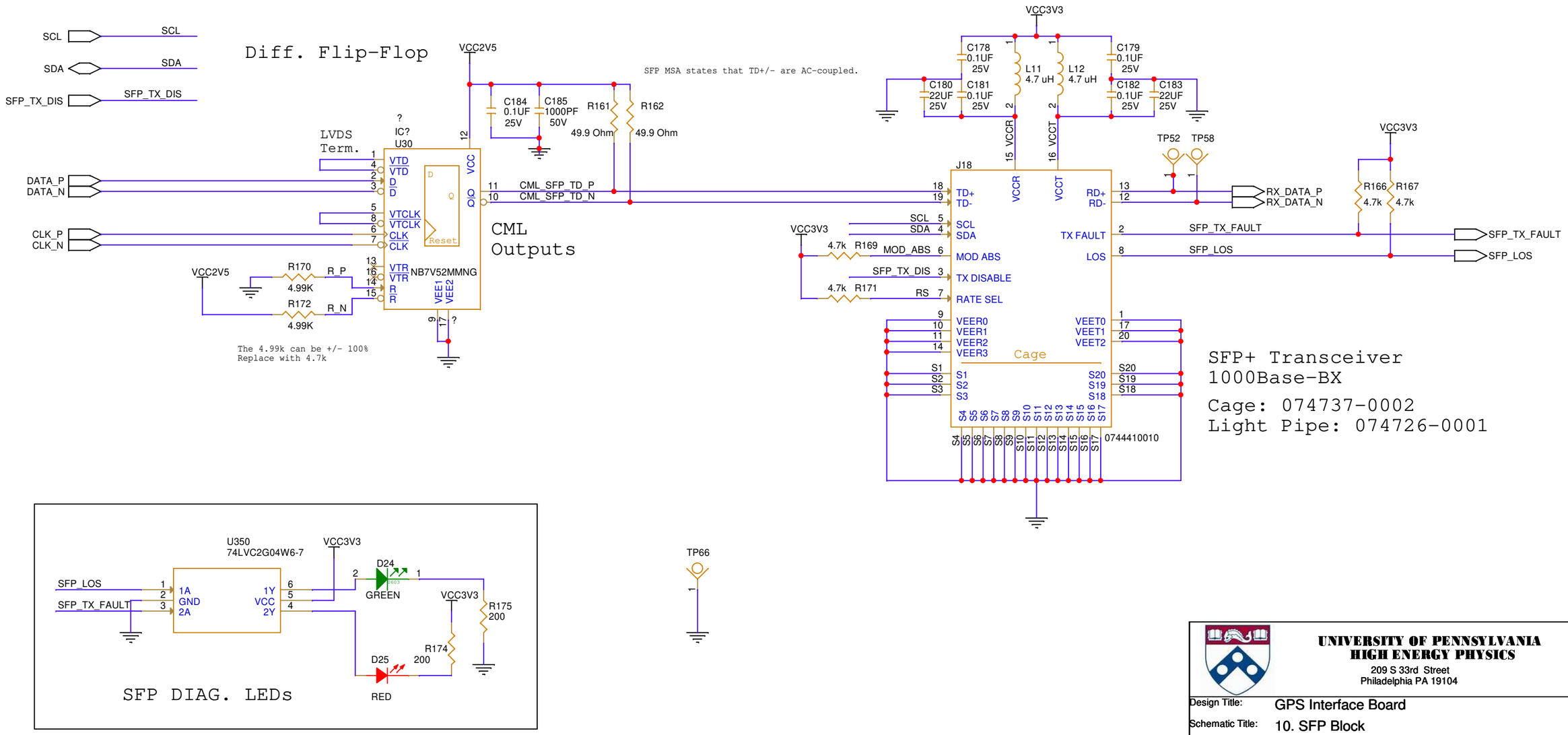

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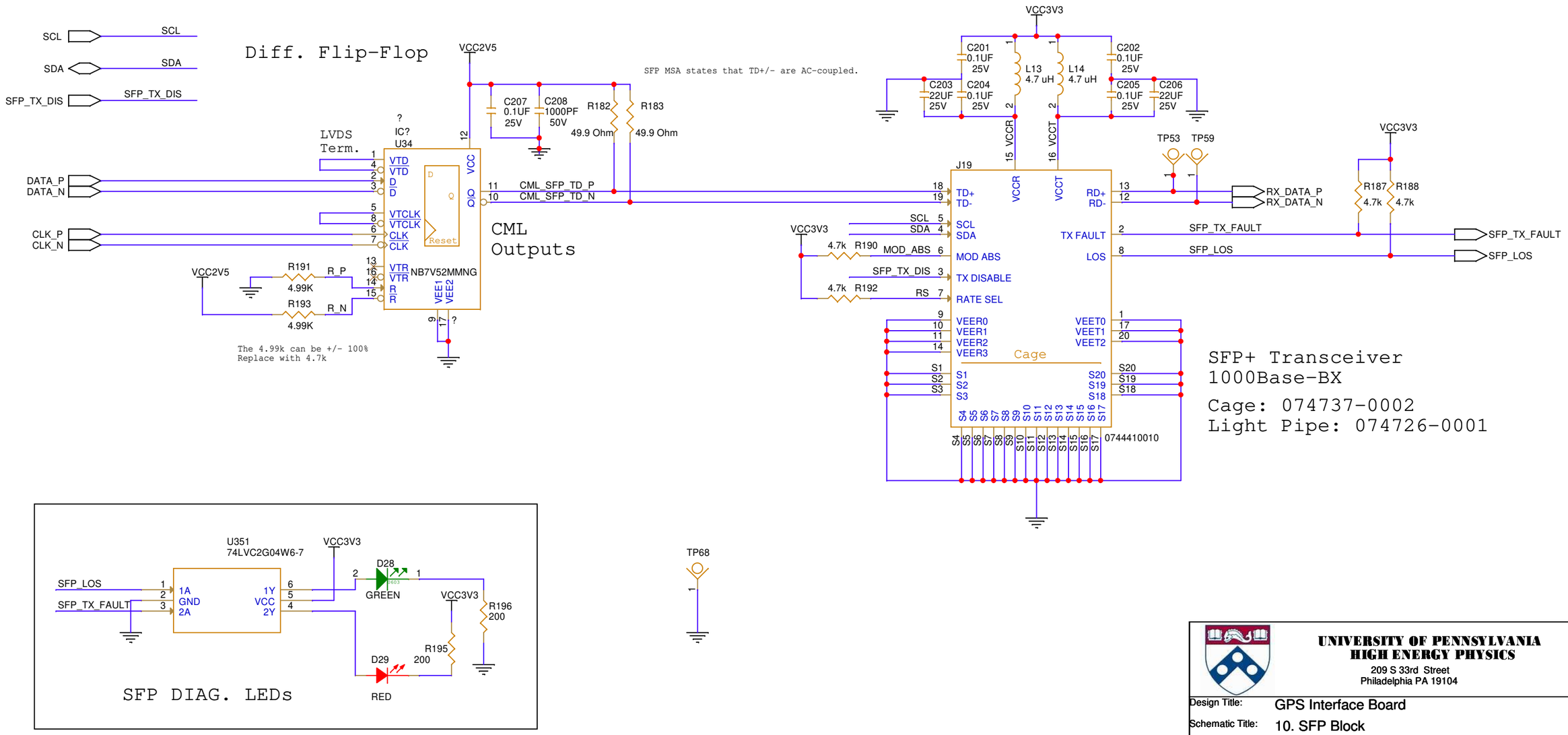

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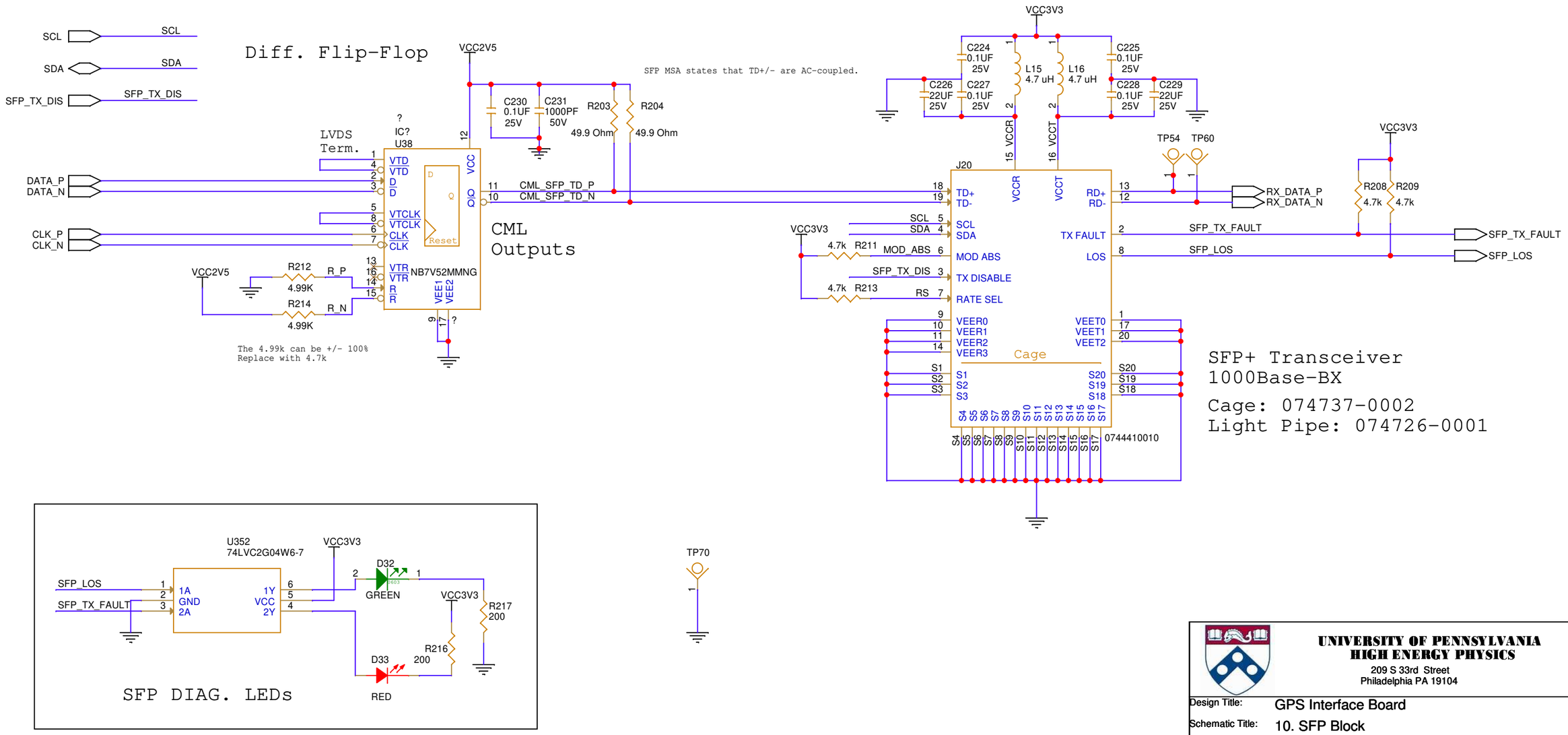

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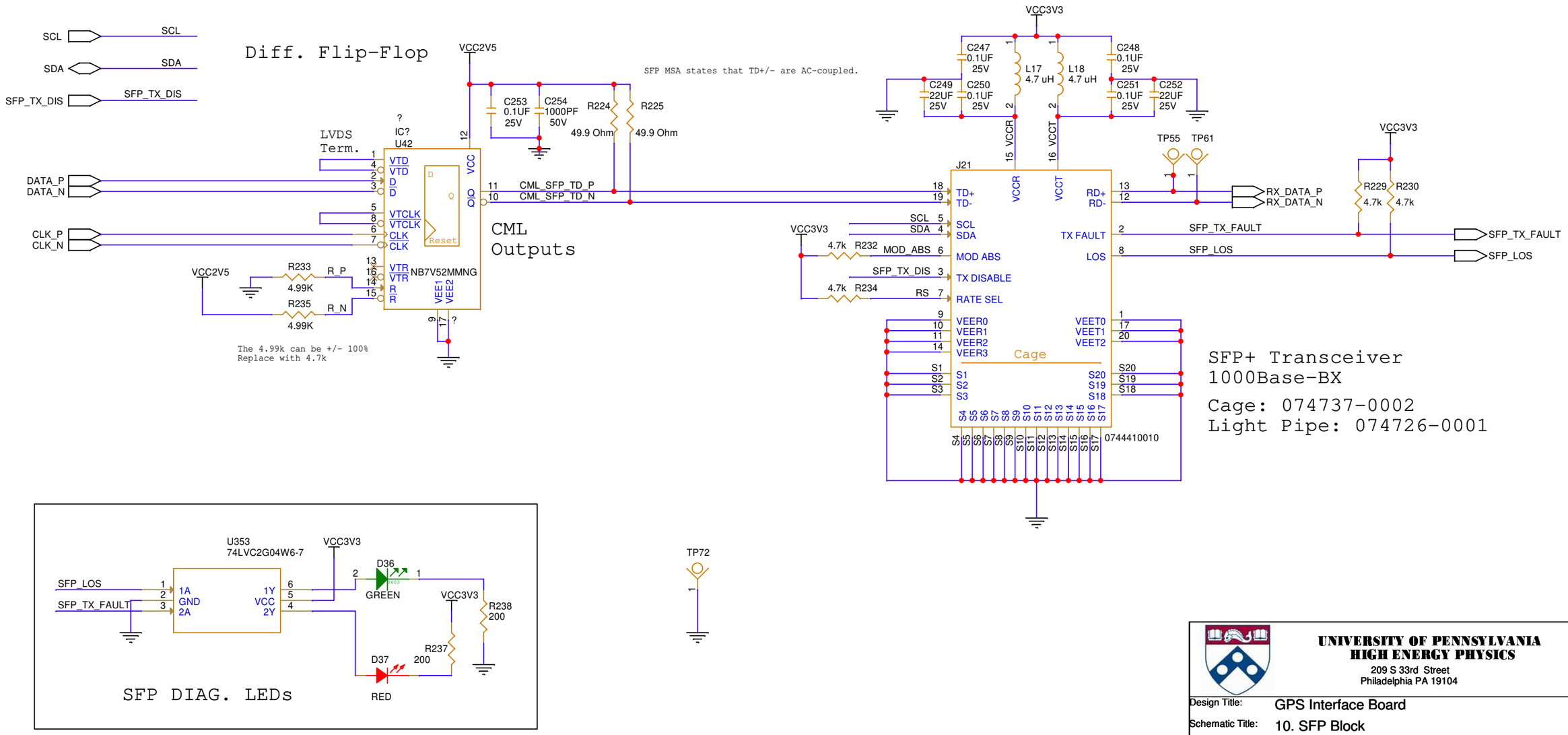

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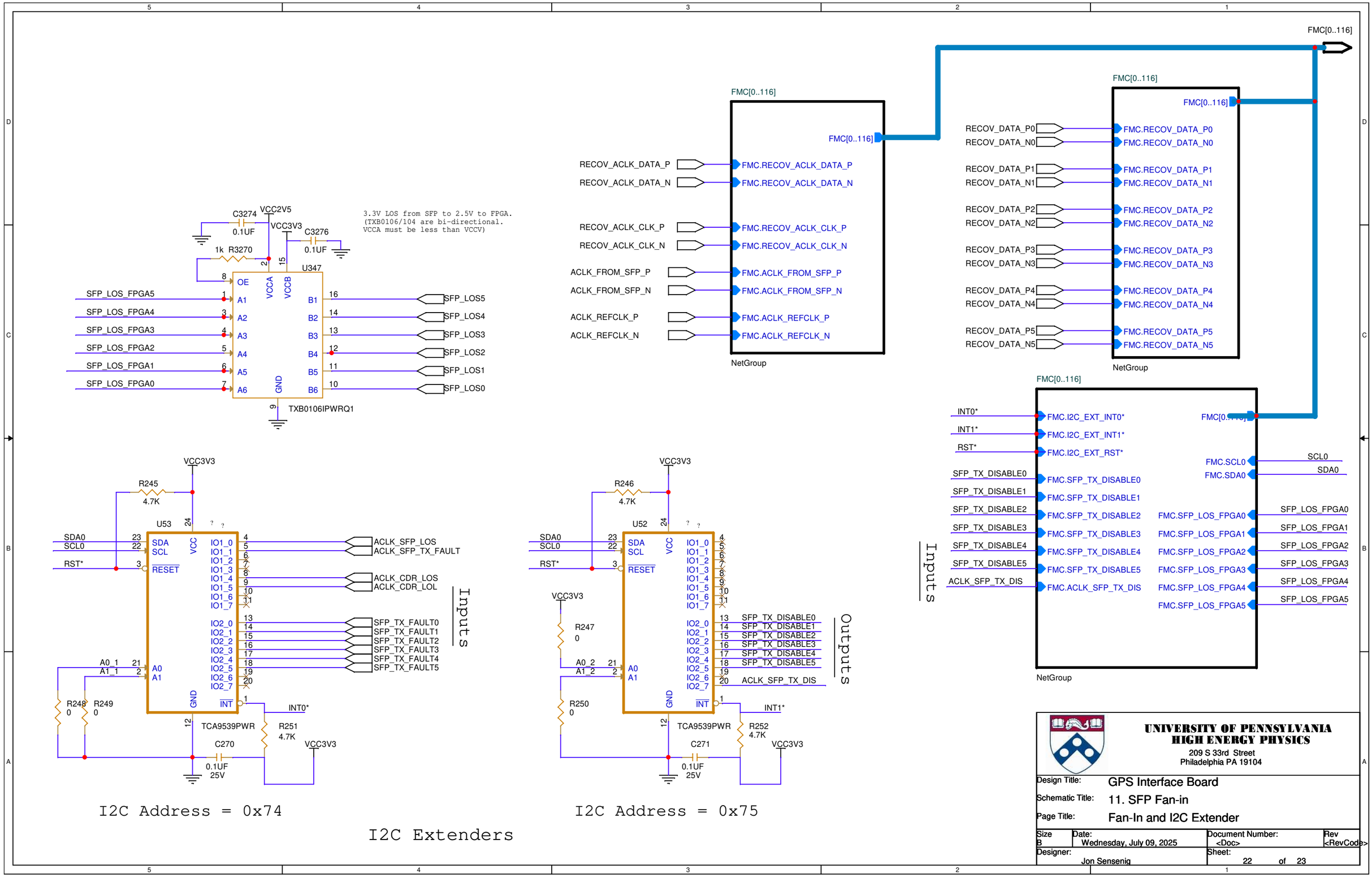

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Design Title:	GPS Interface Board
Schematic Title:	11. SFP Fan-in
Page Title:	Fan-In and I2C Extender

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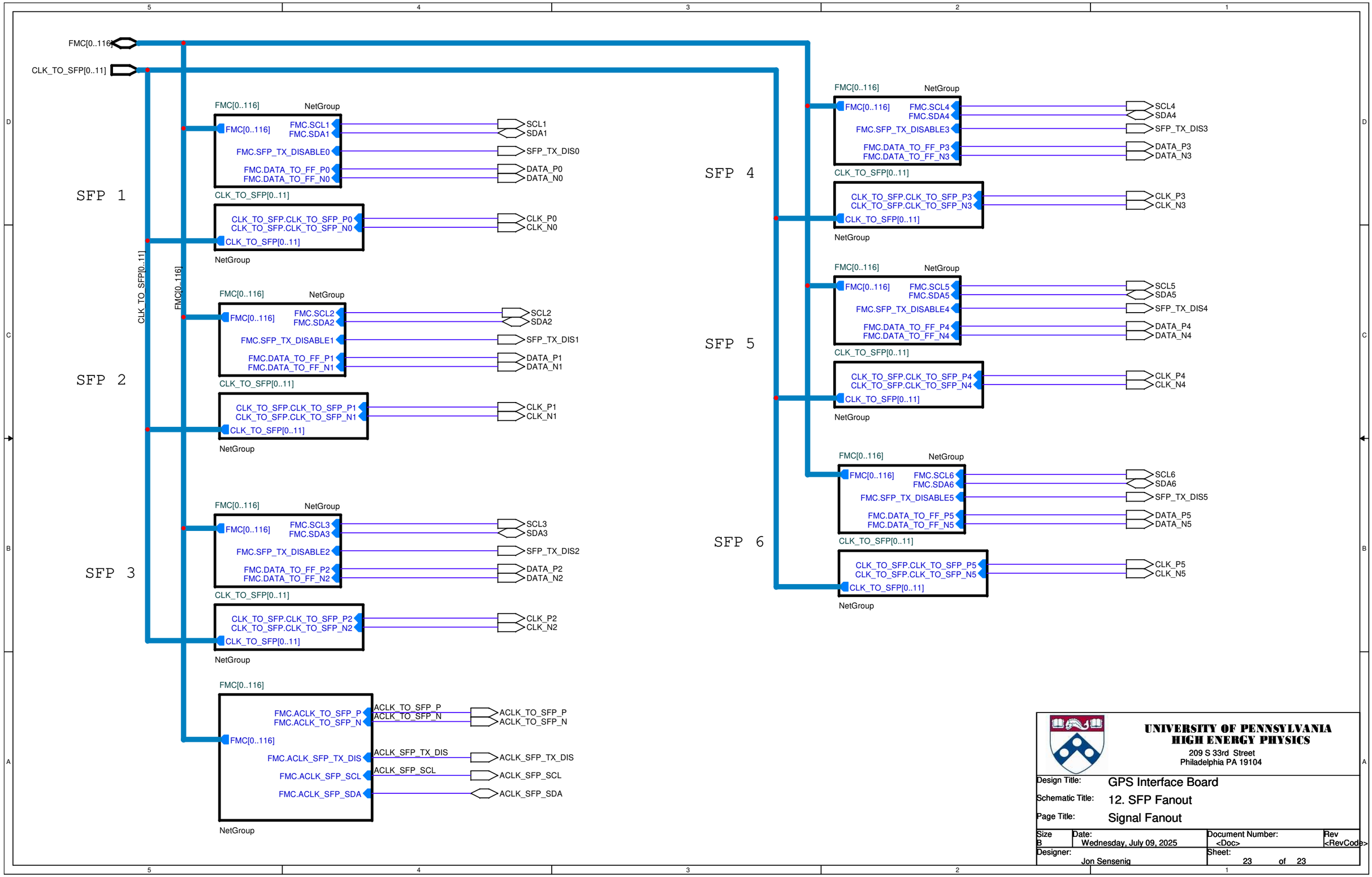

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Design Title:	GPS Interface Board
Schematic Title:	12. SFP Fanout
Page Title:	Signal Fanout

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