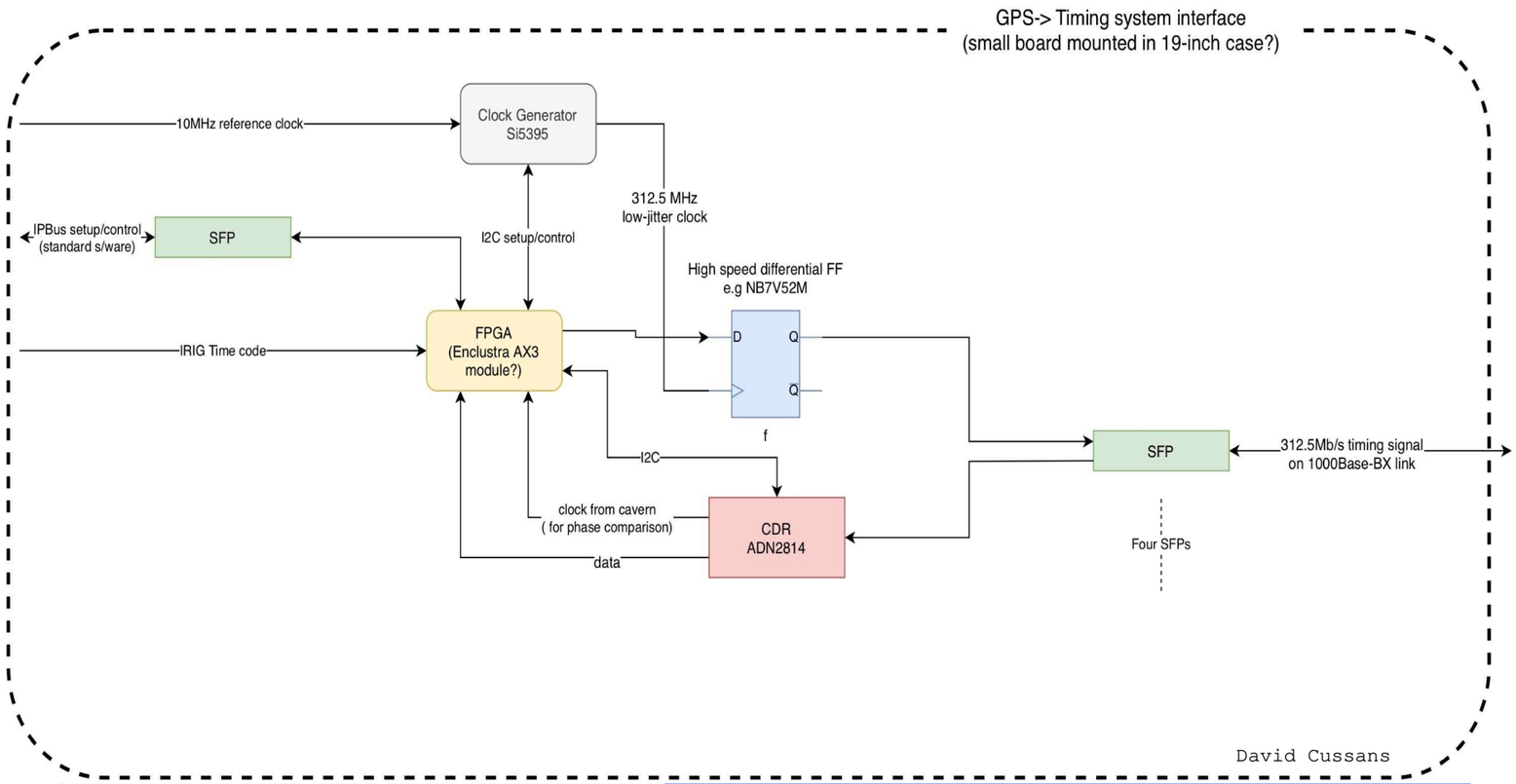

Part	I2C Address
CDR 1	0x40
CDR 2	0x60
CDR 3	0x41
CDR 4	0x61
CDR 5	0x42
CDR 6	0x62
SFP 1	
SFP 2	
SFP 3	
SFP 4	
SFP 5	
SFP 6	

Part	I2C Address
Board ID EEPROM	0x50
SI5395 Clock Gen.	0x68
I2C Extender 1	0x74
I2C Extender 2	0x75
VCC5V Power Monitor	0x67
VCC3V3 Power Monitor	0x6A
VCC2V5 Power Monitor	0x69
I2C Switch	0x70
Temperature Monitor	0x48

Power Estimate			Max Current (mA)				
Part	Description	Occurence	VCC5V	VCC3V3	VCC2V5	VCC1V8	12V Main PWR
LTC6957-2	Sine Wave to LVDS	1		72			
MAX9371	Low Jitter 5V TTL to LVDS	2	16				
SN74avc2t45	5V <--> 3.3V	1	100	100			
SN74avc2t45	3.3V <--> 2.5V	5		100	100		
SI5395	Clock Generator	1		302		300	
LTC2945	Power Monitor	4	1.2				
24AA025E48T	Board ID EEPROM	1		3			
LEDs		13		20			
NB7V52M	Diff. Flip-Flop	6			90		
ADN2814	CDR	6		145			
SFP		6		280			
SN74lvc1g32	OR Gate	12		100			
PCA9539	I2C Extender	2		160			
TCA9548A	I2C Switch	1			100		
LM75A	Temp Monitor	1		20			
NC7SZ08	AND Gate	1		50			
SN65LVDM176	LVDS Transceiver	2		15			
TXB0104(6)	Level Translator	2		100	100		
	Totals	Current (A)	0.14	5.41	1.14	0.30	
		Power (W)	0.68	17.84	3.76	0.54	22.83
	Max Power Supply	Current (A)	2	8			4
		Power (W)	11	28			48

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Design Title: GPS Interface Board
Schematic Title: GIB Top
Page Title: 01. Address Table

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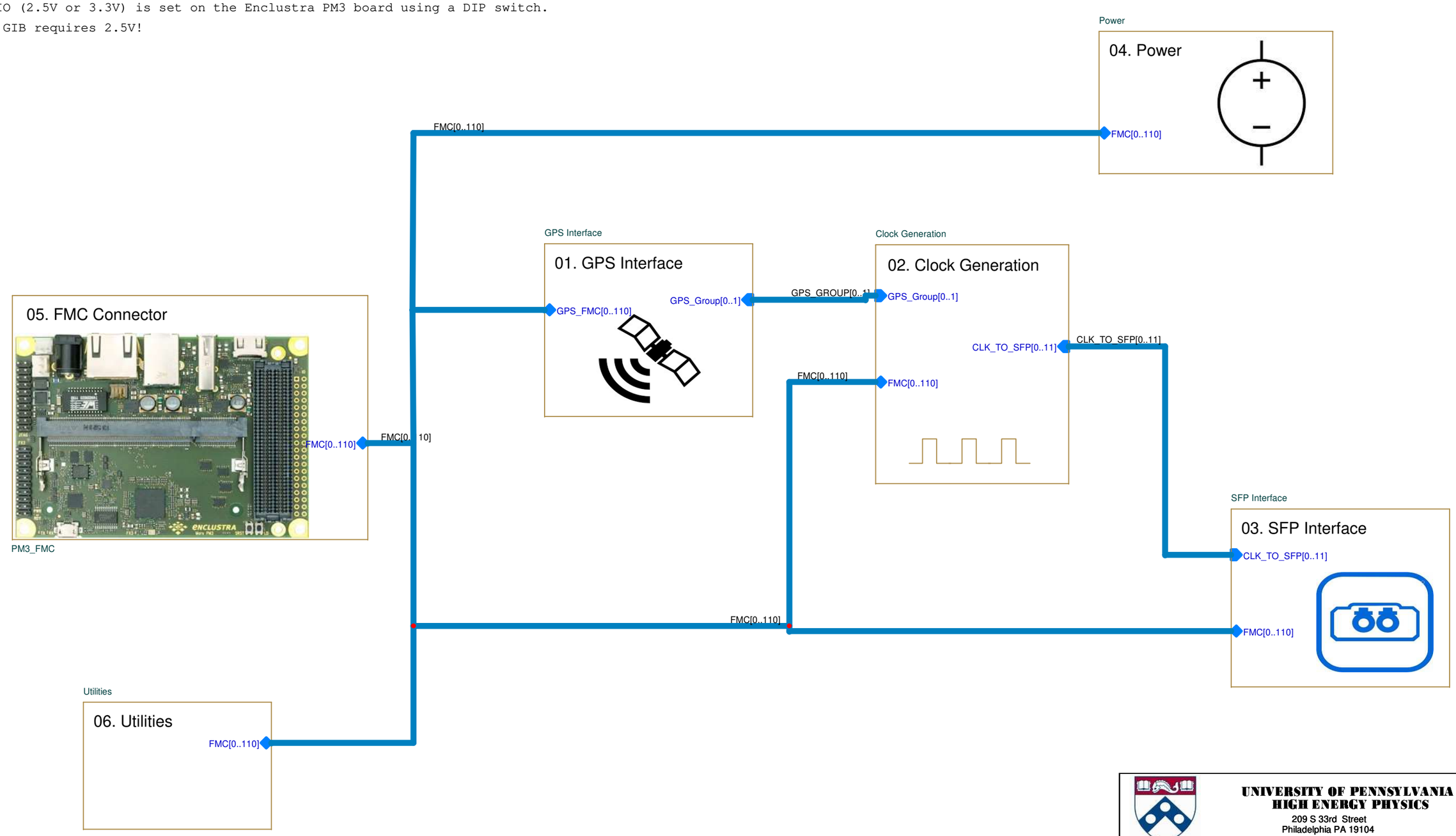
Sheet: 1 of 23

VCCIO (2.5V or 3.3V) is set on the Enclustra PM3 board using a DIP switch.
The GIB requires 2.5V!



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Design Title:	GPS Interface Board
Schematic Title:	GIB Top
Page Title:	02. Top Level

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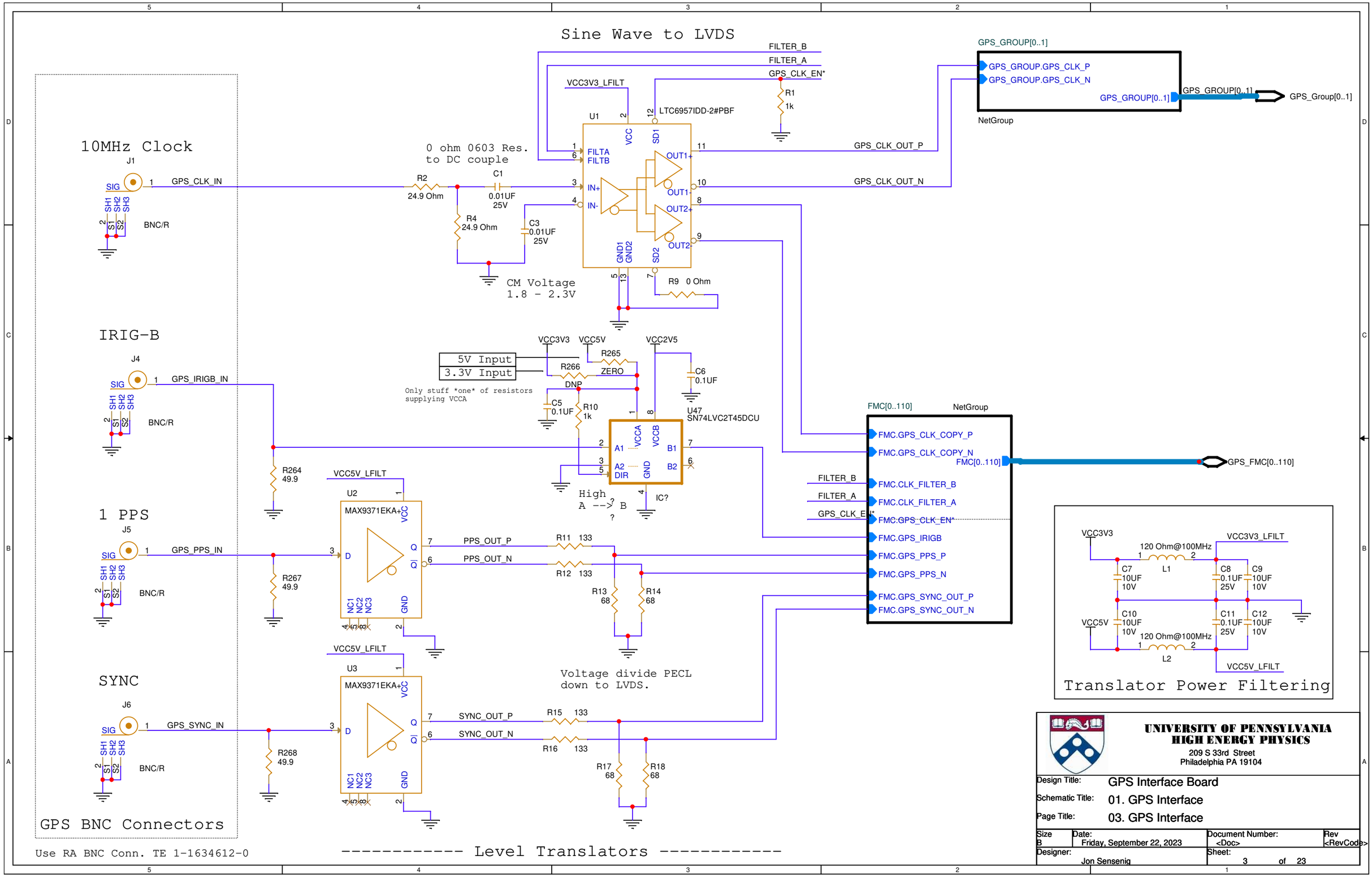
Designer: Jon Sensenig		Sheet: 2 of 23	


Sine Wave to LVDS
10MHz Clock
J1
SIG
GPS_CLK_IN
BNC/R
0 ohm 0603 Res.
to DC couple
R2
24.9 Ohm
C1
0.01UF
25V
R4
24.9 Ohm
C3
0.01UF
25V
CM Voltage
1.8 - 2.3V
U1
LTC6957IDD-2#PBF
FILTA
FILTB
IN+
IN-
OUT1+
OUT1-
OUT2+
OUT2-
VCC
SD1
GND1
GND2
SD2
VCC3V3_LFILT
FILTER_B
FILTER_A
GPS_CLK_EN*
R1
1k
GPS_CLK_OUT_P
GPS_CLK_OUT_N
R9 0 Ohm
GPS_GROUP[0..1]
GPS_GROUP.GPS_CLK_P
GPS_GROUP.GPS_CLK_N
NetGroup
GPS_Group[0..1]
IRIG-B
J4
GPS_IRIGB_IN
5V Input
3.3V Input
Only stuff *one* of resistors
supplying VCCA
VCC3V3
VCC5V
VCC2V5
R265
R266
ZERO
DNP
C5
0.1UF
R10
1k
C6
0.1UF
U47
SN74LVC2T45DCU
VCCA
VCCB
A1
A2
DIR
GND
B1
B2
High
A --> B
IC?
R264
49.9
1 PPS
J5
GPS_PPS_IN
R267
49.9
VCC5V_LFILT
U2
MAX9371EKA+
VCC
D
Q
Q|
NC1
NC2
NC3
GND
PPS_OUT_P
PPS_OUT_N
R11 133
R12 133
R13
68
R14
68
SYNC
J6
GPS_SYNC_IN
R268
49.9
U3
SYNC_OUT_P
SYNC_OUT_N
R15 133
R16 133
R17
68
R18
68
Voltage divide PECL
down to LVDS.
GPS BNC Connectors
Use RA BNC Conn. TE 1-1634612-0
---------- Level Translators ----------
FMC[0..110]
NetGroup
FMC.GPS_CLK_COPY_P
FMC.GPS_CLK_COPY_N
FMC.CLK_FILTER_B
FMC.CLK_FILTER_A
FMC.GPS_CLK_EN*
FMC.GPS_IRIGB
FMC.GPS_PPS_P
FMC.GPS_PPS_N
FMC.GPS_SYNC_OUT_P
FMC.GPS_SYNC_OUT_N
GPS_FMC[0..110]
VCC3V3
VCC3V3_LFILT
120 Ohm@100MHz
L1
C7
10UF
10V
C8
0.1UF
25V
C9
10UF
10V
VCC5V
C10
10UF
10V
C11
0.1UF
25V
C12
10UF
10V
L2
VCC5V_LFILT
Translator Power Filtering
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Design Title: GPS Interface Board
Schematic Title: 01. GPS Interface
Page Title: 03. GPS Interface
Size B
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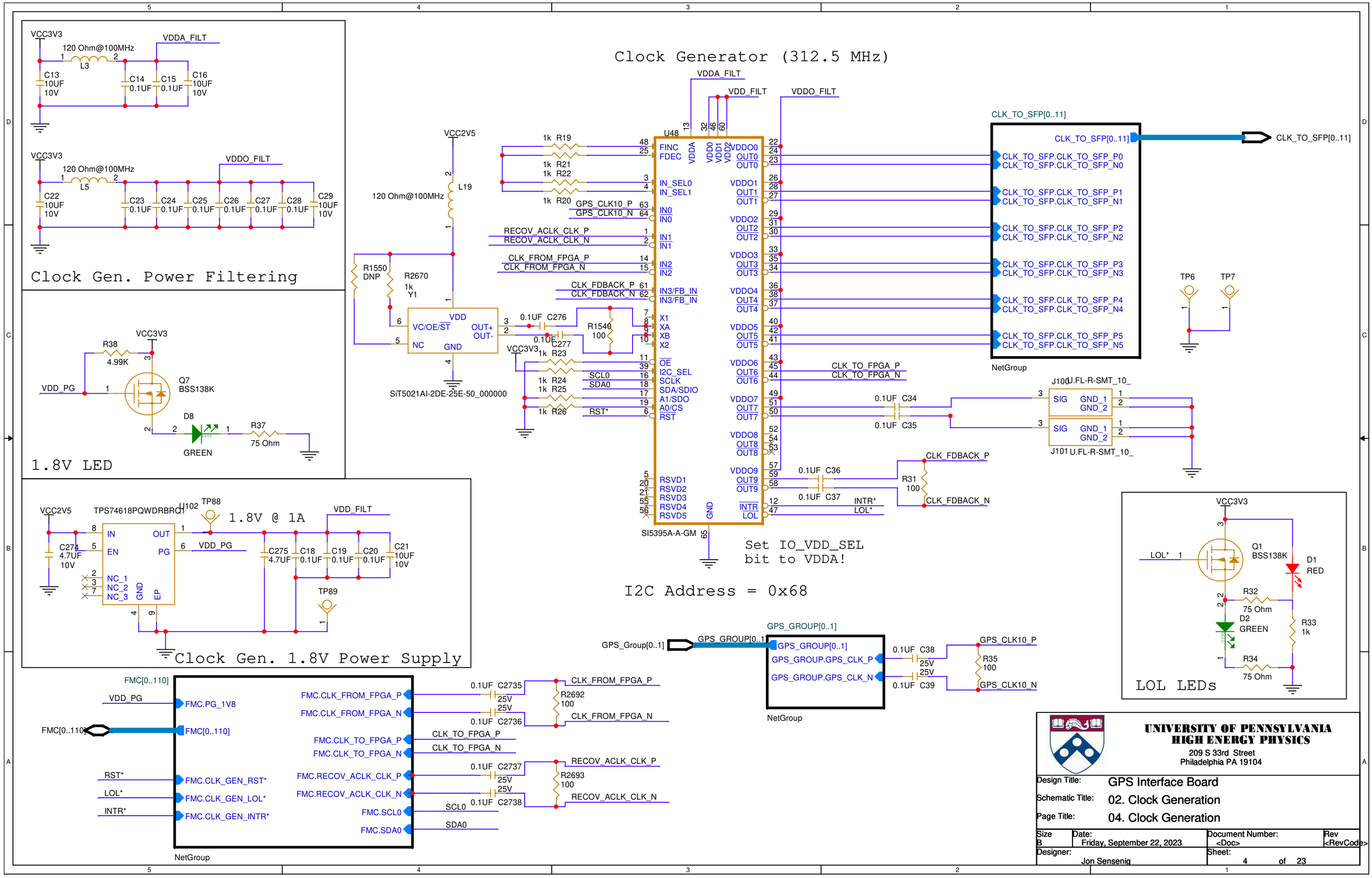
Clock Generator (312.5 MHz)
Clock Gen. Power Filtering
1.8V LED
Clock Gen. 1.8V Power Supply
1.8V @ 1A
I2C Address = 0x68
Set IO_VDD_SEL bit to VDDA!
LOL LEDs
U48
SI5395A-A-GM
SiT5021AI-2DE-25E-50_000000
TPS74618PQWDRBRQ1
NetGroup
J100 J.FL-R-SMT_10_
J101 U.FL-R-SMT_10_
CLK_TO_SFP[0..11]
GPS_GROUP[0..1]
GPS_Group[0..1]
FMC[0..110]
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Design Title: GPS Interface Board
Schematic Title: 02. Clock Generation
Page Title: 04. Clock Generation
Size B
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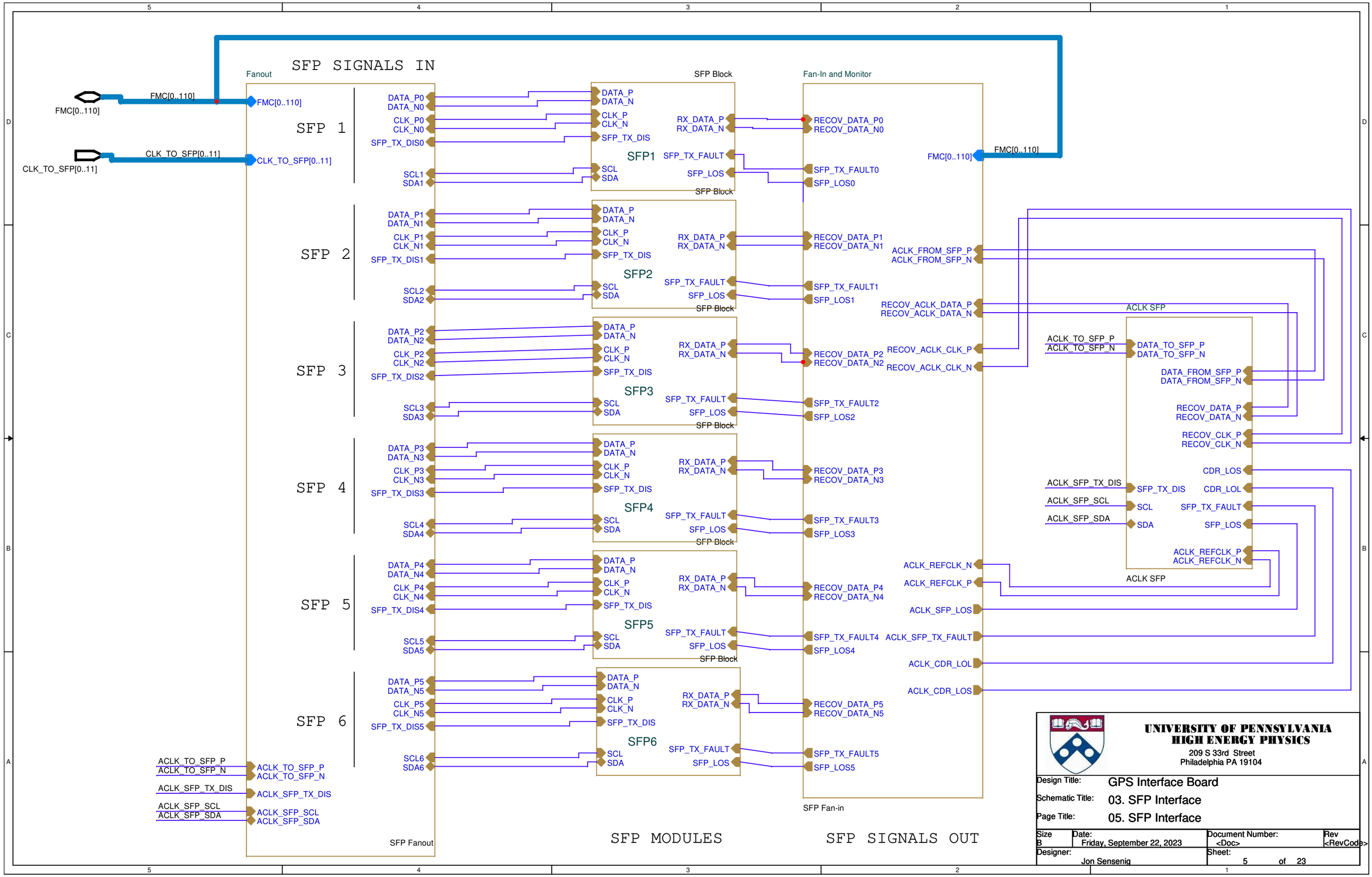
Designer: Jon Sensenig
Sheet: 4 of 23



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Design Title:	GPS Interface Board
Schematic Title:	03. SFP Interface
Page Title:	05. SFP Interface

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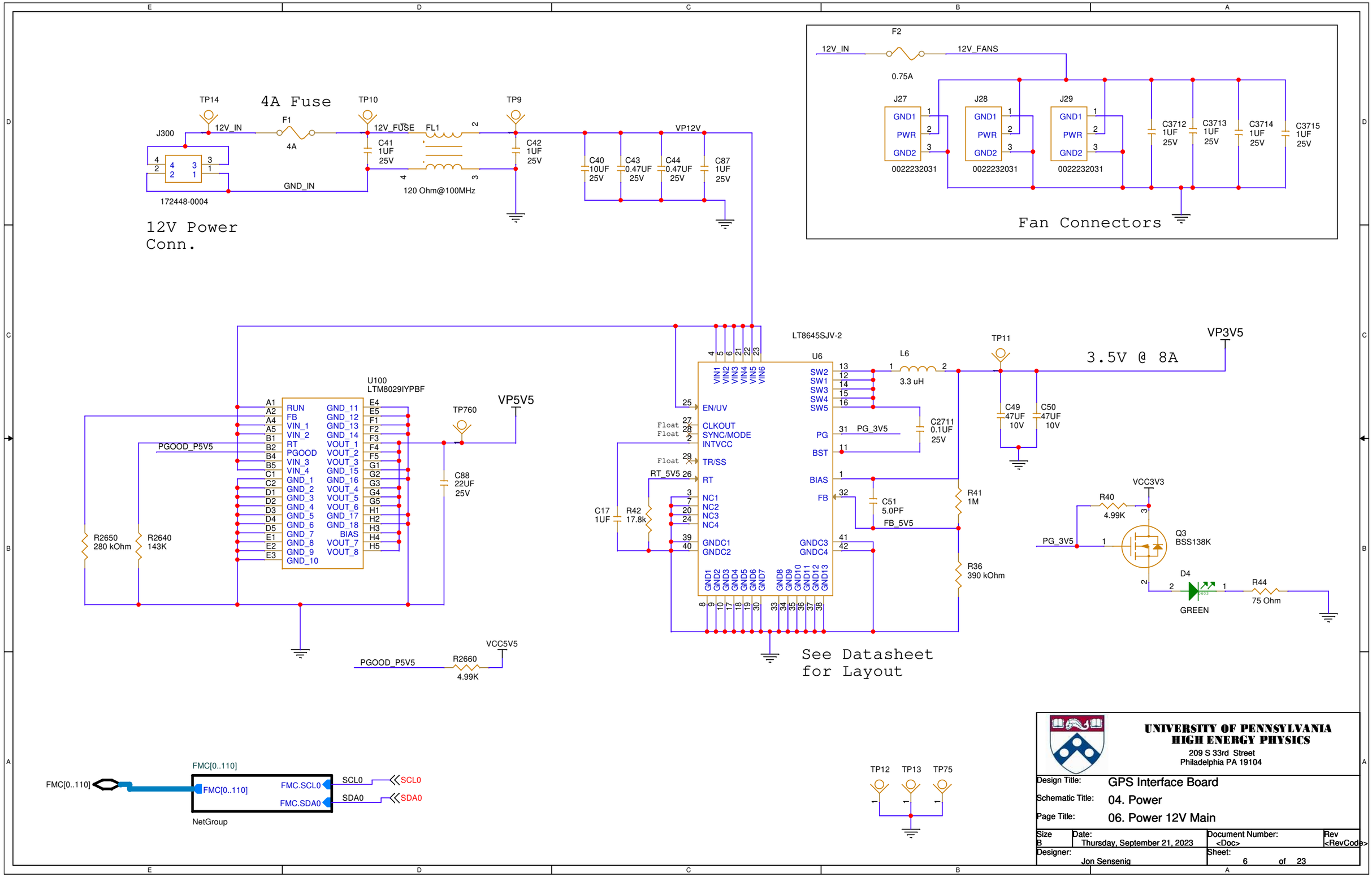

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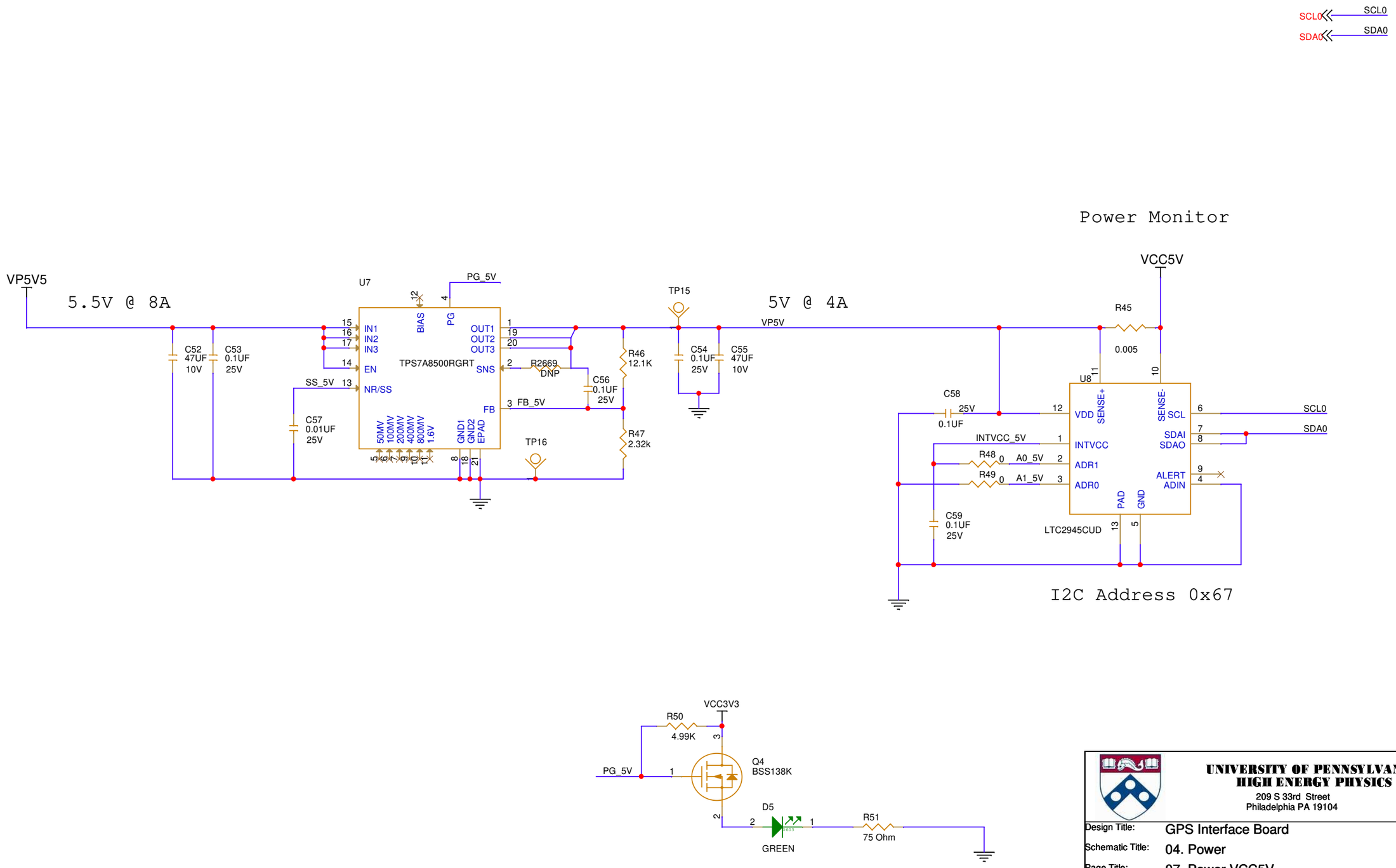
Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	06. Power 12V Main
Size: B	Date: Thursday, September 21, 2023
Document Number:	<Doc>
Rev	<RevCode>
Designer:	Jon Sensenig
Sheet:	6 of 23



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Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	07. Power VCC5V

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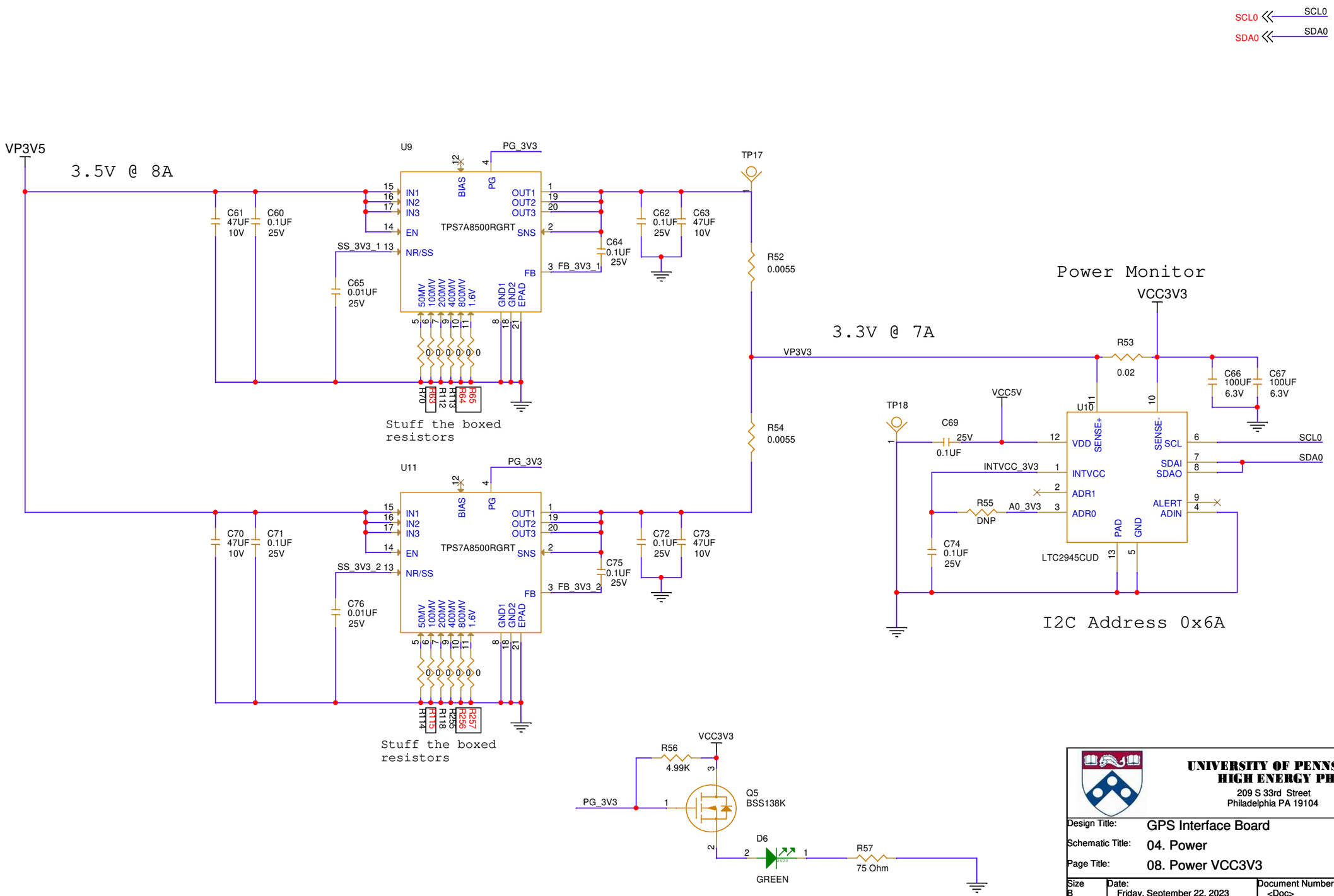
Designer: Jon Sensenig		Sheet: 7 of 23	



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Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	08. Power VCC3V3

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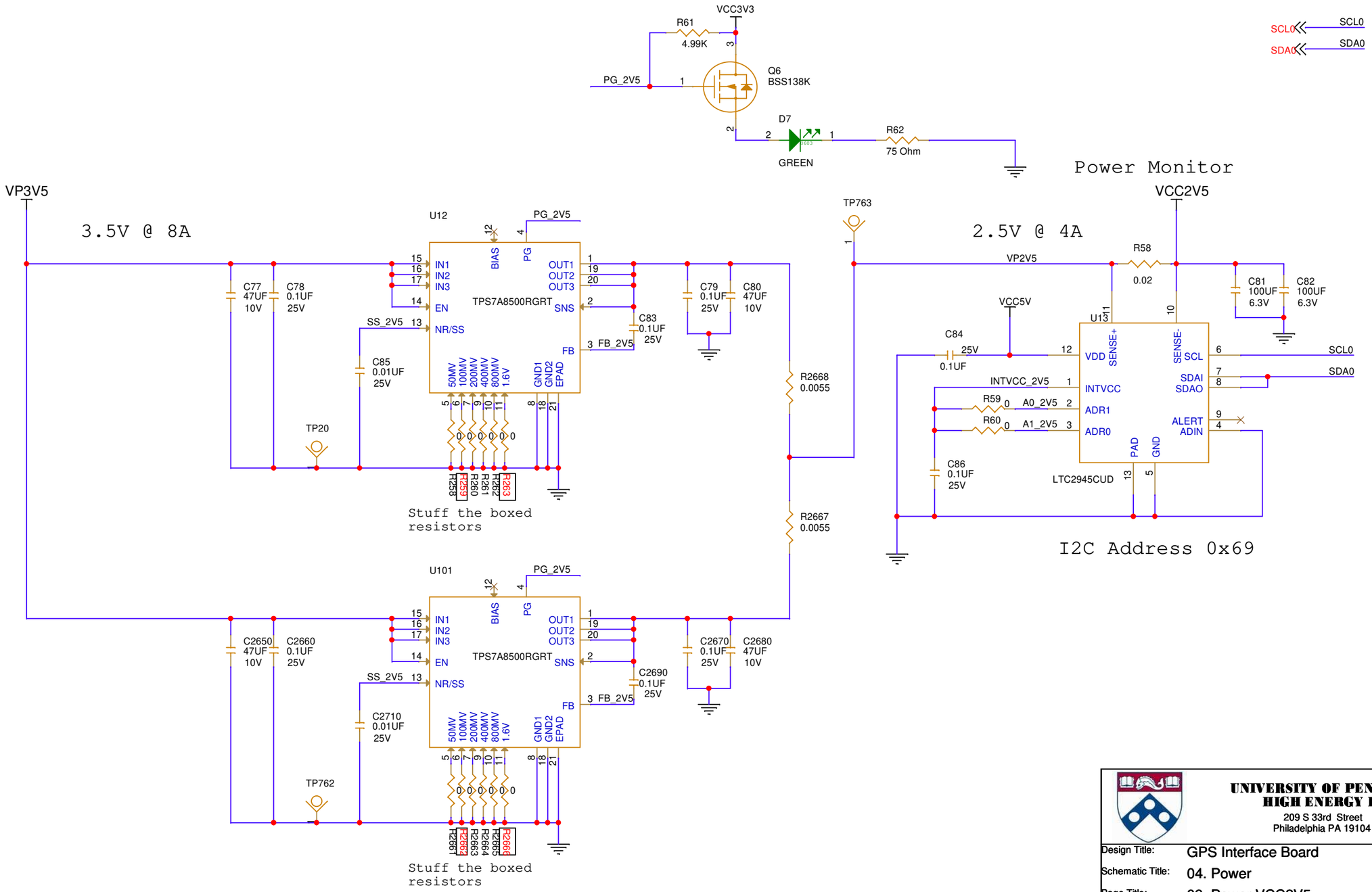

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Design Title:	GPS Interface Board
Schematic Title:	04. Power
Page Title:	09. Power VCC2V5

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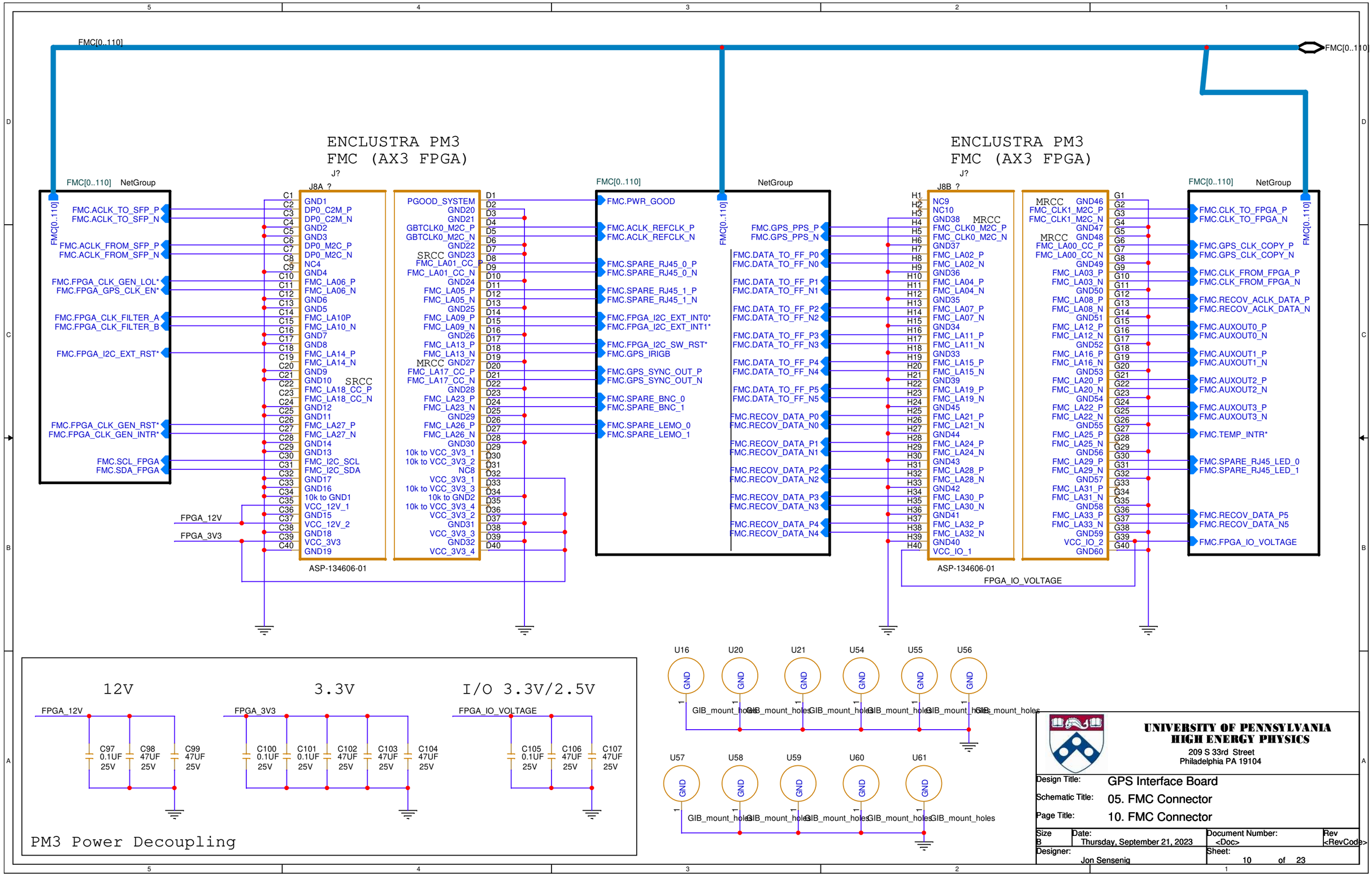
FMC[0..110]
ENCLUSTRA PM3
FMC (AX3 FPGA)
J?
J8A ?
NetGroup
FMC.ACLK_TO_SFP_P
FMC.ACLK_TO_SFP_N
FMC.ACLK_FROM_SFP_P
FMC.ACLK_FROM_SFP_N
FMC.FPGA_CLK_GEN_LOL*
FMC.FPGA_GPS_CLK_EN*
FMC.FPGA_CLK_FILTER_A
FMC.FPGA_CLK_FILTER_B
FMC.FPGA_I2C_EXT_RST*
FMC.FPGA_CLK_GEN_RST*
FMC.FPGA_CLK_GEN_INTR*
FMC.SCL_FPGA
FMC.SDA_FPGA
FPGA_12V
FPGA_3V3
ASP-134606-01
FMC.PWR_GOOD
FMC.ACLK_REFCLK_P
FMC.ACLK_REFCLK_N
FMC.SPARE_RJ45_0_P
FMC.SPARE_RJ45_0_N
FMC.SPARE_RJ45_1_P
FMC.SPARE_RJ45_1_N
FMC.FPGA_I2C_EXT_INT0*
FMC.FPGA_I2C_EXT_INT1*
FMC.FPGA_I2C_SW_RST*
FMC.GPS_IRIGB
FMC.GPS_SYNC_OUT_P
FMC.GPS_SYNC_OUT_N
FMC.SPARE_BNC_0
FMC.SPARE_BNC_1
FMC.SPARE_LEMO_0
FMC.SPARE_LEMO_1
J8B ?
FMC.GPS_PPS_P
FMC.GPS_PPS_N
FMC.DATA_TO_FF_P0
FMC.DATA_TO_FF_N0
FMC.DATA_TO_FF_P1
FMC.DATA_TO_FF_N1
FMC.DATA_TO_FF_P2
FMC.DATA_TO_FF_N2
FMC.DATA_TO_FF_P3
FMC.DATA_TO_FF_N3
FMC.DATA_TO_FF_P4
FMC.DATA_TO_FF_N4
FMC.DATA_TO_FF_P5
FMC.DATA_TO_FF_N5
FMC.RECOV_DATA_P0
FMC.RECOV_DATA_N0
FMC.RECOV_DATA_P1
FMC.RECOV_DATA_N1
FMC.RECOV_DATA_P2
FMC.RECOV_DATA_N2
FMC.RECOV_DATA_P3
FMC.RECOV_DATA_N3
FMC.RECOV_DATA_P4
FMC.RECOV_DATA_N4
FMC.CLK_TO_FPGA_P
FMC.CLK_TO_FPGA_N
FMC.GPS_CLK_COPY_P
FMC.GPS_CLK_COPY_N
FMC.CLK_FROM_FPGA_P
FMC.CLK_FROM_FPGA_N
FMC.RECOV_ACLK_DATA_P
FMC.RECOV_ACLK_DATA_N
FMC.AUXOUT0_P
FMC.AUXOUT0_N
FMC.AUXOUT1_P
FMC.AUXOUT1_N
FMC.AUXOUT2_P
FMC.AUXOUT2_N
FMC.AUXOUT3_P
FMC.AUXOUT3_N
FMC.TEMP_INTR*
FMC.SPARE_RJ45_LED_0
FMC.SPARE_RJ45_LED_1
FMC.RECOV_DATA_P5
FMC.RECOV_DATA_N5
FMC.FPGA_IO_VOLTAGE
FPGA_IO_VOLTAGE
12V
3.3V
I/O 3.3V/2.5V
C97 0.1UF 25V
C98 47UF 25V
C99 47UF 25V
C100 0.1UF 25V
C101 0.1UF 25V
C102 47UF 25V
C103 47UF 25V
C104 47UF 25V
C105 0.1UF 25V
C106 47UF 25V
C107 47UF 25V
PM3 Power Decoupling
U16
U20
U21
U54
U55
U56
U57
U58
U59
U60
U61
GND
GIB_mount_holes
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Design Title: GPS Interface Board
Schematic Title: 05. FMC Connector
Page Title: 10. FMC Connector
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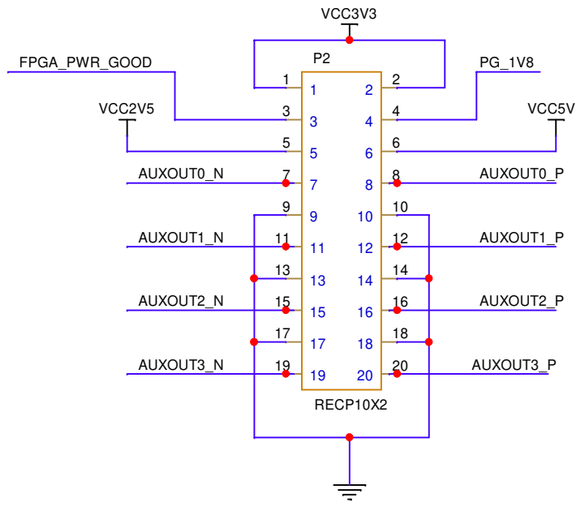
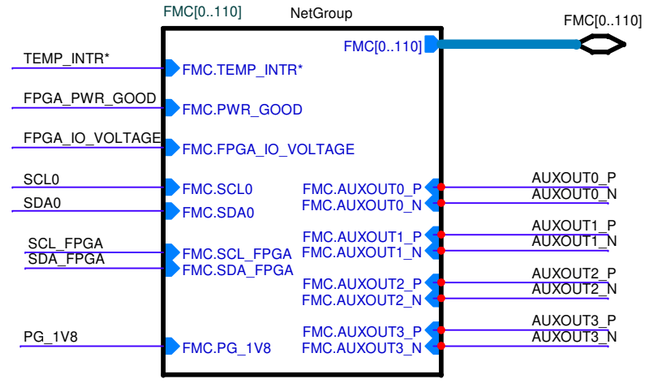
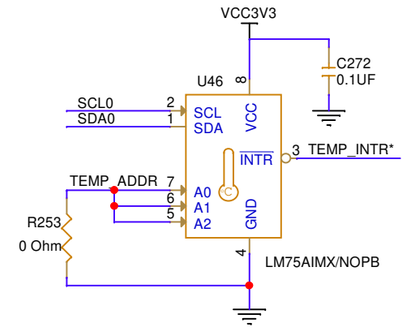


Connections to front panel LEDs / Auxilliary I/O





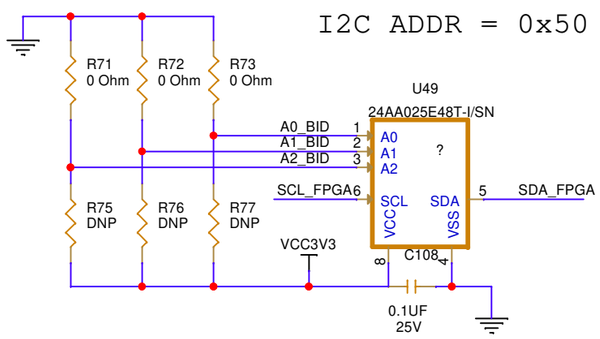
I2C ADDR = 0x48

Temp. Monitor

Note: Temperature measured from component's die.

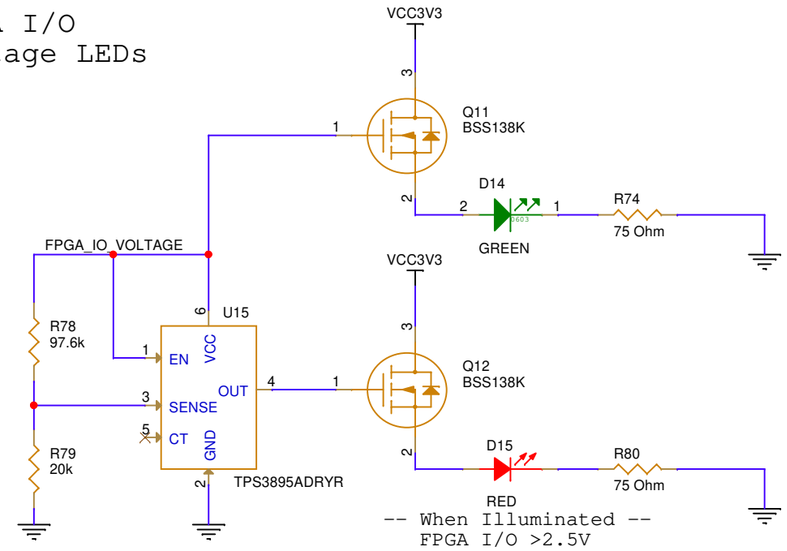
EEPROM

I2C ADDR = 0x50



Board ID

FPGA I/O
Voltage LEDs



-- When Illuminated --
FPGA I/O >2.5V
Change setting!

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Design Title:	GPS Interface Board
Schematic Title:	06. Utilities
Page Title:	11. Utilities

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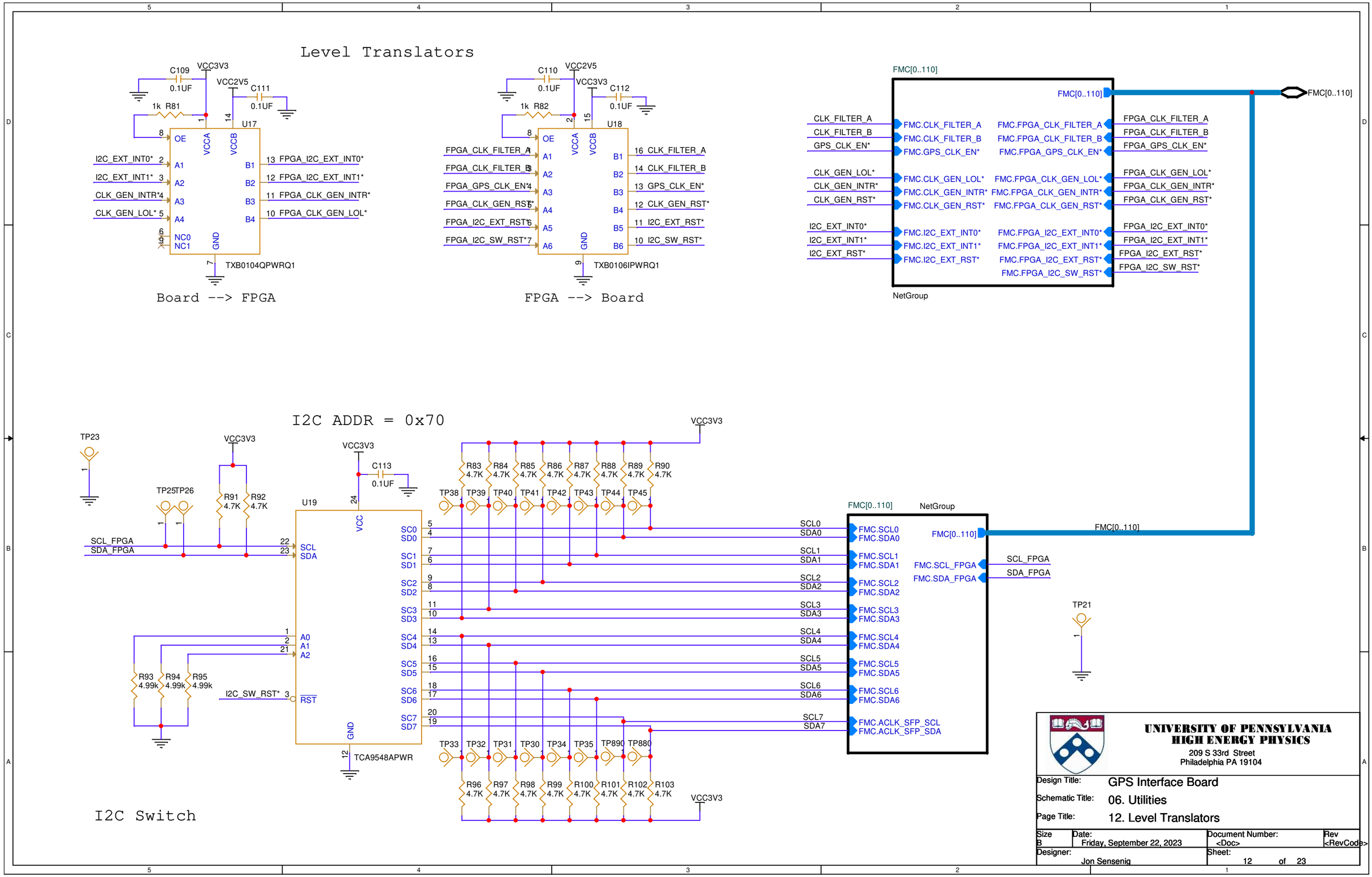
Level Translators
C109 0.1UF
VCC3V3
VCC2V5
C111 0.1UF
1k R81
U17
OE
VCCA
VCCB
I2C_EXT_INT0* 2 A1
I2C_EXT_INT1* 3 A2
CLK_GEN_INTR* 4 A3
CLK_GEN_LOL* 5 A4
NC0
NC1
GND
B1 13 FPGA_I2C_EXT_INT0*
B2 12 FPGA_I2C_EXT_INT1*
B3 11 FPGA_CLK_GEN_INTR*
B4 10 FPGA_CLK_GEN_LOL*
TXB0104QPWRQ1
Board --> FPGA
C110 0.1UF
VCC2V5
VCC3V3
C112 0.1UF
1k R82
U18
FPGA_CLK_FILTER_A
FPGA_CLK_FILTER_B
FPGA_GPS_CLK_EN*
FPGA_CLK_GEN_RST*
FPGA_I2C_EXT_RST*
FPGA_I2C_SW_RST*
A1
A2
A3
A4
A5
A6
B1 16 CLK_FILTER_A
B2 14 CLK_FILTER_B
B3 13 GPS_CLK_EN*
B4 12 CLK_GEN_RST*
B5 11 I2C_EXT_RST*
B6 10 I2C_SW_RST*
TXB0106IPWRQ1
FPGA --> Board
FMC[0..110]
NetGroup
CLK_FILTER_A
CLK_FILTER_B
GPS_CLK_EN*
CLK_GEN_LOL*
CLK_GEN_INTR*
CLK_GEN_RST*
I2C_EXT_INT0*
I2C_EXT_INT1*
I2C_EXT_RST*
FMC.CLK_FILTER_A
FMC.CLK_FILTER_B
FMC.GPS_CLK_EN*
FMC.CLK_GEN_LOL*
FMC.CLK_GEN_INTR*
FMC.CLK_GEN_RST*
FMC.I2C_EXT_INT0*
FMC.I2C_EXT_INT1*
FMC.I2C_EXT_RST*
FMC.FPGA_CLK_FILTER_A
FMC.FPGA_CLK_FILTER_B
FMC.FPGA_GPS_CLK_EN*
FMC.FPGA_CLK_GEN_LOL*
FMC.FPGA_CLK_GEN_INTR*
FMC.FPGA_CLK_GEN_RST*
FMC.FPGA_I2C_EXT_INT0*
FMC.FPGA_I2C_EXT_INT1*
FMC.FPGA_I2C_EXT_RST*
FMC.FPGA_I2C_SW_RST*
FPGA_CLK_FILTER_A
FPGA_CLK_FILTER_B
FPGA_GPS_CLK_EN*
FPGA_CLK_GEN_LOL*
FPGA_CLK_GEN_INTR*
FPGA_CLK_GEN_RST*
FPGA_I2C_EXT_INT0*
FPGA_I2C_EXT_INT1*
FPGA_I2C_EXT_RST*
FPGA_I2C_SW_RST*
I2C ADDR = 0x70
TP23
VCC3V3
TP25TP26
R91 4.7K
R92 4.7K
SCL_FPGA
SDA_FPGA
U19
VCC
SCL
SDA
A0
A1
A2
RST
GND
TCA9548APWR
C113 0.1UF
R93 4.99k
R94 4.99k
R95 4.99k
I2C_SW_RST* 3
SC0 SD0
SC1 SD1
SC2 SD2
SC3 SD3
SC4 SD4
SC5 SD5
SC6 SD6
SC7 SD7
R83 4.7K
R84 4.7K
R85 4.7K
R86 4.7K
R87 4.7K
R88 4.7K
R89 4.7K
R90 4.7K
TP38 TP39 TP40 TP41 TP42 TP43 TP44 TP45
TP33 TP32 TP31 TP30 TP34 TP35 TP890 TP880
R96 4.7K
R97 4.7K
R98 4.7K
R99 4.7K
R100 4.7K
R101 4.7K
R102 4.7K
R103 4.7K
SCL0 SDA0
SCL1 SDA1
SCL2 SDA2
SCL3 SDA3
SCL4 SDA4
SCL5 SDA5
SCL6 SDA6
SCL7 SDA7
FMC.SCL0
FMC.SDA0
FMC.SCL1
FMC.SDA1
FMC.SCL2
FMC.SDA2
FMC.SCL3
FMC.SDA3
FMC.SCL4
FMC.SDA4
FMC.SCL5
FMC.SDA5
FMC.SCL6
FMC.SDA6
FMC.ACLK_SFP_SCL
FMC.ACLK_SFP_SDA
FMC.SCL_FPGA
FMC.SDA_FPGA
TP21
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HIGH ENERGY PHYSICS
209 S 33rd Street
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Design Title: GPS Interface Board
Schematic Title: 06. Utilities
Page Title: 12. Level Translators
Size B
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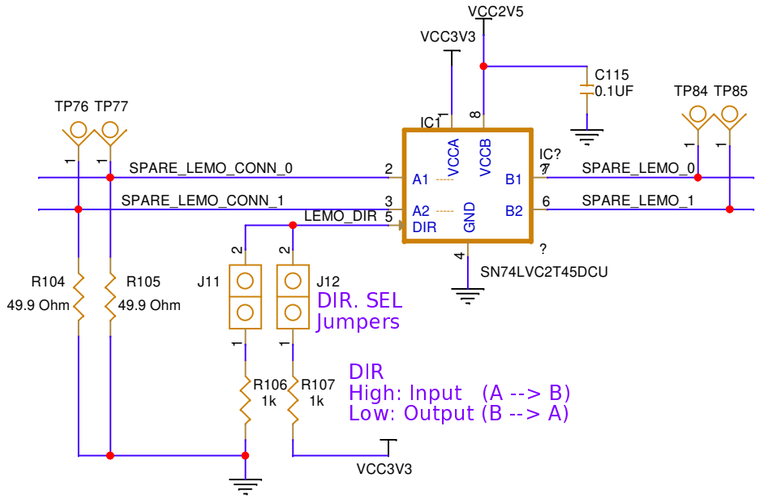
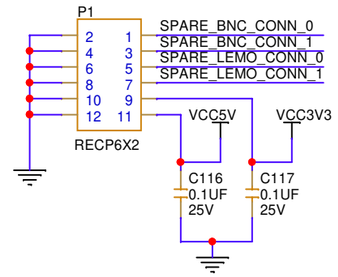
SPARE I/O
LEMO





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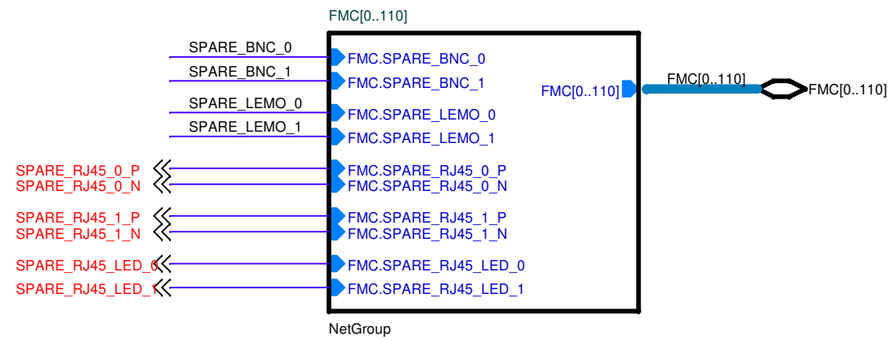
to BNC & LEMO



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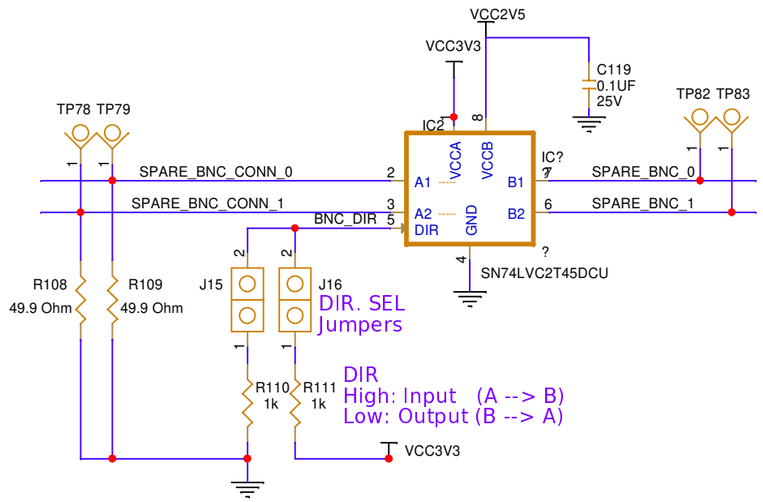
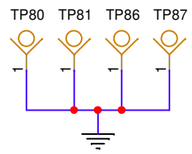
BNC





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Schematic Title:	06. Utilities
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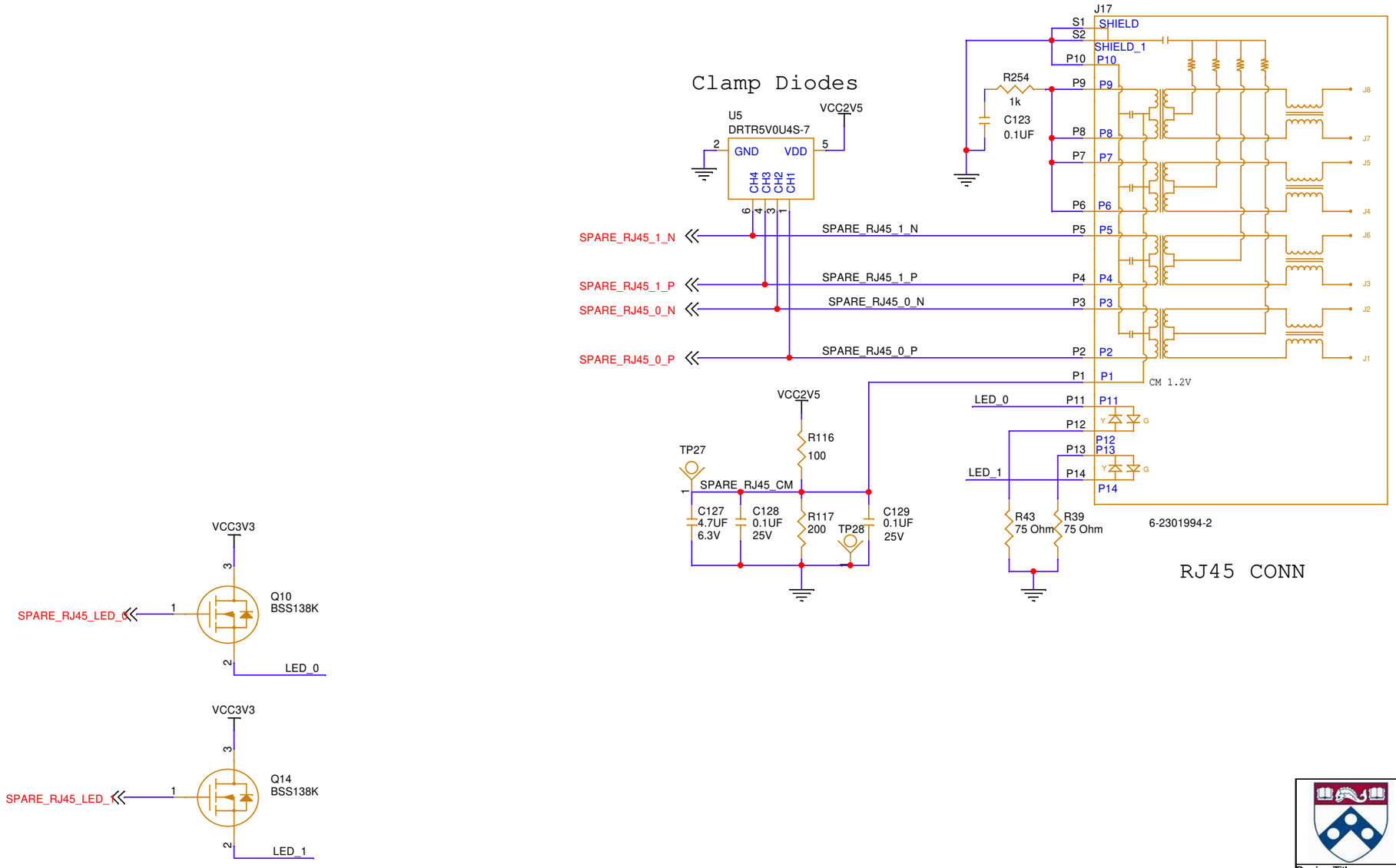

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Design Title:	GPS Interface Board
Schematic Title:	06. Utilities
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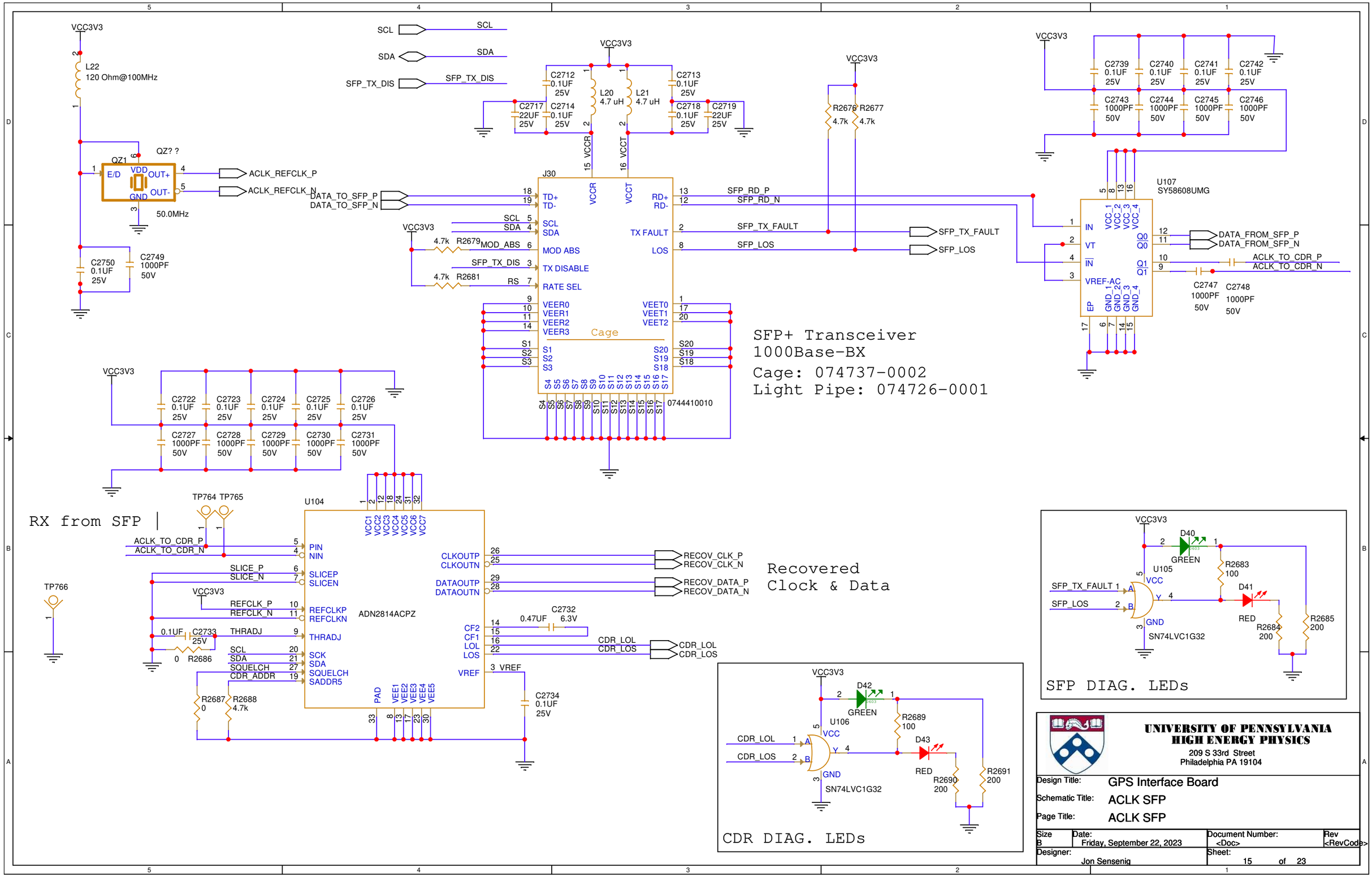
SFP+ Transceiver
1000Base-BX
Cage: 074737-0002
Light Pipe: 074726-0001
RX from SFP
Recovered
Clock & Data
SFP DIAG. LEDs
CDR DIAG. LEDs
J30
Cage
0744410010
U107
SY58608UMG
U104
ADN2814ACPZ
U105
U106
SN74LVC1G32
VCC3V3
L22
120 Ohm@100MHz
QZ1
QZ? ?
50.0MHz
ACLK_REFCLK_P
ACLK_REFCLK_N
DATA_TO_SFP_P
DATA_TO_SFP_N
SFP_RD_P
SFP_RD_N
SFP_TX_FAULT
SFP_LOS
DATA_FROM_SFP_P
DATA_FROM_SFP_N
ACLK_TO_CDR_P
ACLK_TO_CDR_N
RECOV_CLK_P
RECOV_CLK_N
RECOV_DATA_P
RECOV_DATA_N
CDR_LOL
CDR_LOS
SCL
SDA
SFP_TX_DIS
MOD_ABS
RS
SLICE_P
SLICE_N
REFCLK_P
REFCLK_N
THRADJ
SQUELCH
CDR_ADDR
TP764
TP765
TP766
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Page Title: ACLK SFP
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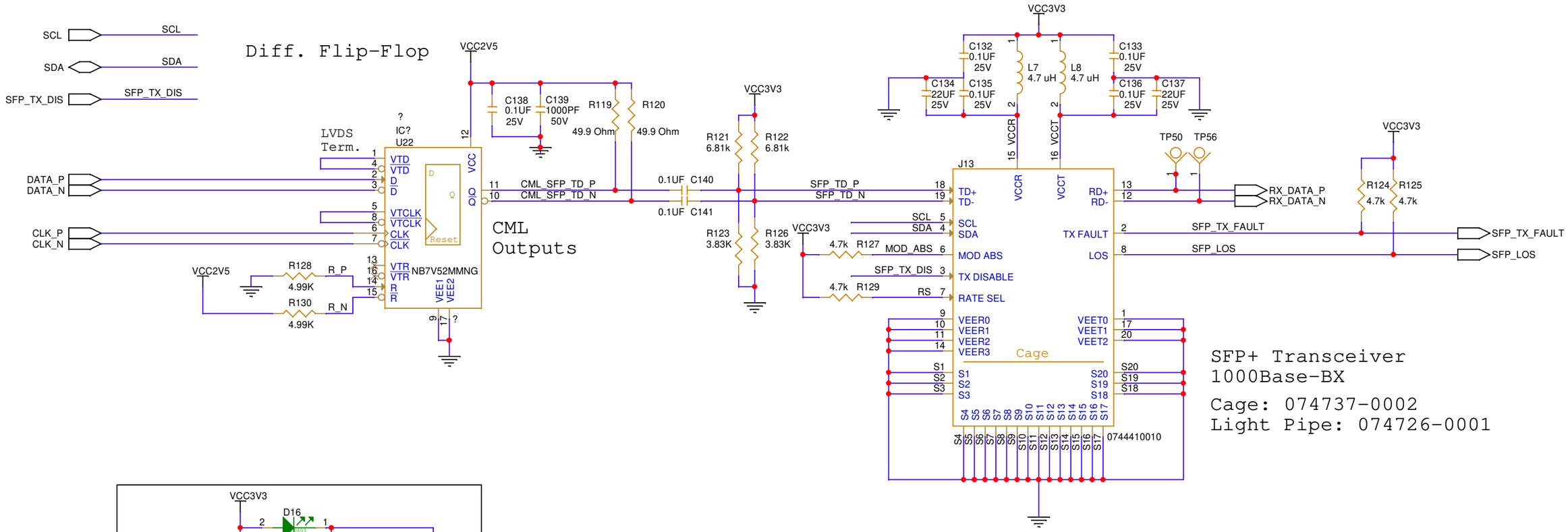

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Schematic Title:	SFP Block
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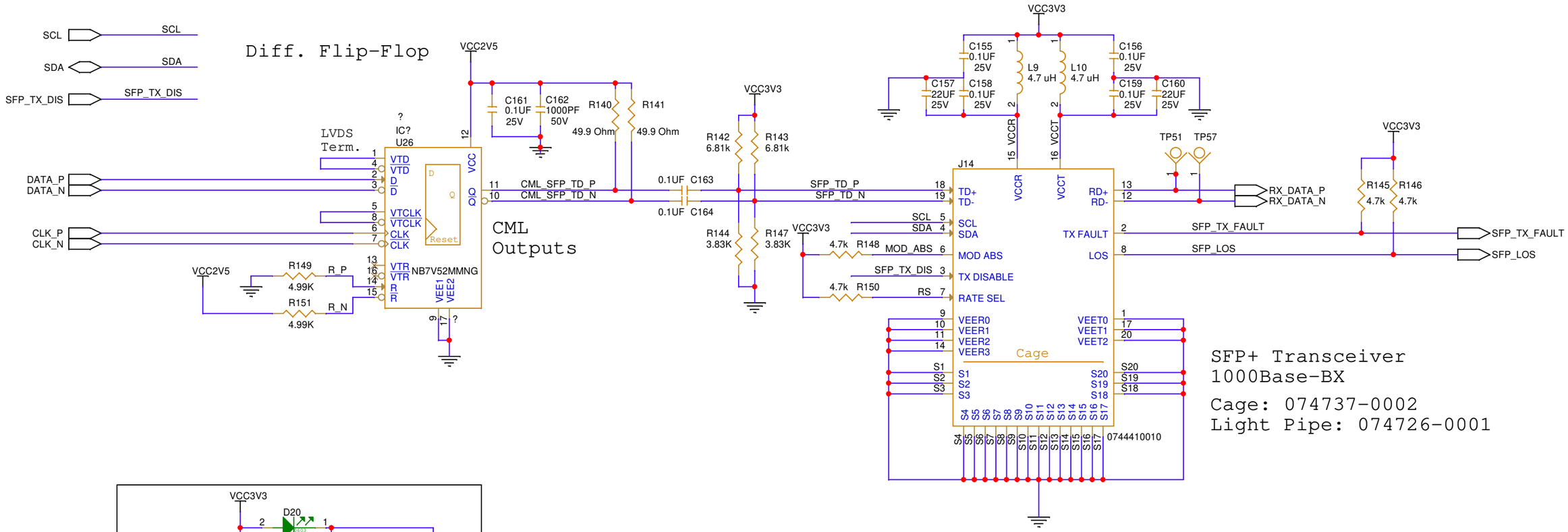

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Page Title:	SFP

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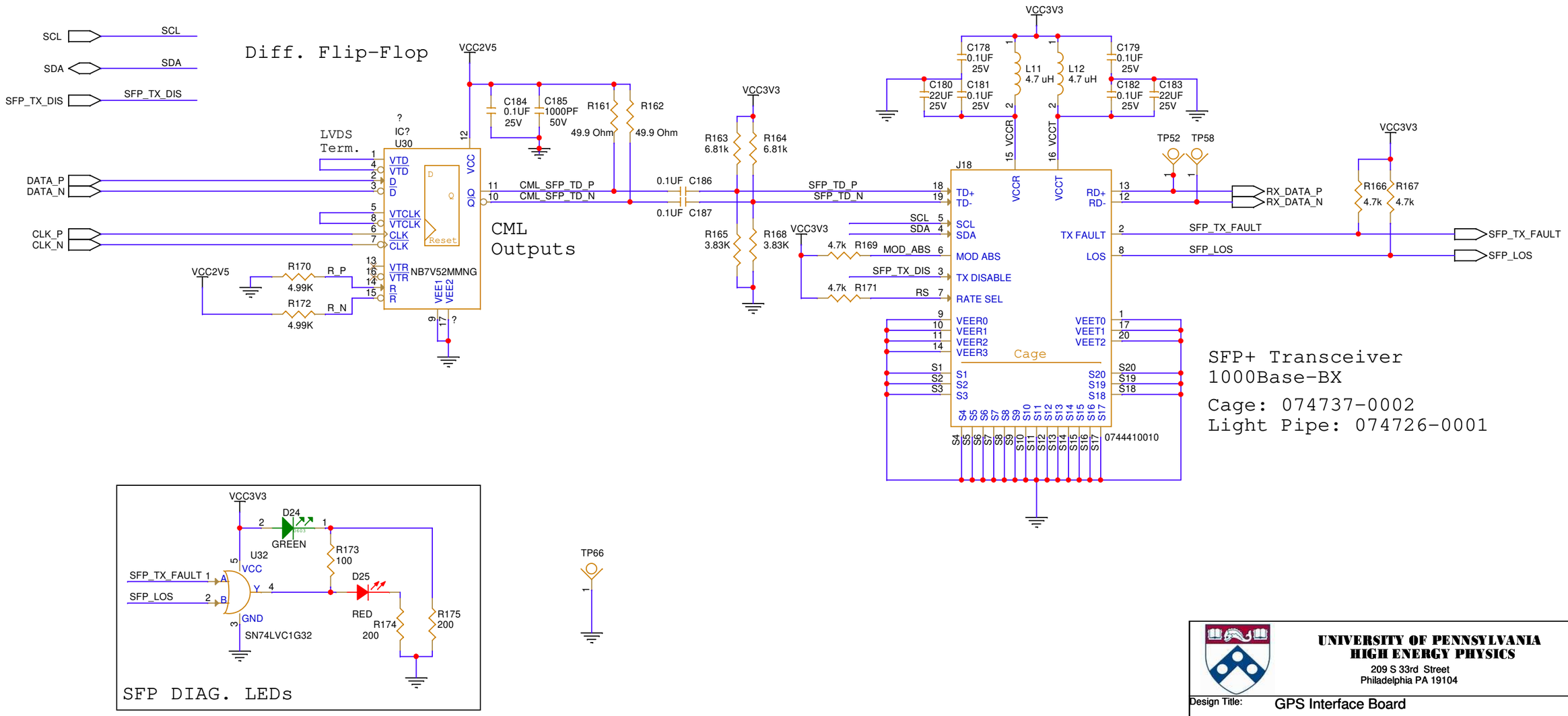

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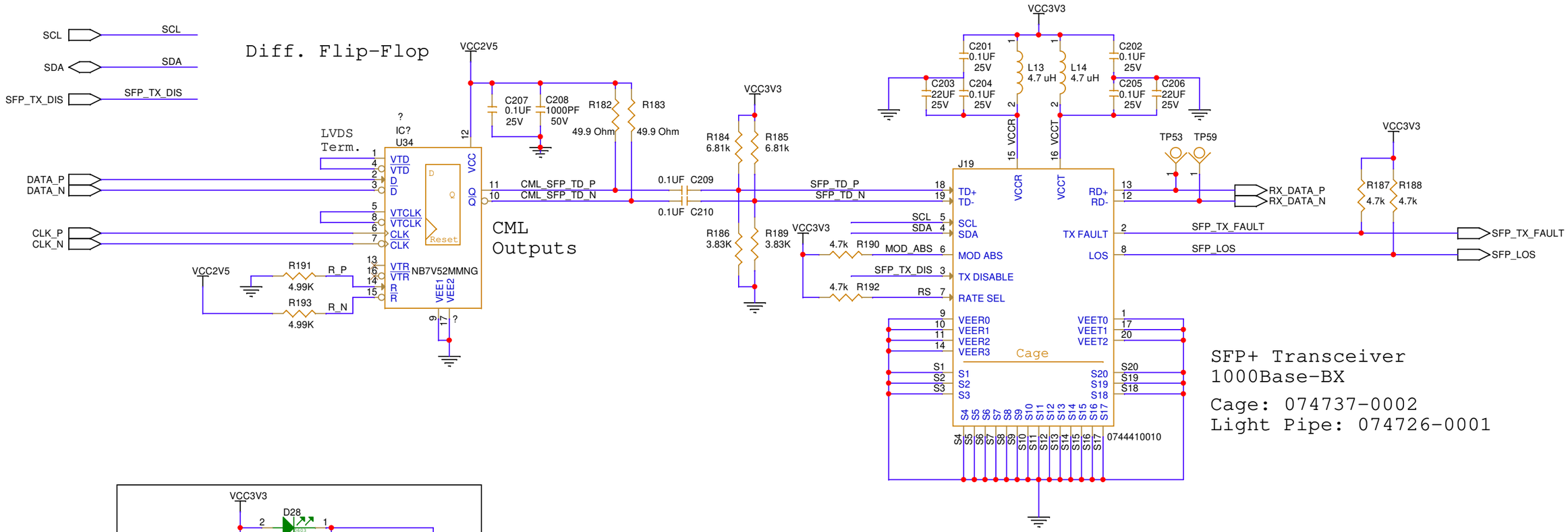

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Design Title:	GPS Interface Board
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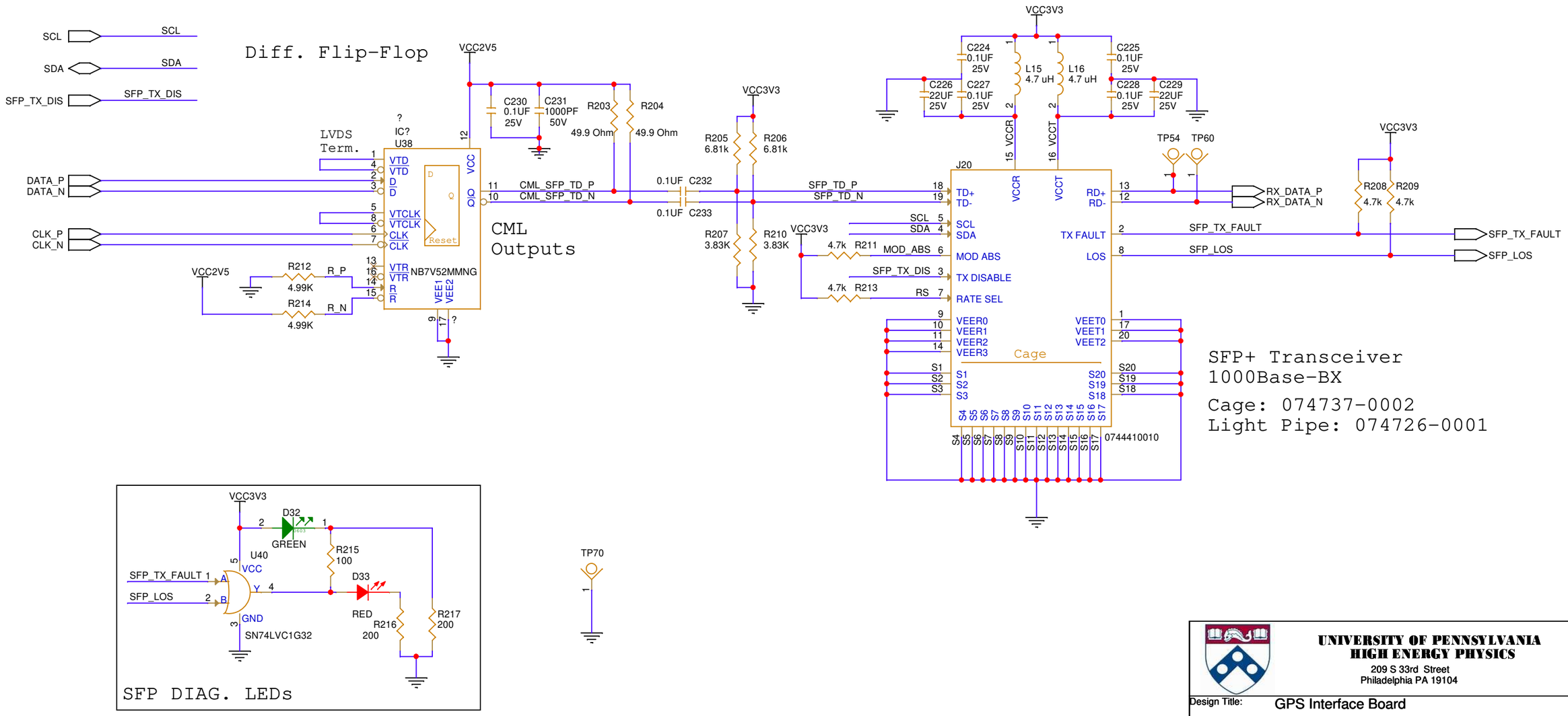

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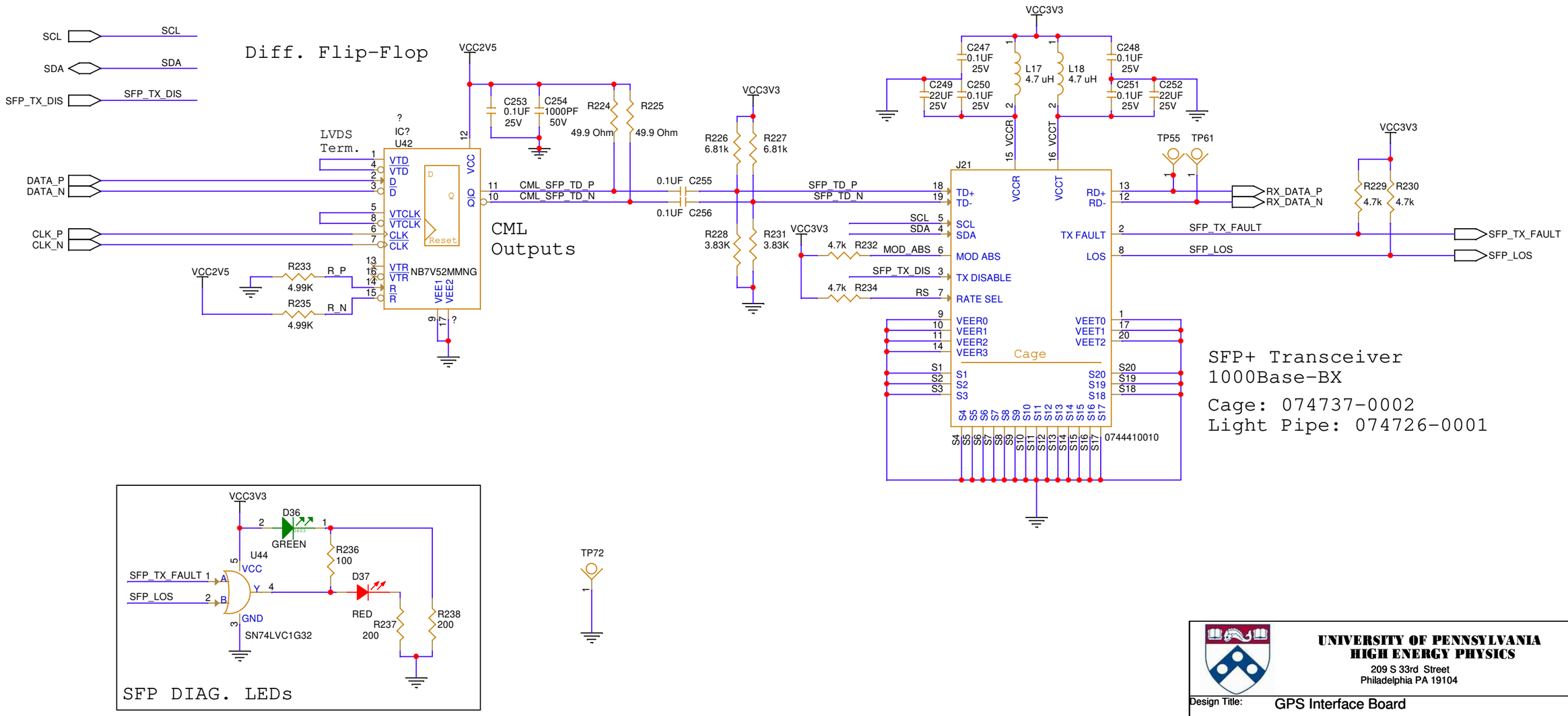

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Schematic Title:	SFP Block
Page Title:	SFP

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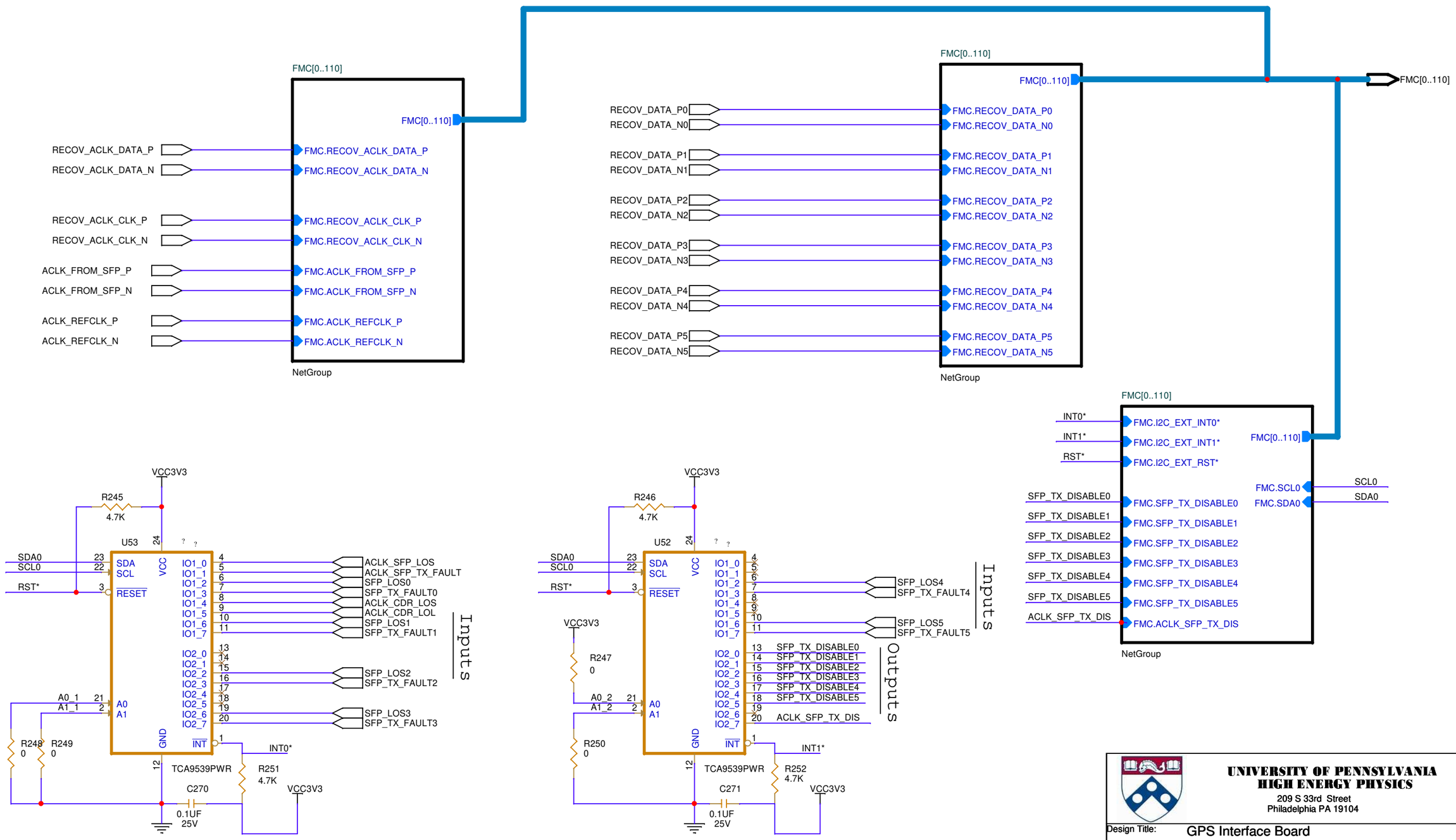

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Design Title:	GPS Interface Board
Schematic Title:	SFP Fan-in
Page Title:	Fan-In and I2C Extender

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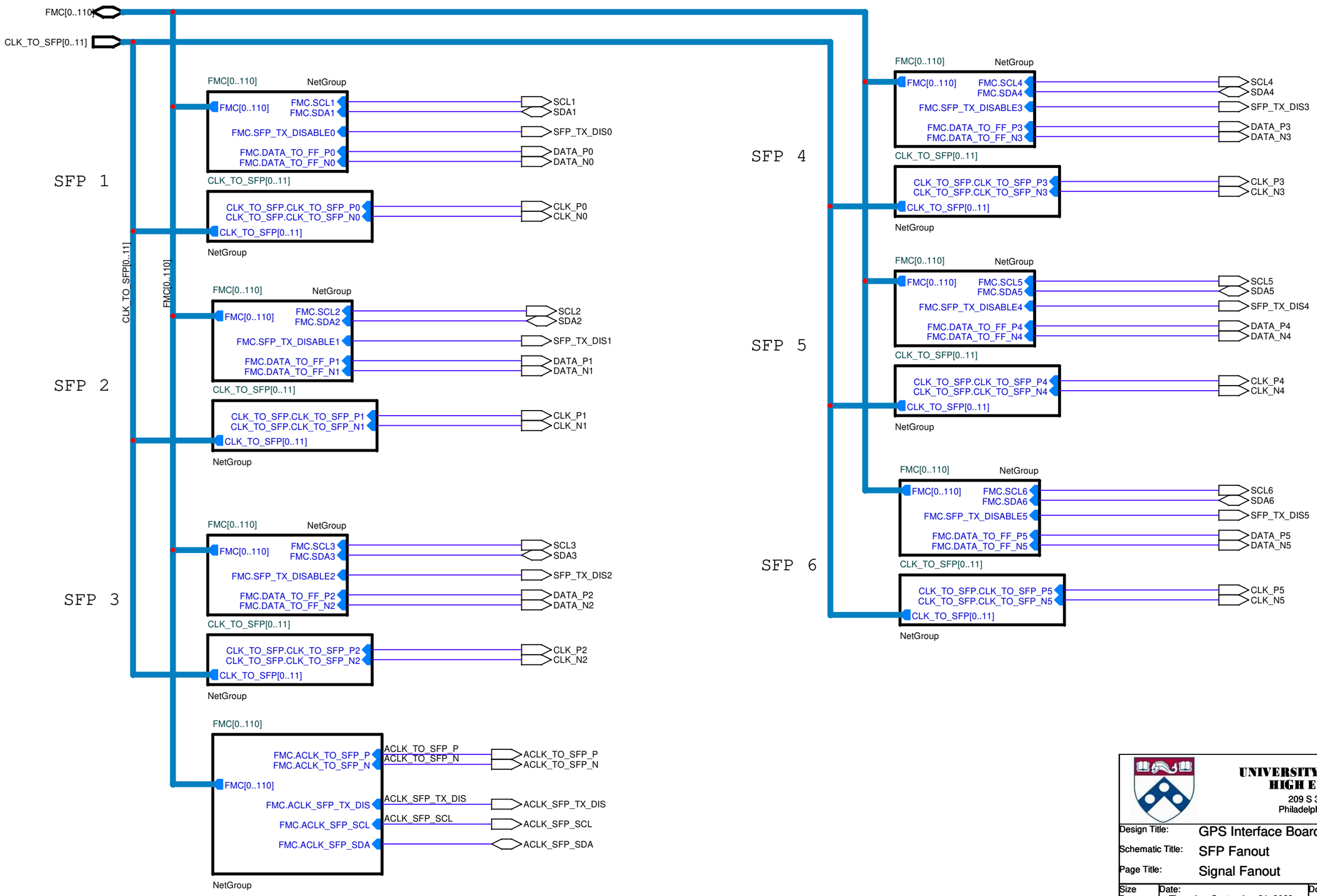

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Design Title:	GPS Interface Board
Schematic Title:	SFP Fanout
Page Title:	Signal Fanout

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