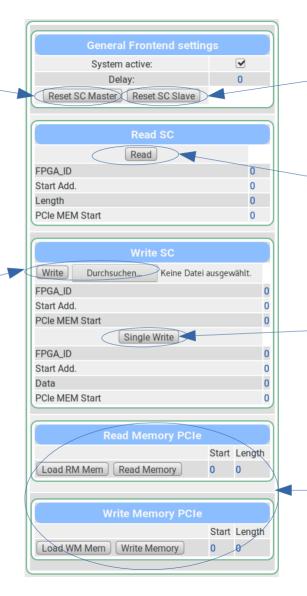
Resets the SC Master.
This part of the firmware
checks if there is a SC command
in the PCIe Write Memory. It will look a
address 0 for the start word 0xBAD and
will then loop until the stop word 0x9c.
Then it will wait at address
0 + length until 0x9c. The reset sets it
back to address 0.

With this one can send a write sc command to the FEB for multi address. First upload a .csv file with the data in decimal for each address starting from The start add. An example is in switching\_pc/midas\_fe/test\_sc.csv FPGA\_ID: 0 means send via all channels. At the moment let it at 0.

Start Add.: set the start address for the ram on the FEB PCIe MEM Start: Address for the PCIe write Memory on the Arria10



Resets the SC Slave.
This part of the firmware
checks if there is a SC command
on the link and it will write it to the
PCIe Read Memory. At the moment
this feature is not fully running.

With this one can send a read sc command to the FEB.
FPGA\_ID: 0 means send via all channels.
At the moment let it at 0.
Start Add.: set start address for the ram on the FEB
Length: Set length for ram on FEB
PCIe MEM Start: Address for the PCIe write Memory on the Arria10

With this one can send a single write sc command to the FEB.

FPGA\_ID: 0 means send via all channels.
At the moment let it at 0.

Start Add.: set address for the ram on the FEB

Data: data in decimal

PCIe MEM Start: Address for the PCIe write Memory on the Arria10

One can read the PCIe read and write
Memory of the Arria10 board with
this section. First specify the start address
And length then click read memory
And the load mem.