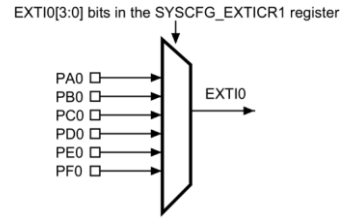
1. Why can't you use both pins PA0 and PC0 for external interrupts at the same time?

Because PA0 and PC0 are multiplexed in the SYSCFG_EXTICR1 register



2. What software priority level gives the highest priority? What level gives the lowest?

3 is the lowest priority and 0 is the highest priority.

3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?

Each register (IPR0-IPR7) has four 8-bit regions, including non-implemented bits. The upper two bits from the regions are implemented.

4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.

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5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?

If it isn't cleared, the handler will loop because the interrupt request was never acknowledged.