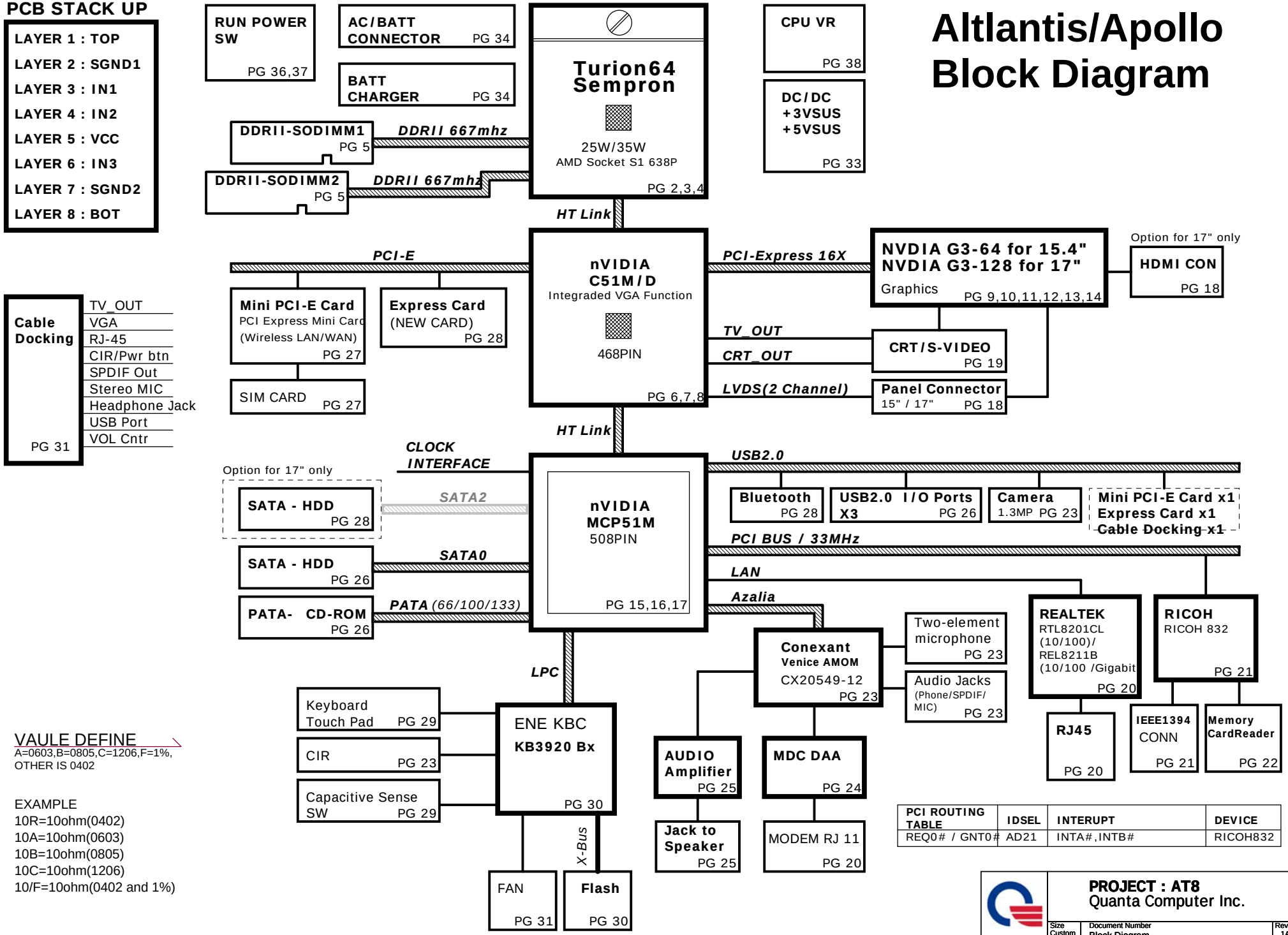
Altlantis/Apollo Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

VAULE DEFINE
A=0603,B=0805,C=1206,F=1%,
OTHER IS 0402

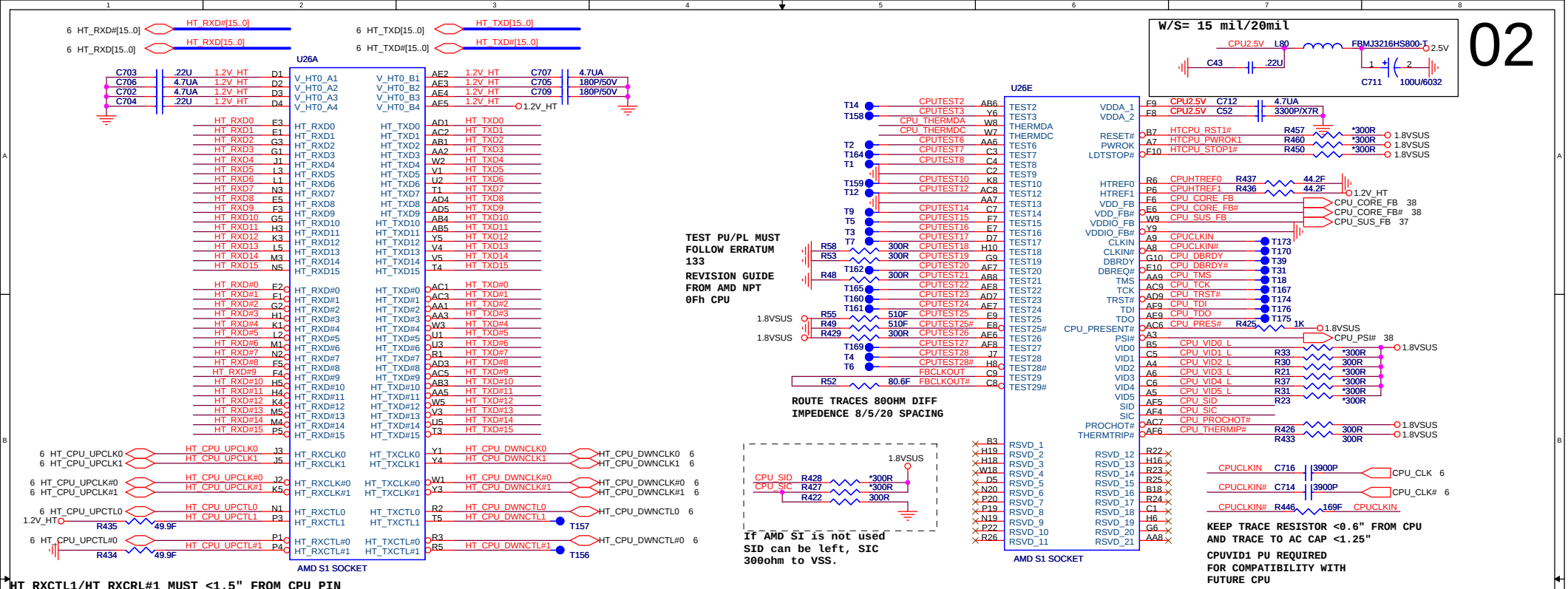
EXAMPLE
10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10/F=10ohm(0402 and 1%)

NB5/RD2/HW1

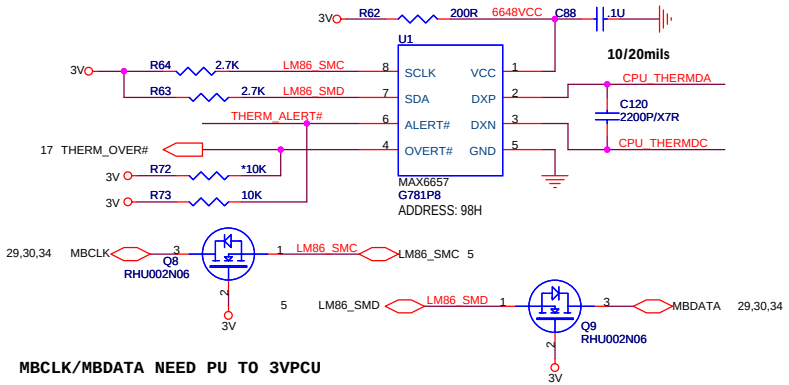
PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Wednesday, June 14, 2006 Sheet 1 of 39

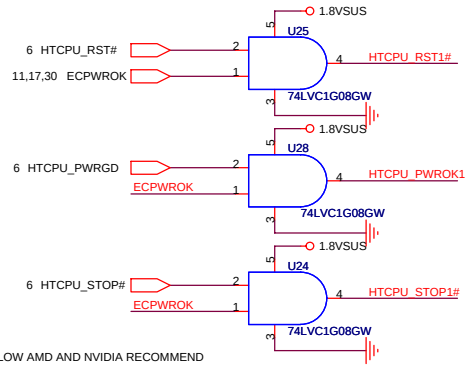


CPU THERMAL SENSOR & CONTROL

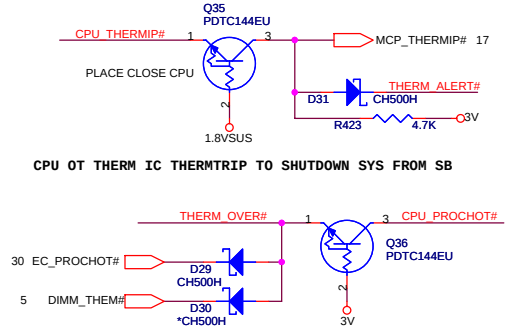


MUST KEEP LOW DURING S3-S5 TO MEET HT IO LINK SPEC

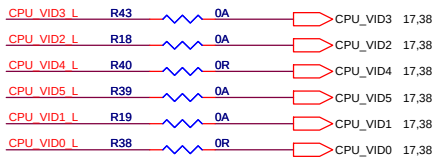
HT LINK CONTROL LEVEL SHIFTER



OVER TEMP CONTROL



NEED TO CONFIRM NVIDIA FOR THE USAGE CONNECTION TO SB



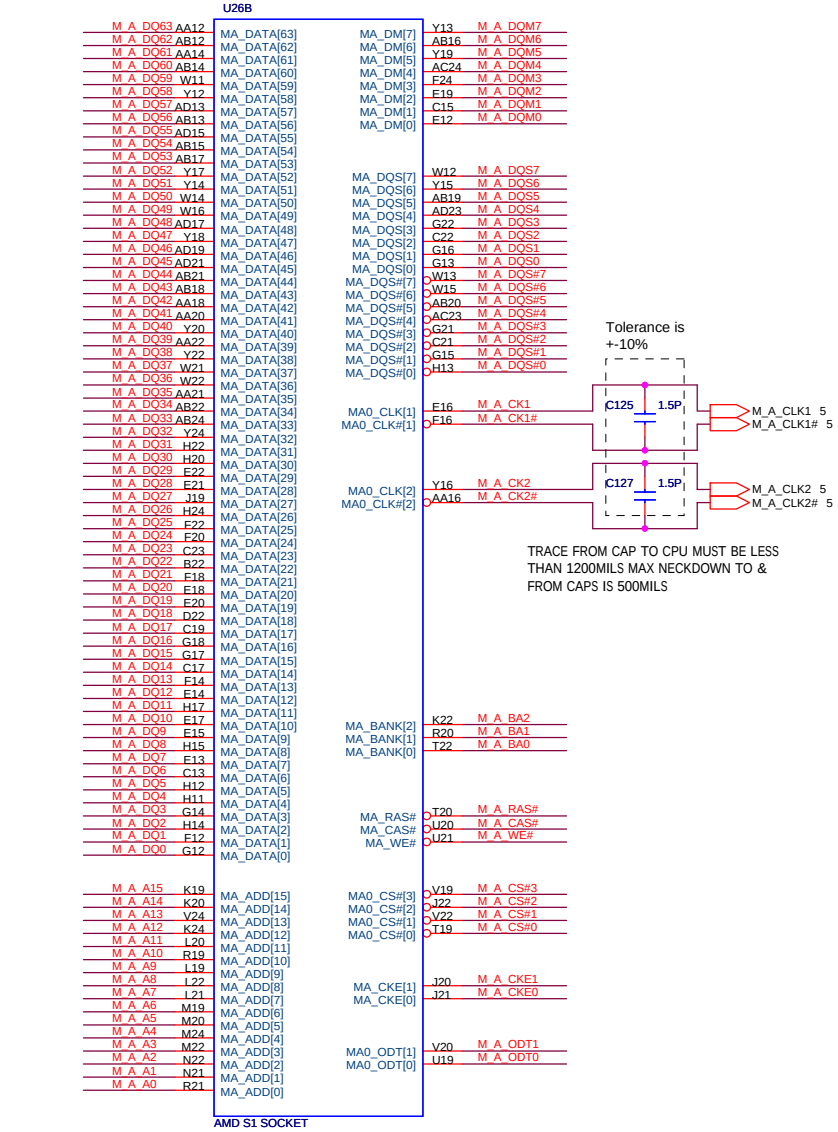
CPU_VID3_L	R43	0A	CPU_VID3	17,38
CPU_VID2_L	R18	0A	CPU_VID2	17,38
CPU_VID4_L	R40	0R	CPU_VID4	17,38
CPU_VID5_L	R39	0A	CPU_VID5	17,38
CPU_VID1_L	R19	0A	CPU_VID1	17,38
CPU_VID0_L	R38	0R	CPU_VID0	17,38

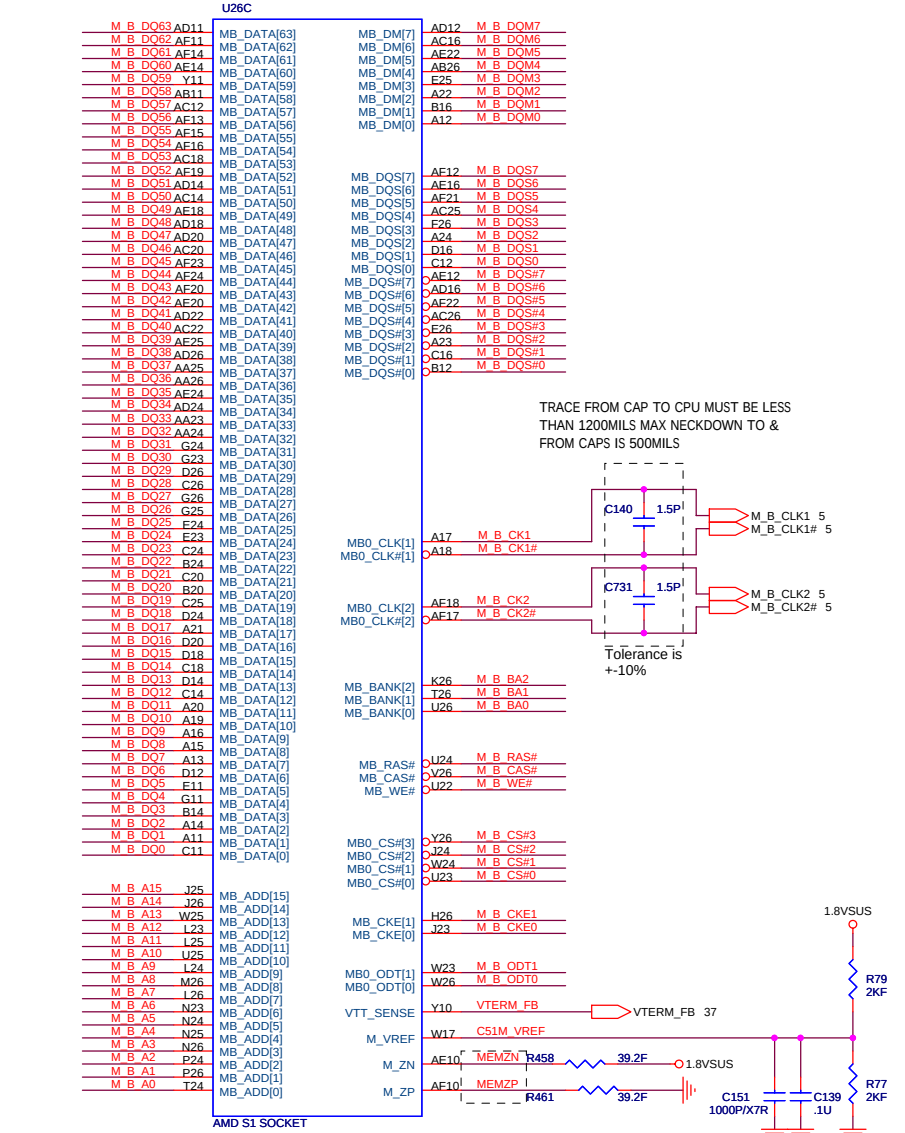
PROJECT : AT8
Quanta Computer Inc.

NB5/RD2/HW1

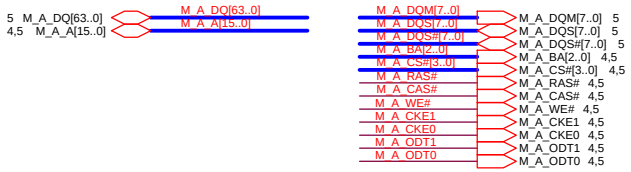
Size	Document Number	Rev
Custom	CPU(HT_LINK /CTL)	2A

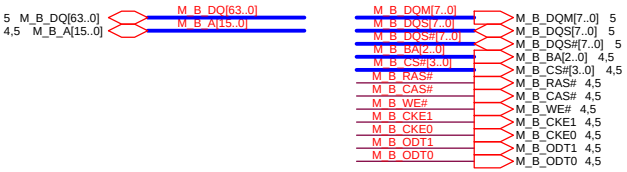
Date: Wednesday, June 14, 2006 | Sheet 2 of 39





C51MVREF : W =20MIL AND SPACE = 20MIL





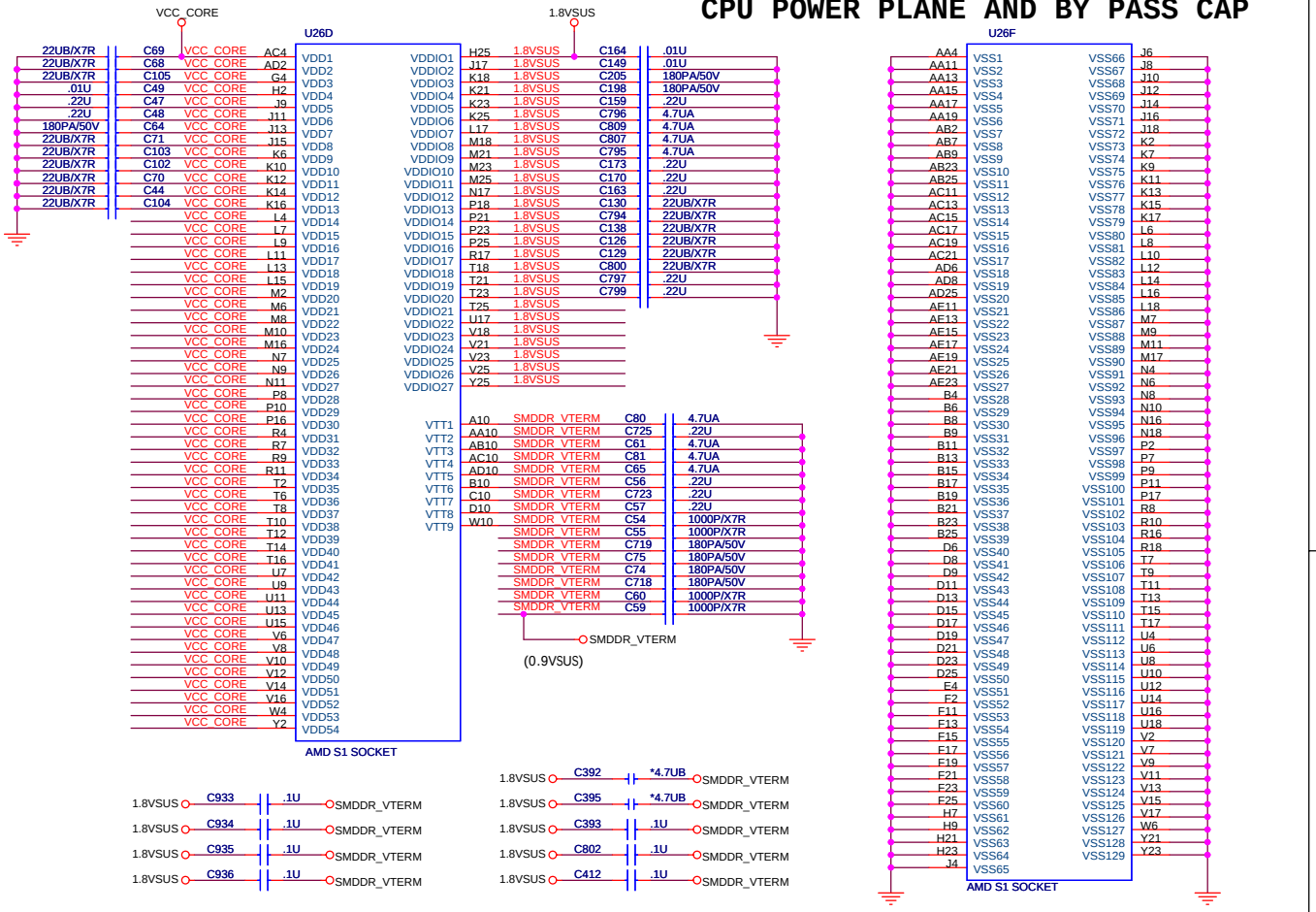
PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU(MEM/IF)	1A

NB5/RD2/HW1

Date: Wednesday, June 14, 2006 | Sheet 3 of 39

CPU POWER PLANE AND BY PASS CAP

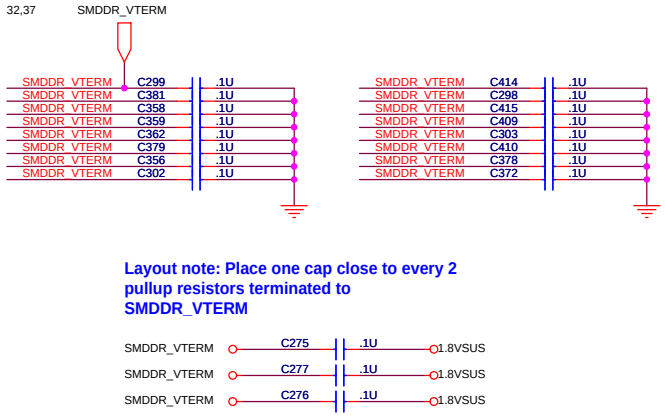


DDR2 TERMINATION BYPASS CAP

04

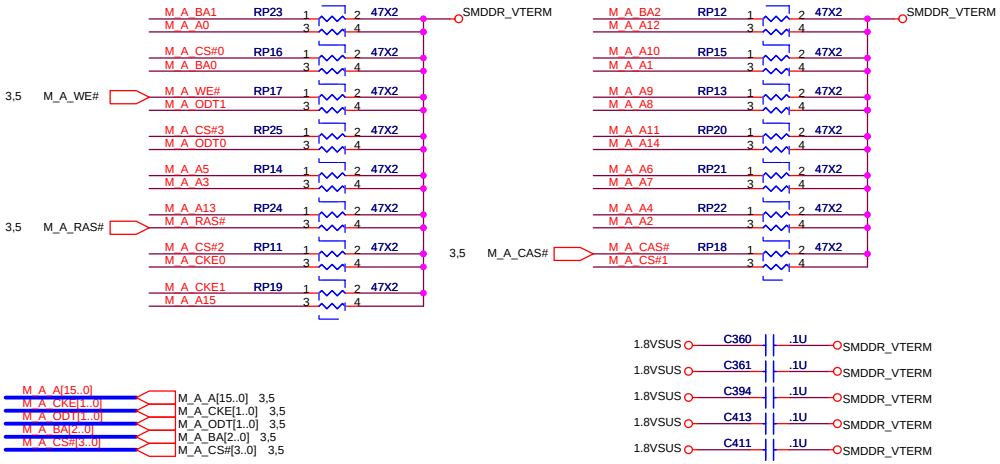
CHANNEL A

CHANNEL B

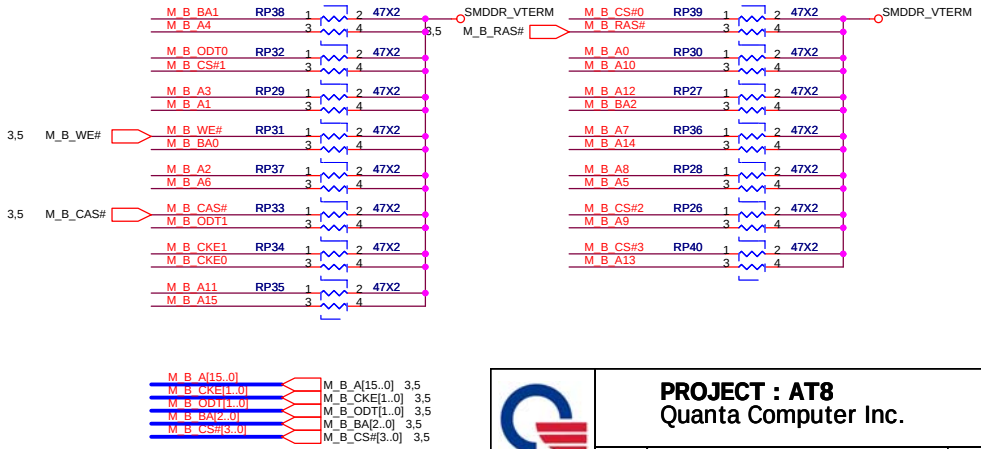


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

DDRII CHANNEL A TERMINATION



DDRII CHANNEL B TERMINATION

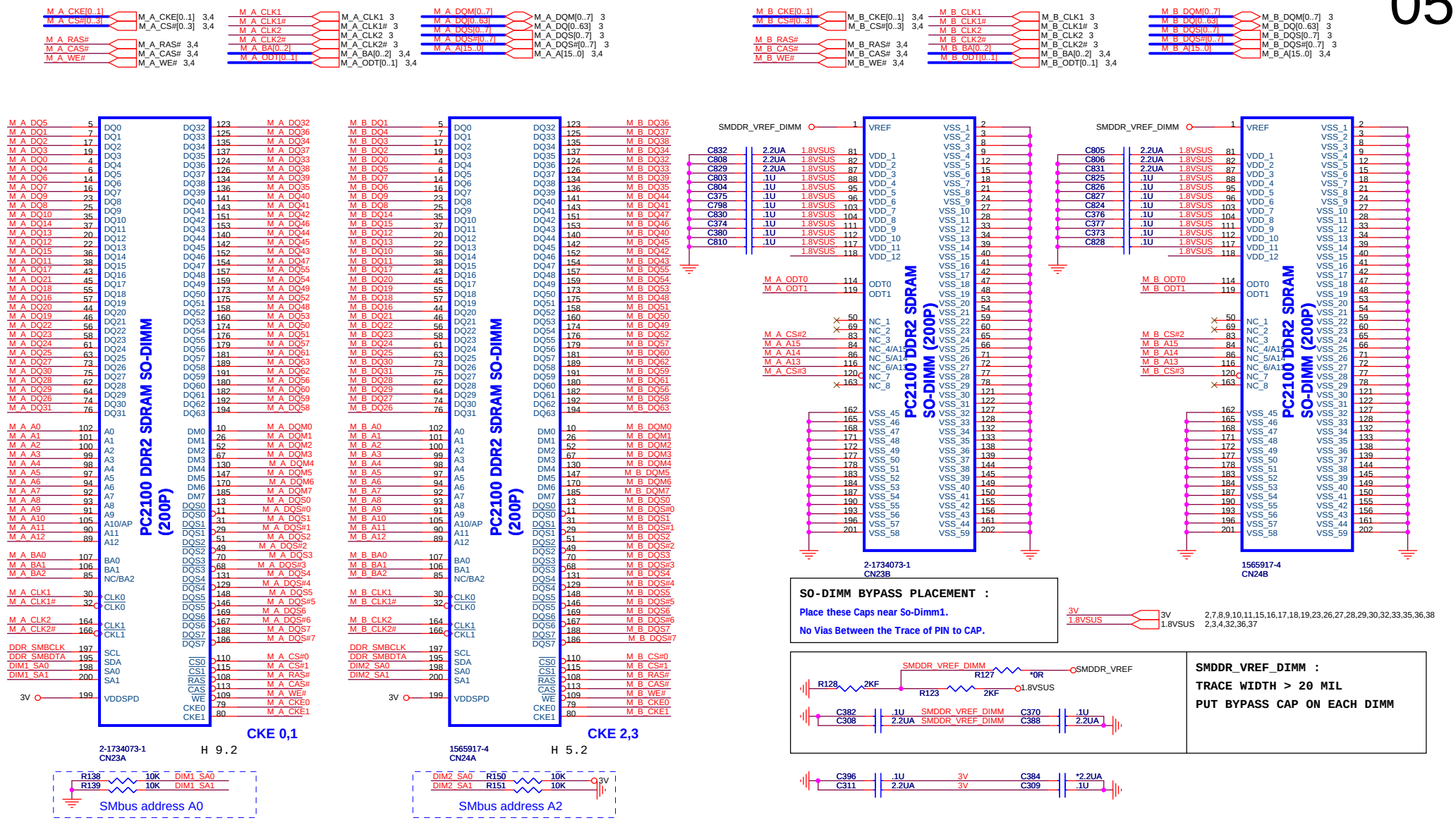


PROJECT : AT8
Quanta Computer Inc.

NB5/RD2/HW1

Size	Document Number	Rev
Custom	CPU(POWER/GND)	1A

Date: Wednesday, June 14, 2006 | Sheet 4 of 39

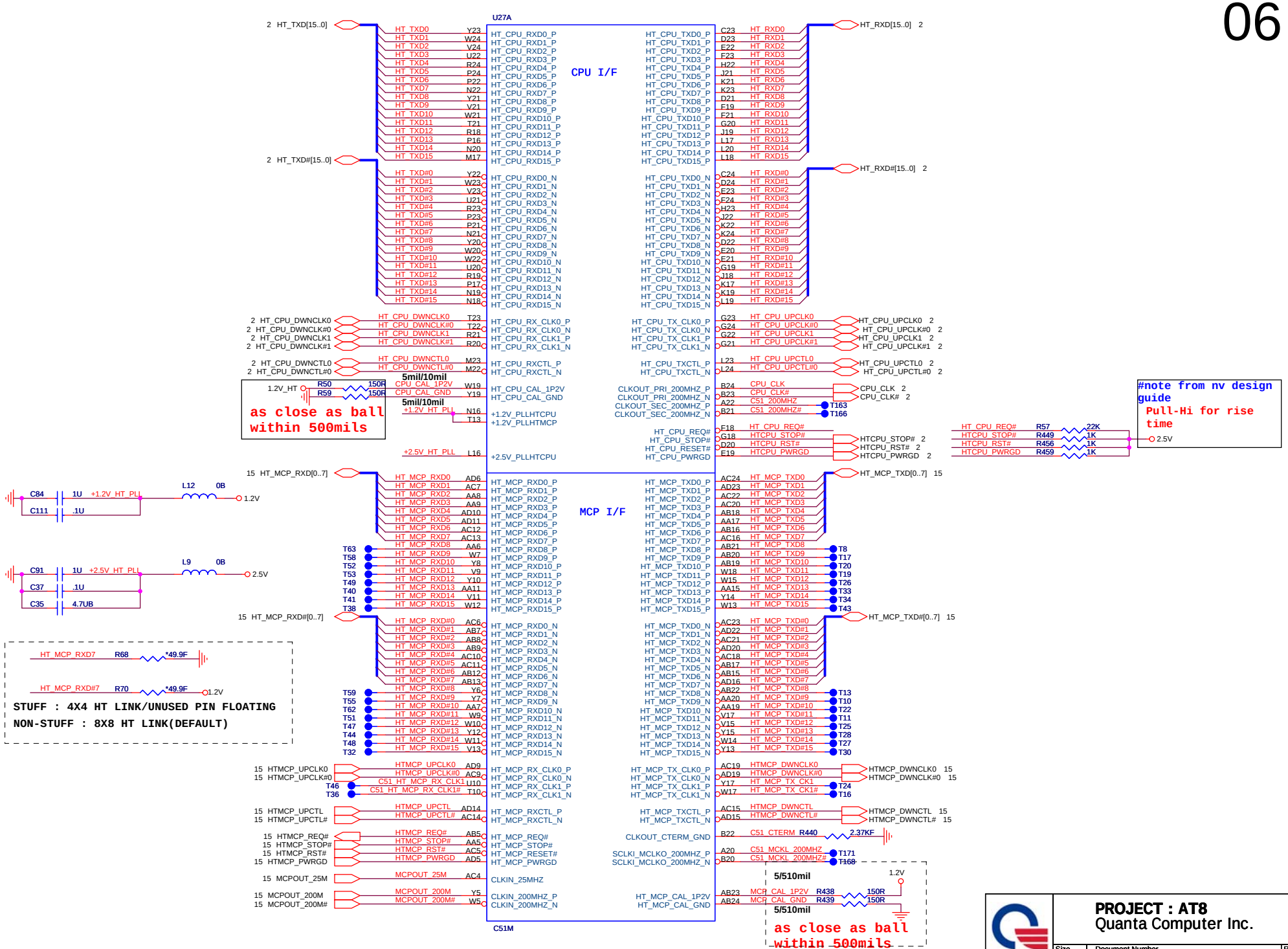


PROJECT : AT8
Quanta Computer Inc.

NB5/RD2/HW1

Size	Document Number	Rev
Custom	CPU(MEM/IF)	2A

Date: Wednesday, June 14, 2006 | Sheet 5 of 39

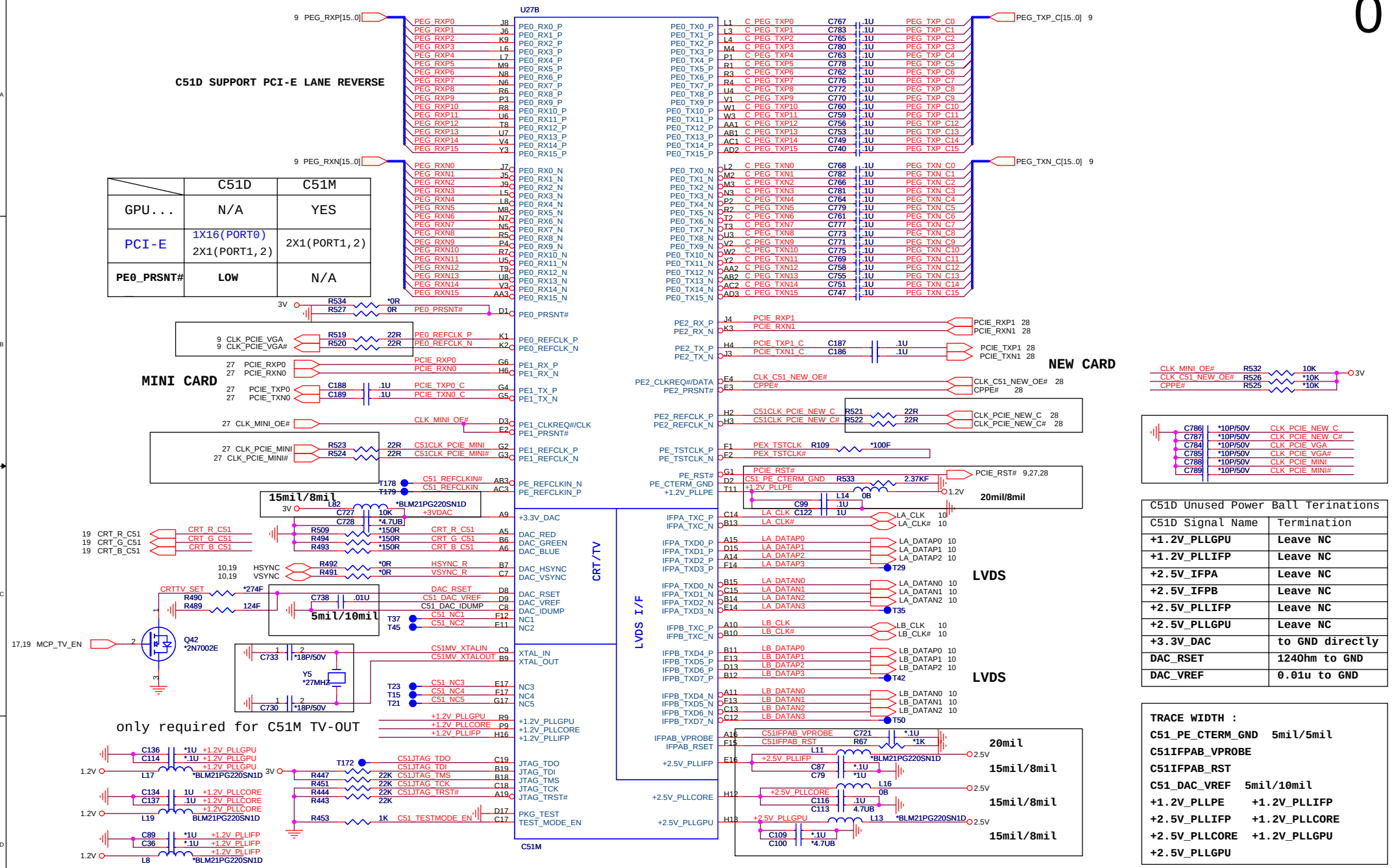


PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	C51MV (HT LINK)	1A

Date: Wednesday, June 14, 2006 | Sheet 6 of 39

NB5/RD2/HW1



	C51D	C51M
GPU...	N/A	YES
PCI-E	1X16(PORT0) 2X1(PORT1,2)	2X1(PORT1,2)
PE0_PRSNT#	LOW	N/A

C51D Unused Power Ball Terinations	
C51D Signal Name	Termination
+1.2V_PLLGPU	Leave NC
+1.2V_PLLIFP	Leave NC
+2.5V_IFPA	Leave NC
+2.5V_IFPB	Leave NC
+2.5V_PLLIFP	Leave NC
+2.5V_PLLGPU	Leave NC
+3.3V_DAC	to GND directly
DAC_RSET	124Ohm to GND
DAC_VREF	0.01u to GND

TRACE WIDTH :
C51_PE_CTERM_GND 5mil/5mil
C51IFPAB_VPROBE
C51IFPAB_RST
C51_DAC_VREF 5mil/10mil
+1.2V_PLLPE +1.2V_PLLIFP
+2.5V_PLLIFP +1.2V_PLLCORE
+2.5V_PLLCORE +1.2V_PLLGPU
+2.5V_PLLGPU

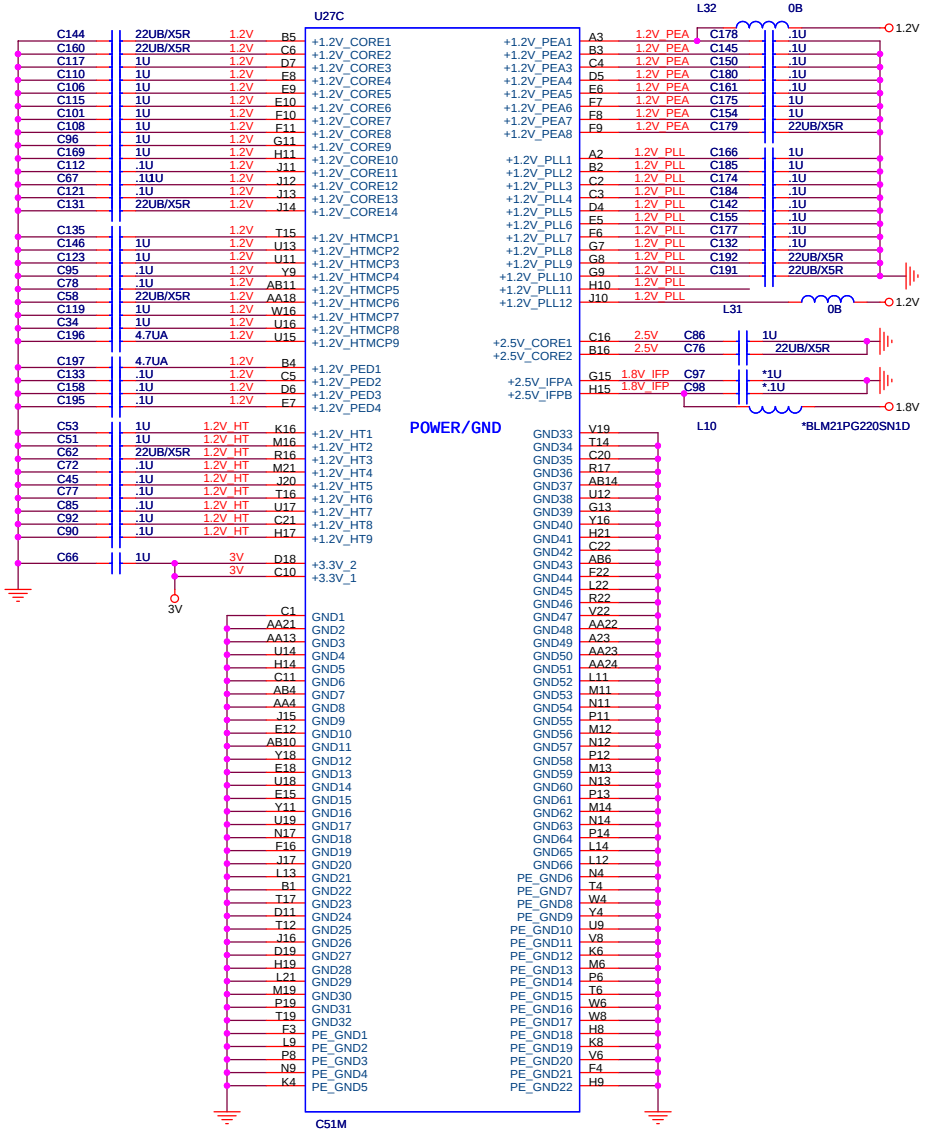
PROJECT : AT8
Quanta Computer Inc.

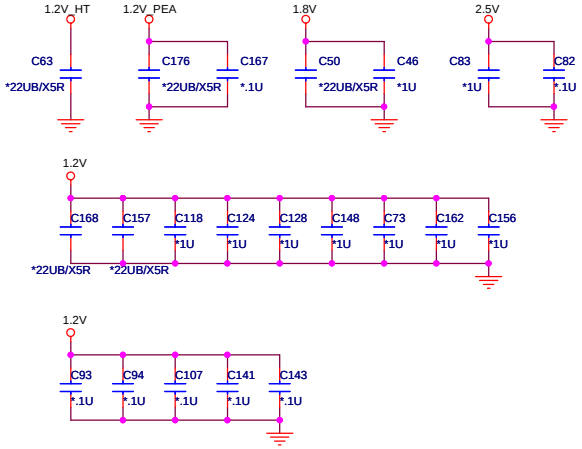
NB5/RD2/HW1

Size	Document Number	Rev
Custom	C51MV (PCIE/LCD/RGB)	1A

Date: Wednesday, June 14, 2006 Sheet 7 of 39

C51M/C51D POWER PLANE/GND & BYPASS



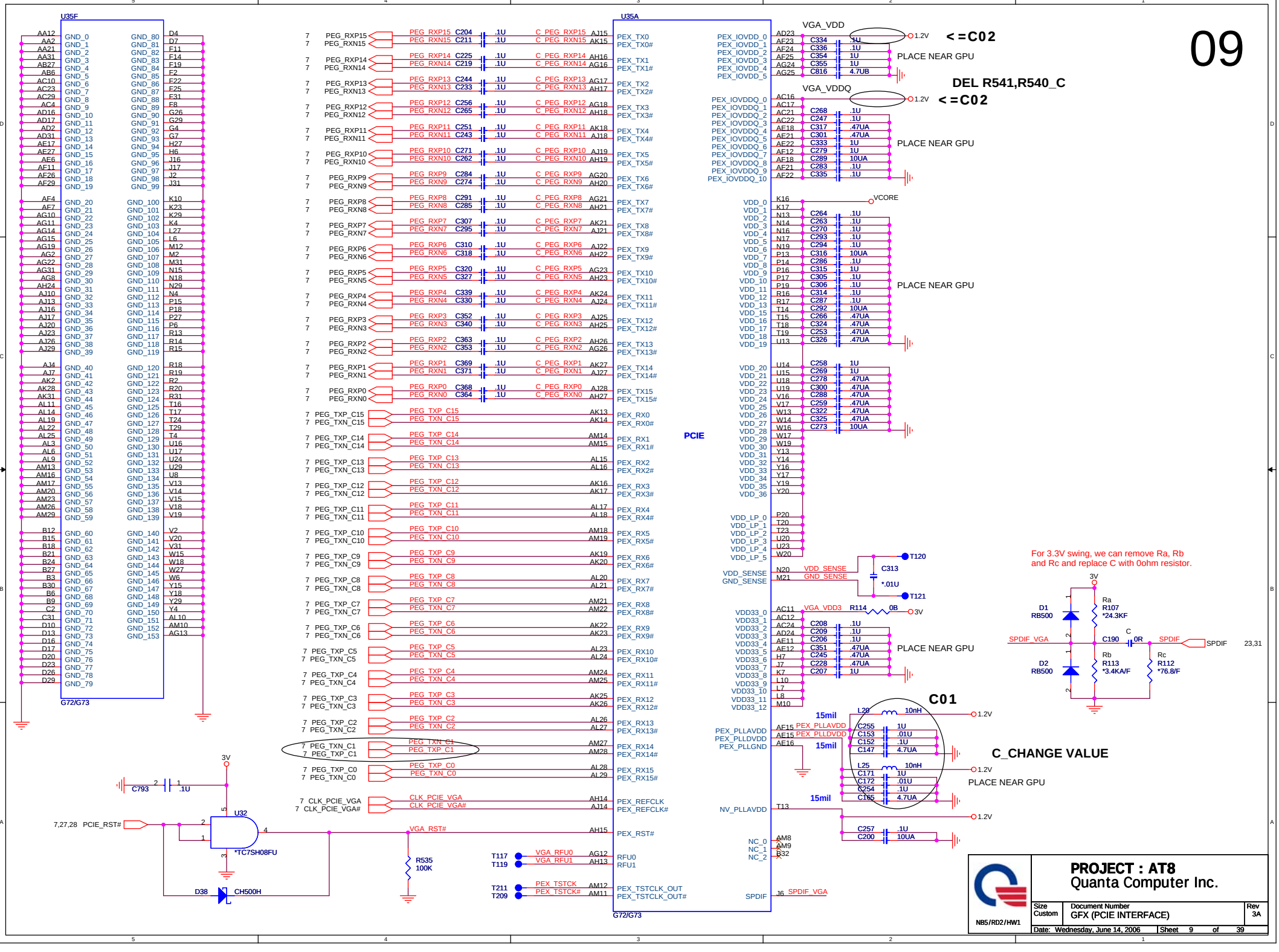


PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	C51MV (POWER/GND)	1A

NB5/RD2/HW1

Date: Wednesday, June 14, 2006 | Sheet 8 of 39


09
U35F
G72/G73
U35A
PCIE
VGA_VDD
1.2V
<=C02
PLACE NEAR GPU
DEL R541,R540_C
VGA_VDDQ
VCORE
VDD_SENSE
GND_SENSE
T120
T121
C313
*.01U
VGA_VDD3
R114
0B
3V
C01
C_CHANGE VALUE
15mil
PEX_PLLAVDD
PEX_PLLDVDD
PEX_PLLGND
NV_PLLAVDD
SPDIF_VGA
SPDIF
For 3.3V swing, we can remove Ra, Rb and Rc and replace C with 0ohm resistor.
D1 RB500
D2 RB500
Ra R107 *24.3KF
Rb R113 *3.4KA/F
Rc R112 *76.8/F
C190 0R
C793 .1U
U32
*TC7SH08FU
7,27,28 PCIE_RST#
VGA_RST#
R535 100K
D38 CH500H
VGA_RFU0
VGA_RFU1
PEX_TSTCK
PEX_TSTCK#
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
CLK_PCIE_VGA
CLK_PCIE_VGA#
PEX_REFCLK
PEX_REFCLK#
PEX_RST#
PROJECT : AT8
Quanta Computer Inc.
Size Custom
Document Number
GFX (PCIE INTERFACE)
Rev 3A
NB5/RD2/HW1
Date: Wednesday, June 14, 2006
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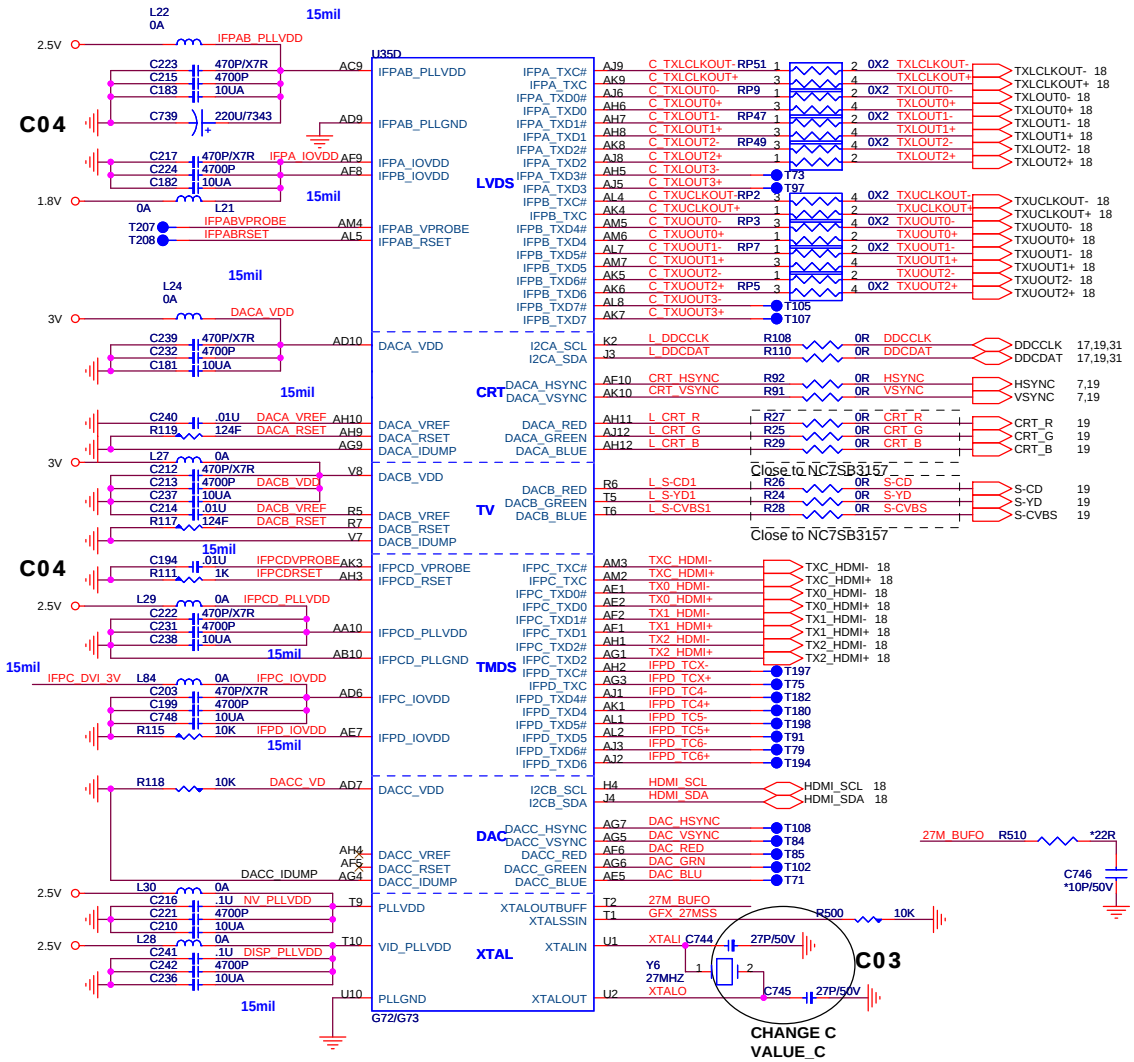
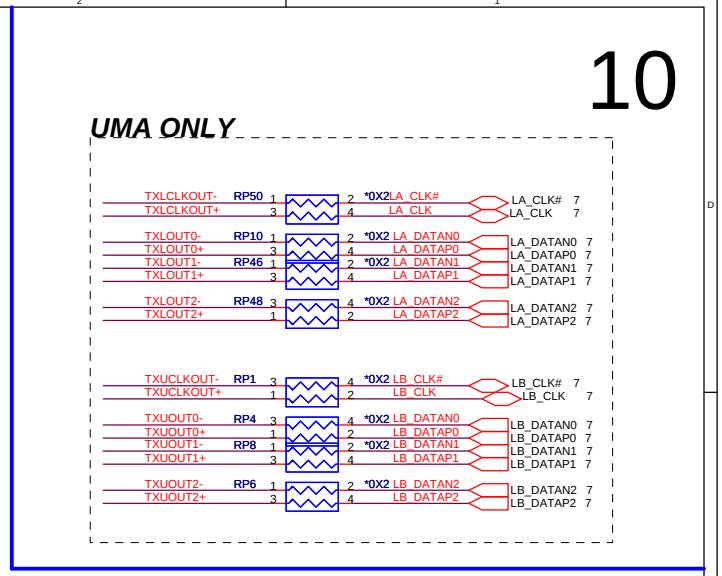
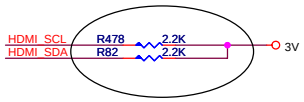
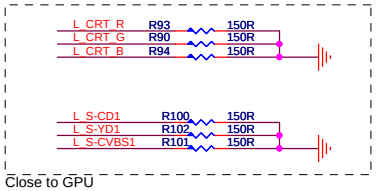


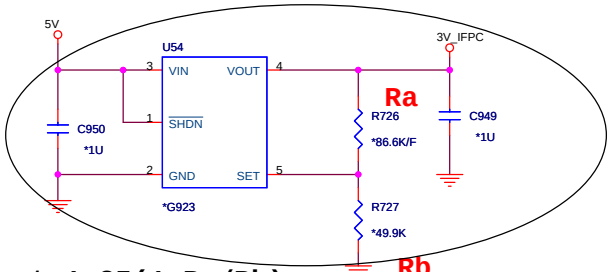




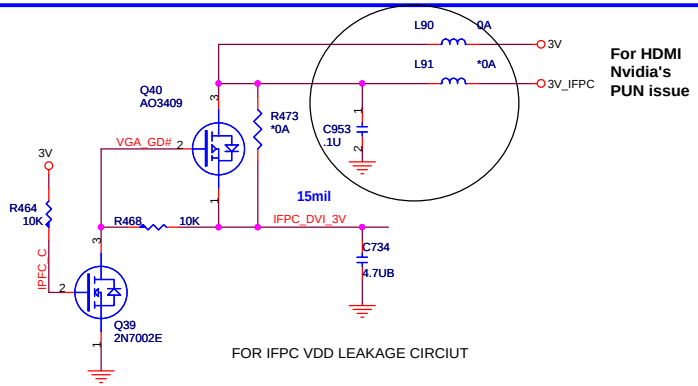
CHANGE DDC bus from 2.2K to 2K

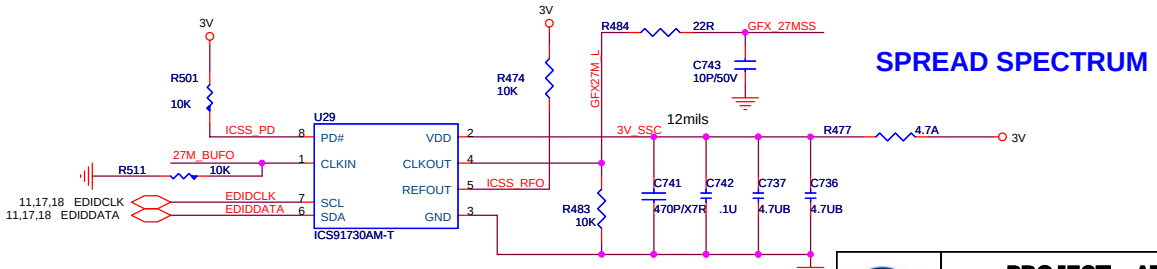


Close to GPU



Vout=1.25(1+Ra/Rb)





I2C ADDRESS: 0xD4H

PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GFX(LVDS, CRT, TV)	2A

NB5/RD2/HW1

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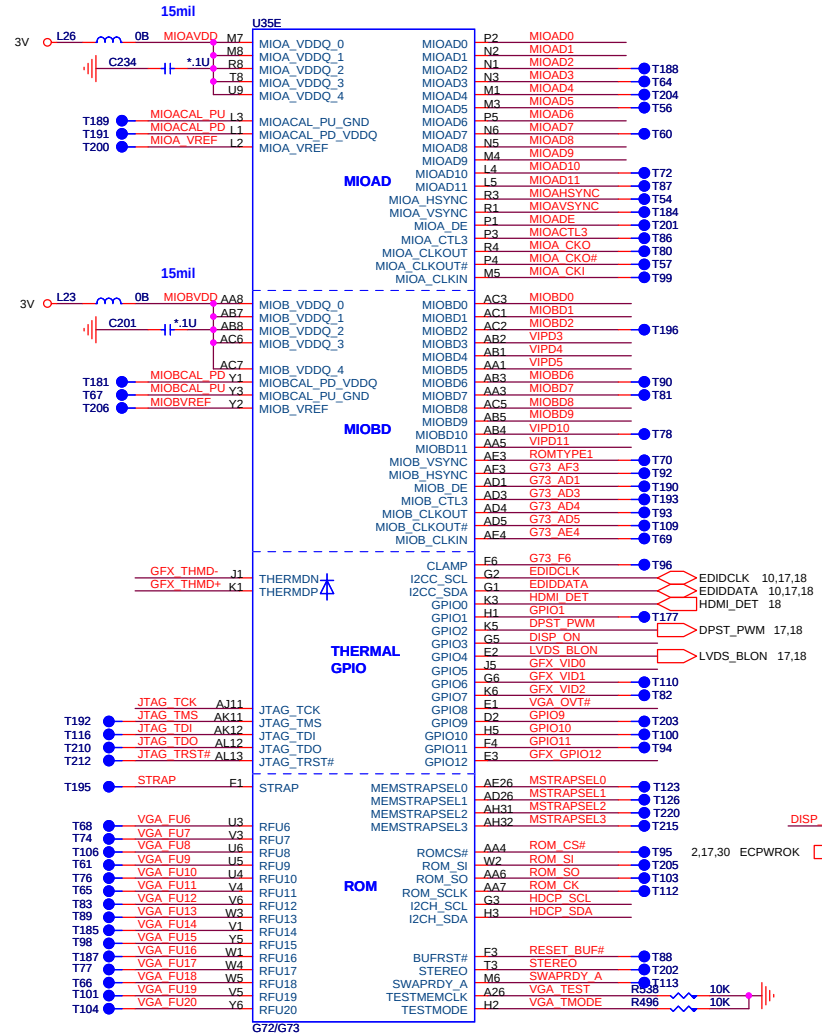
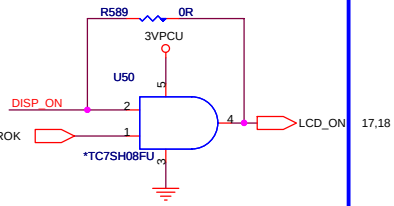
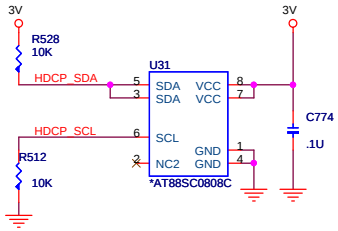


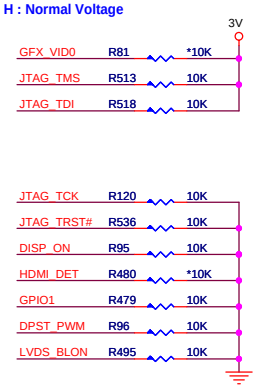


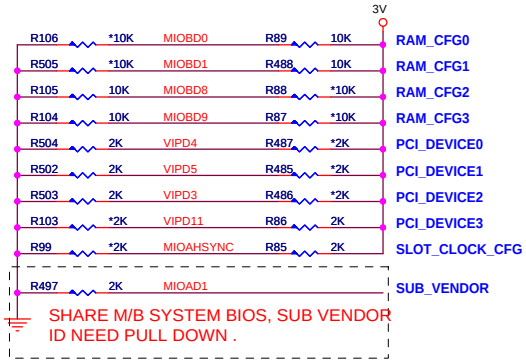


PCI DEVICE

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0111	G72M-V/G73M-V
others	Reserved

GFX_VID0
L : Low Voltage
H : Normal Voltage



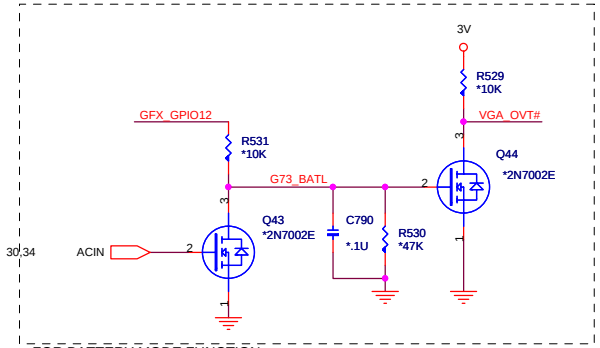


G72M VRAM Configuration Table

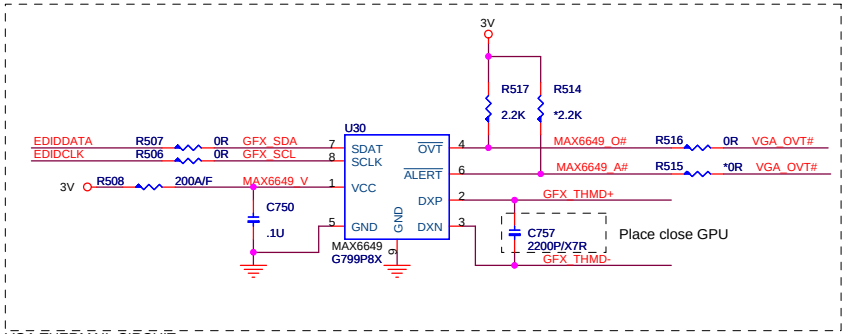
RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

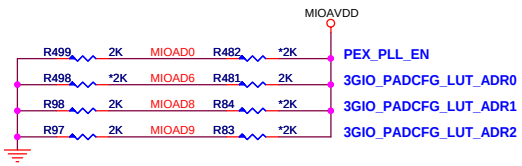
RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



FOR BATTERY MODE FUNCTION
GFX_GPIO12=H ENABLE
GFX_GPIO12=L DISABLE



VGA THERMAIL CIRCUIT



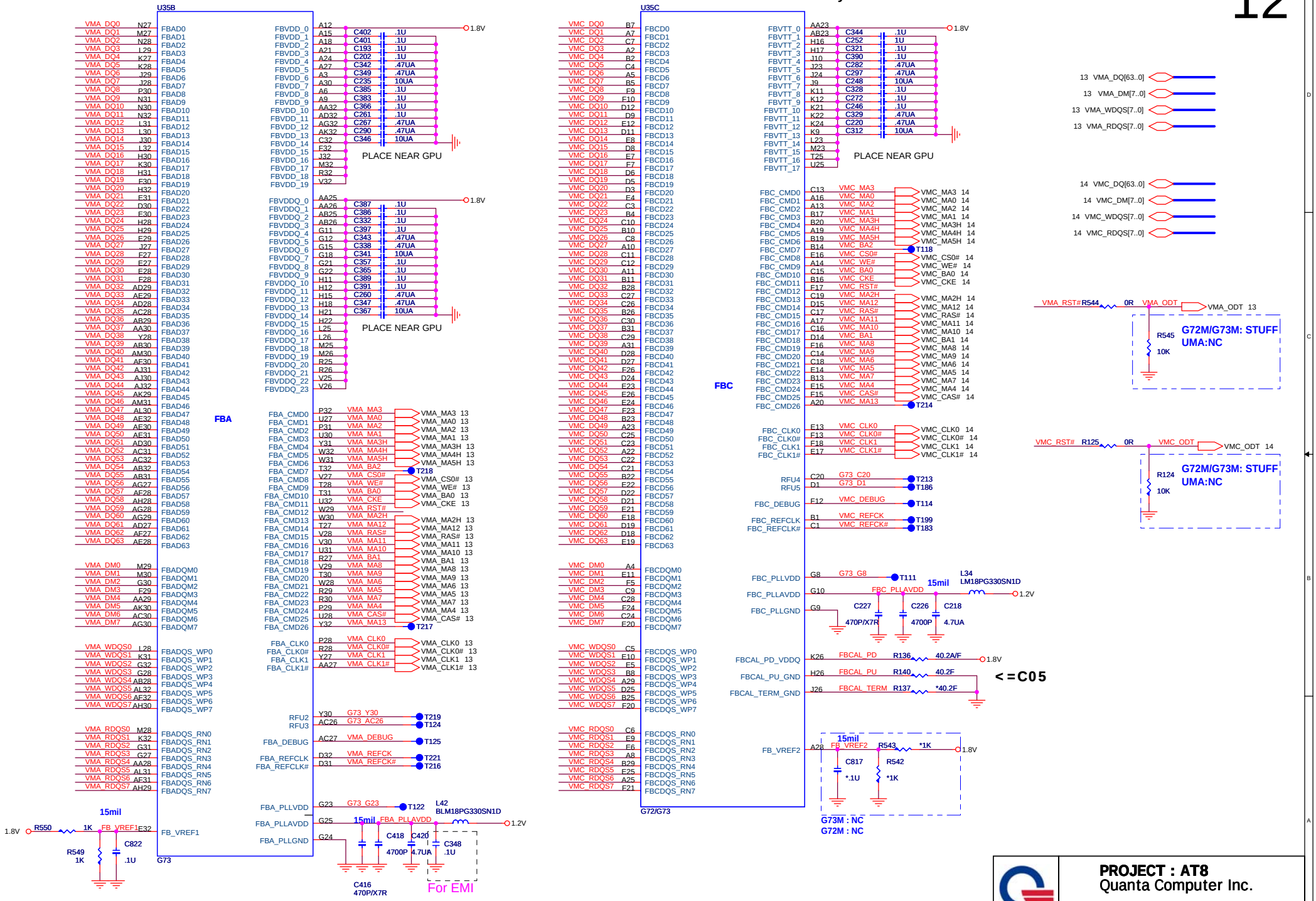
PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GFX(ROM, GPIO, STRAP)	2A

NB5/RD2/HW1

Date: Wednesday, June 14, 2006 | Sheet 11 of 39

Channel C is available on G73M only



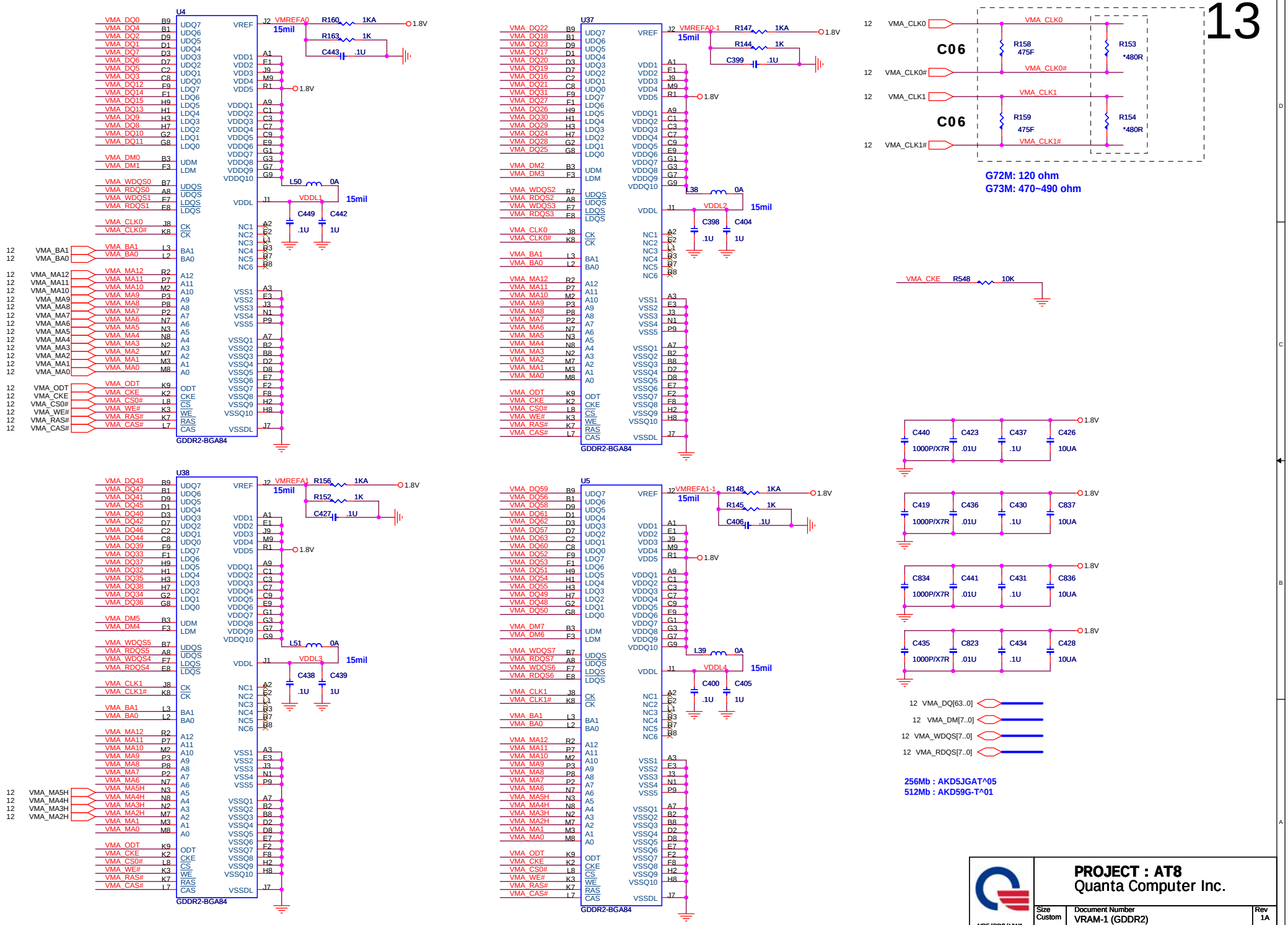
VREF = FBVDDQ * Rbot/(Rtop + Rbot)

PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GFX (MEM INTERFACE)	1A

Date: Wednesday, June 14, 2006 | Sheet 12 of 39

NB5/RD2/HW1

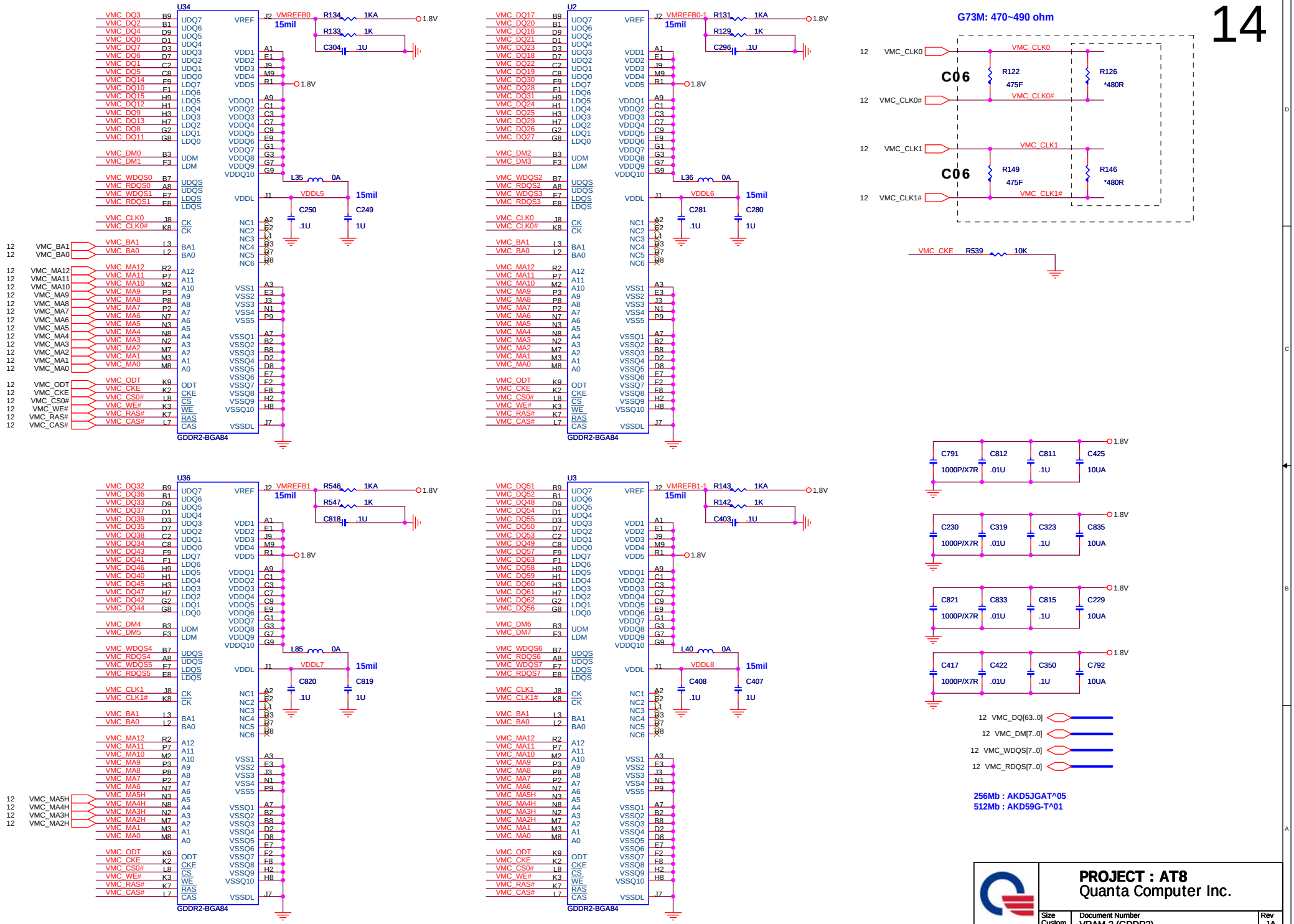


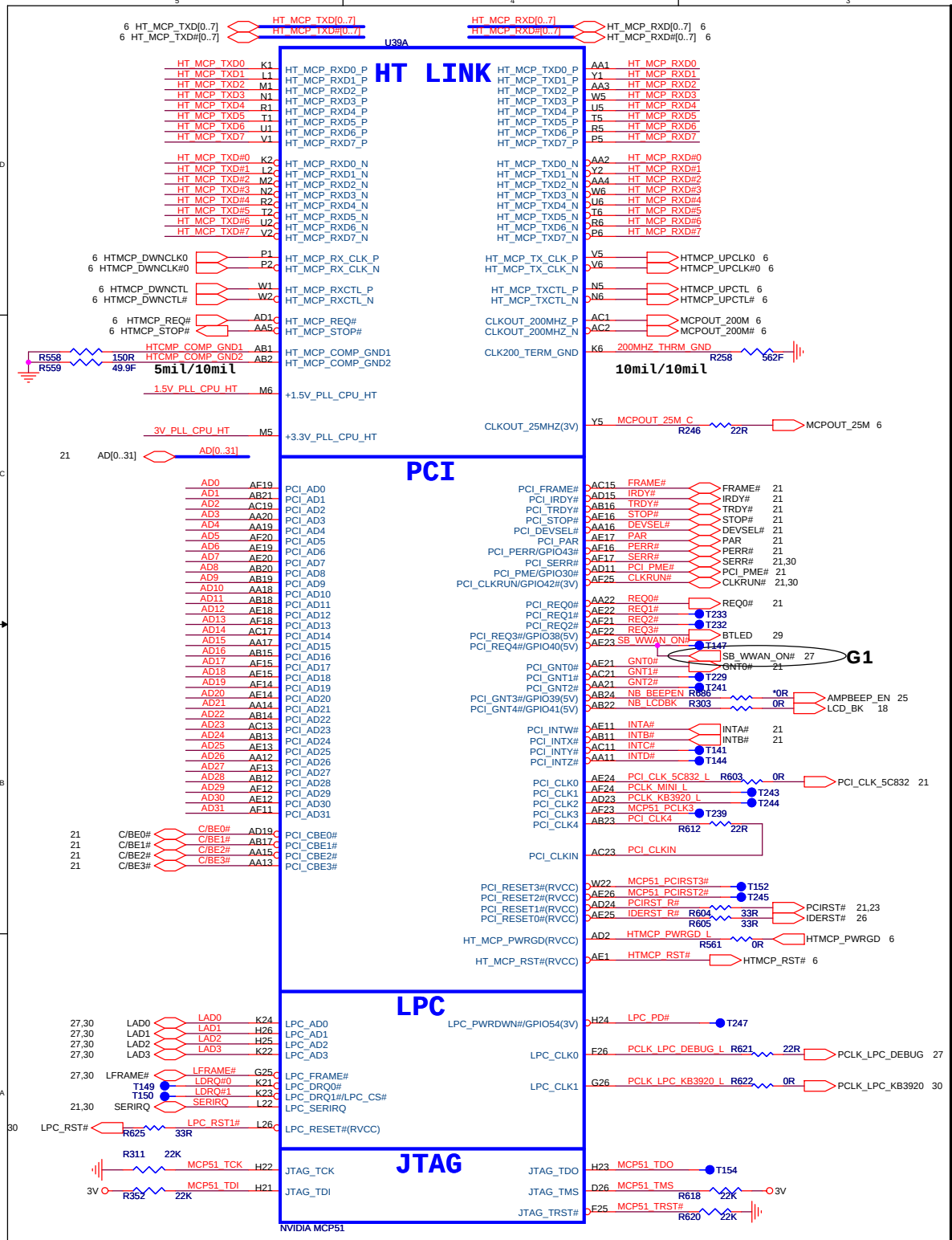
PROJECT : AT8
Quanta Computer Inc.

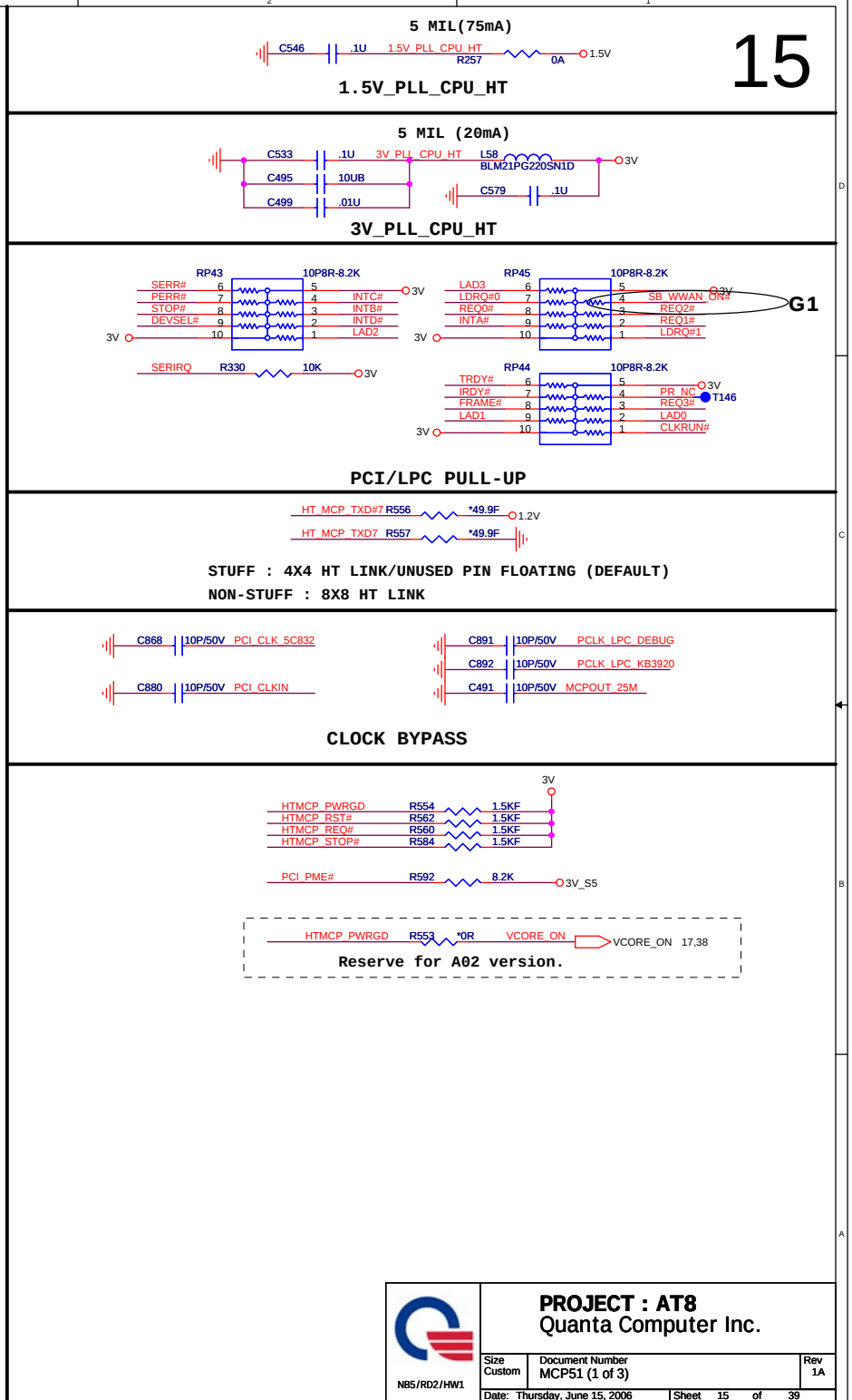
Size	Document Number	Rev
Custom	VRAM-1 (GDDR2)	1A

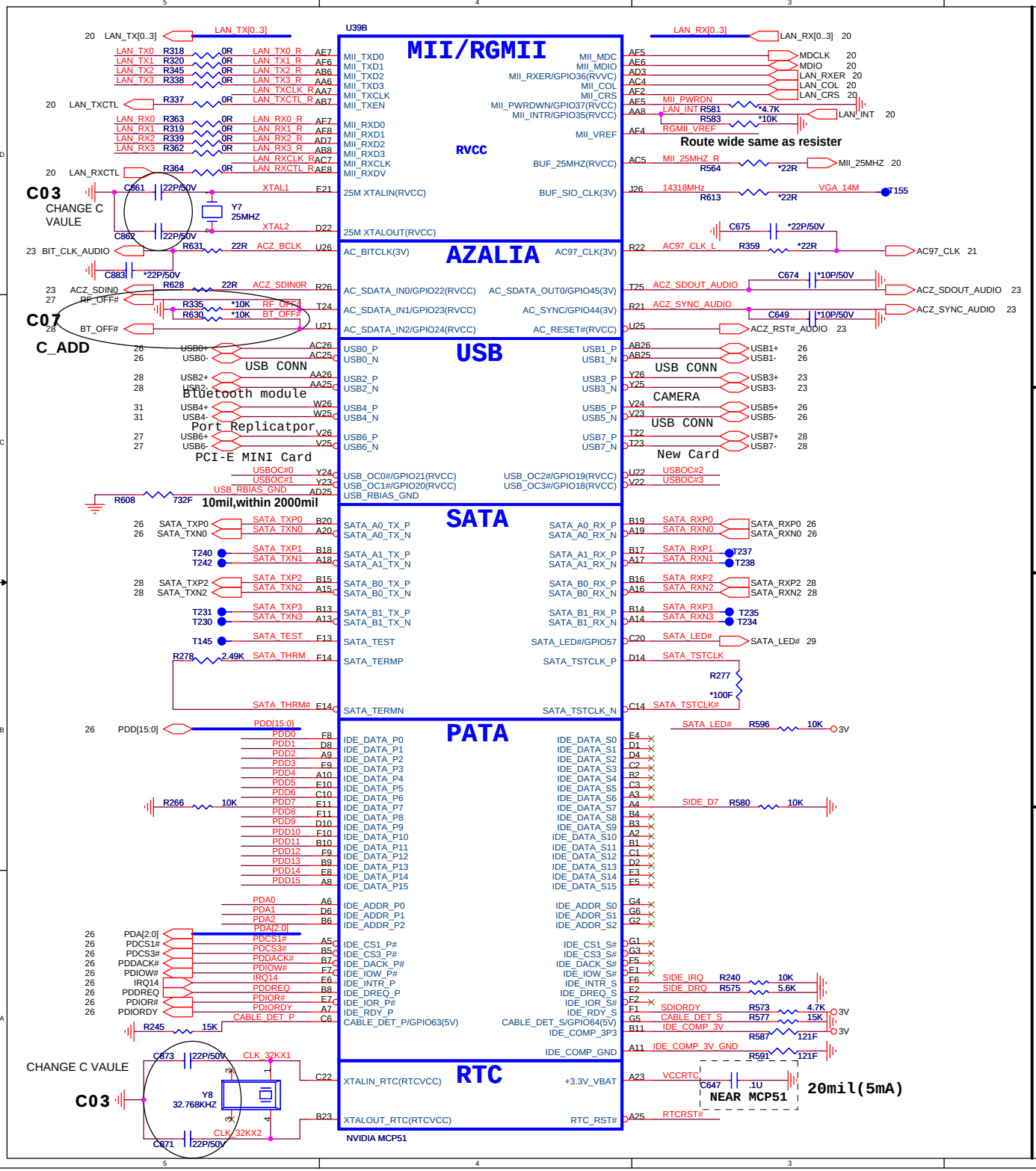
N85/RD2/HW1

Date: Wednesday, June 14, 2006 | Sheet 13 of 39


U34
U2
U36
U3
GDDR2-BGA84
VMREFB0
VMREFB0-1
VMREFB1
VMREFB1-1
R134 1KA
R133 1K
C304 .1U
R131 1KA
R129 1K
C296 .1U
R546 1KA
R547 1K
C818 .1U
R143 1KA
R142 1K
C403 .1U
1.8V
15mil
L35 0A
L36 0A
L85 0A
L40 0A
VDDL5
VDDL6
VDDL7
VDDL8
C250 .1U
C249 1U
C281 .1U
C280 1U
C820 .1U
C819 1U
C408 .1U
C407 1U
G73M: 470~490 ohm
C06
R122 475F
R126 *480R
R149 475F
R146 *480R
VMC_CLK0
VMC_CLK0#
VMC_CLK1
VMC_CLK1#
VMC_CKE R539 10K
C791 1000P/X7R
C812 .01U
C811 .1U
C425 10UA
C230 1000P/X7R
C319 .01U
C323 .1U
C835 10UA
C821 1000P/X7R
C833 .01U
C815 .1U
C229 10UA
C417 1000P/X7R
C422 .01U
C350 .1U
C792 10UA
12 VMC_DQ[63..0]
12 VMC_DM[7..0]
12 VMC_WDQS[7..0]
12 VMC_RDQS[7..0]
256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01
PROJECT : AT8
Quanta Computer Inc.
NB5/RD2/HW1
Size Custom
Document Number
VRAM-2 (GDDR2)
Rev 1A
Date: Wednesday, June 14, 2006
Sheet 14 of 39

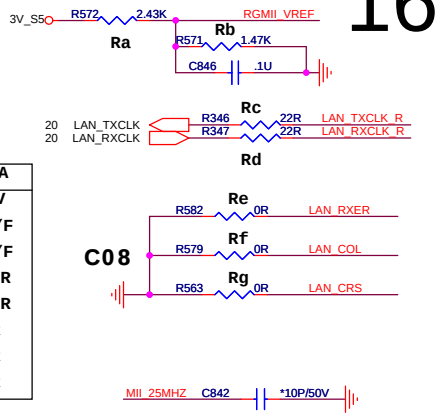

U39A
HT LINK
PCI
LPC
JTAG
NVIDIA MCP51
5mil/10mil
10mil/10mil
G1
G1


15
5 MIL(75mA)
1.5V_PLL_CPU_HT
5 MIL (20mA)
3V_PLL_CPU_HT
PCI/LPC PULL-UP
STUFF : 4X4 HT LINK/UNUSED PIN FLOATING (DEFAULT)
NON-STUFF : 8X8 HT LINK
CLOCK BYPASS
Reserve for A02 version.
PROJECT : AT8
Quanta Computer Inc.
NB5/RD2/HW1
Size Custom
Document Number
MCP51 (1 of 3)
Rev 1A
Date: Thursday, June 15, 2006
Sheet 15 of 39



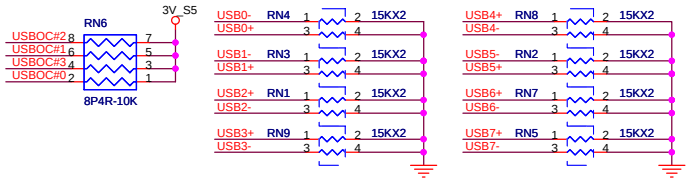
10/100 - GIAG LAN STUFF OPTION

16



	10/100	GIGA
VREF	1.65V	1.25V
Ra	1K/F	2.43K/F
Rb	1K/F	1.47K/F
Rc	0R	22R
Rd	0R	22R
Re	NC	0R
Rf	NC	0R
Rg	NC	0R

C_CHANGE



ACZ_SPKR STRAP (Boot MODE)	
0	User Table*
1	Safe table

*DEFAULT

ACZ_RST# STRAP (LAN)	
0	MII
1	RGMII*

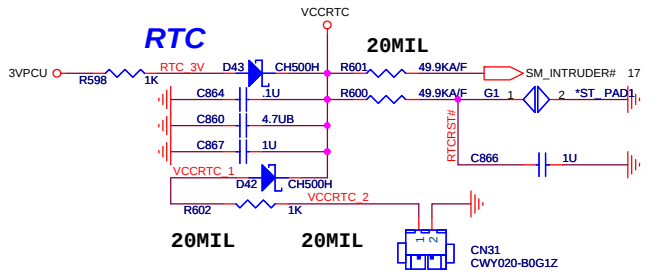
*DEFAULT

SPDIF0 STRAP (SIO CLK)	
0	14.318MHZ*
1	24.000MHZ

*DEFAULT

SUSCLK STRAP (MCP MODE)	
0	NORMAL*
1	SLAVE

*DEFAULT



CHANGE C VAULE

C03

PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP51 (1 of 3)	3A

N85/RD2/HW1

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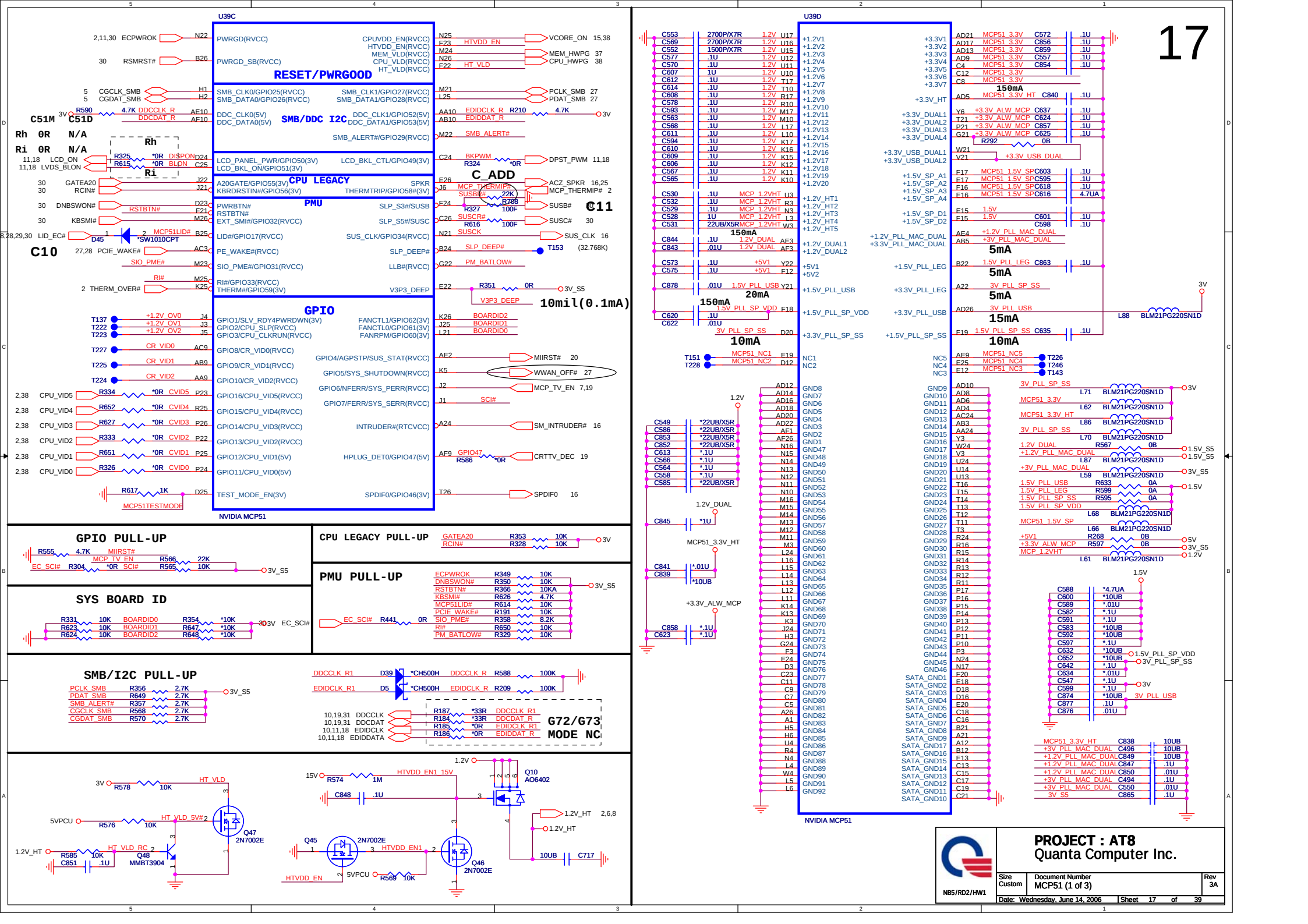
17
U39C
RESET/PWRGOOD
SMB/DDC I2C
CPU LEGACY
PMU
GPIO
NVIDIA MCP51
U39D
C51M C51D
Rh 0R N/A
Ri 0R N/A
C10
C11
C_ADD
10mil(0.1mA)
GPIO PULL-UP
CPU LEGACY PULL-UP
PMU PULL-UP
SYS BOARD ID
SMB/I2C PULL-UP
G72/G73
MODE NC
PROJECT : AT8
Quanta Computer Inc.
Size Custom
Document Number
MCP51 (1 of 3)
Rev 3A
NB5/RD2/HW1
Date: Wednesday, June 14, 2006
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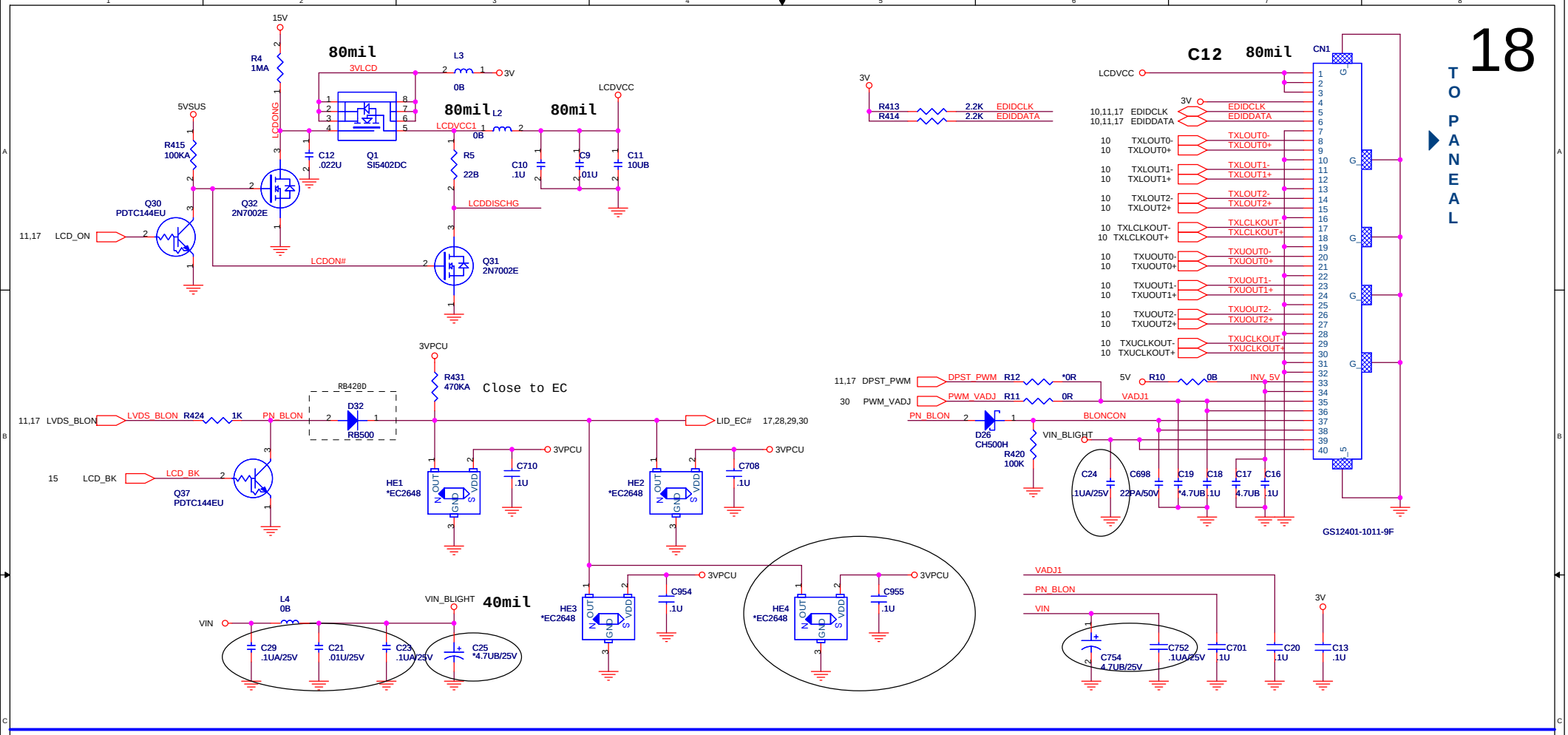
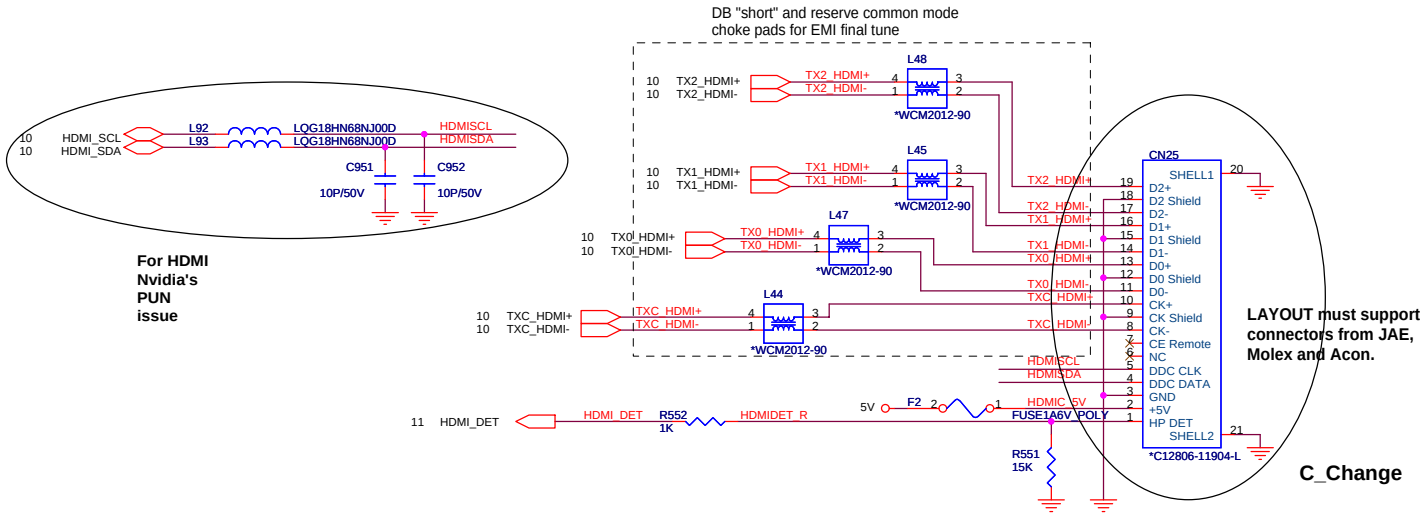
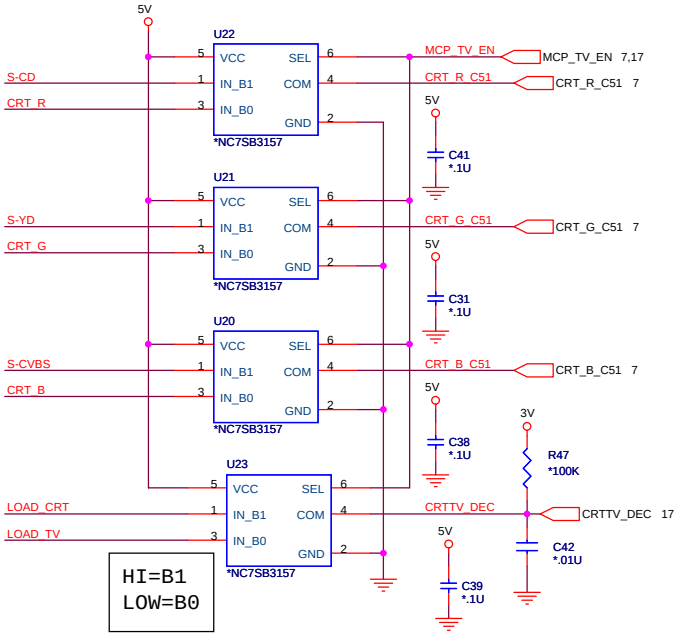




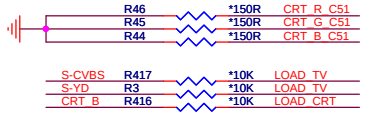
HDMI PORT

NB5/RD2/HW1	**PROJECT : AT8** Quanta Computer Inc.	
Size Custom	Document Number LCD CONN,HDMI CONN	Rev 3A
	Date: Wednesday, June 14, 2006	Sheet 18 of 39

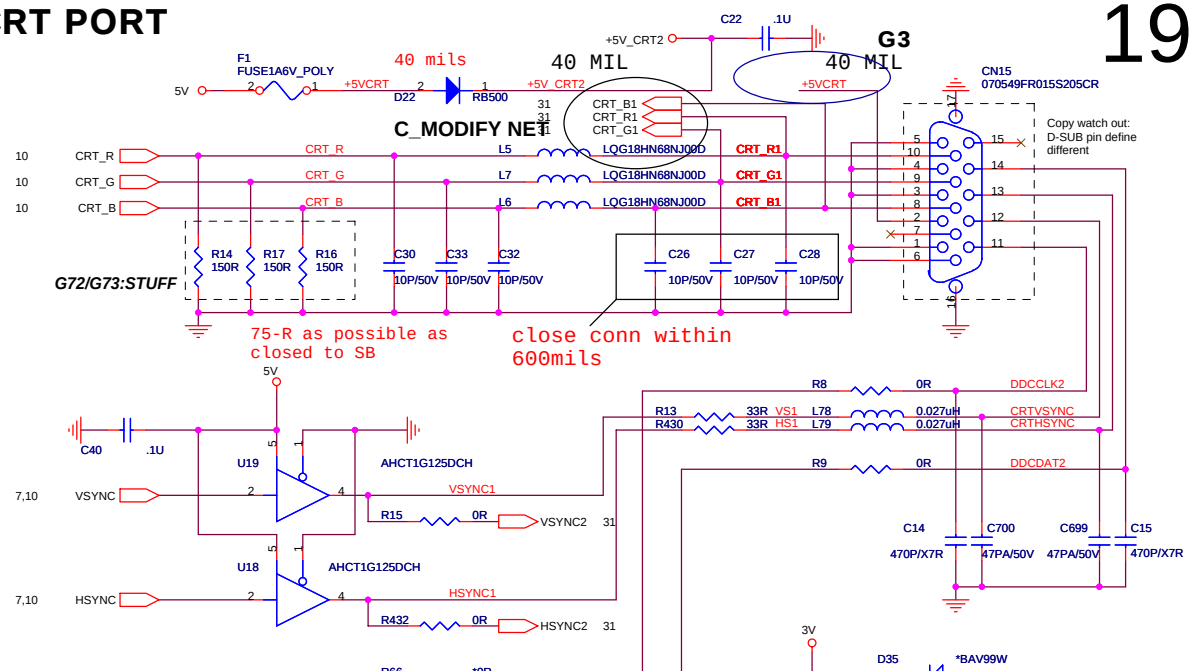
For UMA only

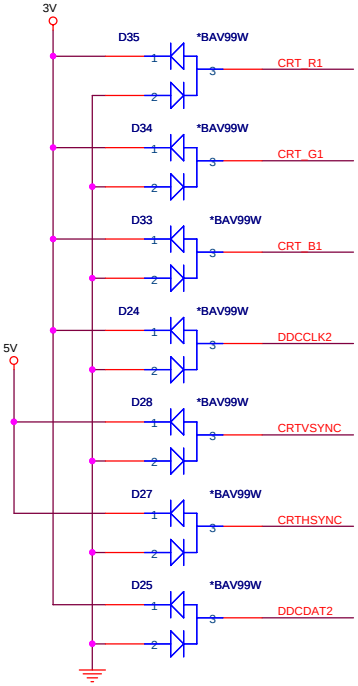


close within 600mils

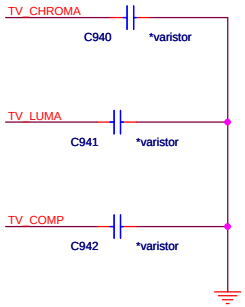


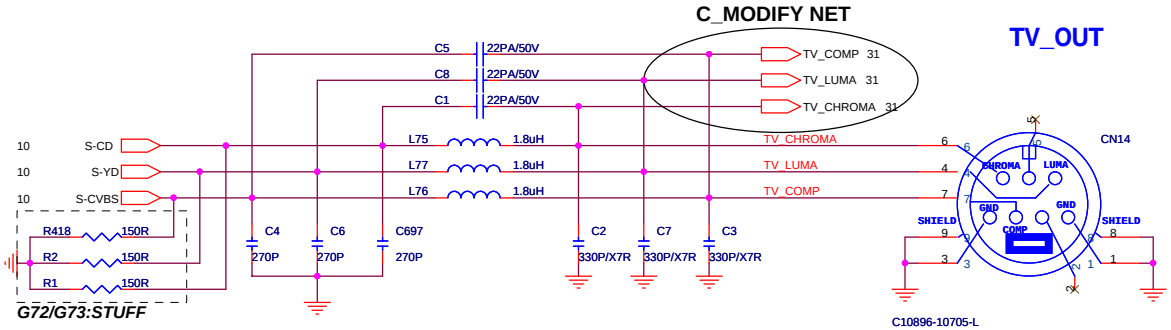
CRT PORT





C13





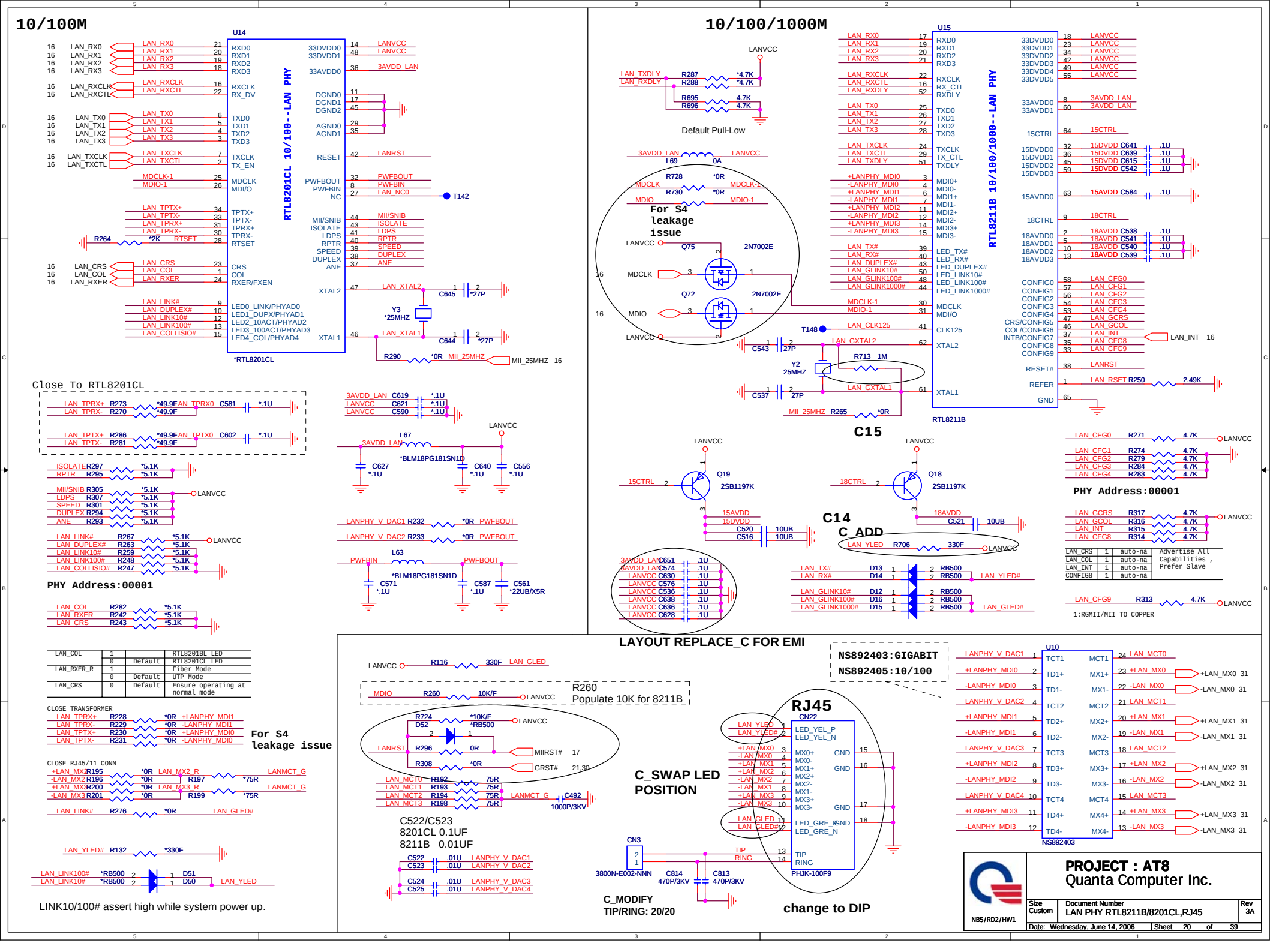
TV_OUT

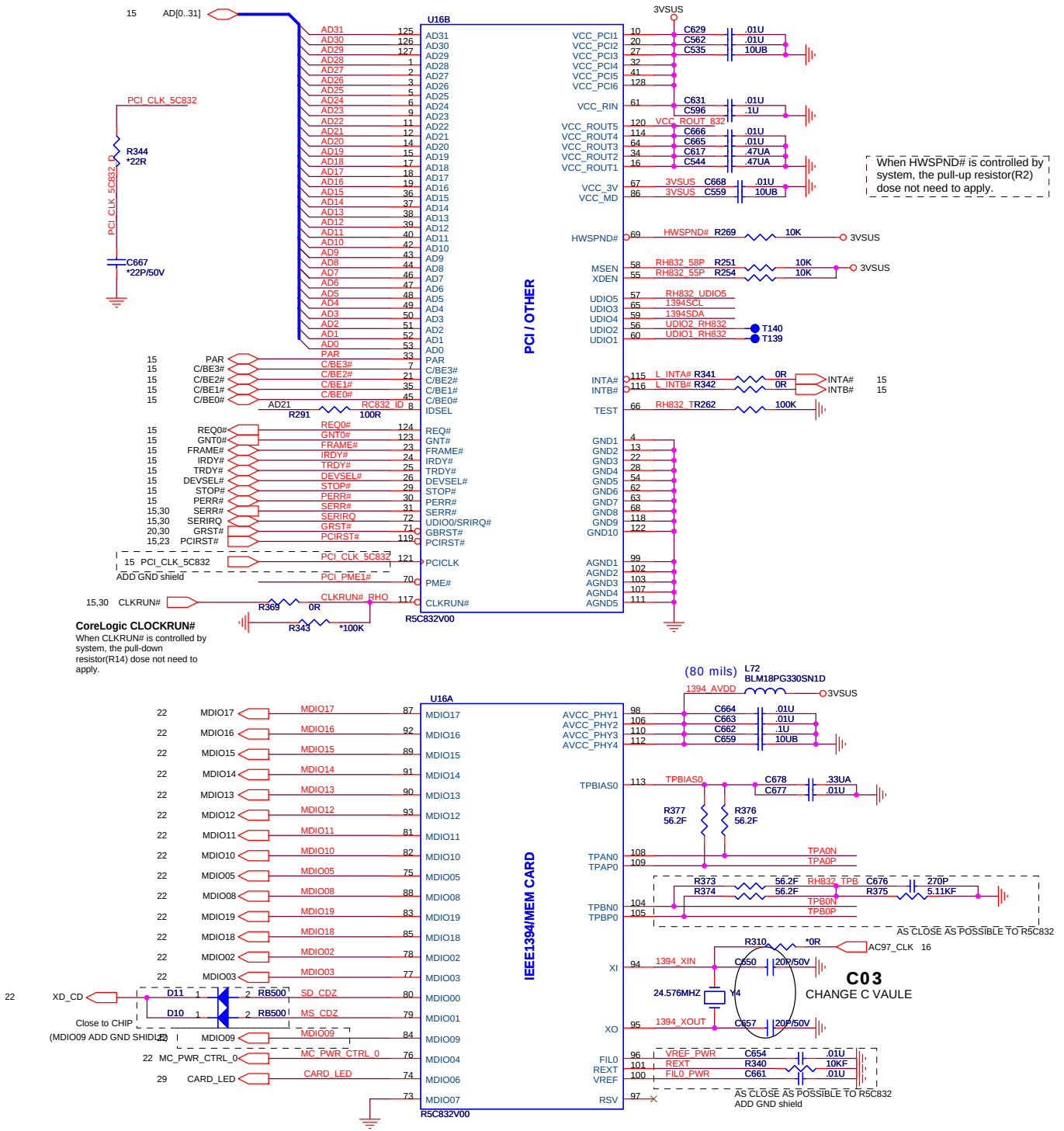
NB5/RD2/HW1

PROJECT : AT8
Quanta Computer Inc.

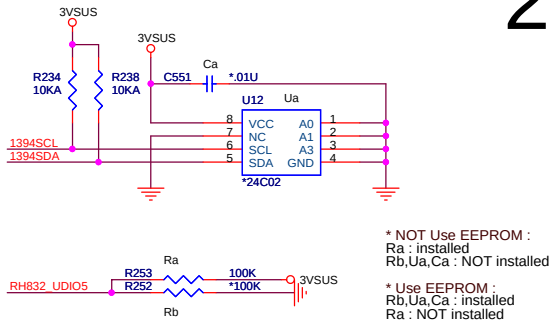
Size	Document Number	Rev
Custom	CRT,TV_OUT	2A

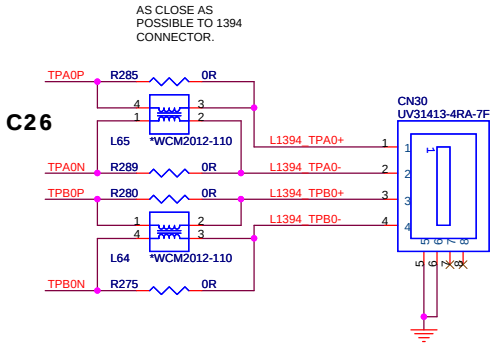
Date: Thursday, June 15, 2006 | Sheet 19 of 39


10/100M
U14
RTL8201CL 10/100--LAN PHY
*RTL8201CL
LAN_RX0
LAN_RX1
LAN_RX2
LAN_RX3
LAN_RXCLK
LAN_RXCTL
LAN_TX0
LAN_TX1
LAN_TX2
LAN_TX3
LAN_TXCLK
LAN_TXCTL
MDCLK-1
MDIO-1
LAN_TPTX+
LAN_TPTX-
LAN_TPRX+
LAN_TPRX-
R264 *2K RTSET
LAN_CRS
LAN_COL
LAN_RXER
LAN_LINK#
LAN_DUPLEX#
LAN_LINK10#
LAN_LINK100#
LAN_COLLISIO#
LANVCC
3AVDD_LAN
LANRST
PWFBOUT
PWFBIN
LAN_NC0
T142
MII/SNIB
ISOLATE
LDPS
RPTR
SPEED
DUPLEX
ANE
LAN_XTAL2
LAN_XTAL1
C645 *27P
C644 *27P
Y3 *25MHZ
R290 *0R MII_25MHZ
MII_25MHZ 16
Close To RTL8201CL
LAN_TPRX+ R273 *49.9F
LAN_TPRX- R270 *49.9F
LAN_TPRX0 C581 *.1U
LAN_TPTX+ R286 *49.9F
LAN_TPTX- R281 *49.9F
LAN_TPTX0 C602 *.1U
ISOLATE R297 *5.1K
RPTR R295 *5.1K
MII/SNIB R305 *5.1K
LDPS R307 *5.1K
SPEED R301 *5.1K
DUPLEX R294 *5.1K
ANE R293 *5.1K
LAN_LINK# R267 *5.1K
LAN_DUPLEX# R263 *5.1K
LAN_LINK10# R259 *5.1K
LAN_LINK100# R248 *5.1K
LAN_COLLISIO# R247 *5.1K
PHY Address:00001
LAN_COL R282 *5.1K
LAN_RXER R242 *5.1K
LAN_CRS R243 *5.1K
3AVDD_LAN C619 *.1U
LANVCC C621 *.1U
LANVCC C590 *.1U
L67
*BLM18PG181SN1D
C627 *.1U
C640 *.1U
C556 *.1U
LANPHY_V_DAC1 R232 *0R PWFBOUT
LANPHY_V_DAC2 R233 *0R PWFBOUT
L63
PWFBIN
PWFBOUT
*BLM18PG181SN1D
C571 *.1U
C587 *.1U
C561 *22UB/X5R
LAN_COL 1 RTL8201BL LED
0 Default RTL8201CL LED
LAN_RXER_R 1 Fiber Mode
0 Default UTP Mode
LAN_CRS 0 Default Ensure operating at normal mode
CLOSE TRANSFORMER
LAN_TPRX+ R228 *0R +LANPHY_MDI1
LAN_TPRX- R229 *0R -LANPHY_MDI1
LAN_TPTX+ R230 *0R +LANPHY_MDI0
LAN_TPTX- R231 *0R -LANPHY_MDI0
For S4 leakage issue
CLOSE RJ45/11 CONN
+LAN_MX2 R195 *0R LAN_MX2_R
-LAN_MX2 R196 *0R R197 *75R LANMCT_G
+LAN_MX3 R200 *0R LAN_MX3_R
-LAN_MX3 R201 *0R R199 *75R LANMCT_G
LAN_LINK# R276 *0R LAN_GLED#
LAN_YLED# R132 *330F
LAN_LINK100# *RB500 D51
LAN_LINK10# *RB500 D50 LAN_YLED
LINK10/100# assert high while system power up.
10/100/1000M
U15
RTL8211B 10/100/1000--LAN PHY
RTL8211B
LAN_TXDLY R287 *4.7K
LAN_RXDLY R288 *4.7K
R695 4.7K
R696 4.7K
Default Pull-Low
3AVDD_LAN L69 0A
R728 *0R
R730 *0R
MDCLK
MDIO
MDCLK-1
MDIO-1
For S4 leakage issue
Q75 2N7002E
Q72 2N7002E
T148
LAN_CLK125
LAN_GXTAL2
LAN_GXTAL1
C543 27P
C537 27P
Y2 25MHZ
R713 1M
MII_25MHZ R265 *0R
C15
LAN_CFG0 R271 4.7K
LAN_CFG1 R274 4.7K
LAN_CFG2 R279 4.7K
LAN_CFG3 R284 4.7K
LAN_CFG4 R283 4.7K
PHY Address:00001
LAN_GCRS R317 4.7K
LAN_GCOL R316 4.7K
LAN_INT R315 4.7K
LAN_CFG8 R314 4.7K
LAN_INT 16
LAN_RSET R250 2.49K
LAN_CFG9 R313 4.7K
1:RGMII/MII TO COPPER
15CTRL Q19 2SB1197K
18CTRL Q18 2SB1197K
15AVDD C520 10UB
15DVDD C516 10UB
18AVDD C521 10UB
C14
C_ADD
LAN_YLED R706 330F
LAN_TX# D13 RB500
LAN_RX# D14 RB500
LAN_YLED#
LAN_GLINK10# D12 RB500
LAN_GLINK100# D16 RB500
LAN_GLINK1000# D15 RB500
LAN_GLED#
LAYOUT REPLACE_C FOR EMI
LAN_CRS 1 auto-na
LAN_COL 1 auto-na
LAN_INT 1 auto-na
CONFIG8 1 auto-na
Advertise All Capabilities , Prefer Slave
NS892403:GIGABIT
NS892405:10/100
LANVCC R116 330F LAN_GLED
MDIO R260 10K/F
R260 Populate 10K for 8211B
R724 *10K/F
D52 *RB500
LANRST R296 0R MIIRST# 17
R308 *0R GRST# 21,30
LAN_MCT0 R192 75R
LAN_MCT1 R193 75R
LAN_MCT2 R194 75R
LAN_MCT3 R198 75R
LANMCT_G C492 1000P/3KV
C522/C523
8201CL 0.1UF
8211B 0.01UF
C522 .01U LANPHY_V_DAC1
C523 .01U LANPHY_V_DAC2
C524 .01U LANPHY_V_DAC3
C525 .01U LANPHY_V_DAC4
C_SWAP LED POSITION
RJ45
CN22
LED_YEL_P
LED_YEL_N
LED_GRE_P
LED_GRE_N
PHJK-100F9
CN3
3800N-E002-NNN
TIP
RING
C814 470P/3KV
C813 470P/3KV
C_MODIFY
TIP/RING: 20/20
change to DIP
U10
NS892403
LANPHY_V_DAC1
+LANPHY_MDI0
-LANPHY_MDI0
LANPHY_V_DAC2
+LANPHY_MDI1
-LANPHY_MDI1
LANPHY_V_DAC3
+LANPHY_MDI2
-LANPHY_MDI2
LANPHY_V_DAC4
+LANPHY_MDI3
-LANPHY_MDI3
+LAN_MX0 31
-LAN_MX0 31
+LAN_MX1 31
-LAN_MX1 31
+LAN_MX2 31
-LAN_MX2 31
+LAN_MX3 31
-LAN_MX3 31
PROJECT : AT8
Quanta Computer Inc.
Size Custom
Document Number
LAN PHY RTL8211B/8201CL,RJ45
Rev 3A
Date: Wednesday, June 14, 2006
Sheet 20 of 39
NB5/RD2/HW1

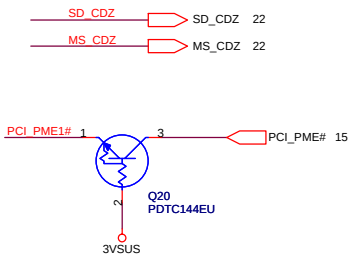


Serial EEPROM





*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically And layout with shields.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	R5C832 CONTROL	1A

NB5/RD2/HW1

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4 IN1 CARD READER
XD,MMC/SD,MS/MSP

CHECK CONN.

TD

CN37 — 4IN1-R013-J00-LR-42P

Pin	Signal	Pin	Signal
1	CD_SD	41	VCC_XD
2	DAT2_SD	40	D7_XD
3	CD/DAT3_SD	39	D6_XD
4	CMD_SD	38	D5_XD
5	VSS_SD	37	D4_XD
6	VDD_SD	36	D3_XD
7	CLK_SD	35	D2_XD
8	VSS_SD	34	D1_XD
9	DAT0_SD	33	D0_XD
10	DAT1_SD	32	GND_XD
11	WP_SD	31	-WP_XD
12	VSS_MS	30	-WE_XD
13	VCC_MS	29	ALE_XD
14	SCLK_MS	28	CLE_XD
15	RESERVE_MS	27	-CE_XD
16	INS_MS	26	-RE_XD
17	RESERVE_MS	25	R/-B_XD
18	SDIO_MS	24B	GND_XD
19	RESERVE_MS	23	GND
20	BS_MS	24A	GND
21	VSS_MS		
22	GND		

Signal nets:
SD_CDZ, MS_DATA2_SD_DAT2, MS_DATA3_SD_DAT3, MS_BS_SD_CMD, SD_CLK_MS_CLK_XD-RE#, MS_DATA0_SD_DAT0, MS_DATA1_SD_DAT1, SD_WP, SD_CLK_MS_CLK_XD-RE#, MS_DATA3_SD_DAT3, MS_CDZ, MS_DATA2_SD_DAT2, MS_DATA0_SD_DAT0, MS_DATA1_SD_DAT1, MS_BS_SD_CMD

C695 270P; C688 .01U; C690 .01U; C696 270P; R399 0A; R400 10KA; VCC_XD; XD-D7, XD-D6, XD-D5, XD-D4, MS_DATA3_SD_DAT3, MS_DATA2_SD_DAT2, MS_DATA1_SD_DAT1, MS_DATA0_SD_DAT0, XD-WP# L, MS_BS_SD_CMD, XD-ALE, XD-CLE, XD-CE#, SD_CLK_MS_CLK_XD-RE#, SD_WP, XD_CD, XD-WP#, XD_CD

Note: Need to add WP# and CD# pad for Proconn

Signal	Net	Resistor	Value	Signal
MDIO03	MDIO03	R398	56R	SD_WP
MDIO17	MDIO17	R409	56R	XD-D7
MDIO16	MDIO16	R408	56R	XD-D6
MDIO15	MDIO15	R407	56R	XD-D5
MDIO14	MDIO14	R406	56R	XD-D4
MDIO13	MDIO13	R405	56R	MS_DATA3_SD_DAT3
MDIO12	MDIO12	R404	56R	MS_DATA2_SD_DAT2
MDIO11	MDIO11	R403	56R	MS_DATA1_SD_DAT1
MDIO10	MDIO10	R402	56R	MS_DATA0_SD_DAT0
MDIO08	MDIO08	R397	56R	MS_BS_SD_CMD
MDIO05	MDIO05	R401	56R	XD-WP#
MDIO19	MDIO19	R396	56R	XD-ALE
MDIO18	MDIO18	R395	56R	XD-CLE
MDIO02	MDIO02	R394	56R	XD-CE#
MDIO09	MDIO09	R393	56R	SD_CLK_MS_CLK_XD-RE#

CN7 — *MSX039-X0-0X00

Pin	Signal	Pin	Signal
1	CD_SD	41	VCC_XD
2	DAT2_SD	40	D7_XD
3	CD/DAT3_SD	39	D6_XD
4	CMD_SD	38	D5_XD
5	VSS_SD	37	D4_XD
6	VDD_SD	36	D3_XD
7	CLK_SD	35	D2_XD
8	VSS_SD	34	D1_XD
9	DAT0_SD	33	D0_XD
10	DAT1_SD	32	GND_XD
11	WP_SD	31	-WP_XD
12	VSS_MS	30	-WE_XD
13	VCC_MS	29	ALE_XD
14	SCLK_MS	28	CLE_XD
15	RESERVE_MS	27	-CE_XD
16	INS_MS	26	-RE_XD
17	RESERVE_MS	25	R/-B_XD
18	SDIO_MS	24B	GND_XD
19	RESERVE_MS	23	GND
20	BS_MS	24A	GND
21	VSS_MS		
22	GND		

Signal nets:
SD_CDZ, MS_DATA2_SD_DAT2, MS_DATA3_SD_DAT3, MS_BS_SD_CMD, SD_CLK_MS_CLK_XD-RE#, MS_DATA0_SD_DAT0, MS_DATA1_SD_DAT1, SD_WP, SD_CLK_MS_CLK_XD-RE#, MS_DATA3_SD_DAT3, MS_CDZ, MS_DATA2_SD_DAT2, MS_DATA0_SD_DAT0, MS_DATA1_SD_DAT1, MS_BS_SD_CMD

XD-D7, XD-D6, XD-D5, XD-D4, MS_DATA3_SD_DAT3, MS_DATA2_SD_DAT2, MS_DATA1_SD_DAT1, MS_DATA0_SD_DAT0, XD-WP# L, MS_BS_SD_CMD, XD-ALE, XD-CLE, XD-CE#, SD_CLK_MS_CLK_XD-RE#, SD_WP, XD_CD

2'nd source

C905 2.2UA; R663 150KA; CLOSE CONN

Q58 AO3408L; Q57 PDTC144EU; 3VSUS; VCC_XD; 21 MC_PWR_CTRL_0; MC_PWR_CTRL_0; R658 10K; 5VSUS; XD_PWON

C903 .1U; C904 .1U; C902 .1U

Reserve

5VSUS; R702 *10K; U48 *PBLS4005D; OUT1 VOUT; CTRL2 CTRL1; VIN1 GND; VCC_XD; 3VSUS; MC_PWR_CTRL_0; XD_PWON; C932 *.1U

SCREW HOLE

HOLE18 H-C244D181P2; HOLE17 H-C244D181P2; HOLE19 H-C244D181P2; HOLE20 H-C244D181P2; HOLE12 H-S315D110P2; HOLE15 H-D173X118D173X118N; HOLE26 H-S315D110P2; HOLE7 H-S315D110P2

HOLE24 H-S315D110P2; HOLE1 H-TO6X7BO8X9D2_7X3_7P2; HOLE6 H-C244D157P2; HOLE11 H-C256D157P2; HOLE13 H-C256D157P2; HOLE8 H-C256D157P2; HOLE5 H-C244D157P2; HOLE9 H-C244D157P2

HOLE10 H-C244D157P2; HOLE3 H-TR33X299BC276D110PB; HOLE22 H-C315D110P2; HOLE23 H-C315D110P2; HOLE2 H-C315D110P2; HOLE4 H-C315D110P2; HOLE14 H-C315D110N1-256P2; HOLE25 H-C315D110P2

HOLE21 H-C315D110P2; HOLE16 H-S315D110P2; HOLE27 H-C69D69N; HOLE28 H-TC08SD69PB; HOLE29 H-C69D69N; HOLE30 H-c59X98d59x98n

EMI PAD

PAD9 *EMIPAD; PAD3 *EMIPAD; PAD13 *EMIPAD; PAD8 *EMIPAD; PAD1 *EMIPAD; PAD11 *EMIPAD; PAD7 *EMIPAD

PAD10 *EMIPAD; PAD6 *EMIPAD; PAD5 *EMIPAD; PAD4 *EMIPAD; PAD2 *EMIPAD; PAD14 *EMIPAD; PAD12 *EMIPAD

PAD15 EMIPAD; PAD16 EMIPAD; PAD18 EMIPAD; PAD19 EMIPAD

C_ADD; C28

NB5/RD2/HW1

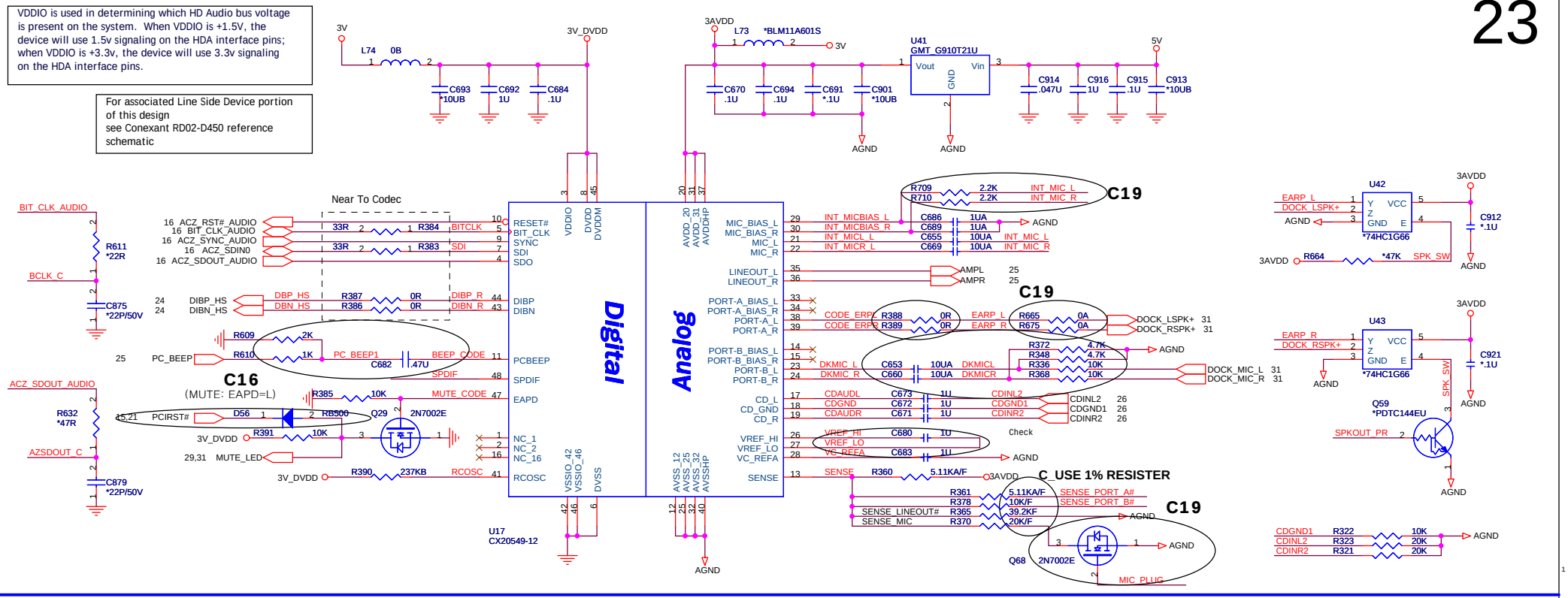
PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CARD READER CONN	3A

Date: Wednesday, June 14, 2006 | Sheet 22 of 39

VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic



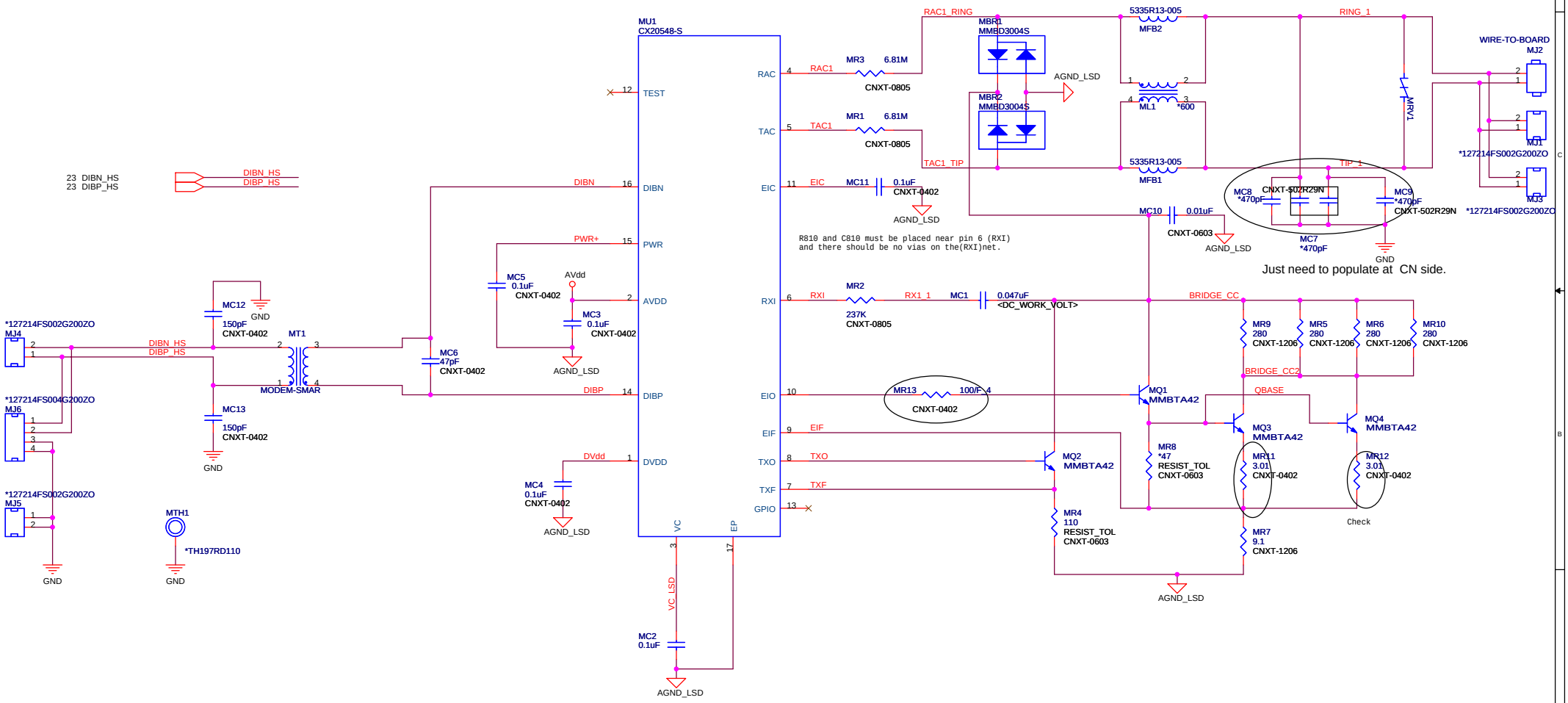
PROJECT : AT8
Quanta Computer Inc.

NB5/RD2/HW1

Size	Document Number	Rev
Custom	Azalia CTRL_CONEXANT20549-12	3A

Date: Wednesday, June 14, 2006 | Sheet 23 of 39

Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005
4		



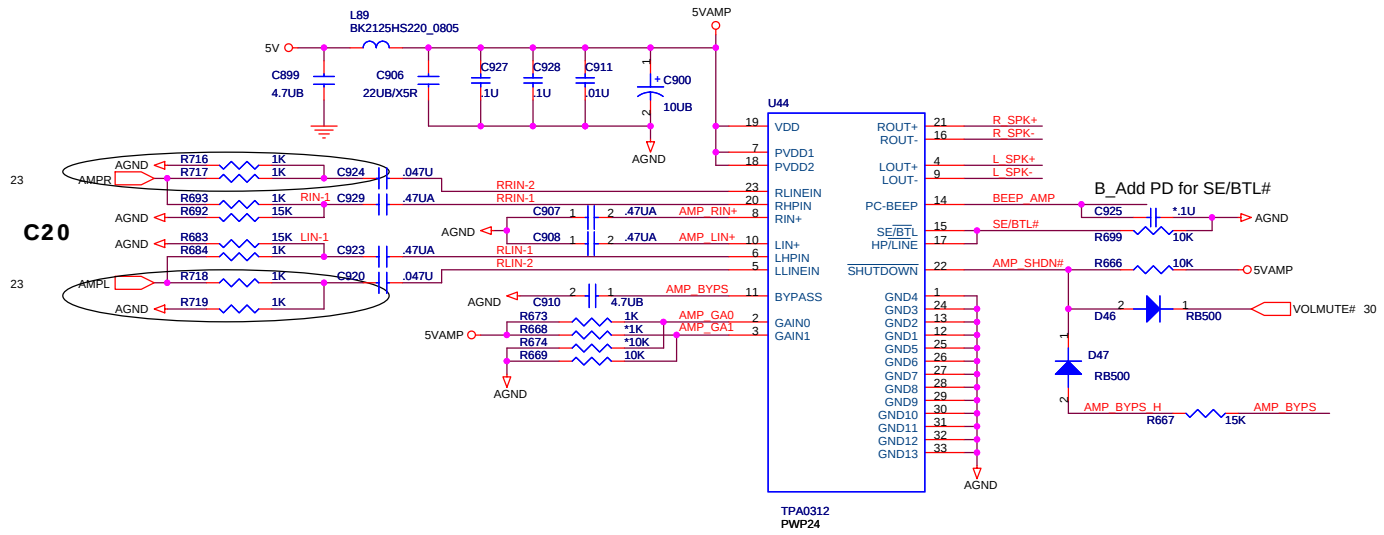
PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MODEM (DAA)	2A

NB5/RD2/HW1

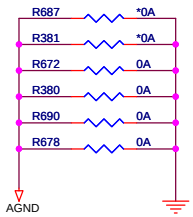
Date: Wednesday, June 14, 2006 Sheet 24 of 39

AUDIO AMPLIFIER

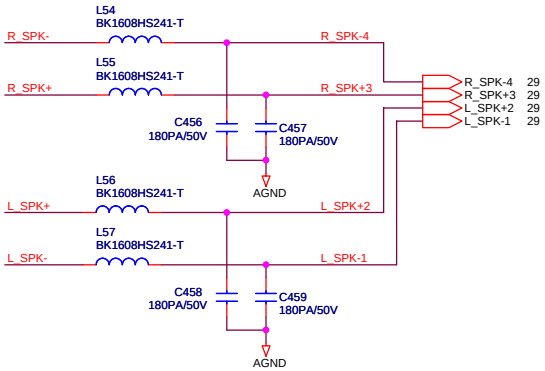


0312 Gain Table

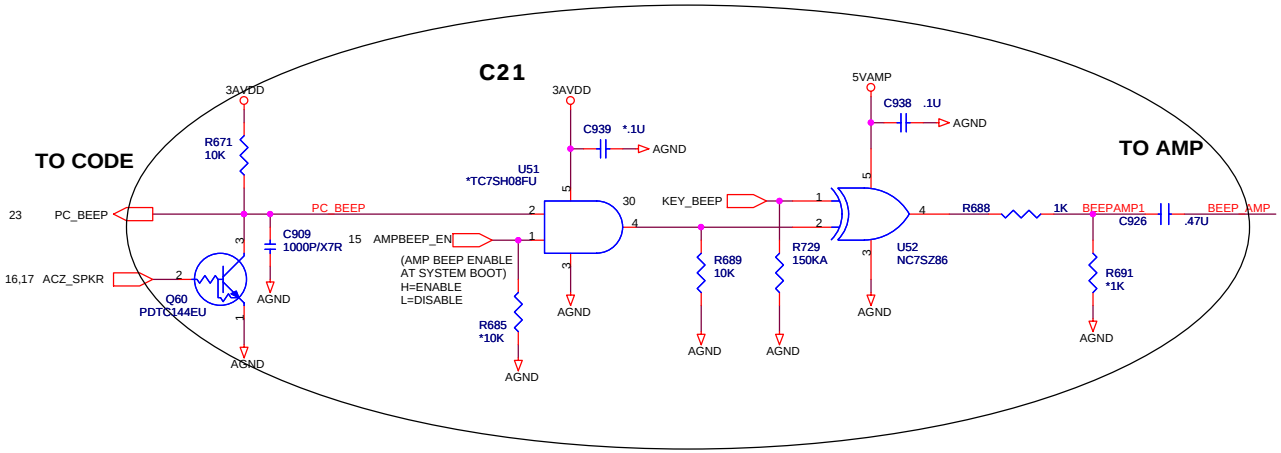
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



INT. SPEAKER



PCSPK BEEP



C_Change

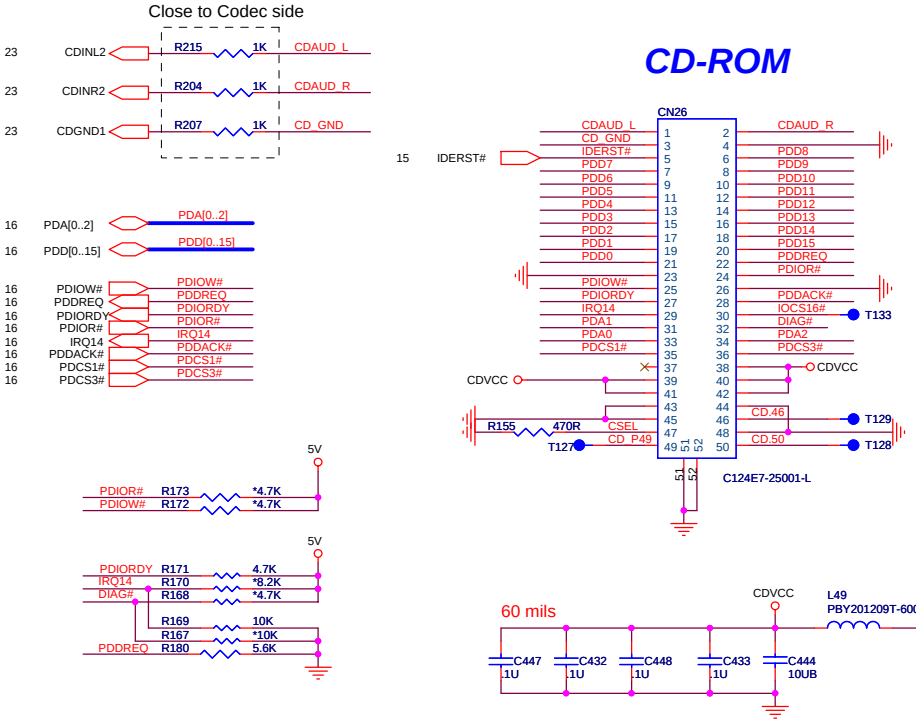
PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	JACK, AMP_TPA0312	3A

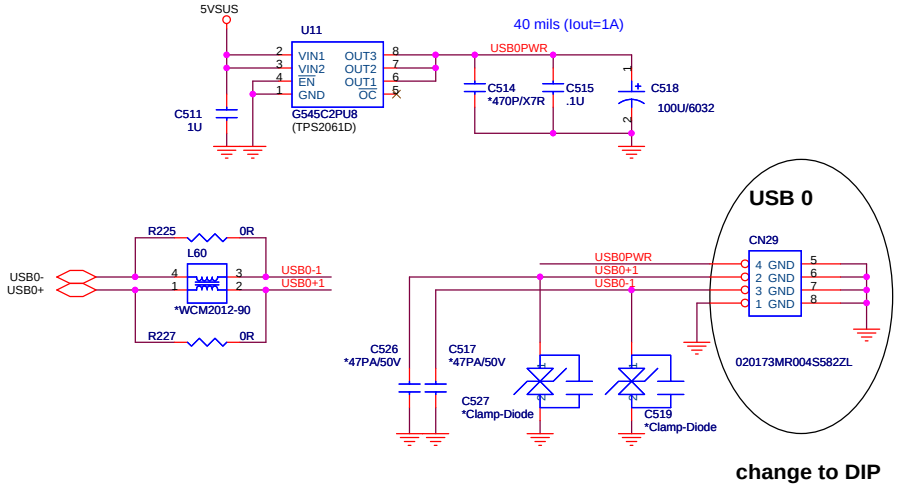
NB5/RD2/HW1

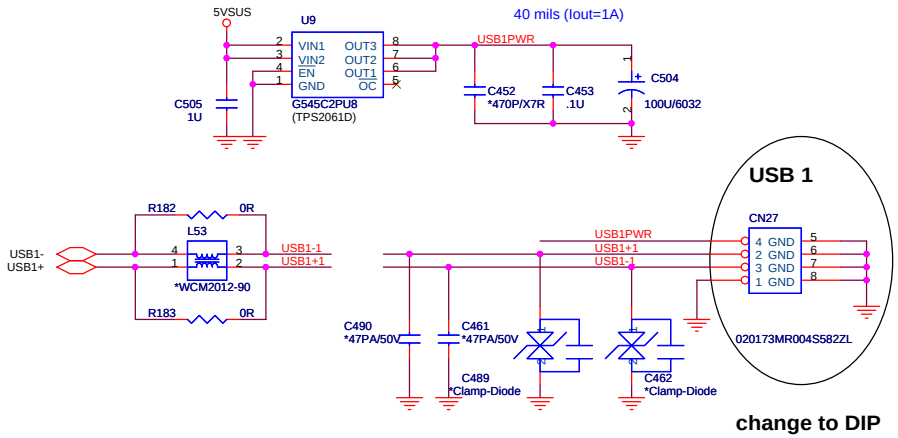
Date: Wednesday, June 14, 2006 | Sheet 25 of 39

CD-ROM

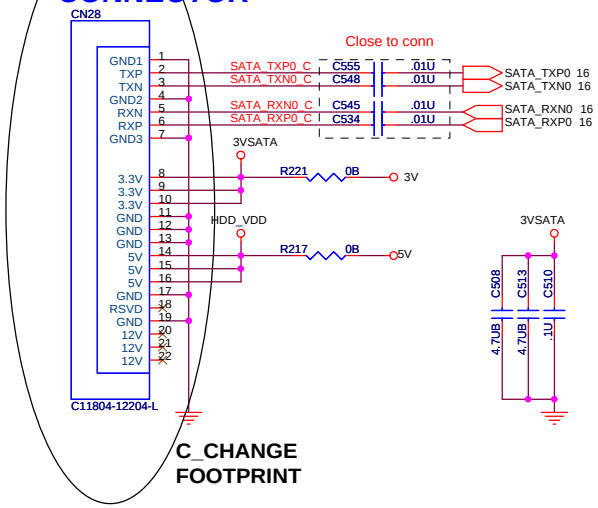


USBX2





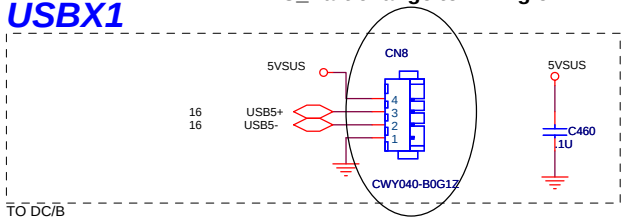
SATA_1 CONNECTOR



C_CHANGE FOOTPRINT

USBX1

C_Part change to R-Angle



PROJECT : AT8
Quanta Computer Inc.

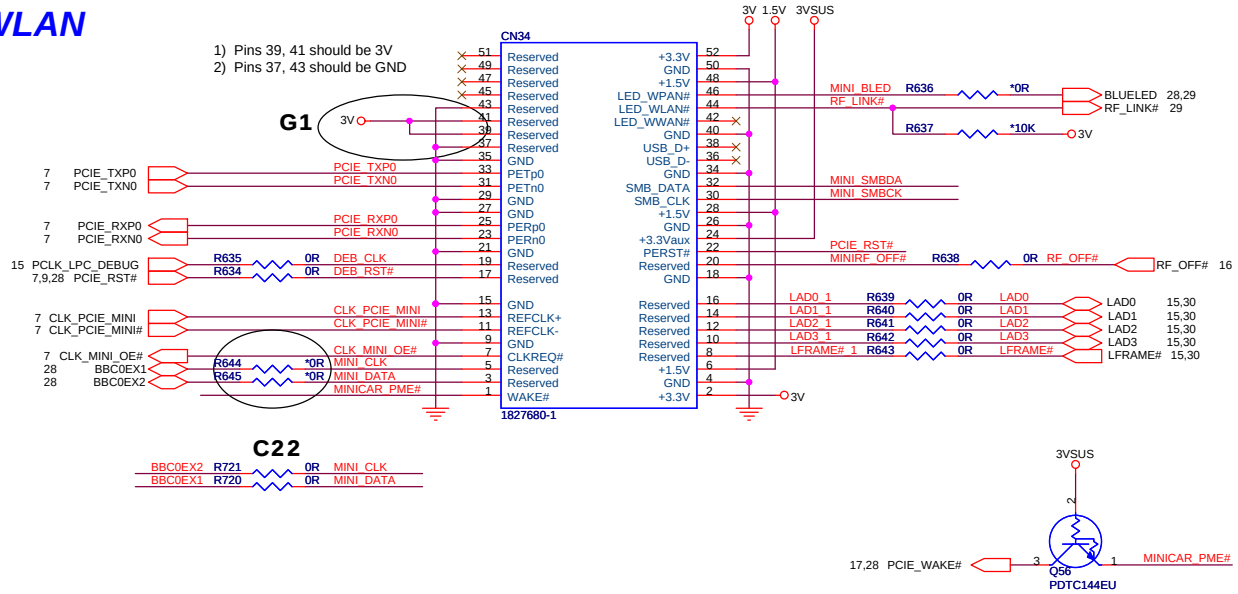
Size	Document Number	Rev
Custom	SATA HDD, CD-ROM,USBX2	3A

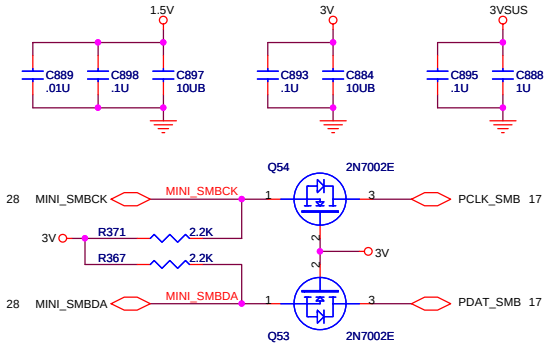
NB5/RD2/HW1

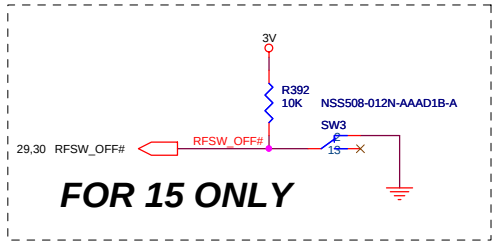
Date: Wednesday, June 14, 2006 | Sheet 26 of 39

Mini PCI-E Card 1
WLAN

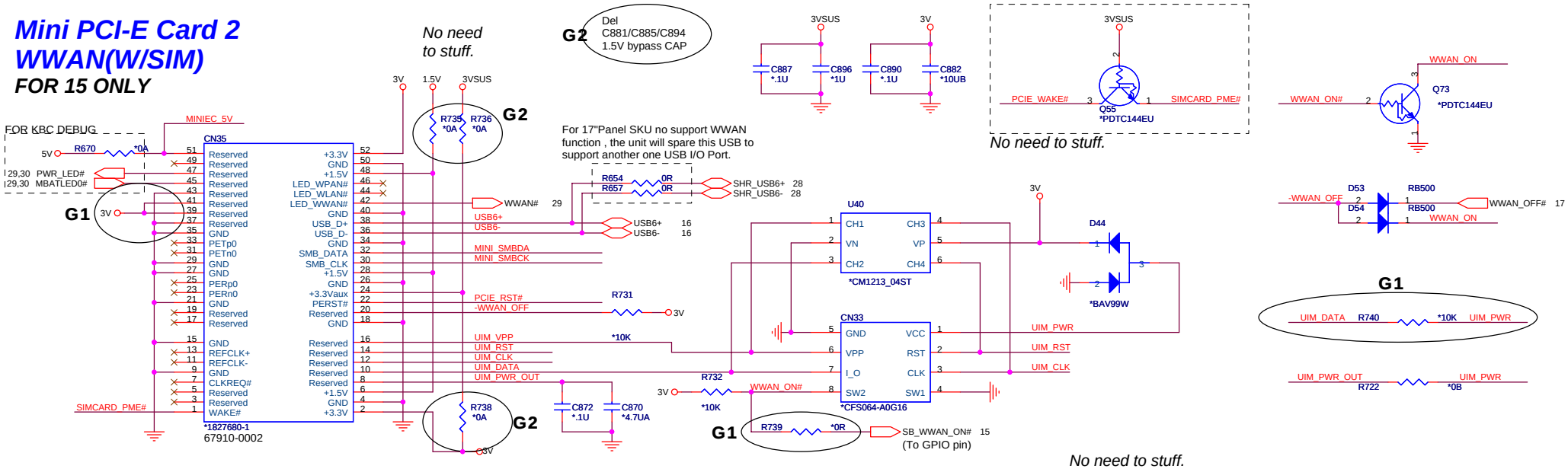
1) Pins 39, 41 should be 3V
2) Pins 37, 43 should be GND





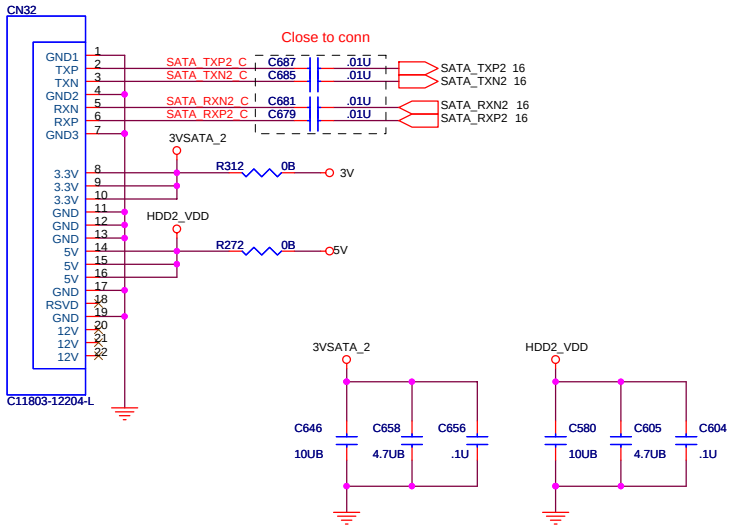


Mini PCI-E Card 2
WWAN(W/SIM)
FOR 15 ONLY

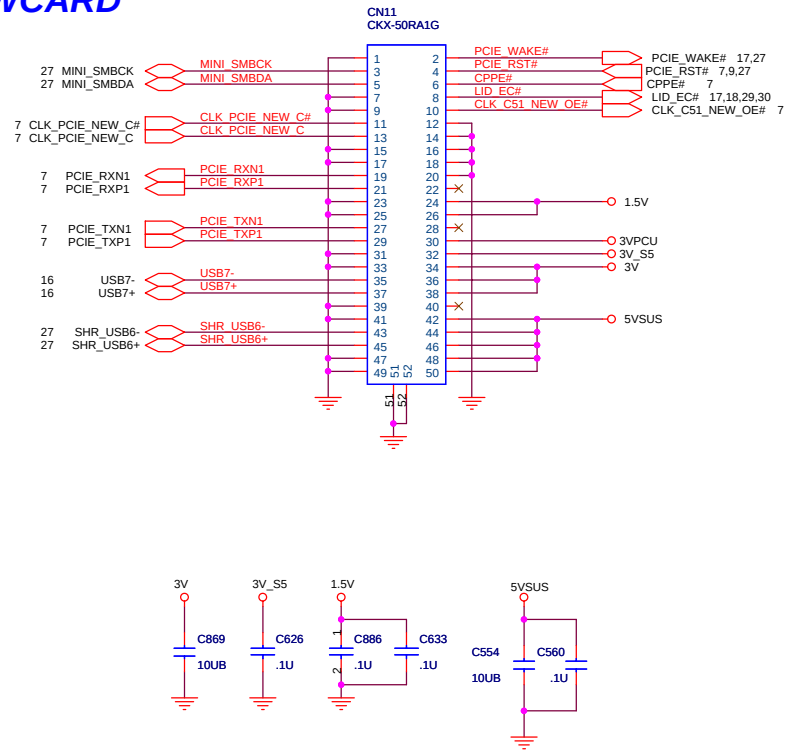


NB5/RD2/HW1	**PROJECT : AT8** Quanta Computer Inc.	
Size Custom	Document Number MINI CARD	Rev 3A
Date: Friday, June 16, 2006	Sheet 27 of 39	

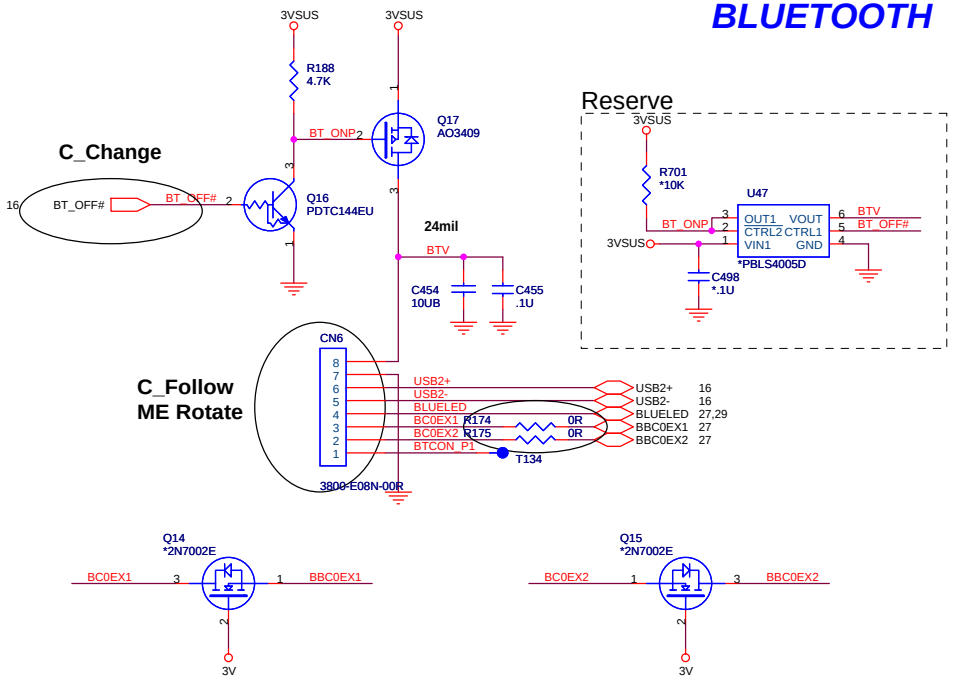
SATA_2 CONNECTOR
For 17"W Second HDD



NEWCARD



BLUETOOTH



PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/BT	3A

NB5/RD2/HW1

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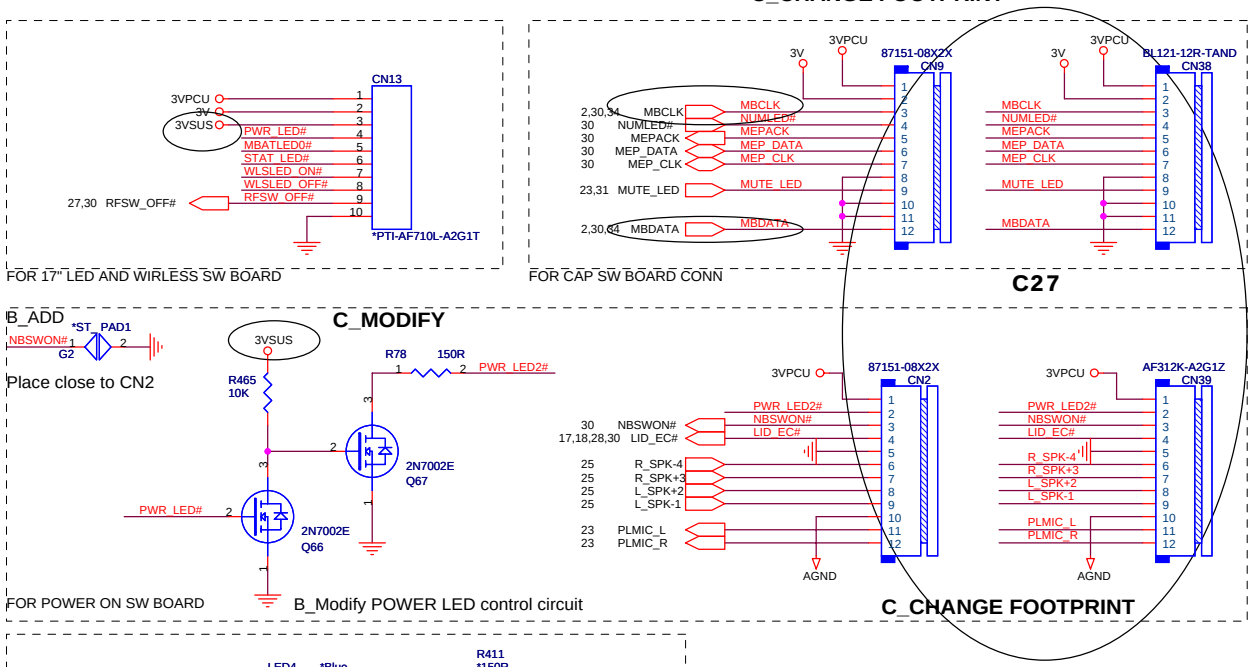
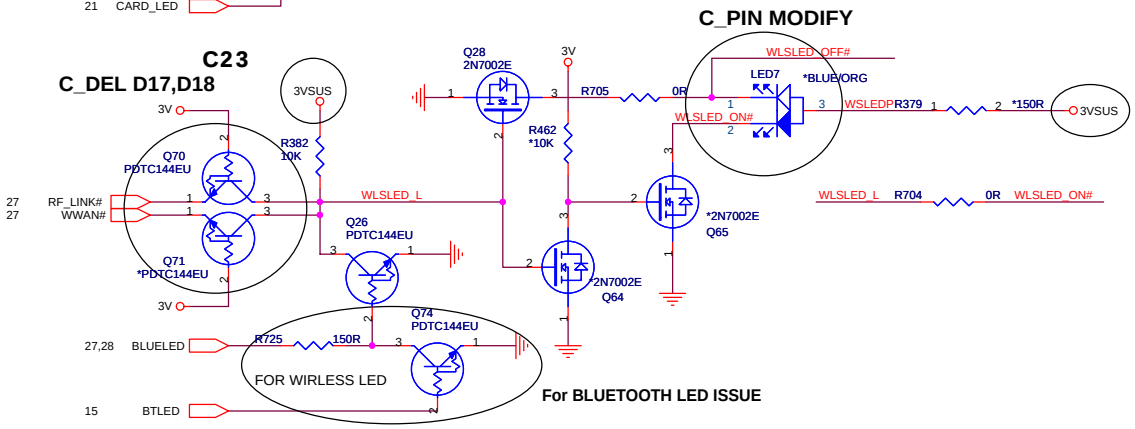
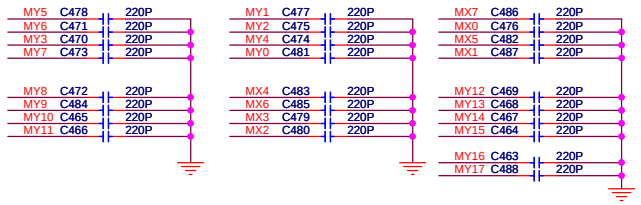
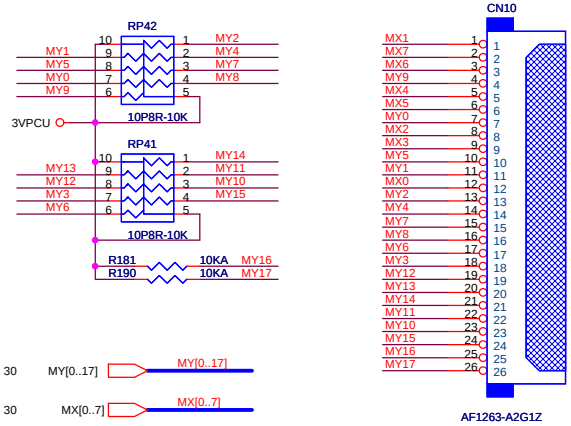
C_RESERVE FOR 2'ND SOURCE
C_CHANGE FOOTPRINT

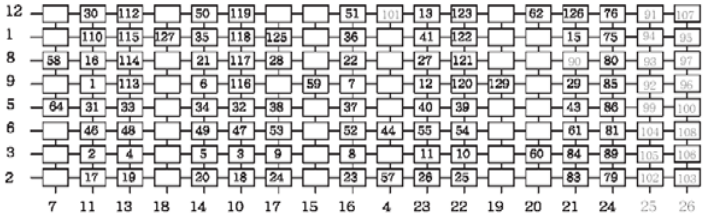






KEYBOARD PULL-UP





12		30	112		50	119			51	101	13	123		62	126	76	91	107
1		110	115	127	35	118	125		36		41	122			15	75	94	95
8	58	16	114		21	117	28		22		27	121			90	80	93	97
9		1	113		6	116		59	7		12	120	129		29	85	92	96
5	64	31	33		34	32	38		37		40	39			43	86	99	100
6		46	48		49	47	53		52	44	55	54			61	81	104	108
3		2	4		5	3	9		8		11	10		60	84	89	105	106
2		17	19		20	18	24		23	57	26	25		83	79	102	103	
	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26

NB5/RD2/HW1

PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KEYBOARD/TP	3A

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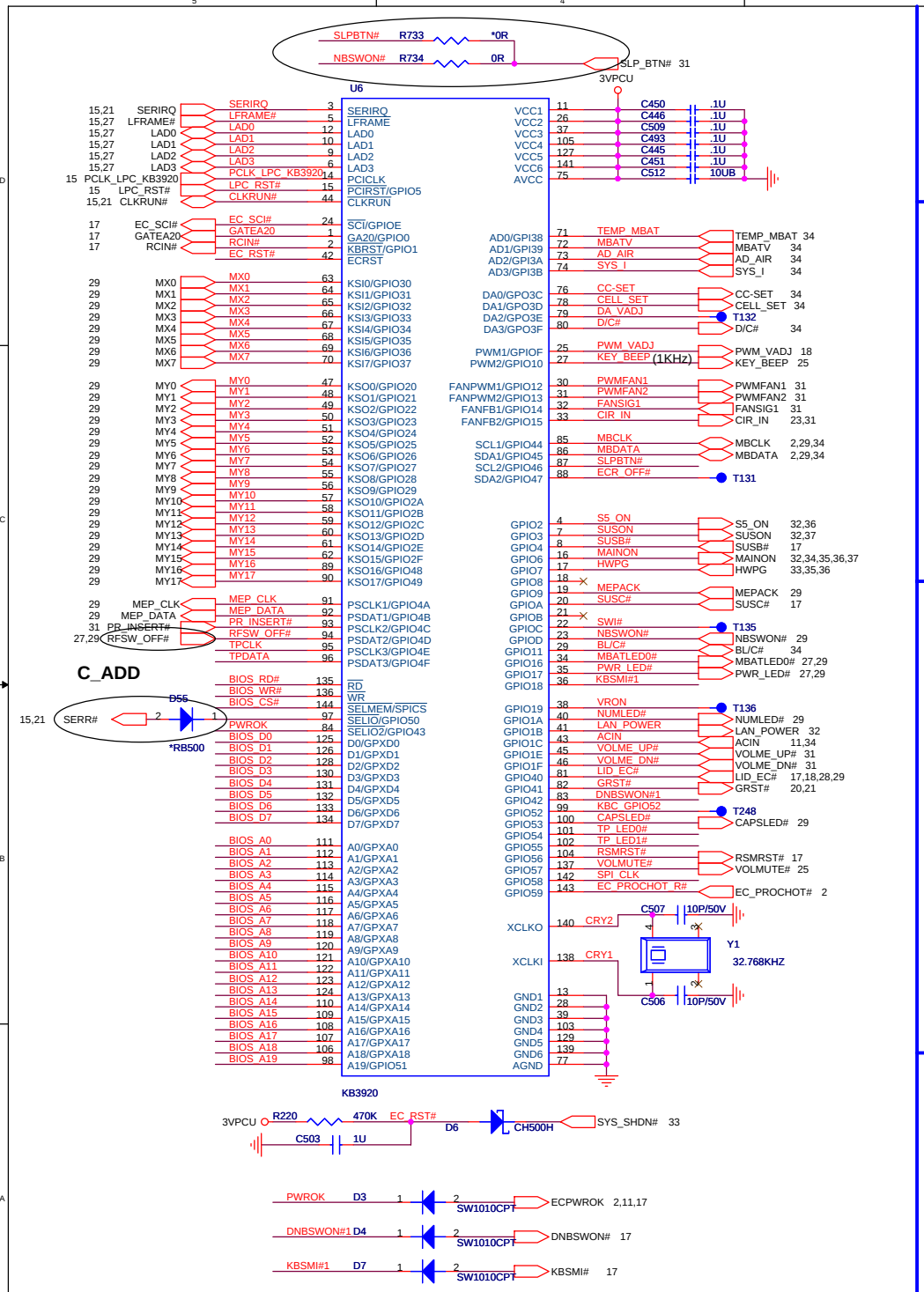
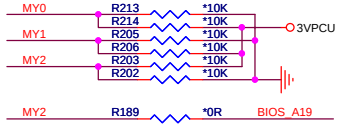
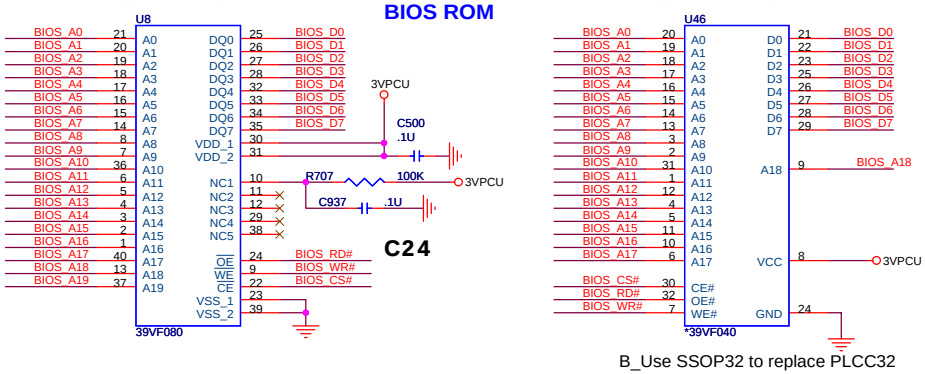


STRAP PIN

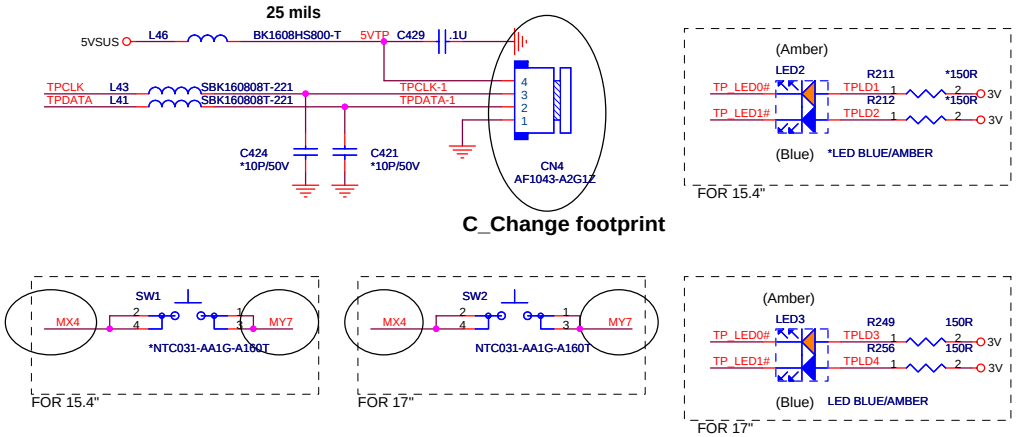
MY0	47	TP_TEST: Clock Test Mode Low: Test Mode. HIGH: 32kHz clock in normal runing
MY1	48	TP_PLL: DPLL Test Mode Low: Test Mode. HIGH: Normal operation
MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

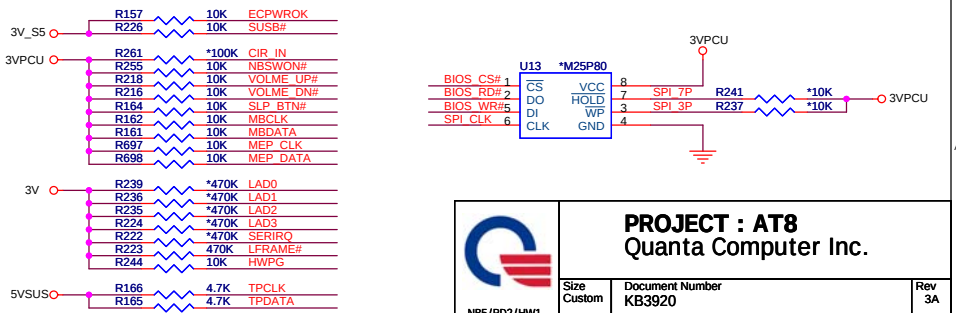


BIOS ROM



TOUCH PAD CONNECTOR





PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3920	3A

NB5/RD2/HW1

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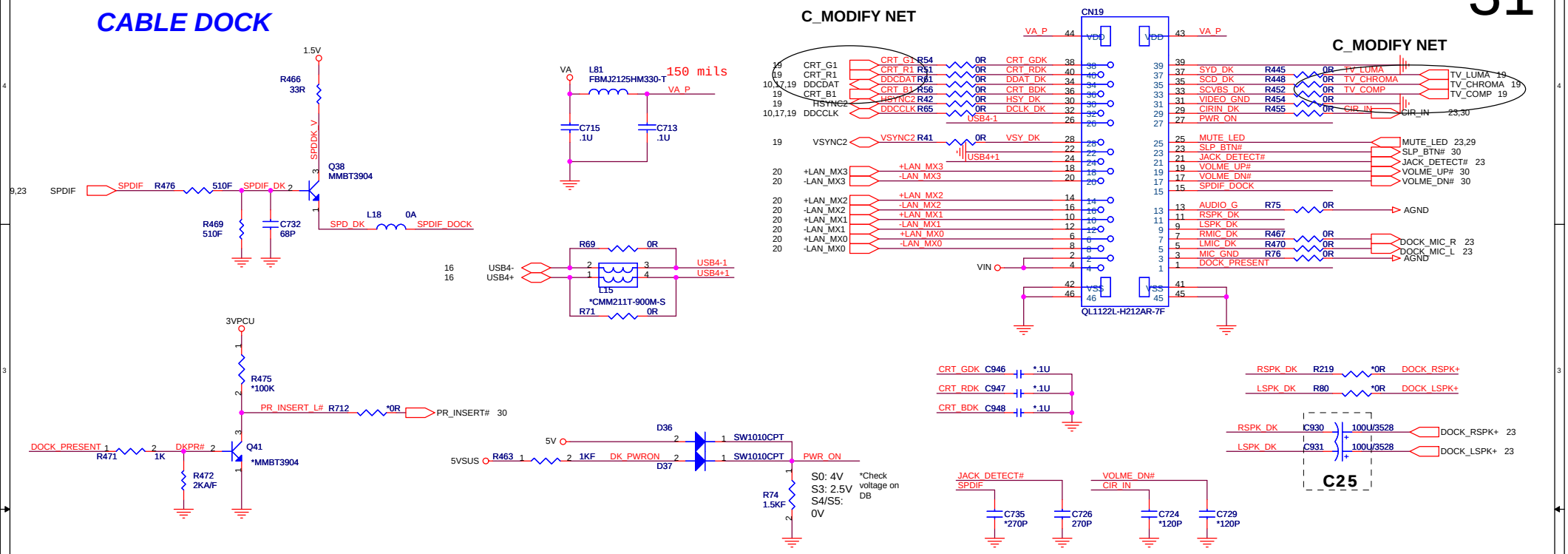
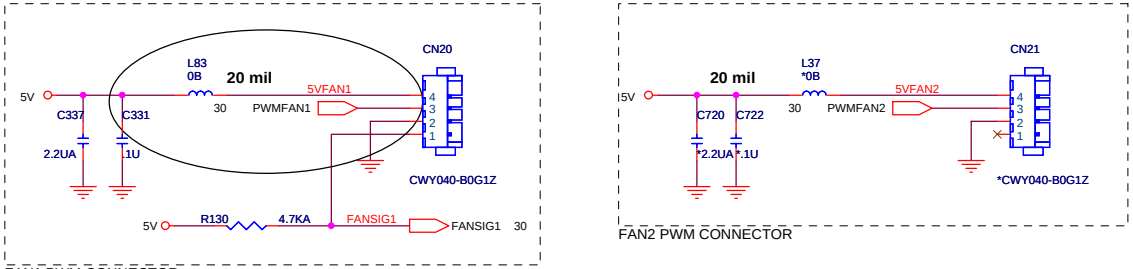
CABLE DOCK



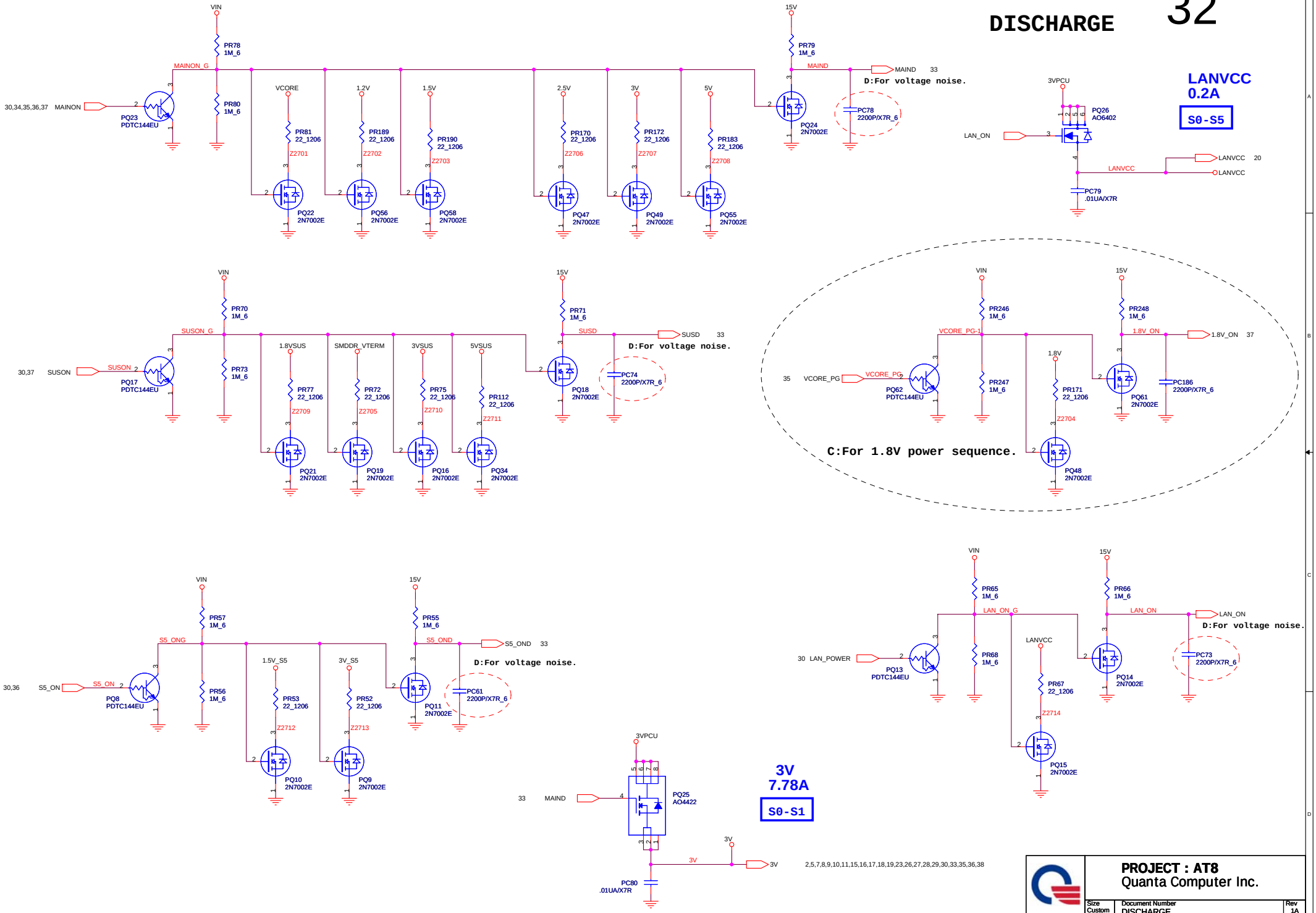
FAN



NB5/RD2/HW1	**PROJECT : AT8** Quanta Computer Inc.	
Size Custom	Document Number CABLE DOCKING	Rev 3A
	Date: Wednesday, June 14, 2006	Sheet 31 of 39

DISCHARGE

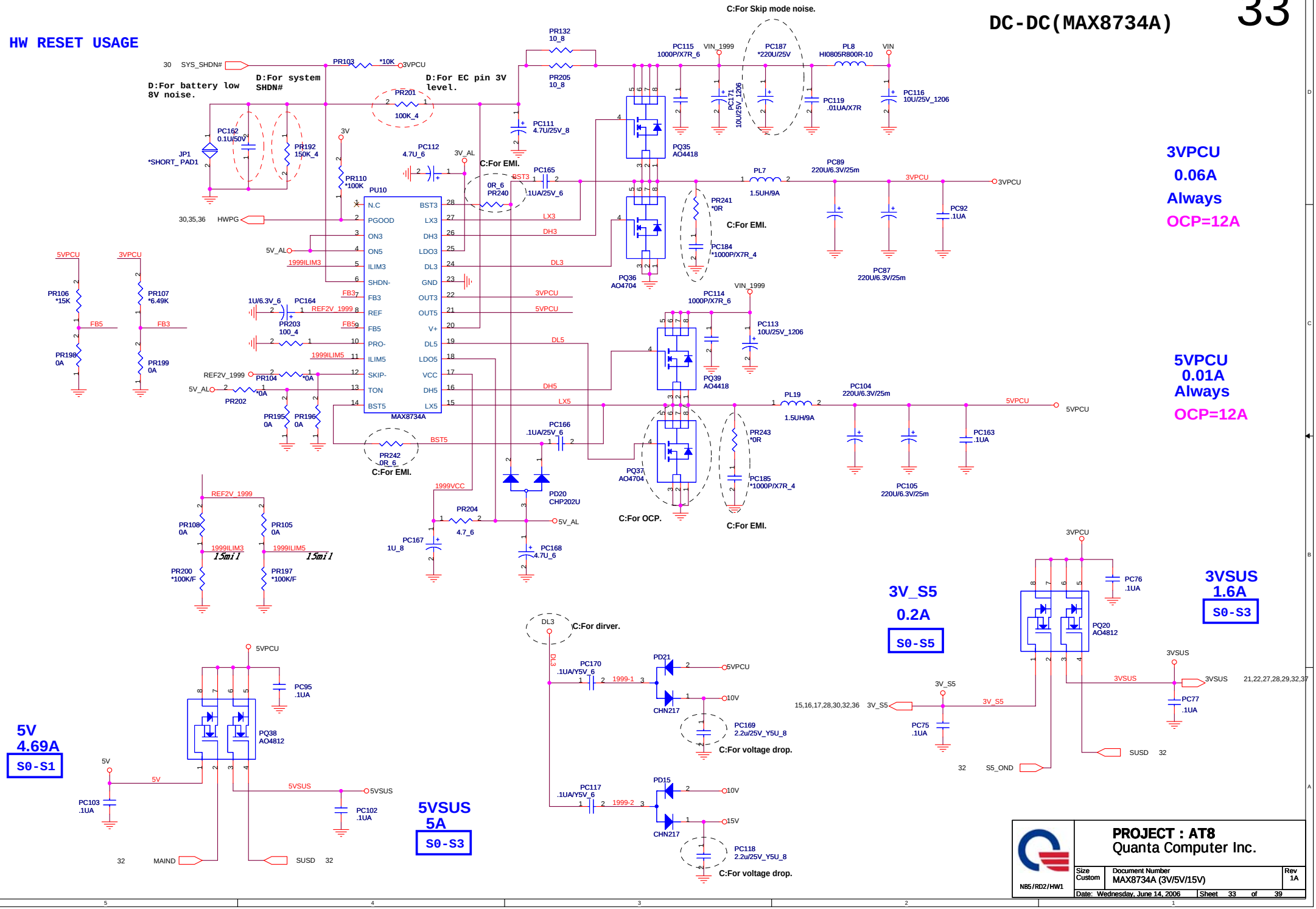
32



NB5/RD2/HW1	PROJECT : AT8 Quanta Computer Inc.	
Size Custom	Document Number DISCHARGE	Rev 1A
Date: Wednesday, June 14, 2006	Sheet 32 of 39	

DC-DC(MAX8734A)

HW RESET USAGE



NB5/RD2/HW1	**PROJECT : AT8** Quanta Computer Inc.	
Size Custom	Document Number MAX8734A (3V/5V/15V)	Rev 1A
	Date: Wednesday, June 14, 2006	Sheet 33 of 39

Adapter 19V/3.4A/65W 4.75A/90W

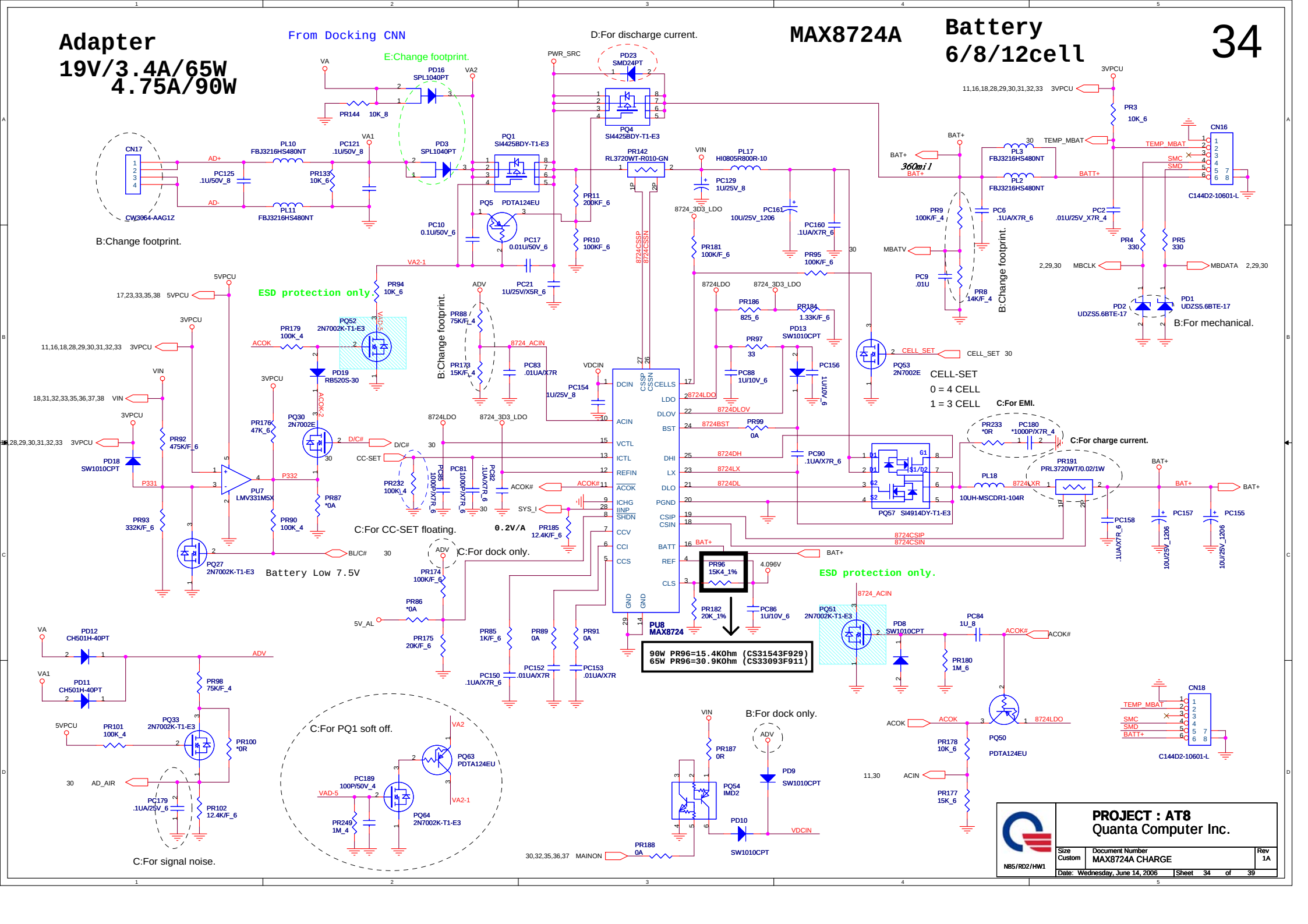
From Docking CNN

E:Change footprint.

D:For discharge current.

MAX8724A

Battery 6/8/12cell



PROJECT : AT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX8724A CHARGE	1A

NB5/RD2/HW1

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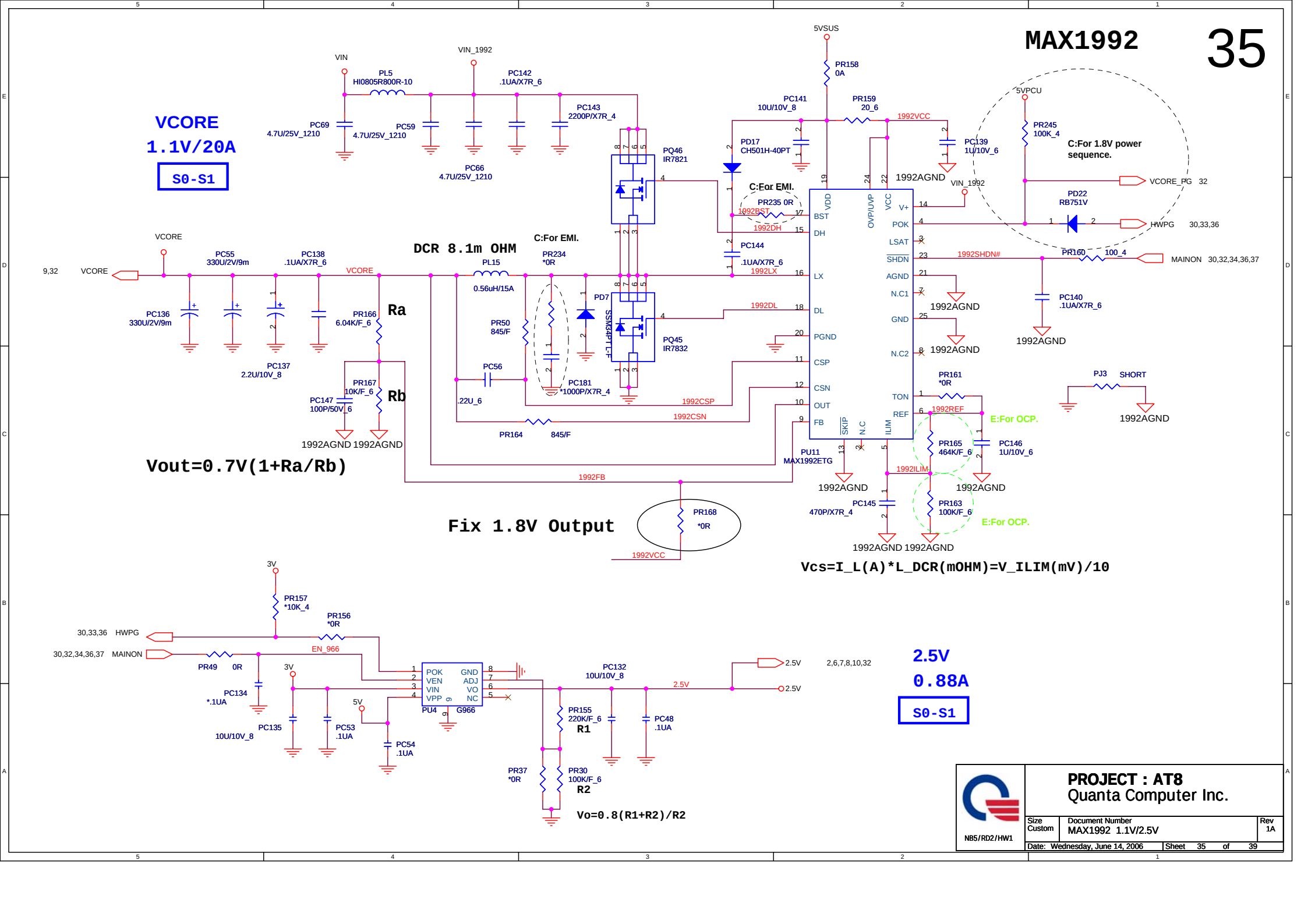
VCORE
1.1V/20A
S0-S1
VIN
PL5
HI0805R800R-10
VIN_1992
PC142
.1UA/X7R_6
PC143
2200P/X7R_4
PC69
4.7U/25V_1210
PC59
4.7U/25V_1210
PC66
4.7U/25V_1210
PQ46
IR7821
5VSUS
PR158
0A
PC141
10U/10V_8
PR159
20_6
1992VCC
PD17
CH501H-40PT
PC139
1U/10V_6
1992AGND
5VPCU
PR245
100K_4
C:For 1.8V power sequence.
VCORE_PG 32
PD22
RB751V
HWPG 30,33,36
C:For EMI.
PR235 0R
1992BST
1992DH
PC144
.1UA/X7R_6
1992LX
1992DL
VDD
BST
DH
LX
DL
PGND
CSP
CSN
OUT
FB
OVP/UVP
VCC
V+
POK
LSAT
SHDN
AGND
N.C1
GND
N.C2
TON
REF
SKIP
N.C
ILIM
PU11
MAX1992ETG
1992SHDN#
PR160
100_4
MAINON 30,32,34,36,37
PC140
.1UA/X7R_6
9,32 VCORE
PC55
330U/2V/9m
PC138
.1UA/X7R_6
PC136
330U/2V/9m
PC137
2.2U/10V_8
DCR 8.1m OHM
PL15
0.56uH/15A
C:For EMI.
PR234
*0R
PD7
SSM34PT-F
PQ45
IR7832
PR166
6.04K/F_6
Ra
PR167
10K/F_6
Rb
PC147
100P/50V_6
PR50
845/F
PC56
.22U_6
PC181
*1000P/X7R_4
1992CSP
1992CSN
PR164
845/F
1992AGND 1992AGND
Vout=0.7V(1+Ra/Rb)
1992FB
PR168
*0R
1992VCC
Fix 1.8V Output
PR161
*0R
1992REF
E:For OCP.
PR165
464K/F_6
PC146
1U/10V_6
1992ILIM
PR163
100K/F_6
E:For OCP.
PC145
470P/X7R_4
1992AGND 1992AGND
PJ3 SHORT
1992AGND
Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10
3V
PR157
*10K_4
PR156
*0R
30,33,36 HWPG
30,32,34,36,37 MAINON
EN_966
PR49 0R
PC134
*.1UA
PC135
10U/10V_8
PC53
.1UA
PC54
.1UA
5V
POK
VEN
VIN
VPP
GND
ADJ
VO
NC
PU4 G966
PC132
10U/10V_8
2.5V
2.5V
2,6,7,8,10,32
PR155
220K/F_6
R1
PC48
.1UA
PR37
*0R
PR30
100K/F_6
R2
Vo=0.8(R1+R2)/R2
2.5V
0.88A
S0-S1
N85/RD2/HW1
PROJECT : AT8
Quanta Computer Inc.
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MAX1992 1.1V/2.5V
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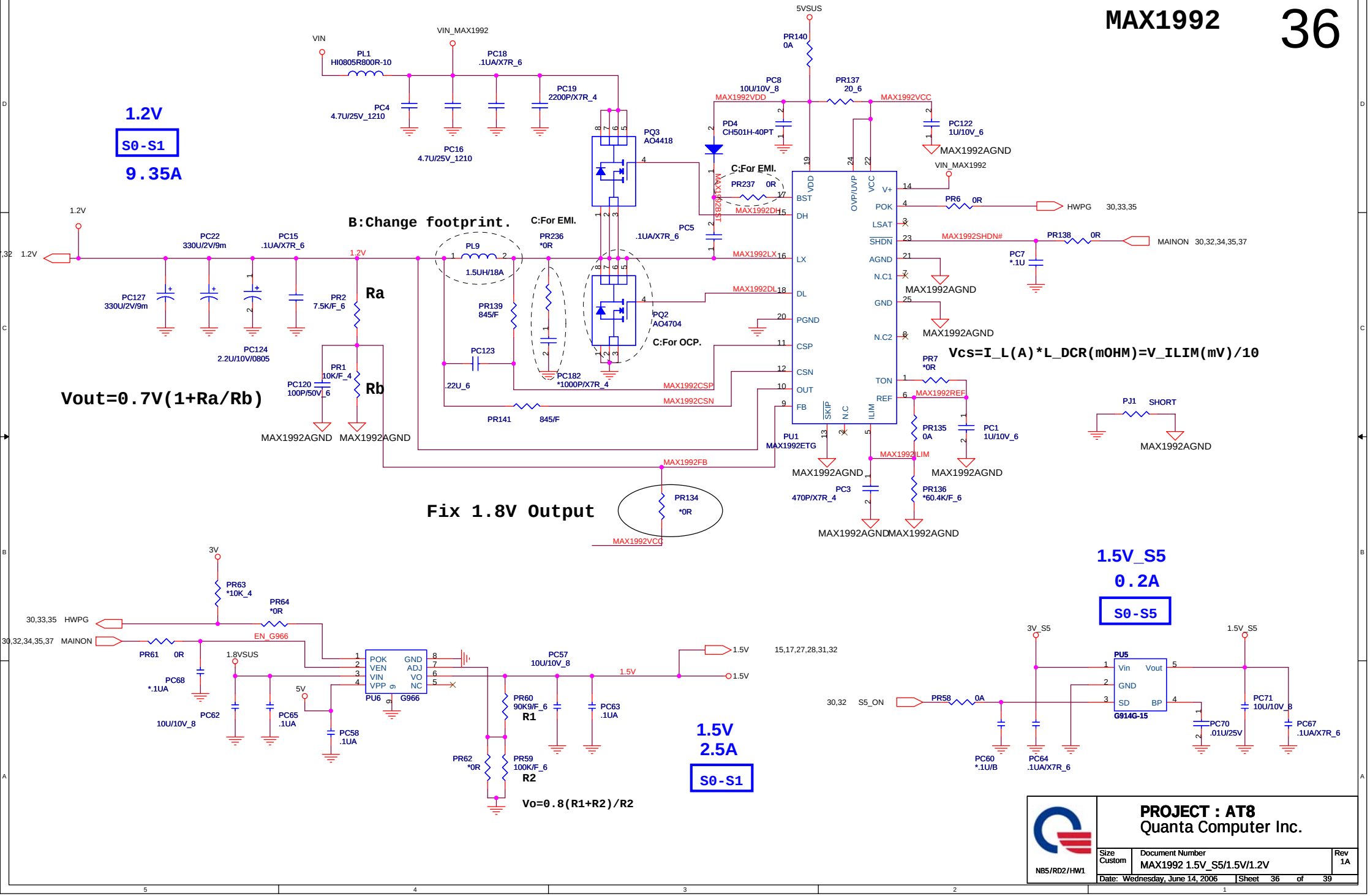

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Quanta Computer Inc.

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NB5/RD2/HW1

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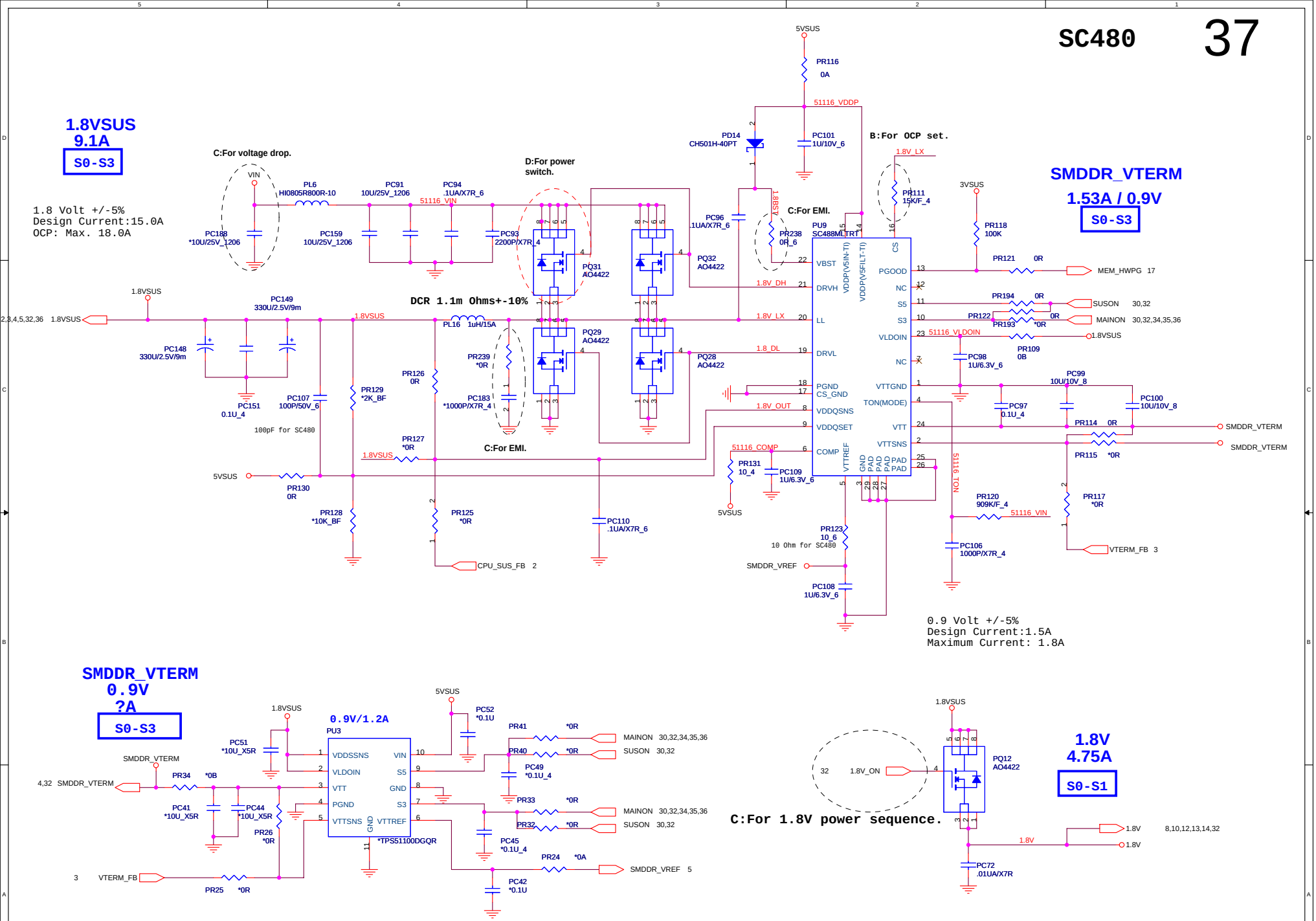

N85/RD2/HW1	PROJECT : AT8 Quanta Computer Inc.	
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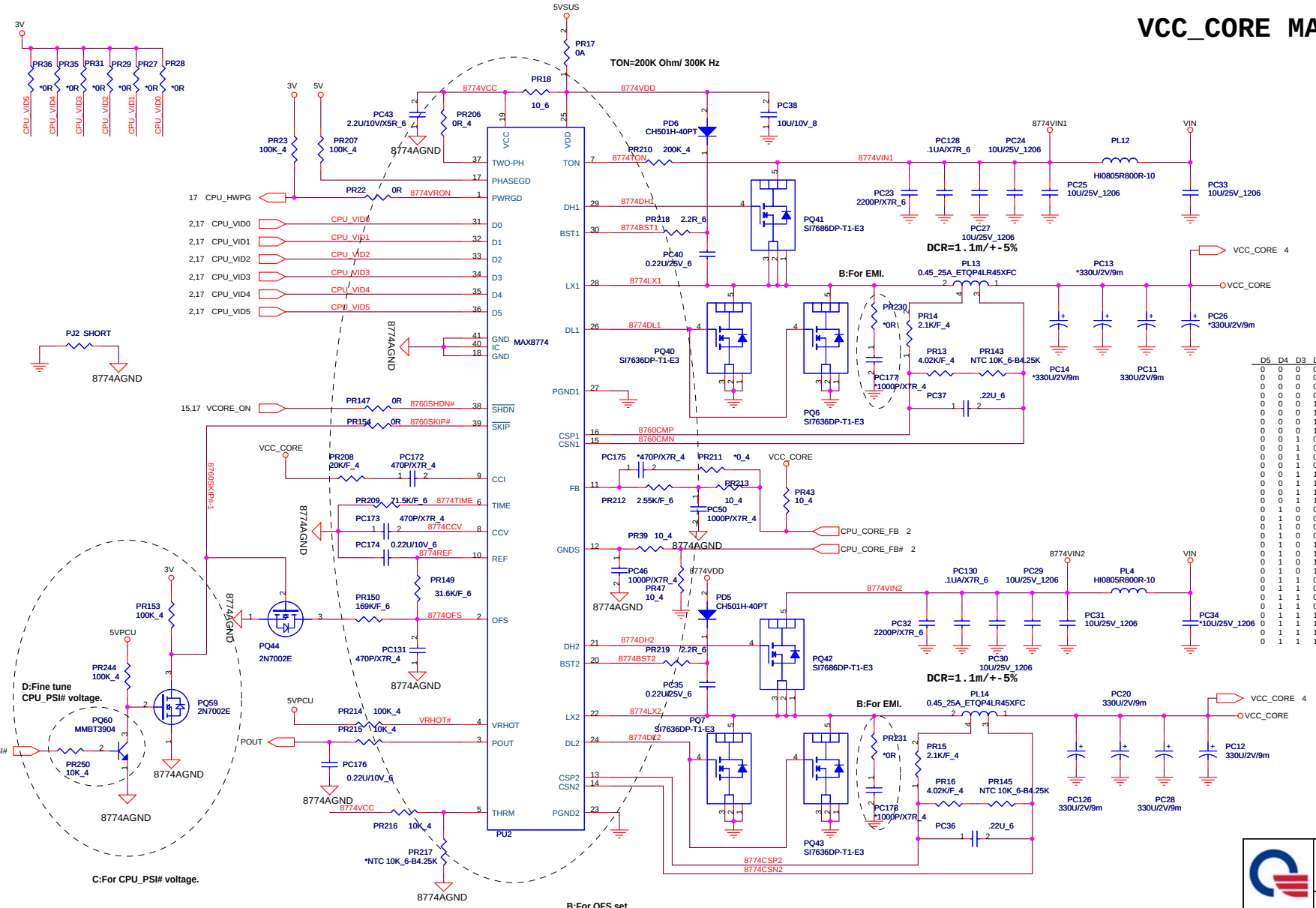
VCC_CORE MAX8774



OCP=44A

VCC_CORE

35A / 1.05V

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0.7625V
0	0	0	0	0	1	1.5250V	1	0	0	0	0	1	0.7500V
0	0	0	0	1	0	1.5000V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	1	1.4750V	1	0	0	0	1	1	0.7250V
0	0	0	1	0	0	1.4500V	1	0	0	1	0	0	0.7125V
0	0	0	1	0	1	1.4250V	1	0	0	1	0	1	0.7000V
0	0	0	1	1	0	1.4000V	1	0	0	1	1	0	0.6875V
0	0	0	1	1	1	1.3750V	1	0	0	1	1	1	0.6750V
0	0	1	0	0	0	1.3500V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	1	1.3250V	1	0	1	0	0	1	0.6500V
0	0	1	0	1	0	1.3000V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	1	1.2750V	1	0	1	0	1	1	0.6250V
0	0	1	1	0	0	1.2500V	1	0	1	1	0	0	0.6125V
0	0	1	1	0	1	1.2250V	1	0	1	1	0	1	0.6000V
0	0	1	1	1	0	1.2000V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	1	1.1750V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.1500V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.1250V	1	1	0	0	0	1	0.5500V
0	1	0	0	1	0	1.1000V	1	1	0	0	1	0	0.5375V
0	1	0	0	1	1	1.0750V	1	1	0	0	1	1	0.5250V
0	1	0	1	0	0	1.0500V	1	1	0	1	0	0	0.5125V
0	1	0	1	0	1	1.0250V	1	1	0	1	0	1	0.5000V
0	1	0	1	1	0	1.0000V	1	1	0	1	1	0	0.4875V
0	1	0	1	1	1	0.9750V	1	1	0	1	1	1	0.4750V
0	1	1	0	0	0	0.9500V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.9250V	1	1	1	0	0	1	0.4500V
0	1	1	0	1	0	0.9000V	1	1	1	0	1	0	0.4375V
0	1	1	0	1	1	0.8750V	1	1	1	0	1	1	0.4250V
0	1	1	1	0	0	0.8500V	1	1	1	1	0	0	0.4125V
0	1	1	1	0	1	0.8250V	1	1	1	1	0	1	0.4000V
0	1	1	1	1	0	0.8000V	1	1	1	1	1	0	0.3875V
0	1	1	1	1	1	0.7750V	1	1	1	1	1	1	0.3750V

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NB5/RD2/HW1

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