TABLE OF CONTENTS

Revisions			Approvals			
REV	ECN NO.	Description Of Change	DATE	DFTG.	ENGR.	REL.

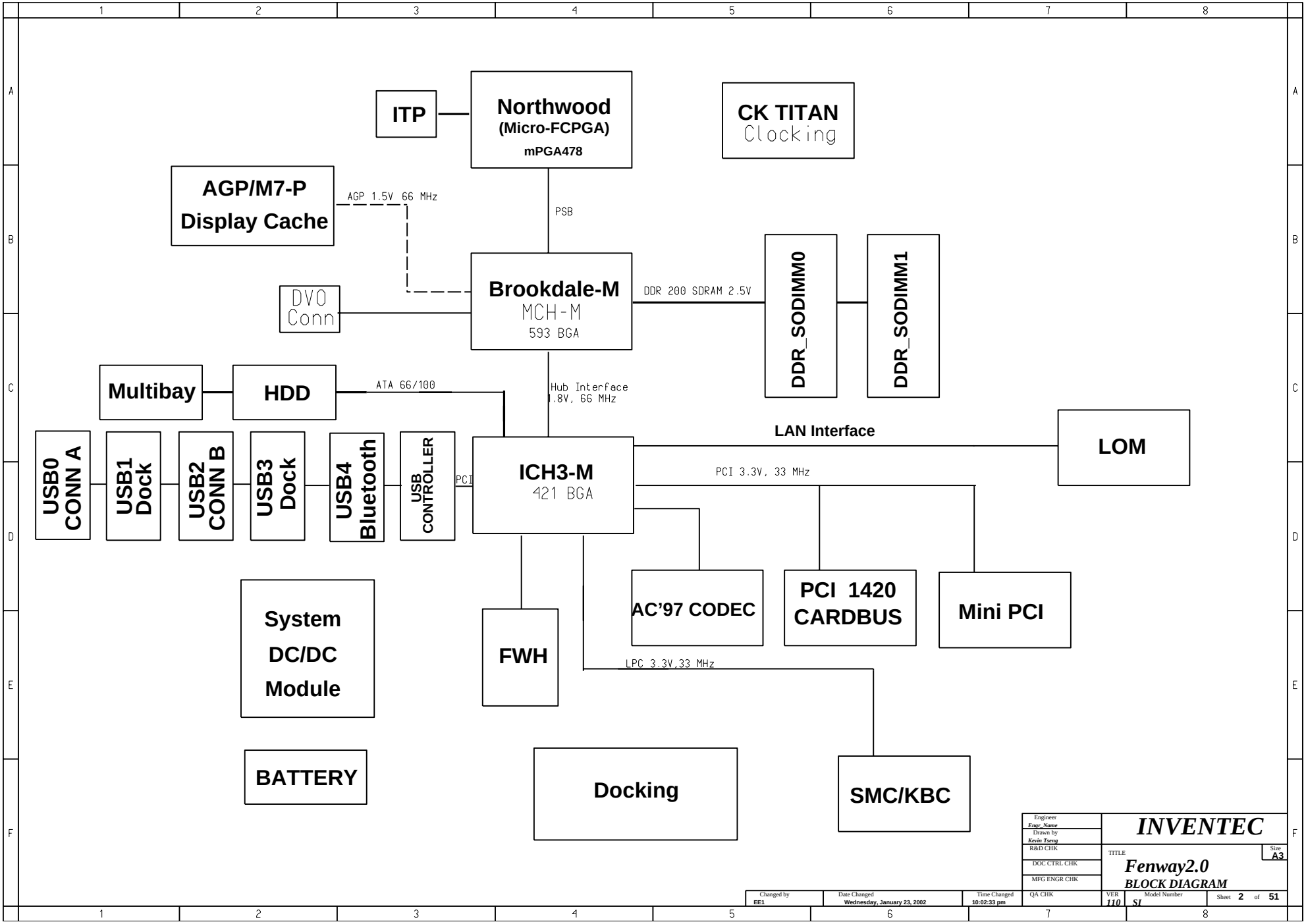
PAGE

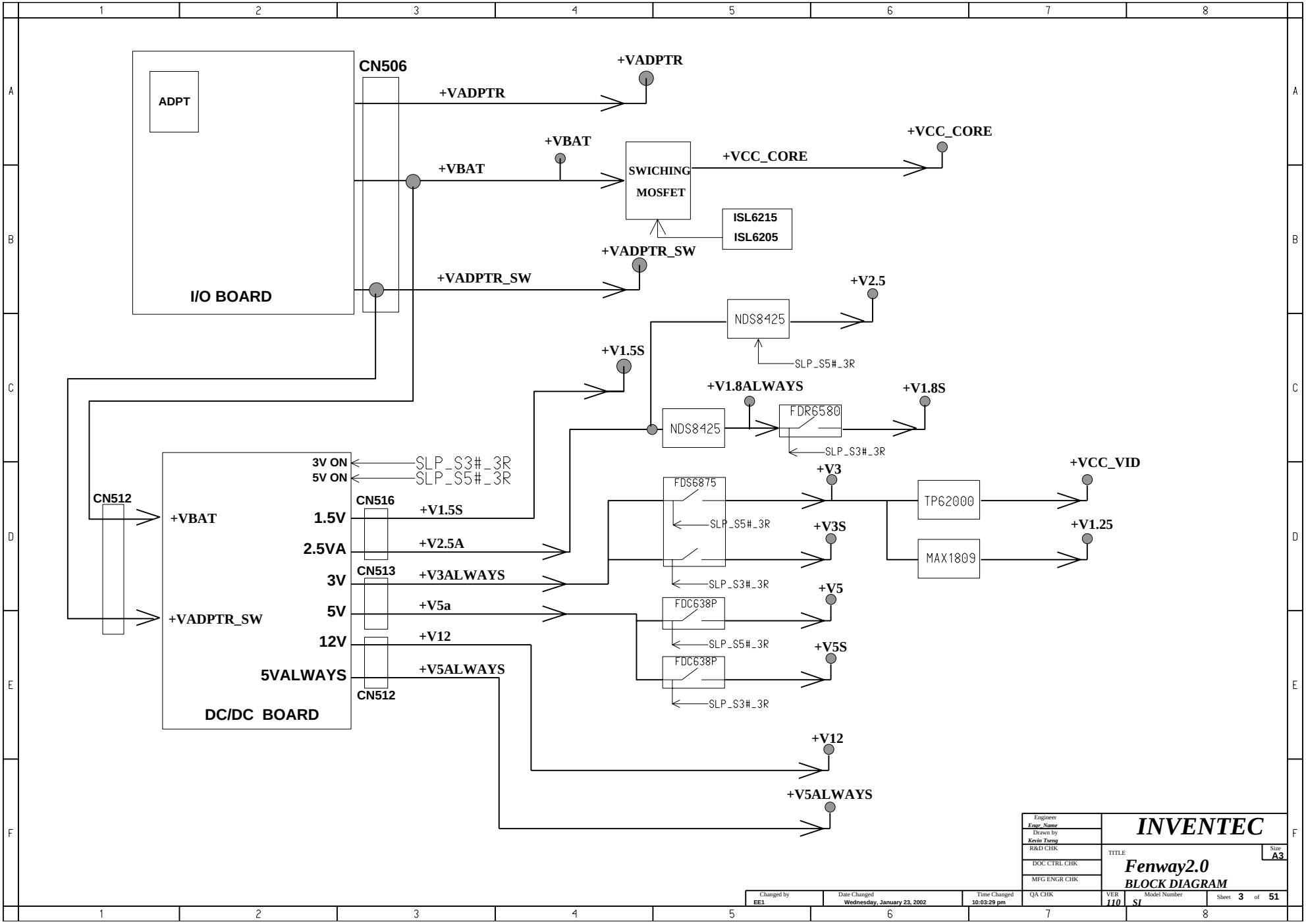
4 - CLOCK GENERATOR
5-7 - NORTHWOOD PROCESSOR
8-10 - BROOKDALE
11-14 - DDR
15,16 - ATI_M7_P
17 - VIDEO RAM
18 - CRT,LCD,INVERTER CONNECTOR INTERFACE
19,20 - ICH3-M
21 - KAHUNA
22 - FWH & EEPROM
23 - SERIAL , PARALLEL AND PS2 PORTS
24 - CARDBUS CONTROLLER
25 - PC CARD SLOT
26 - AC97 CODEC
27 - EQ & MIC JACK
28 - AUDIO AMP & HP JACK
29 - HDD AND MB1 PWR AND SWITCH
30 - HDD CONNECTOR
31 - MULTIBAY

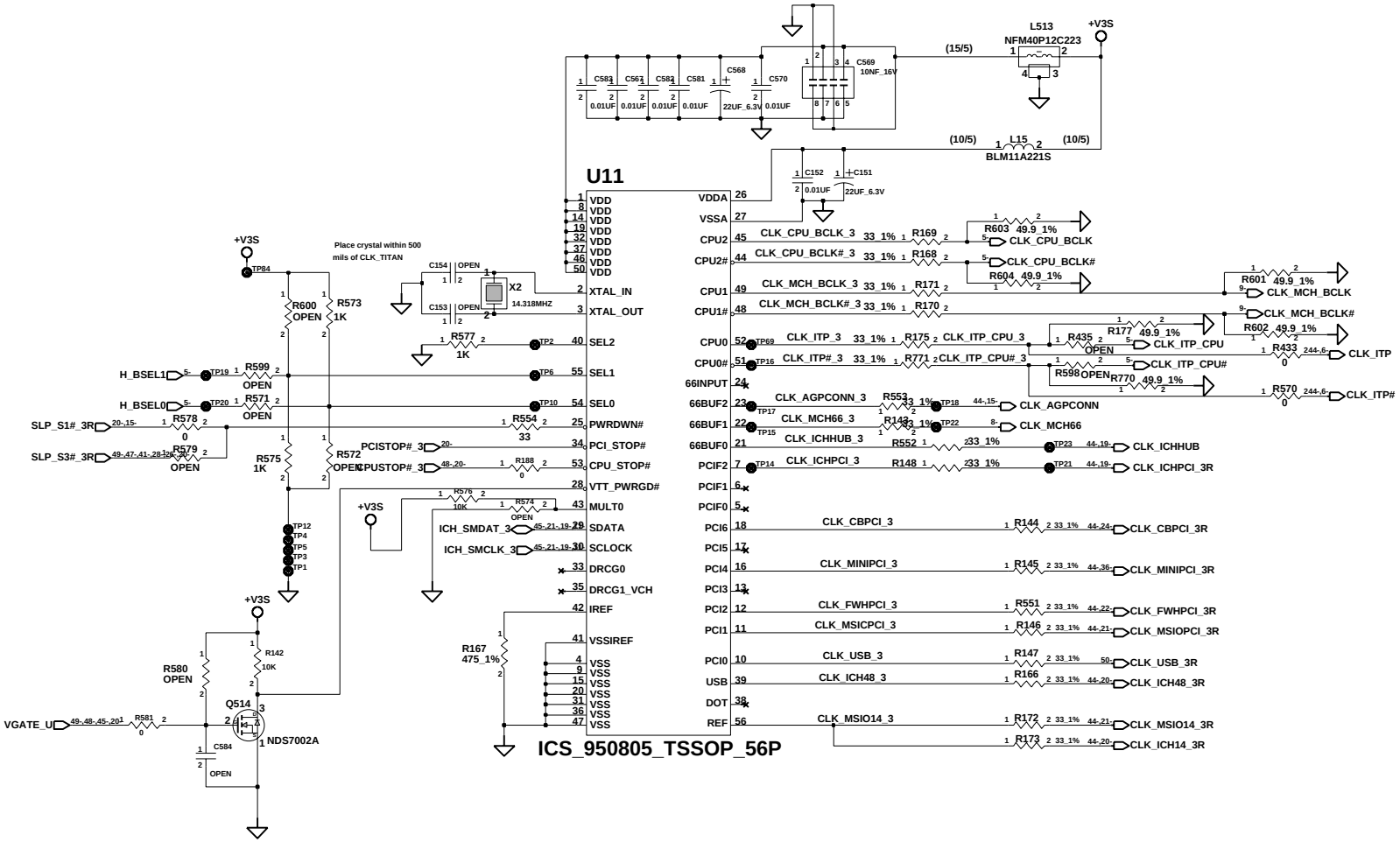
PAGE

32 - DUALBAY
33 - INT KBD./ POINTING DEVICE
34 - LID SWITCH/LEDS
35 - DOCKING CONNCTOR
36 - MINI PCI
37 - USB, IR
38 - BLUETOOTH
39 - THERMAL SENSOR & FAN CONTROLLER
40 - ADAPTER SENSE CIRCUIT & CLAMP CIRCUIT
41 - PWR MODULE CONN
42 - DECOUPLING CAPS
43 - DRILL HOLE
44 - HIGH SPEED
45 - PULL UPS
46 - LAN INTERFACE
47-49 - POWER
50 - USB2.0
51 - IO BOARD

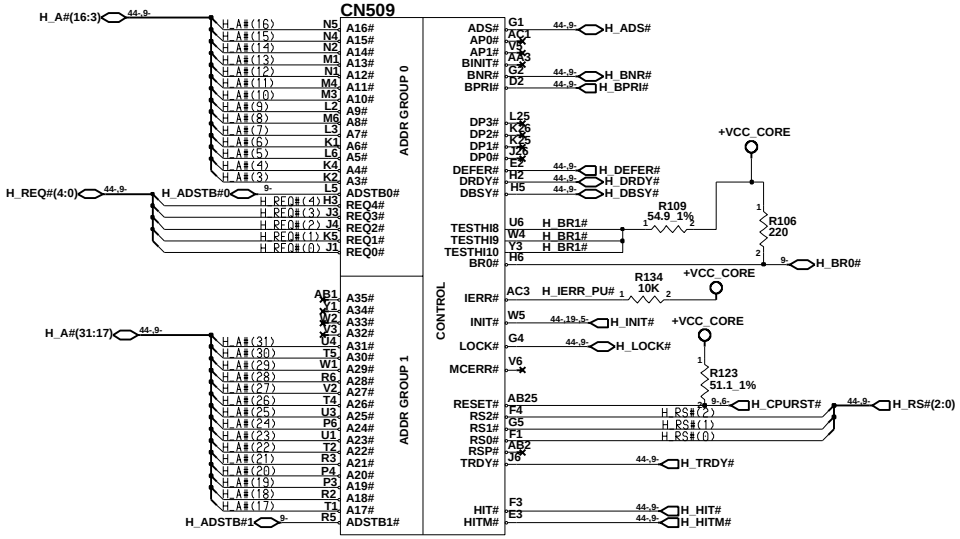
Engineer *Engr_Name*					**INVENTEC**	
Drawn by *Kevin Tseng*						
R&D CHK					TITLE **Fenway2.0**	Size **A3**
DOC CTRL CHK					**TABLE OF CONTENTS**	
MFG ENGR CHK						
	Changed by **EE1**	Date Changed **Friday, April 19, 2002**	Time Changed **9:58:54 am**	QA CHK	VER *110* / Model Number *SI*	Sheet **1** of **51**


ITP
Northwood
(Micro-FCPGA)
mPGA478
CK TITAN
Clocking
AGP/M7-P
Display Cache
AGP 1.5V 66 MHz
PSB
Brookdale-M
MCH-M
593 BGA
DVO
Conn
DDR 200 SDRAM 2.5V
DDR_SODIMM0
DDR_SODIMM1
Multibay
HDD
ATA 66/100
Hub Interface
1.8V, 66 MHz
LAN Interface
LOM
USB0
CONN A
USB1
Dock
USB2
CONN B
USB3
Dock
USB4
Bluetooth
USB
CONTROLLER
PCI
ICH3-M
421 BGA
PCI 3.3V, 33 MHz
AC'97 CODEC
PCI 1420
CARDBUS
Mini PCI
System
DC/DC
Module
FWH
LPC 3.3V,33 MHz
BATTERY
Docking
SMC/KBC
Engineer
Engr_Name
Drawn by
Kevin Tseng
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
INVENTEC
TITLE
Fenway2.0
BLOCK DIAGRAM
Size
A3
Changed by
EE1
Date Changed
Wednesday, January 23, 2002
Time Changed
10:02:33 pm
QA CHK
VER
110
Model Number
SI
Sheet 2 of 51


ADPT
I/O BOARD
CN506
+VADPTR
+VADPTR
+VBAT
+VBAT
SWICHING MOSFET
+VCC_CORE
+VCC_CORE
ISL6215
ISL6205
+VADPTR_SW
+VADPTR_SW
+V2.5
NDS8425
SLP_S5#_3R
+V1.5S
+V1.8ALWAYS
+V1.8S
NDS8425
FDR6580
SLP_S3#_3R
3V ON
5V ON
SLP_S3#_3R
SLP_S5#_3R
CN512
CN516
+VBAT
1.5V
+V1.5S
2.5VA
+V2.5A
CN513
3V
+V3ALWAYS
+VADPTR_SW
5V
+V5a
12V
+V12
5VALWAYS
+V5ALWAYS
CN512
DC/DC BOARD
FDS6875
SLP_S5#_3R
SLP_S3#_3R
+V3
+V3S
TP62000
MAX1809
+VCC_VID
+V1.25
FDC638P
SLP_S5#_3R
+V5
FDC638P
SLP_S3#_3R
+V5S
+V12
+V5ALWAYS
Engineer
Engr_Name
Drawn by
Kevin Tseng
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
INVENTEC
TITLE
Fenway2.0
BLOCK DIAGRAM
Size
A3
Changed by
EE1
Date Changed
Wednesday, January 23, 2002
Time Changed
10:03:29 pm
QA CHK
VER
110
Model Number
SI
Sheet 3 of 51

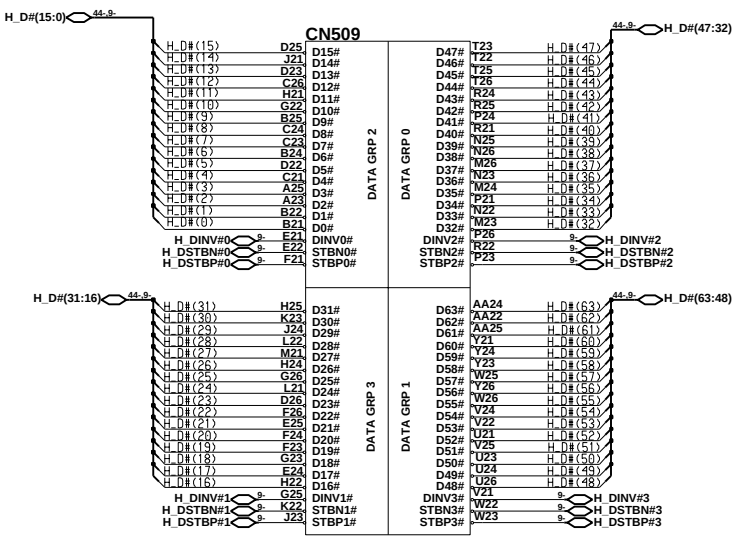


Engineer Engr_Name	INVENTEC		
Drawn by Kevin Tseng	TITLE Fenway2.0 CLK TITAN		Size A3
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK			
Changed by EE1	Date Changed Tuesday, April 16, 2002	Time Changed 1:33:57 pm	QA CHK
VER 110	Model Number SI	Sheet 4 of 51	



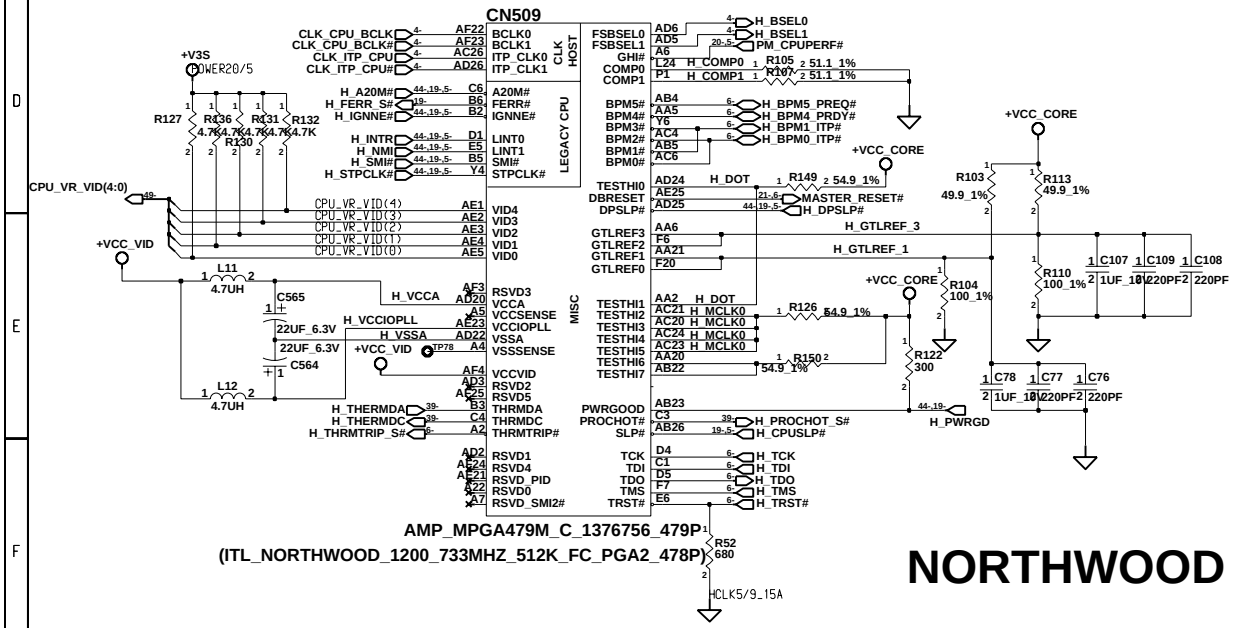
AMP_MPGA479M_C_1376756_479P

(ITL_NORTHWOOD_1200_733MHZ_512K_FC_PGA2_478P)



AMP_MPGA479M_C_1376756_479P

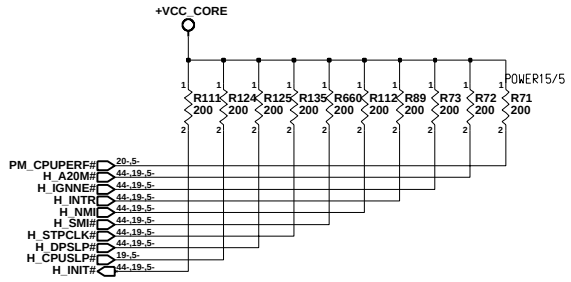
(ITL_NORTHWOOD_1200_733MHZ_512K_FC_PGA2_478P)



AMP_MPGA479M_C_1376756_479P

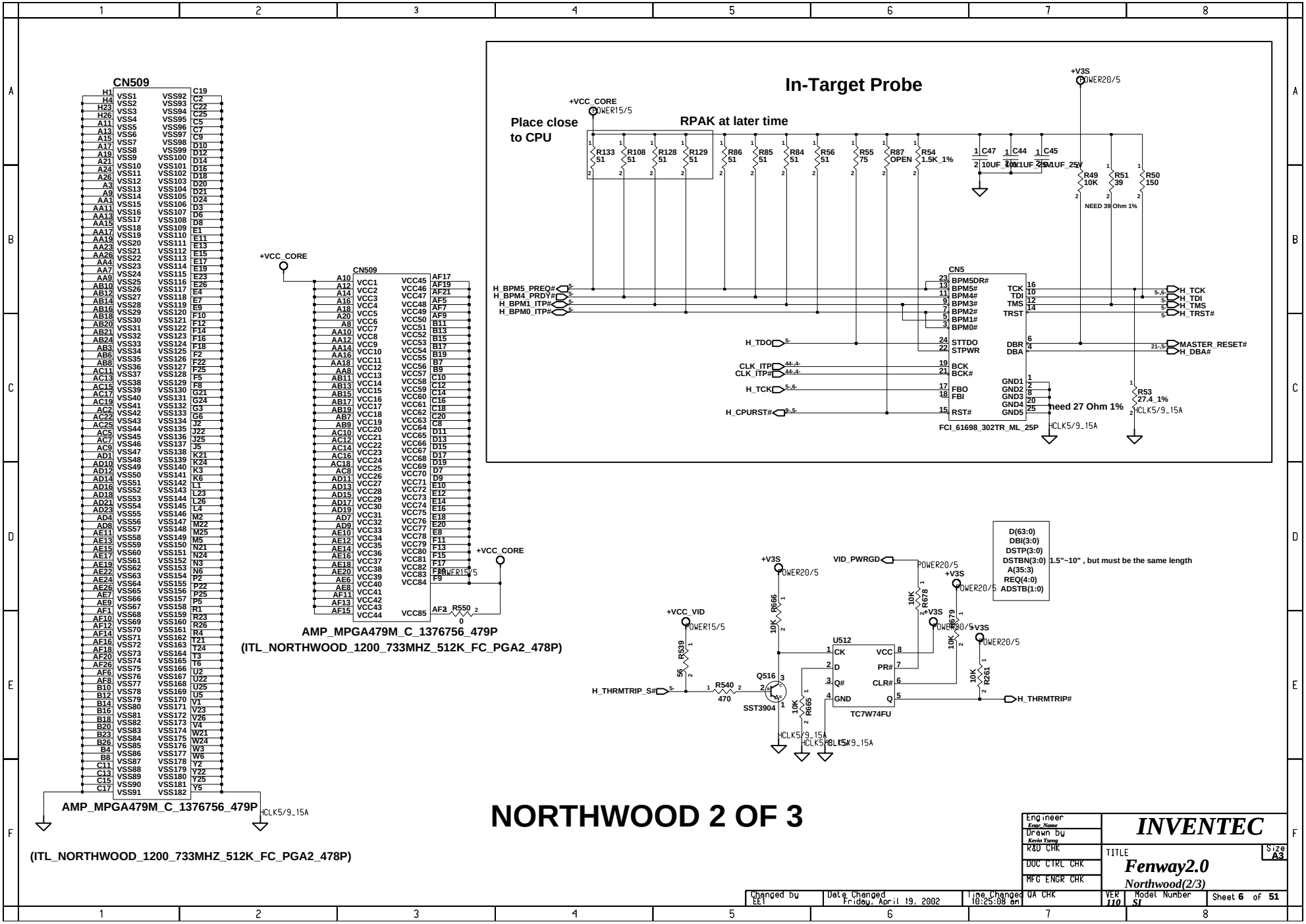
(ITL_NORTHWOOD_1200_733MHZ_512K_FC_PGA2_478P)

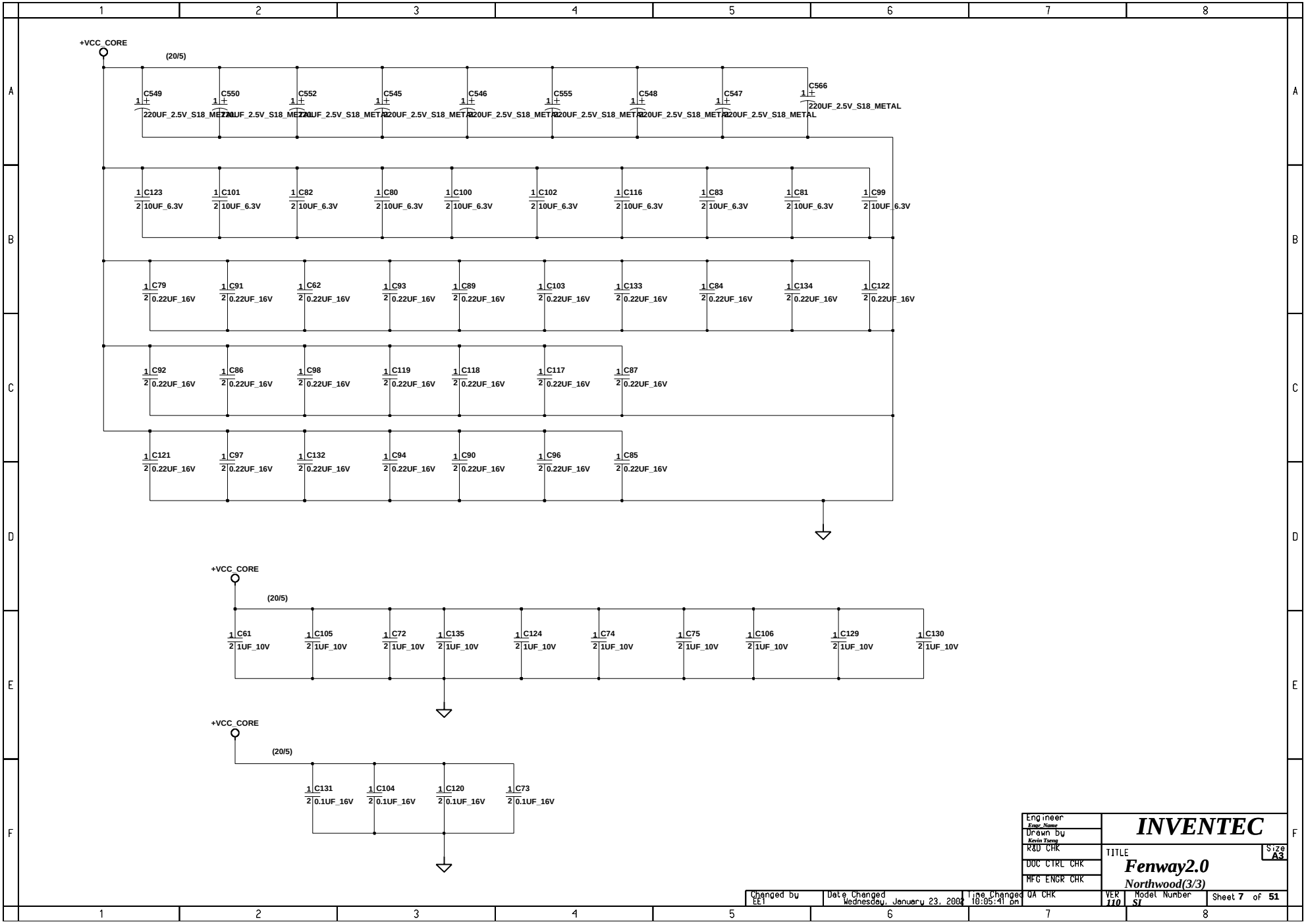
200 Ohm is recommended INSTEAD OF 300 Ohm (RPAK). Placement: 3" from CPU (Max)

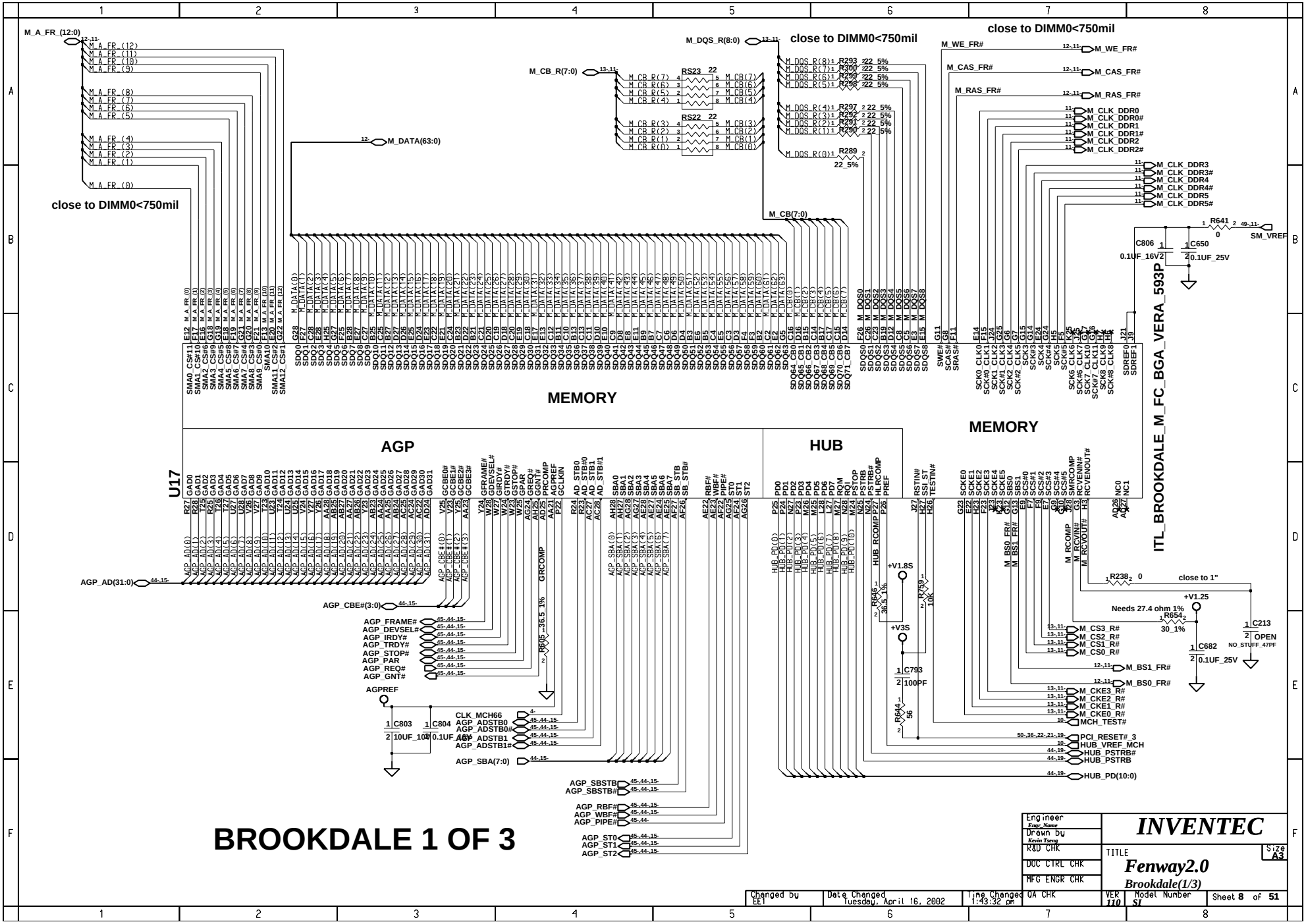


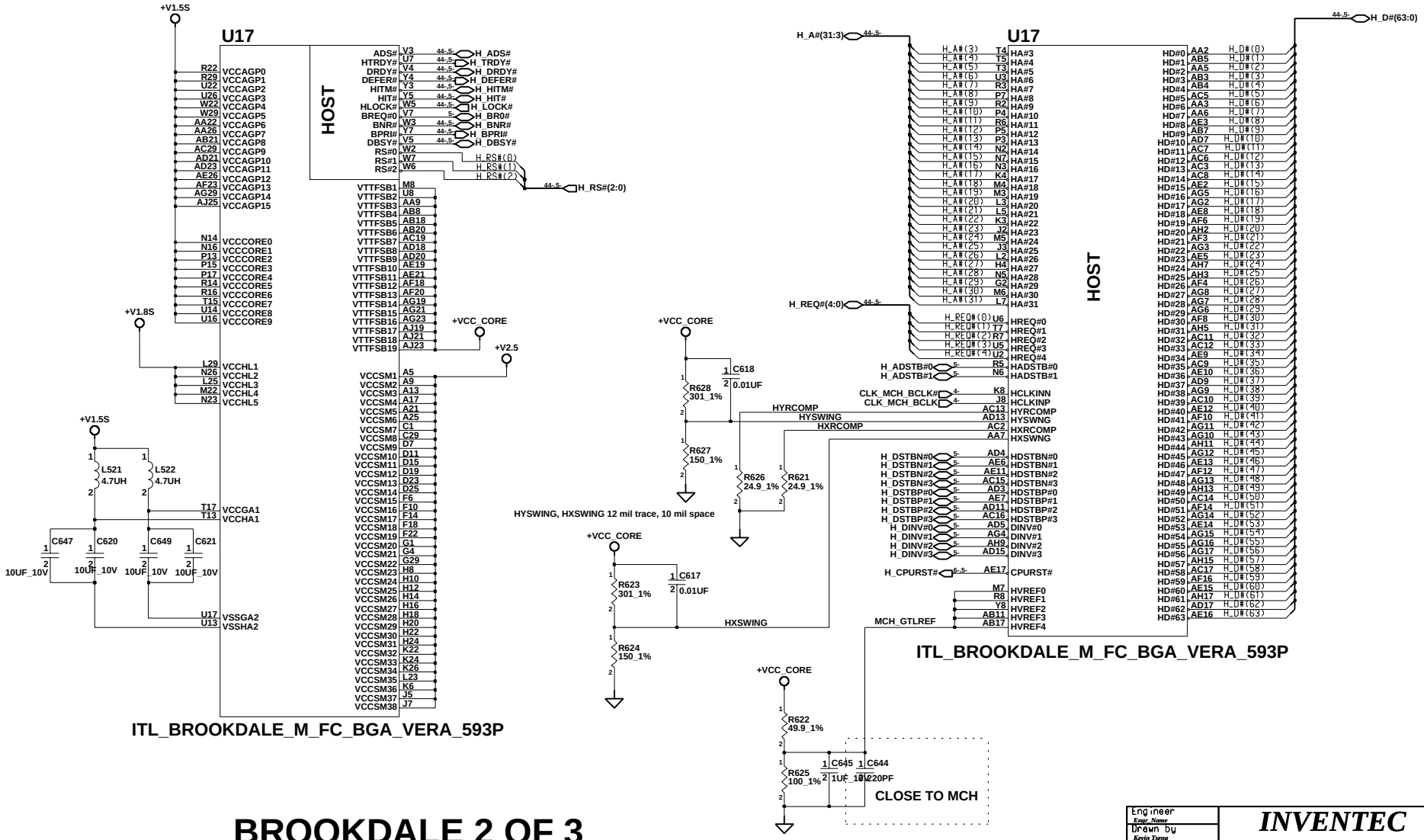
NORTHWOOD 1 OF 3

Engineer Engr_Name	INVENTEC		
Drawn by Kevin Tseng			
R&D CHK	TITLE Fenway2.0 Northwood(1/3)		Size A3
DOC CTRL CHK			
MFG ENGR CHK			
Changed by EE1	Date Changed Monday, May 6, 2002	Time Changed 10:20:54 am	QA CHK
VER 110	Model Number SI	Sheet 5 of 51	


CN509
AMP_MPGA479M_C_1376756_479P
(ITL_NORTHWOOD_1200_733MHZ_512K_FC_PGA2_478P)
In-Target Probe
Place close to CPU
RPAK at later time
+VCC_CORE
+V3S
NEED 39 Ohm 1%
need 27 Ohm 1%
CN5
FCI_61698_302TR_ML_25P
H_BPM5_PREQ#
H_BPM4_PRDY#
H_BPM1_ITP#
H_BPM0_ITP#
H_TDO
CLK_ITP
CLK_ITP#
H_TCK
H_CPURST#
H_TCK
H_TDI
H_TMS
H_TRST#
MASTER_RESET#
H_DBA#
D(63:0)
DBI(3:0)
DSTP(3:0)
DSTBN(3:0)
A(35:3)
REQ(4:0)
ADSTB(1:0)
1.5"~10" , but must be the same length
VID_PWRGD
+VCC_VID
H_THRMTRIP_S#
H_THRMTRIP#
Q516
SST3904
U512
TC7W74FU
NORTHWOOD 2 OF 3
INVENTEC
Fenway2.0
Northwood(2/3)
Engineer
Drawn by
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
Changed by EE1
Date Changed Friday, April 19, 2002
Time Changed 10:25:08 am
QA CHK
VER 110
Model Number SI
Sheet 6 of 51
Size A3

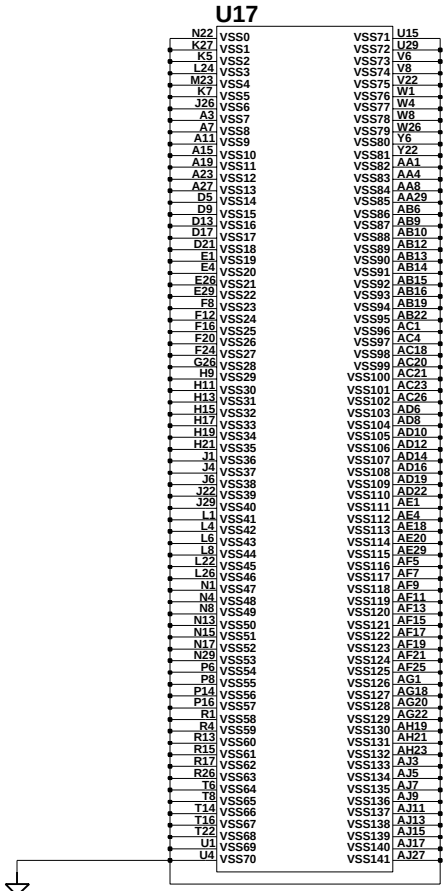

+VCC_CORE
(20/5)
C549 220UF_2.5V_S18_METAL
C550 220UF_2.5V_S18_METAL
C552 220UF_2.5V_S18_METAL
C545 220UF_2.5V_S18_METAL
C546 220UF_2.5V_S18_METAL
C555 220UF_2.5V_S18_METAL
C548 220UF_2.5V_S18_METAL
C547 220UF_2.5V_S18_METAL
C566 220UF_2.5V_S18_METAL
C123 10UF_6.3V
C101 10UF_6.3V
C82 10UF_6.3V
C80 10UF_6.3V
C100 10UF_6.3V
C102 10UF_6.3V
C116 10UF_6.3V
C83 10UF_6.3V
C81 10UF_6.3V
C99 10UF_6.3V
C79 0.22UF_16V
C91 0.22UF_16V
C62 0.22UF_16V
C93 0.22UF_16V
C89 0.22UF_16V
C103 0.22UF_16V
C133 0.22UF_16V
C84 0.22UF_16V
C134 0.22UF_16V
C122 0.22UF_16V
C92 0.22UF_16V
C86 0.22UF_16V
C98 0.22UF_16V
C119 0.22UF_16V
C118 0.22UF_16V
C117 0.22UF_16V
C87 0.22UF_16V
C121 0.22UF_16V
C97 0.22UF_16V
C132 0.22UF_16V
C94 0.22UF_16V
C90 0.22UF_16V
C96 0.22UF_16V
C85 0.22UF_16V
+VCC_CORE
(20/5)
C61 1UF_10V
C105 1UF_10V
C72 1UF_10V
C135 1UF_10V
C124 1UF_10V
C74 1UF_10V
C75 1UF_10V
C106 1UF_10V
C129 1UF_10V
C130 1UF_10V
+VCC_CORE
(20/5)
C131 0.1UF_16V
C104 0.1UF_16V
C120 0.1UF_16V
C73 0.1UF_16V
Engineer
Engr_Name
Drawn by
Kevin Tseng
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
INVENTEC
TITLE
Fenway2.0
Northwood(3/3)
Size
A3
Changed by
EE1
Date Changed
Wednesday, January 23, 2002
Time Changed
10:05:41 pm
QA CHK
VER
110
Model Number
SI
Sheet 7 of 51


MEMORY
AGP
HUB
U17
ITL_BROOKDALE_M_FC_BGA_VERA_593P
close to DIMM0<750mil
close to DIMM0<750mil
close to DIMM0<750mil
close to DIMM0<750mil
M_A_FR (12:0)
M_DATA(63:0)
M_DQS_R(8:0)
M_CB_R(7:0)
M_CB(7:0)
M_WE_FR#
M_CAS_FR#
M_RAS_FR#
M_CLK_DDR0
M_CLK_DDR0#
M_CLK_DDR1
M_CLK_DDR1#
M_CLK_DDR2
M_CLK_DDR2#
M_CLK_DDR3
M_CLK_DDR3#
M_CLK_DDR4
M_CLK_DDR4#
M_CLK_DDR5
M_CLK_DDR5#
SM_VREF
AGP_AD(31:0)
AGP_CBE#(3:0)
AGP_FRAME#
AGP_DEVSEL#
AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR
AGP_REQ#
AGP_GNT#
AGPREF
AGP_SBA(7:0)
AGP_SBSTB
AGP_SBSTB#
AGP_RBF#
AGP_WBF#
AGP_PIPE#
AGP_ST0
AGP_ST1
AGP_ST2
CLK_MCH66
AGP_ADSTB0
AGP_ADSTB0#
AGP_ADSTB1
AGP_ADSTB1#
HUB_PD(10:0)
HUB_PSTRB#
HUB_PSTRB
HUB_VREF_MCH
PCI_RESET# 3
MCH_TEST#
M_CS3_R#
M_CS2_R#
M_CS1_R#
M_CS0_R#
M_BS1_FR#
M_BS0_FR#
M_CKE3_R#
M_CKE2_R#
M_CKE1_R#
M_CKE0_R#
+V1.8S
+V3S
+V1.25
Needs 27.4 ohm 1%
close to 1"
R641 0
C650 0.1UF_25V
C806 0.1UF_16V2
R238 0
R654 30_1%
C682 0.1UF_25V
C213 OPEN
NO_STUFF_47PF
C793 100PF
R644 56
R646 36.5_1%
R759 10K
R605 36.5_1%
C803 10UF_10V
C804 0.1UF_16V
BROOKDALE 1 OF 3
Engineer
Drawn by
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
INVENTEC
TITLE
Fenway2.0
Brookdale(1/3)
Size A3
Changed by EE1
Date Changed Tuesday, April 16, 2002
Time Changed 1:43:32 pm
QA CHK
VER 110
Model Number SI
Sheet 8 of 51

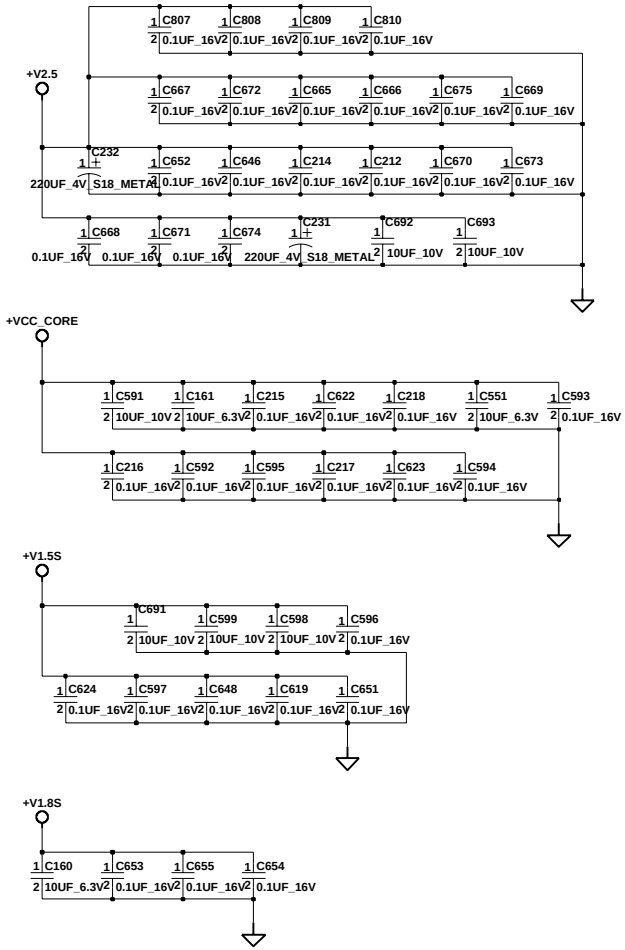


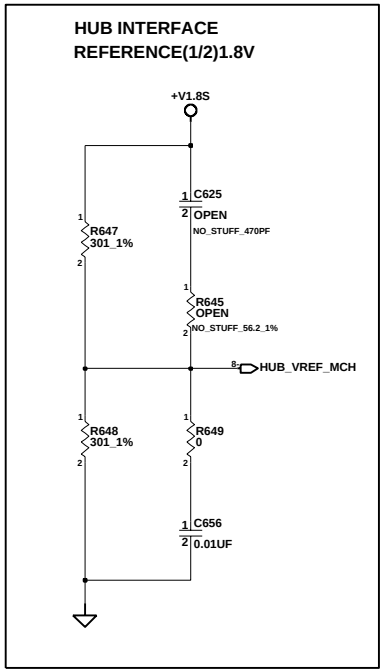
BROOKDALE 2 OF 3

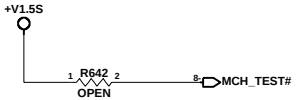
Engineer Engr_Name	INVENTEC		
Drawn by Kevin Tseng	TITLE Fenway2.0 Brookdale(2/3)		Size A3
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK			
Changed by EE1	Date Changed Wednesday, January 23, 2002	Time Changed 10:05:54 pm	QA CHK
VER 110	Model Number SI	Sheet 9 of 51	



ITL_BROOKDALE_M_FC_BGA_VERA_593P

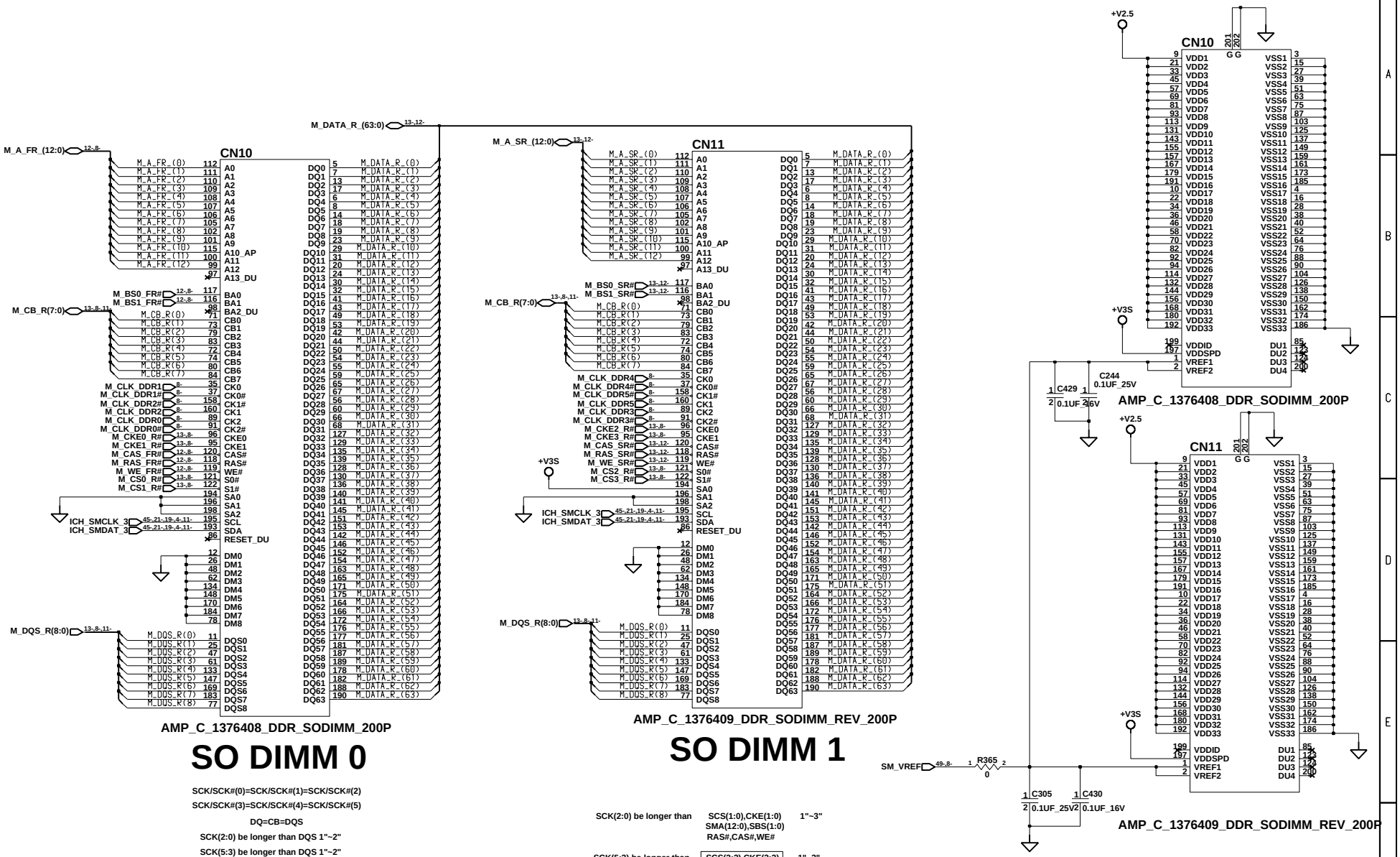






BROOKDALE 3 OF 3

Engineer Engr_Name	INVENTEC		
Drawn by Kevin Tseng	TITLE Fenway2.0 Brookdale(3/3)		Size A3
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK			
Changed by EE1	Date Changed Friday, May 10, 2002	Time Changed 6:30:10 pm	QA CHK
VER 110	Model Number SI	Sheet 10 of 51	



SO DIMM 0

SCK/SCK#(0)=SCK/SCK#(1)=SCK/SCK#(2)

SCK/SCK#(3)=SCK/SCK#(4)=SCK/SCK#(5)

DQ=CB=DQS

SCK(2:0) be longer than DQS 1"~2"

SCK(5:3) be longer than DQS 1"~2"

SDQ(63:0) from MCH to DIMM0 2"~3.5"

SCS#,SCKE from MCH to DIMM0 2"~4.5"

SMA(12:0),SBS(1:0),SRAS#,SCAS#,SWE# 2"~3.5"

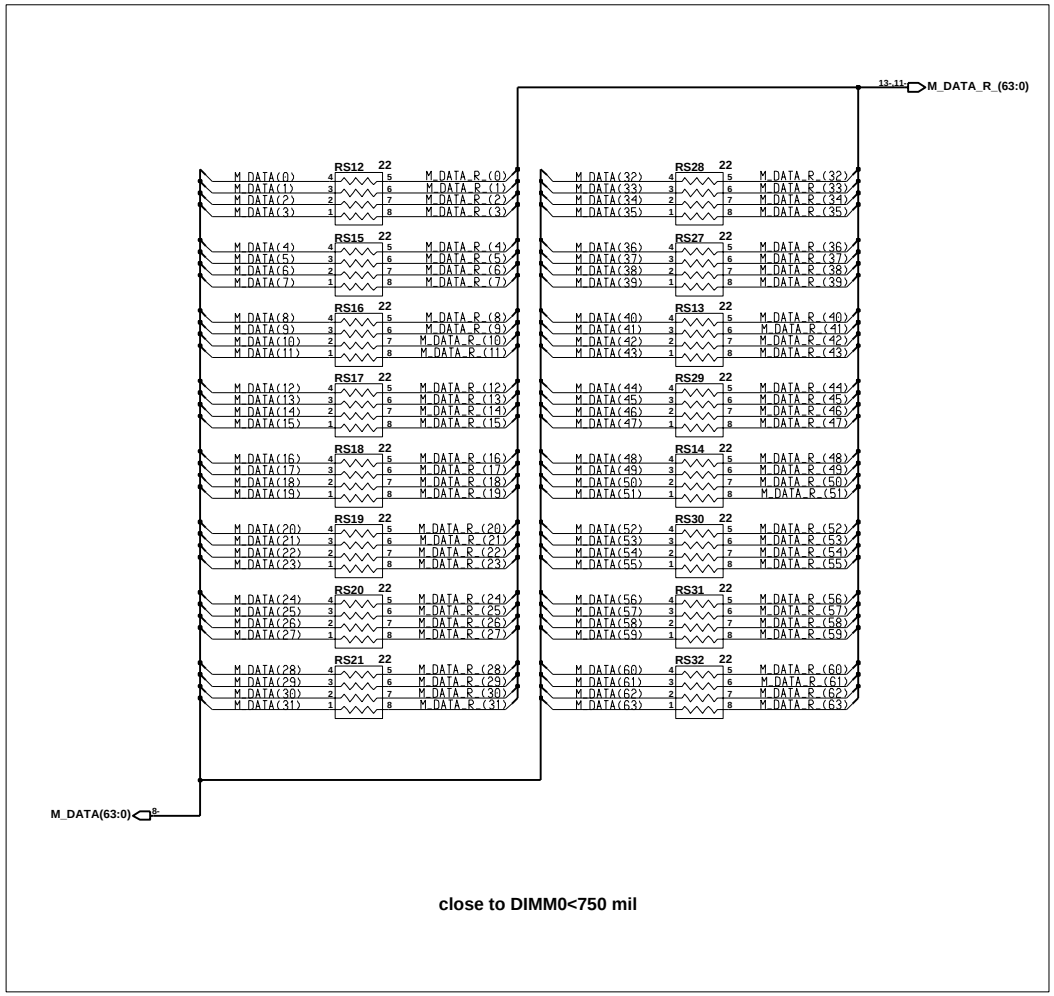
SCK 3"~6.5"

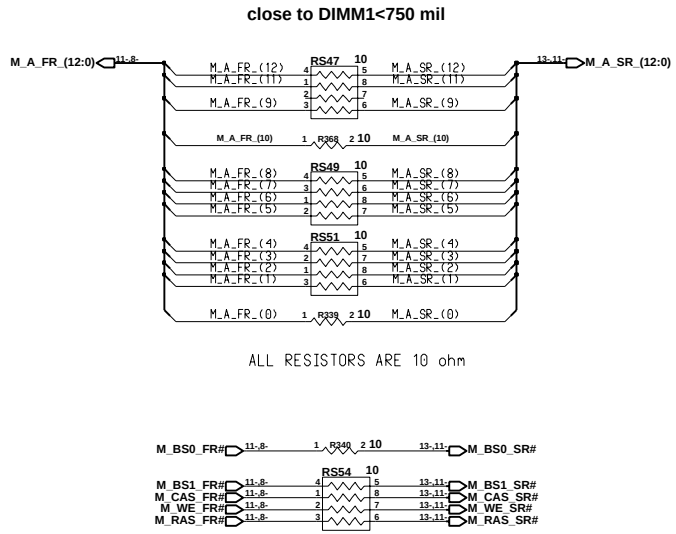
SO DIMM 1

SCK(2:0) be longer than SCS(1:0),CKE(1:0) SMA(12:0),SBS(1:0) RAS#,CAS#,WE# 1"~3"

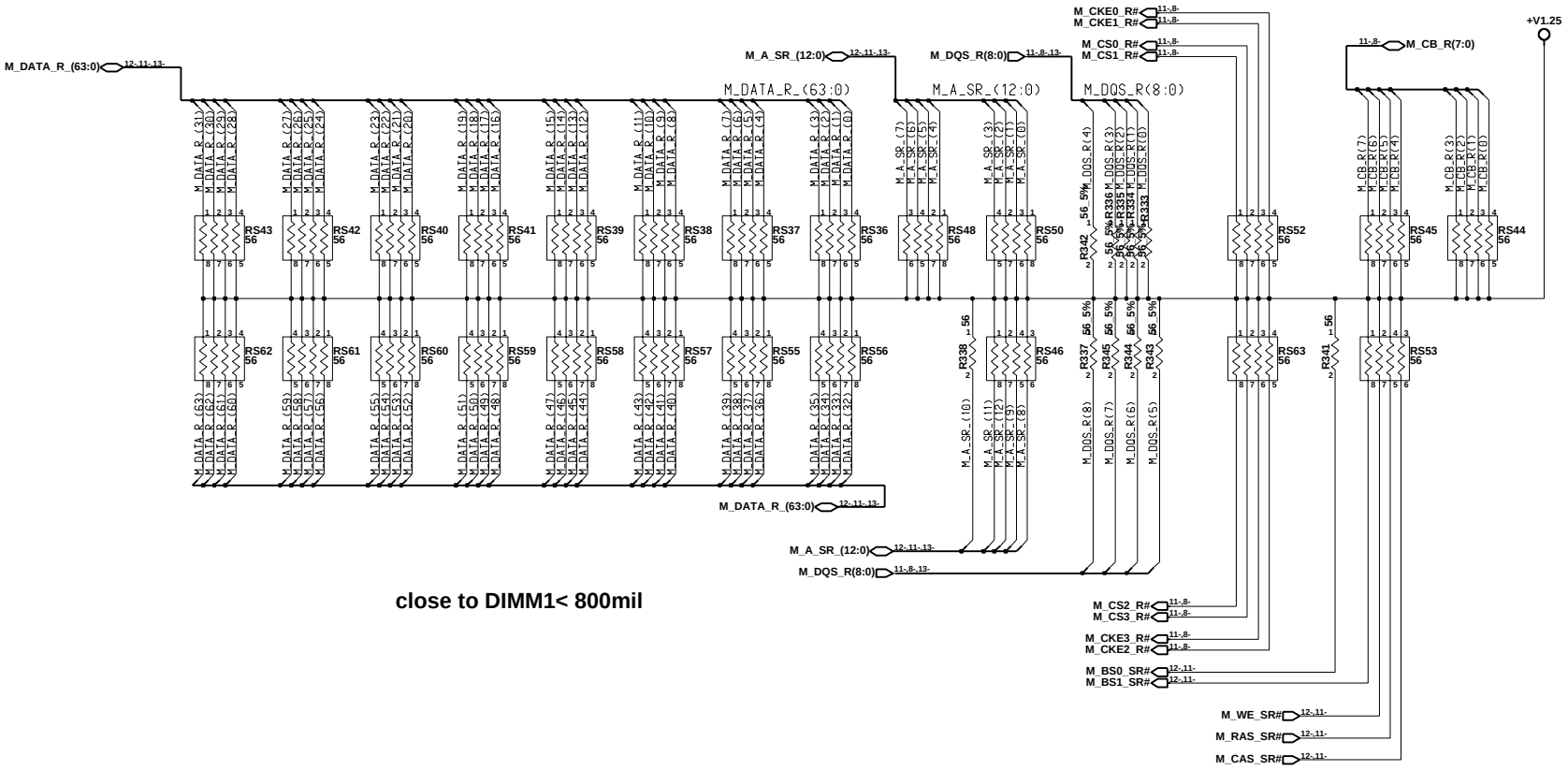
SCK(5:3) be longer than SCS(3:2),CKE(3:2) SMA(12:0),SBS(1:0) RAS#,CAS#,WE# 1"~3"

Engineer Engr_Name	INVENTEC		
Drawn By Kevin Tseng			
R&D CHK	TITLE Fenway2.0 DDR(1/4)		Size A3
DOC CTRL CHK			
MFG ENGR CHK			
Changed by EE1	Date Changed Monday, March 25, 2002	Time Changed 1:34:04 pm	QA CHK
VER 110	Model Number SI	Sheet 11 of 51	



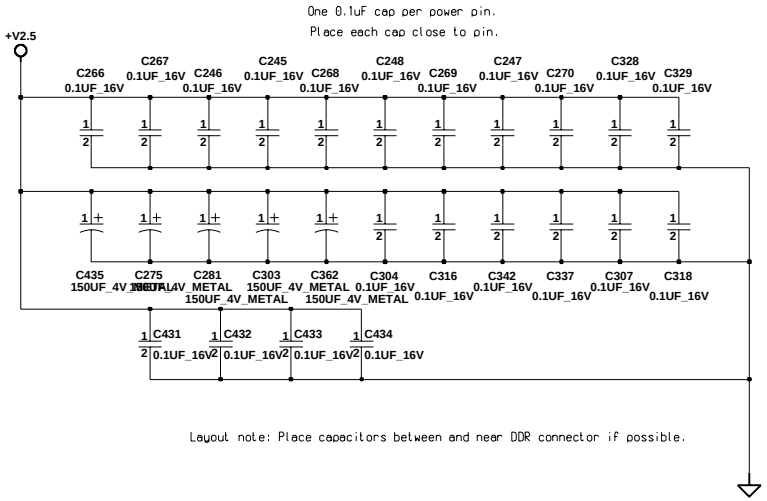


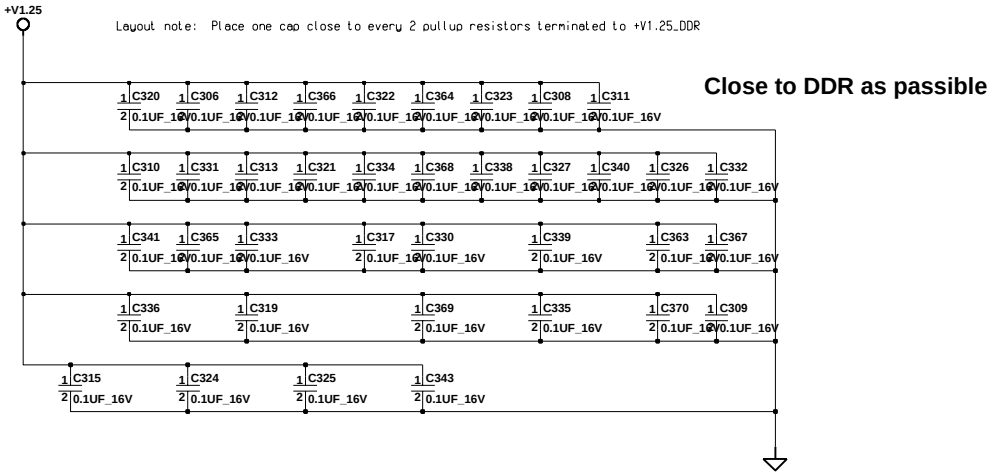
Engineer Engr_Name	INVENTEC				
Drawn by Kevin Tseng					
R&D CHK	TITLE Fenway2.0 DDR(2/4)				Size A3
DOC CTRL CHK					
MFG ENGR CHK					
Changed by EE1	Date Changed Monday, January 28, 2002	Time Changed 11:46:57 am	QA CHK	VER 110	Model Number SI	Sheet 12 of 51



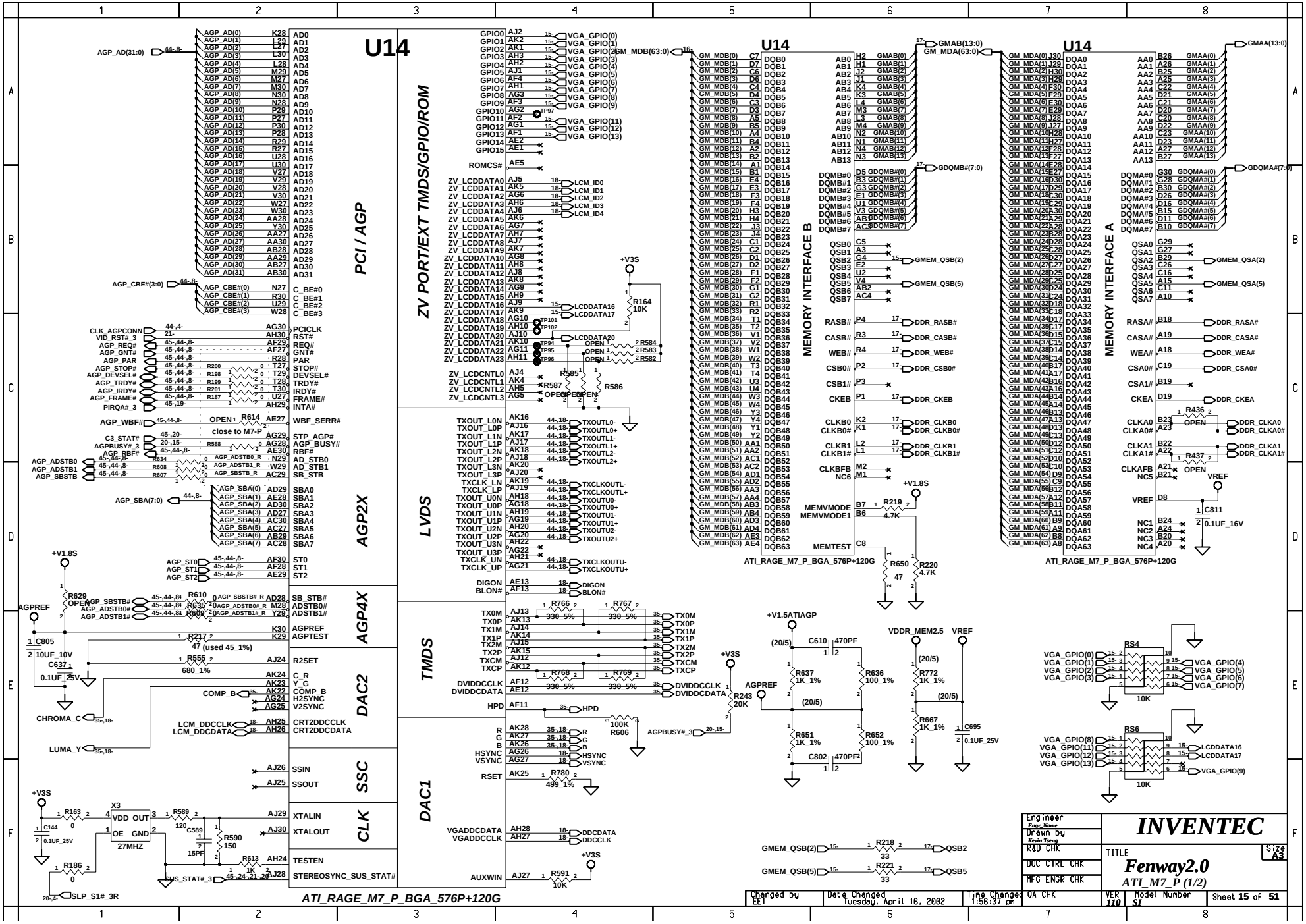
close to DIMM1< 800mil

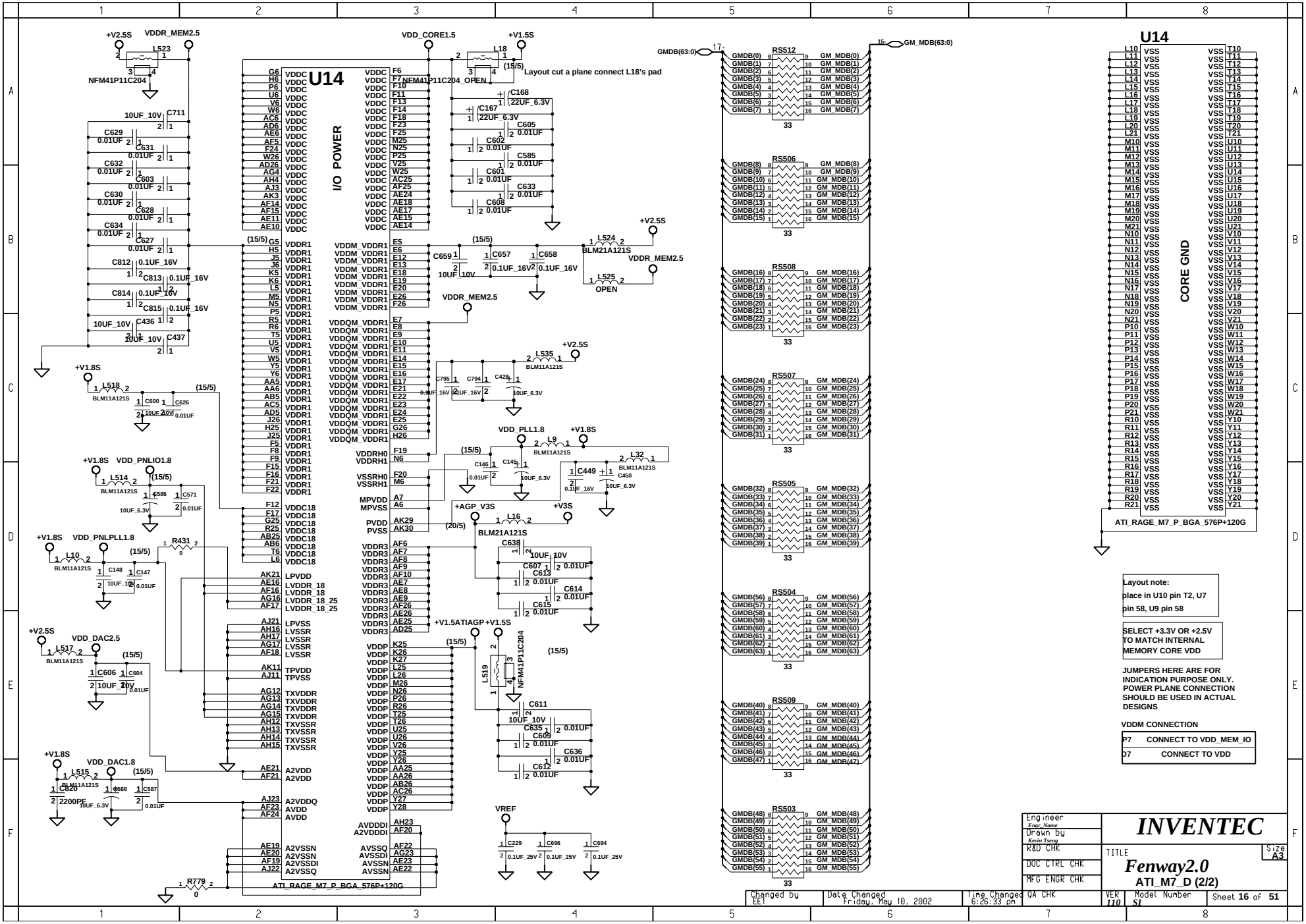
Engineer Engr_Name	INVENTEC				
Drawn by Kevin Tseng					
R&D CHK	TITLE Fenway2.0 DDR(3/4)				Size A3
DOC CTRL CHK					
MFG ENGR CHK					
Changed by EE1	Date Changed Monday, January 28, 2002	Time Changed 11:50:49 am	QA CHK	VER 110	Model Number SI	Sheet 13 of 51

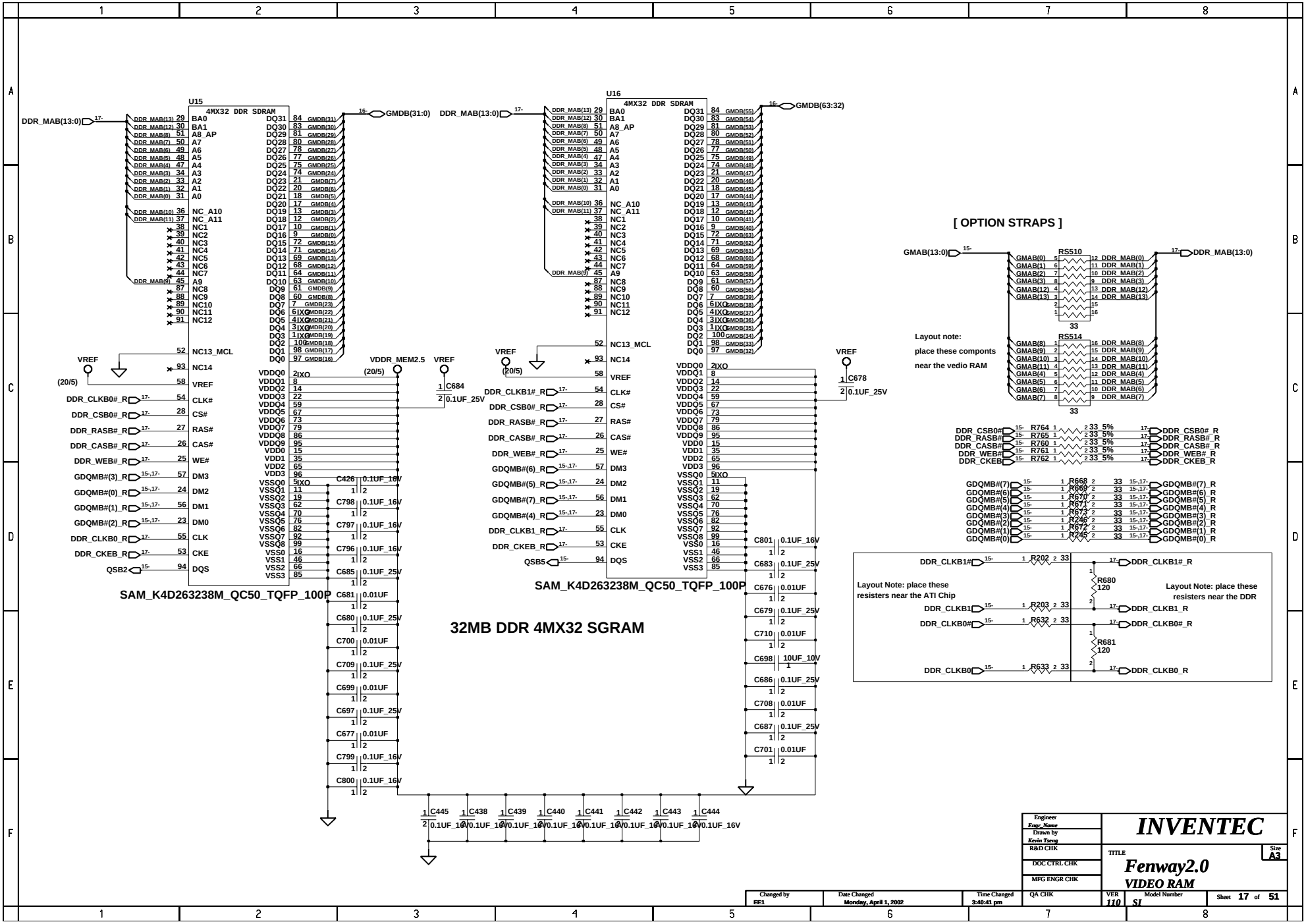


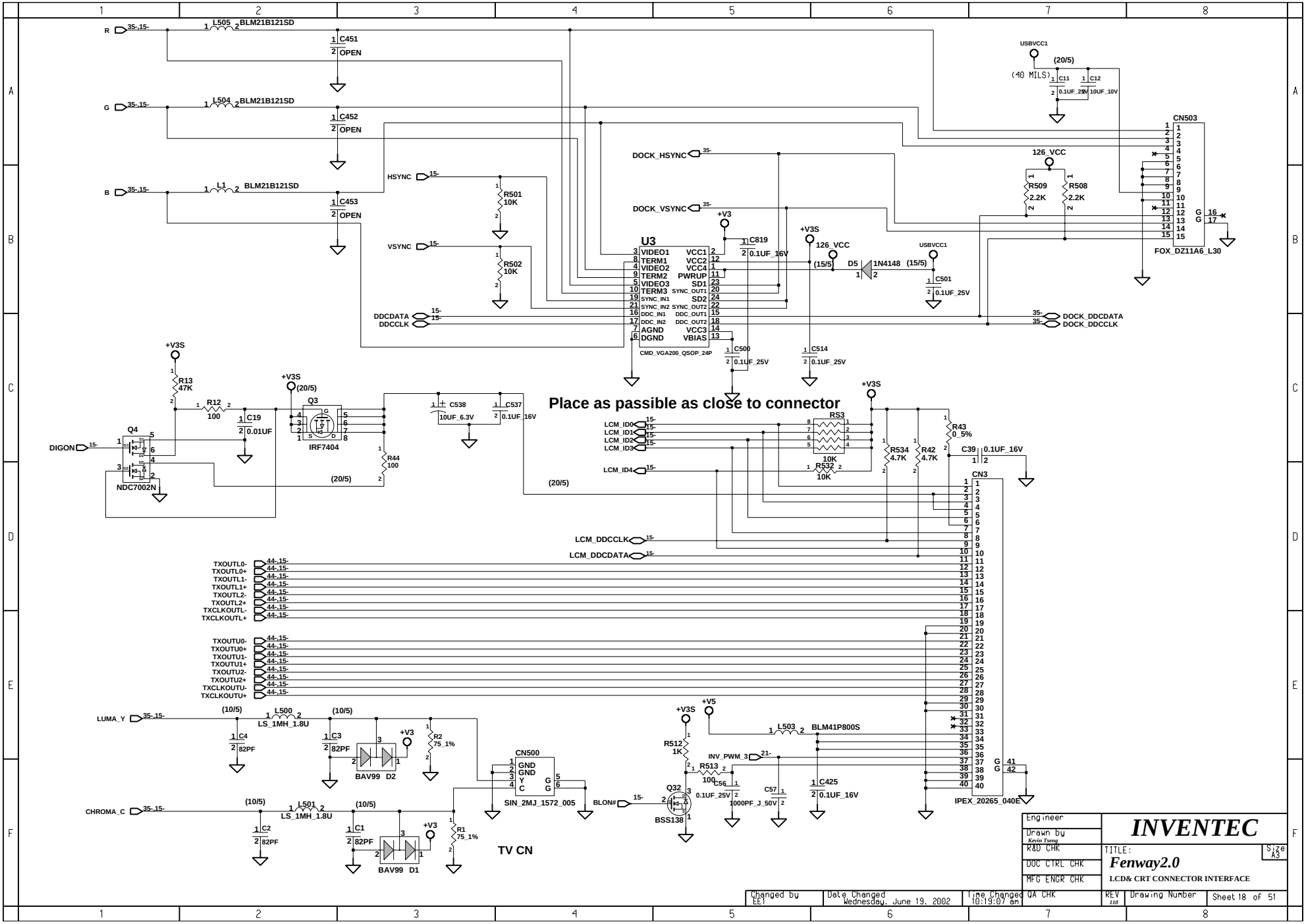


Engineer Engr_Name	INVENTEC				
Drawn by Kevin Tseng	TITLE Fenway2.0 DDR(4/4)				Size A3
R&D CHK					
DOC CTRL CHK					
MFG ENGR CHK					
Changed by EE1	Date Changed Tuesday, April 16, 2002	Time Changed 1:38:04 pm	QA CHK	VER 110	Model Number SI	Sheet 14 of 51

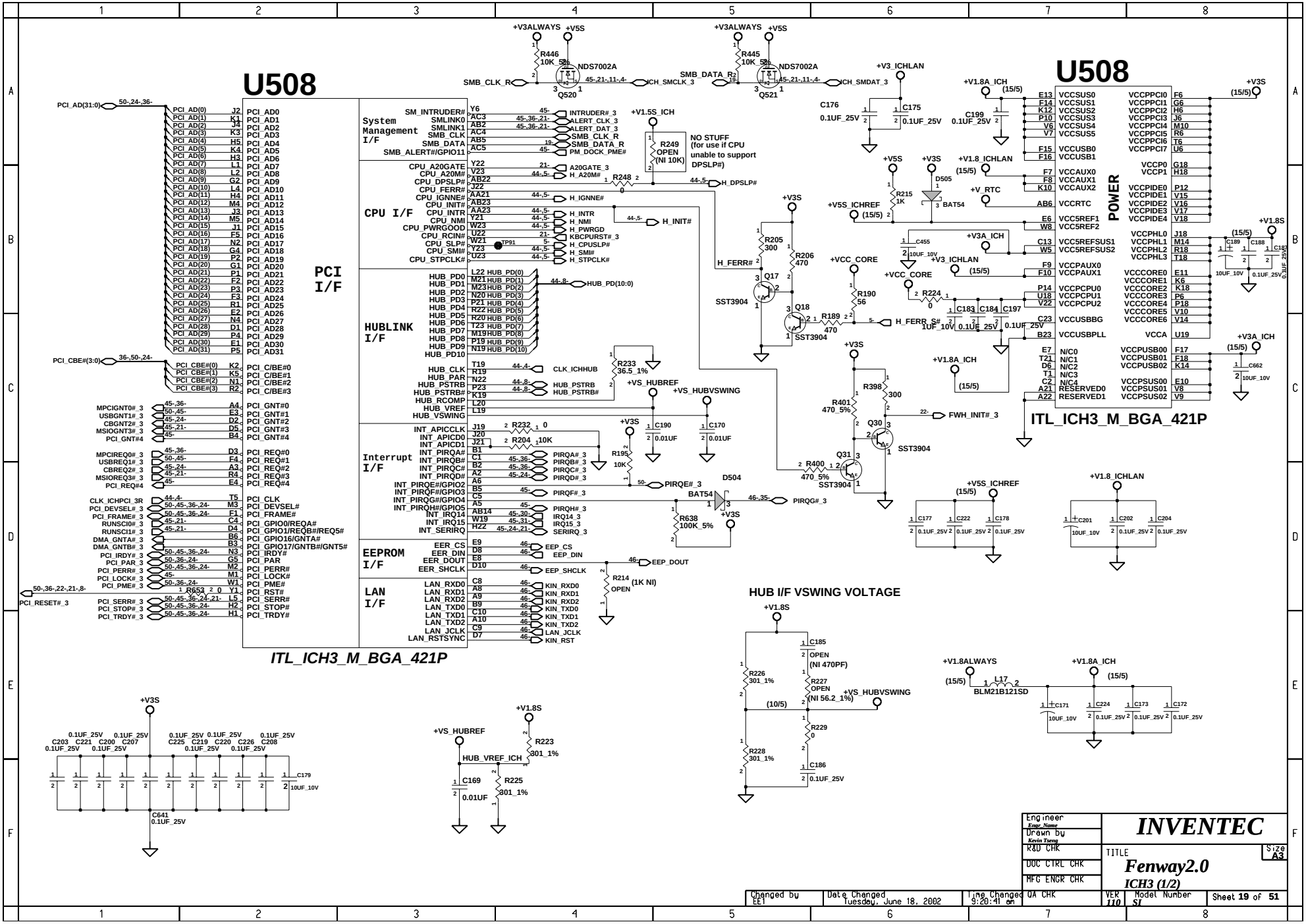

U14
PCI / AGP
ZV PORT/EXT TMDS/GPIO/ROM
LVDS
AGP2X
AGP4X
TMDS
DAC2
SSC
CLK
DAC1
MEMORY INTERFACE B
MEMORY INTERFACE A
ATI_RAGE_M7_P_BGA_576P+120G
INVENTEC
Fenway2.0
ATI_M7_P (1/2)
Engineer
Drawn by
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
QA CHK
Changed by EE1
Date Changed Tuesday, April 16, 2002
Time Changed 1:56:37 pm
VER 110
Model Number SI
Sheet 15 of 51
Size A3

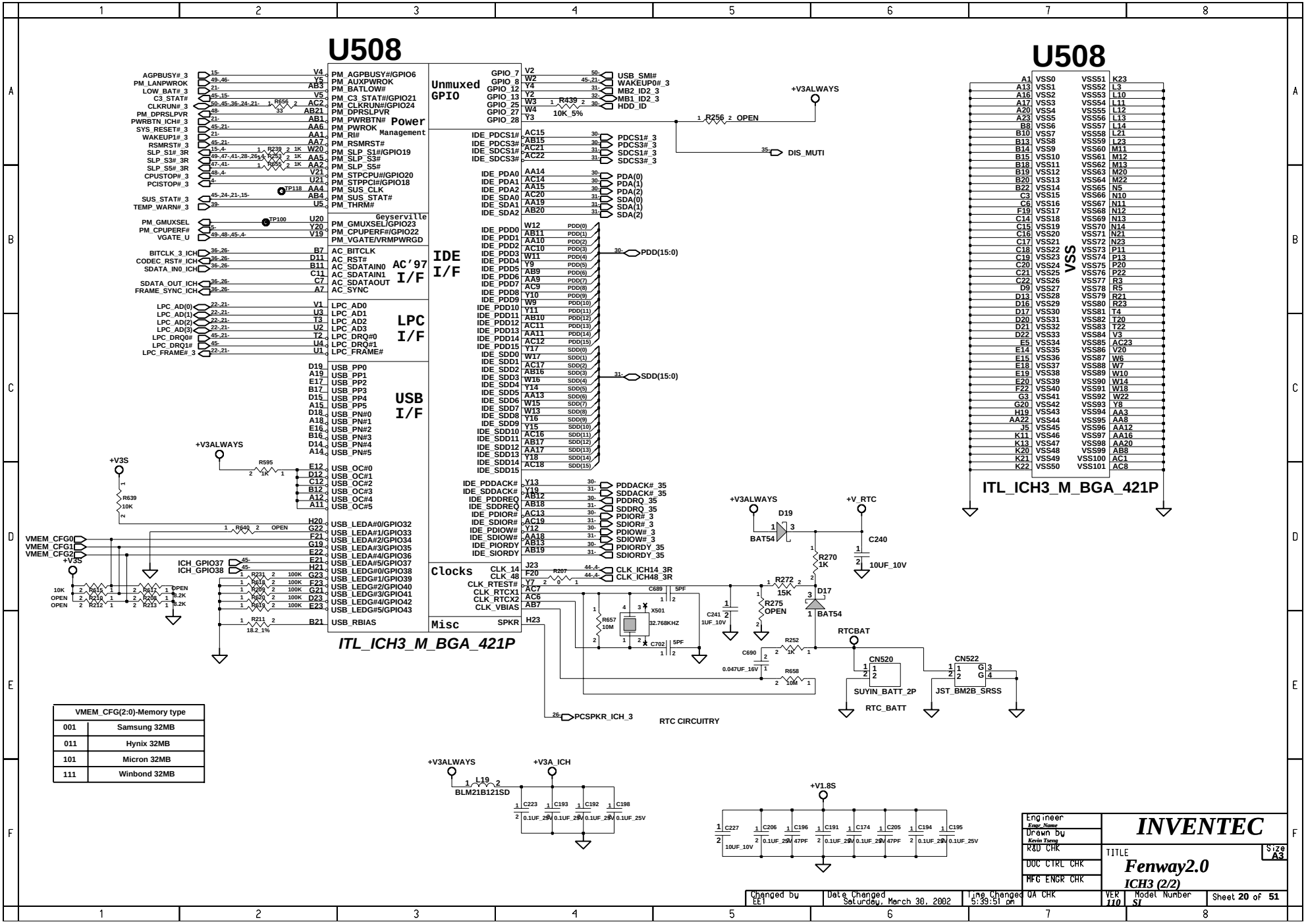

U14
I/O POWER
ATI_RAGE_M7_P_BGA_576P+120G
CORE GND
ATI_RAGE_M7_P_BGA_576P+120G
Layout cut a plane connect L18's pad
Layout note:
place in U10 pin T2, U7 pin 58, U9 pin 58
SELECT +3.3V OR +2.5V TO MATCH INTERNAL MEMORY CORE VDD
JUMPERS HERE ARE FOR INDICATION PURPOSE ONLY. POWER PLANE CONNECTION SHOULD BE USED IN ACTUAL DESIGNS
VDDM CONNECTION
P7 CONNECT TO VDD_MEM_IO
D7 CONNECT TO VDD
INVENTEC
Fenway2.0
ATI_M7_D (2/2)
Size A3
Sheet 16 of 51
Changed by EE1
Date Changed Friday, May 10, 2002
Time Changed 6:26:33 pm
VER 110
Model Number SI

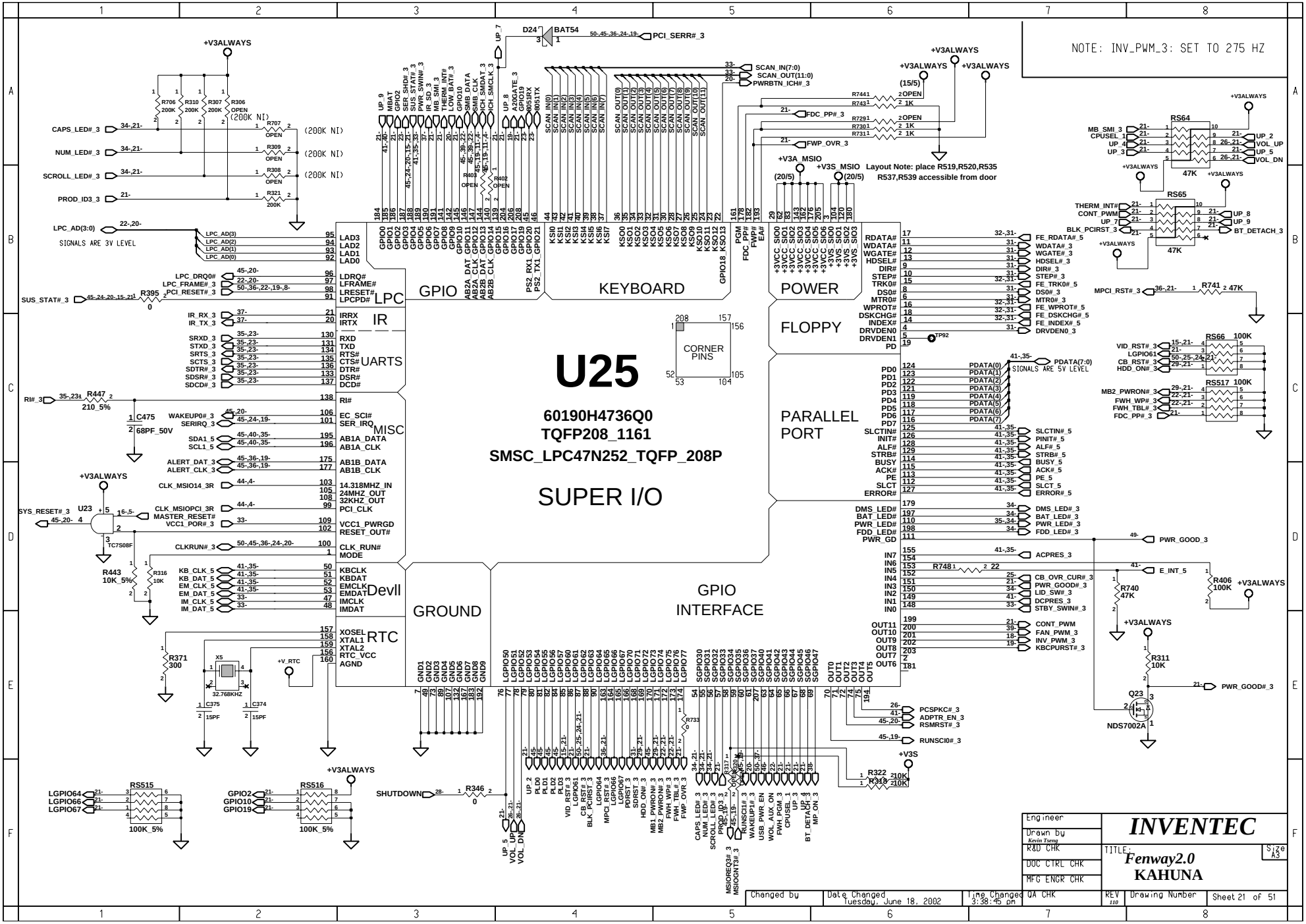

U15
4MX32 DDR SDRAM
SAM_K4D263238M_QC50_TQFP_100P
U16
4MX32 DDR SDRAM
SAM_K4D263238M_QC50_TQFP_100P
32MB DDR 4MX32 SGRAM
[OPTION STRAPS]
Layout note:
place these componts
near the vedio RAM
Layout Note: place these
resisters near the ATI Chip
Layout Note: place these
resisters near the DDR
INVENTEC
Fenway2.0
VIDEO RAM
Engineer
Drawn by
Kevin Tseng
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
Changed by
EE1
Date Changed
Monday, April 1, 2002
Time Changed
3:40:41 pm
QA CHK
VER
110
Model Number
SI
Sheet 17 of 51
Size
A3

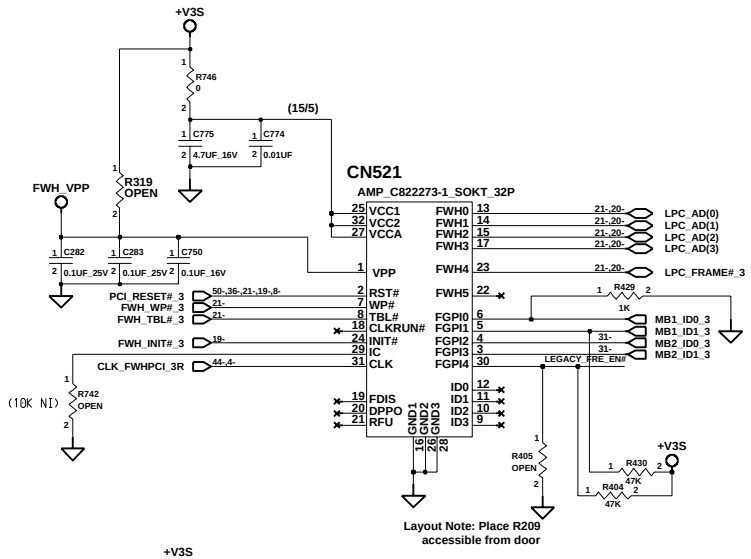


Engineer	INVENTEC				
Drawn by Kevin Tseng	TITLE: Fenway2.0				Size A3
R&D CHK	LCD& CRT CONNECTOR INTERFACE				
DOC CTRL CHK					
MFG ENGR CHK					
Changed by EE1	Date Changed Wednesday, June 19, 2002	Time Changed 10:19:07 am	QA CHK	REV 110	Drawing Number	Sheet 18 of 51

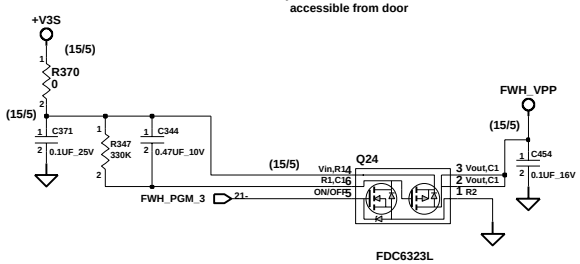

U508
PCI I/F
System Management I/F
CPU I/F
HUBLINK I/F
Interrupt I/F
EEPROM I/F
LAN I/F
ITL_ICH3_M_BGA_421P
U508
POWER
ITL_ICH3_M_BGA_421P
HUB I/F VSWING VOLTAGE
NO STUFF (for use if CPU unable to support DPSLP#)
INVENTEC
Engineer
Drawn by
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
TITLE
Fenway2.0
ICH3 (1/2)
Size A3
Changed by EE1
Date Changed Tuesday, June 18, 2002
Time Changed 9:20:41 am
QA CHK
VER 110
Model Number SI
Sheet 19 of 51


U508
Unmuxed GPIO
Power Management
Geyserville
IDE I/F
AC'97 I/F
LPC I/F
USB I/F
Clocks
Misc
ITL_ICH3_M_BGA_421P
U508
VSS
ITL_ICH3_M_BGA_421P
RTC CIRCUITRY
VMEM_CFG(2:0)-Memory type
001 Samsung 32MB
011 Hynix 32MB
101 Micron 32MB
111 Winbond 32MB
INVENTEC
Fenway2.0
ICH3 (2/2)
Engineer
Drawn By
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
QA CHK
Changed by EE1
Date Changed Saturday, March 30, 2002
Time Changed 5:39:51 pm
VER 110
Model Number SI
Sheet 20 of 51

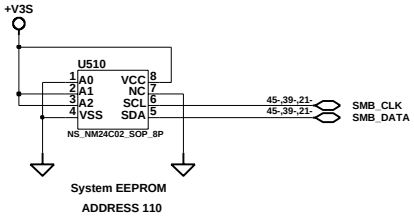

NOTE: INV_PWM_3: SET TO 275 HZ
U25
60190H4736Q0
TQFP208_1161
SMSC_LPC47N252_TQFP_208P
SUPER I/O
GPIO
KEYBOARD
POWER
LPC
IR
UARTS
MISC
Devll
RTC
GROUND
GPIO INTERFACE
FLOPPY
PARALLEL PORT
CORNER PINS
Layout Note: place R519,R520,R535 R537,R539 accessible from door
SIGNALS ARE 3V LEVEL
SIGNALS ARE 5V LEVEL
INVENTEC
Fenway2.0
KAHUNA
Engineer
Drawn by Kevin Tseng
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
Changed by
Date Changed Tuesday, June 18, 2002
Time Changed 3:38:45 pm
QA CHK
REV 110
Drawing Number
Sheet 21 of 51
Size A3



Layout Note: Place R209
accessible from door

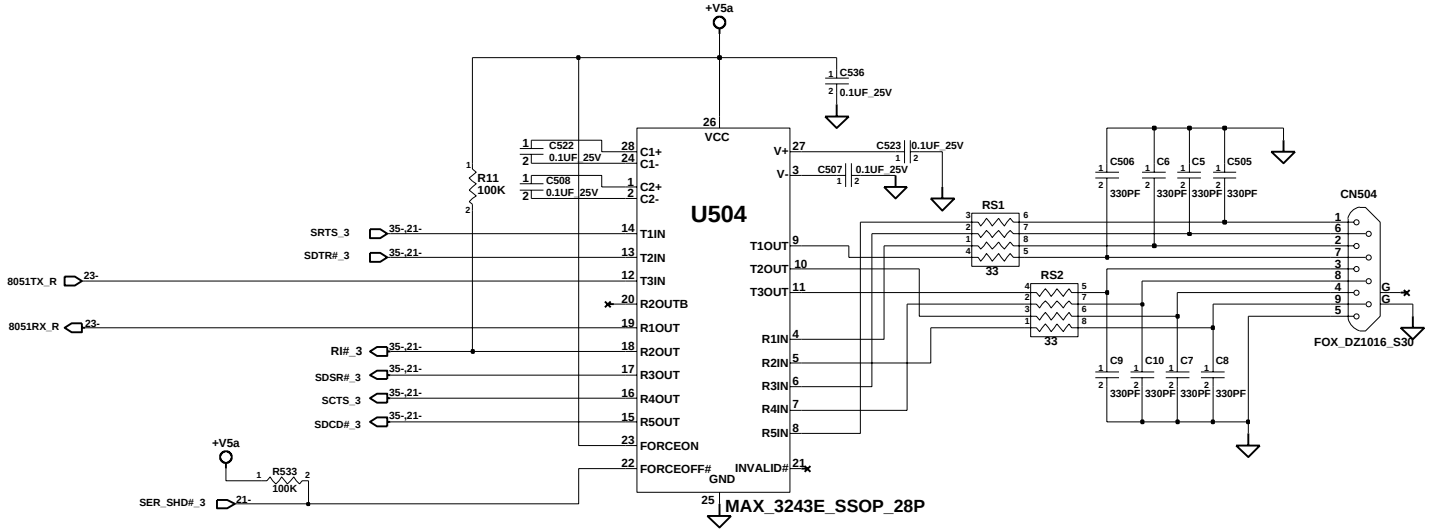


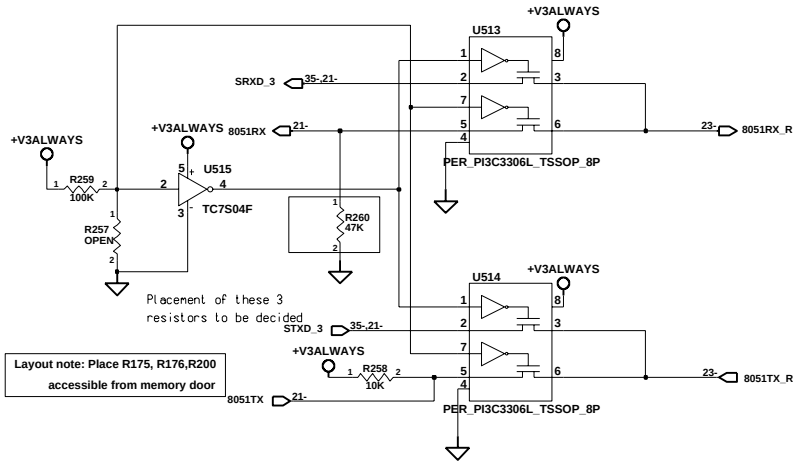
FDC6323L



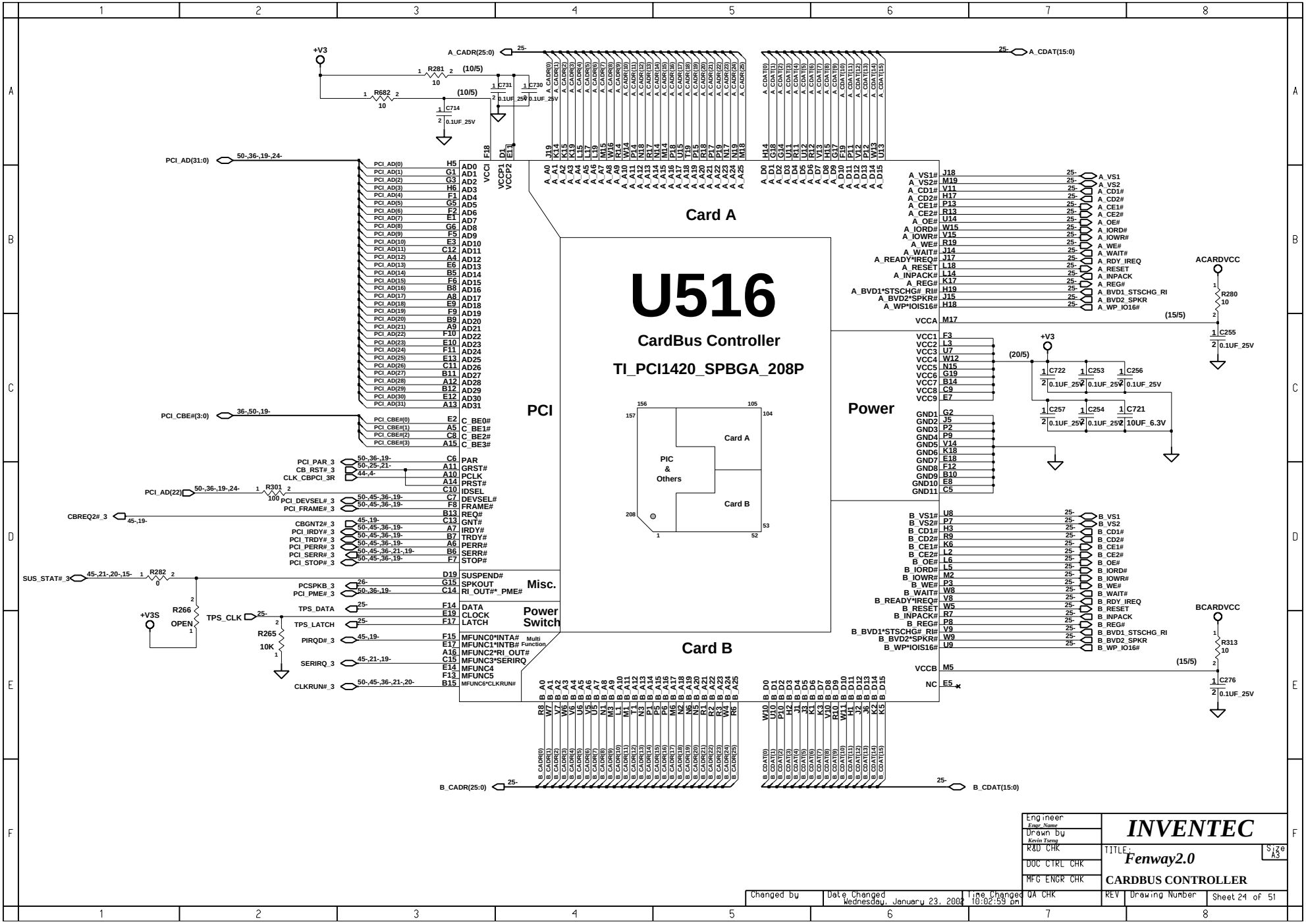
System EEPROM
ADDRESS 110

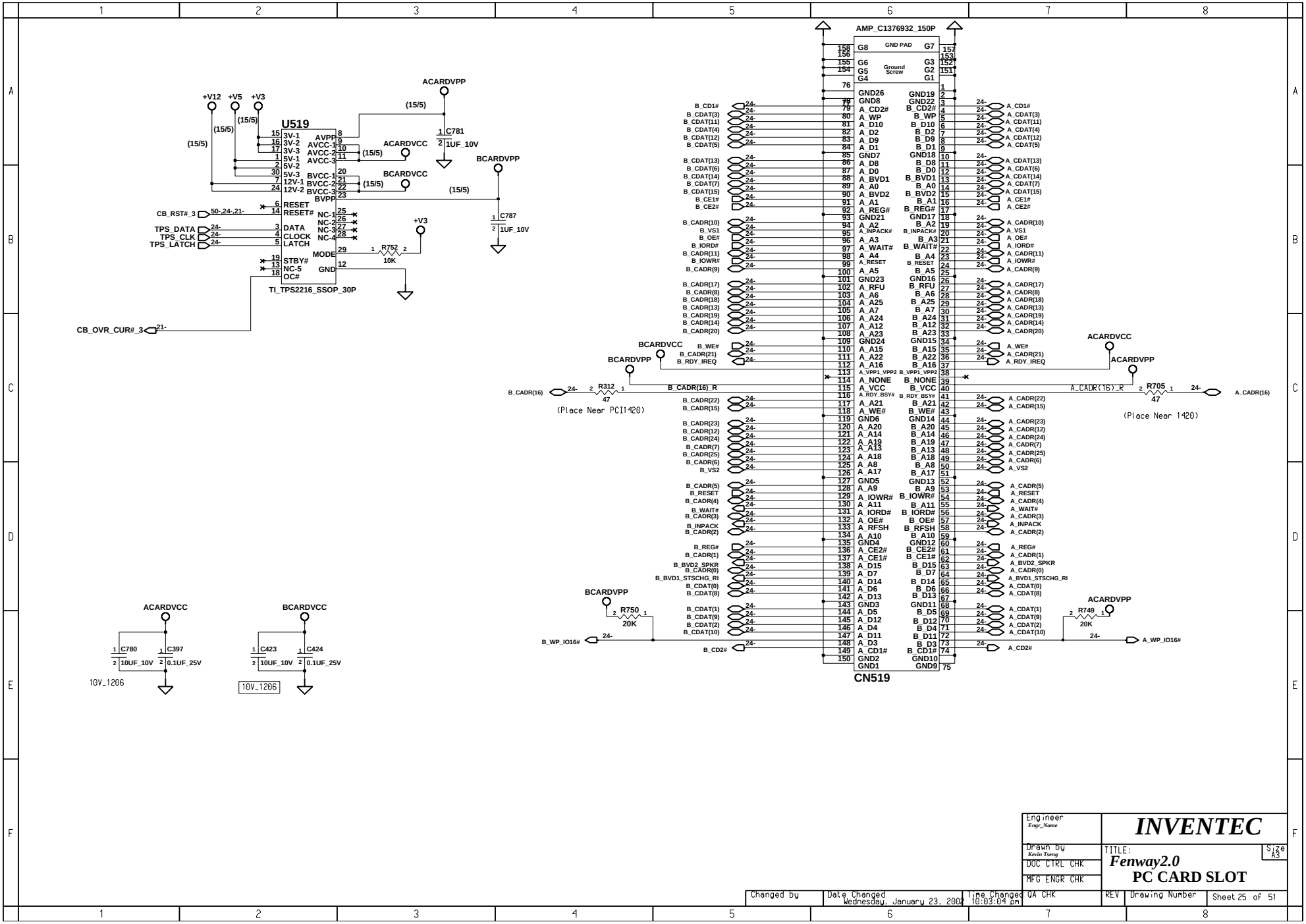
Changed by	Date Changed Tuesday, April 2, 2002	Time Changed 2:51:41 pm	Engineer	INVENTEC			
			Drawn by Kevin Tseng				
			R&D CHK	TITLE: Fenway2.0		Size A3	
			DOC CTRL CHK	FWH&EEPROM			
			MFG ENGR CHK				
			QA CHK	REV	Drawing Number	Sheet 22 of 51	



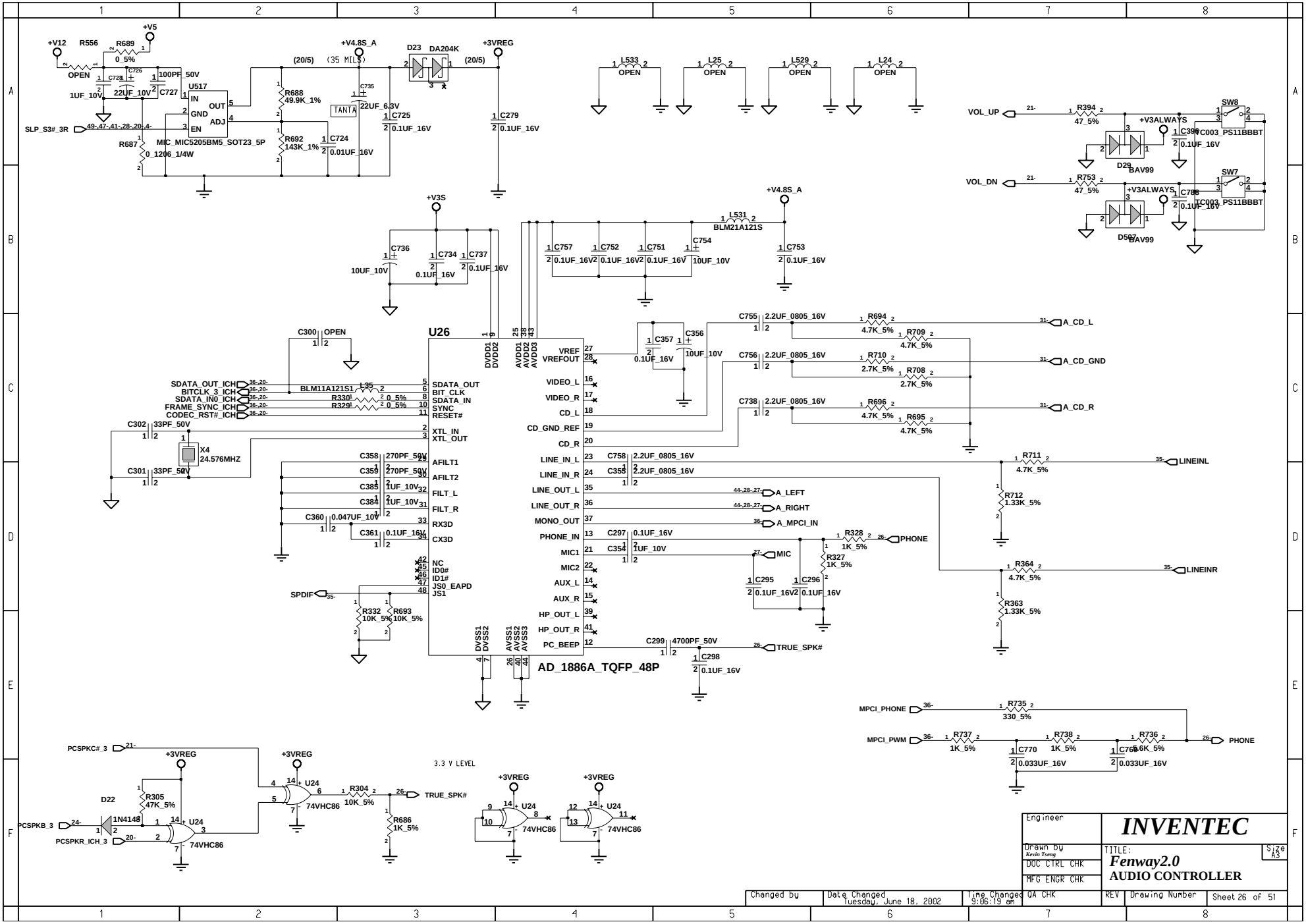


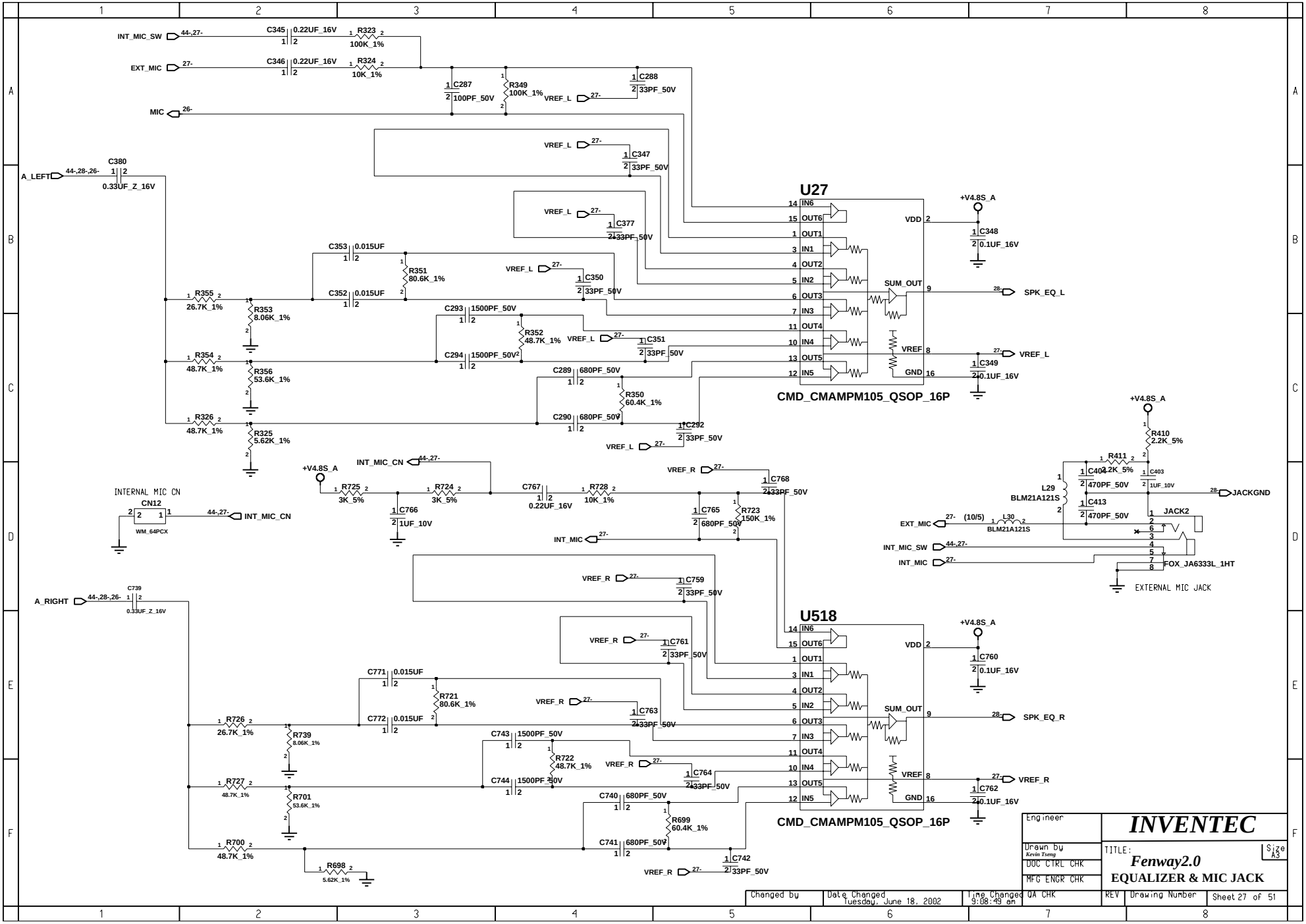
Engineer	INVENTEC				
Drawn by Kevin Tseng	TITLE: Fenway2.0				Size A3
R&D CHK	SERIAL, PARALLEL, PS2 PORTS				
DOC CTRL CHK					
MFG ENGR CHK					
Changed by	Date Changed Wednesday, June 19, 2002	Time Changed 10:23:26 am	QA CHK	REV	Drawing Number	Sheet 23 of 51

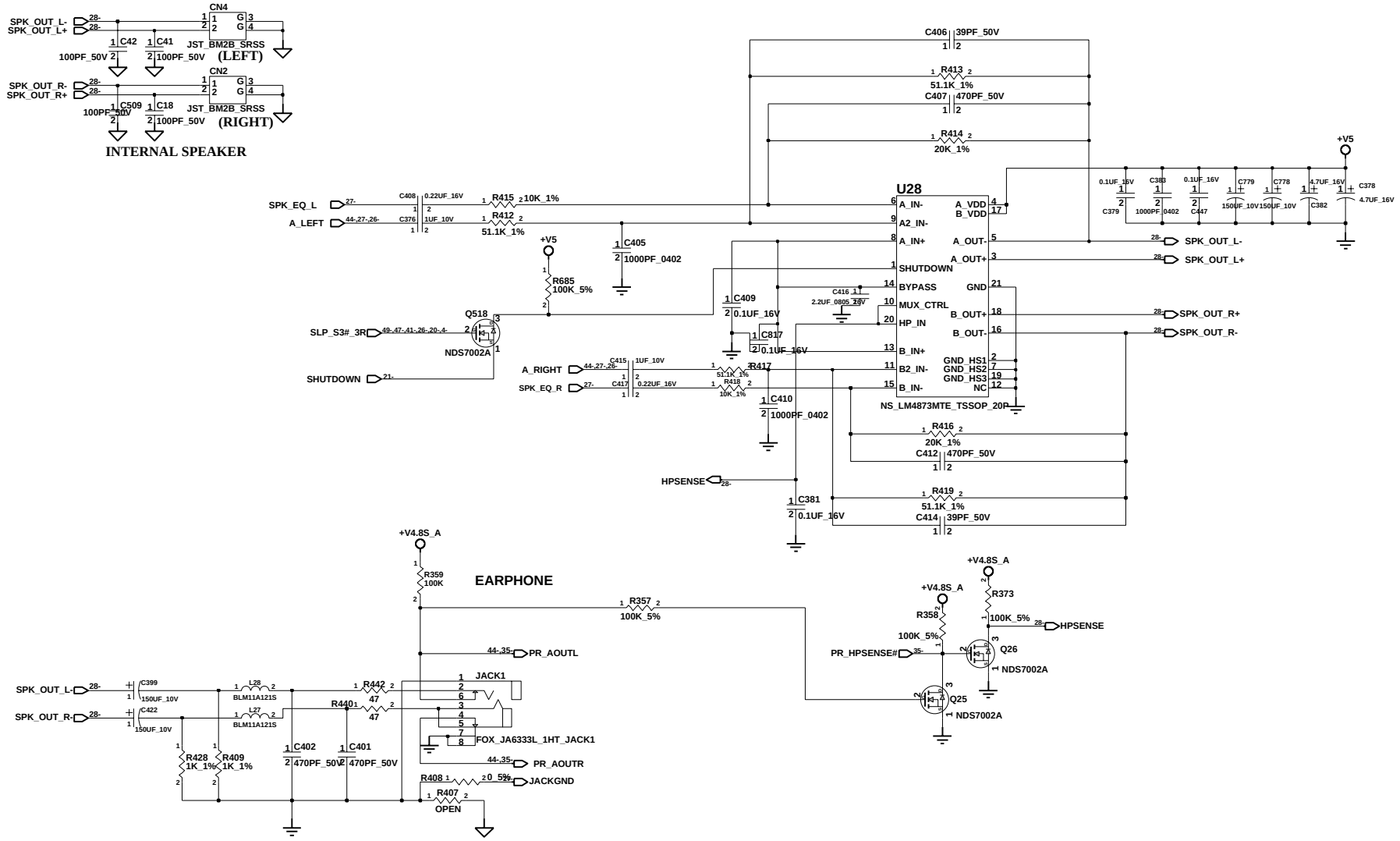

U516
CardBus Controller
TI_PCI1420_SPBGA_208P
Card A
Card B
PIC & Others
PCI
Power
Misc.
Power Switch
Multi Function
A_CADR(25:0)
A_CDAT(15:0)
B_CADR(25:0)
B_CDAT(15:0)
PCI_AD(31:0)
PCI_CBE#(3:0)
+V3
+V3S
ACARDVCC
BCARDVCC
R281 10 (10/5)
R682 10 (10/5)
C714 0.1UF_25V
C731 0.1UF_25V
C730 0.1UF_25V
R280 10 (15/5)
C255 0.1UF_25V
C722 0.1UF_25V
C253 0.1UF_25V
C256 0.1UF_25V
C257 0.1UF_25V
C254 0.1UF_25V
C721 10UF_6.3V (20/5)
R313 10 (15/5)
C276 0.1UF_25V
R301 100
R282 0
R266 OPEN
R265 10K
TPS_CLK
Engineer
Drawn by
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
INVENTEC
TITLE: Fenway2.0
CARDBUS CONTROLLER
Size A3
Changed by
Date Changed Wednesday, January 23, 2002
Time Changed 10:02:59 pm
QA CHK
REV
Drawing Number
Sheet 24 of 51



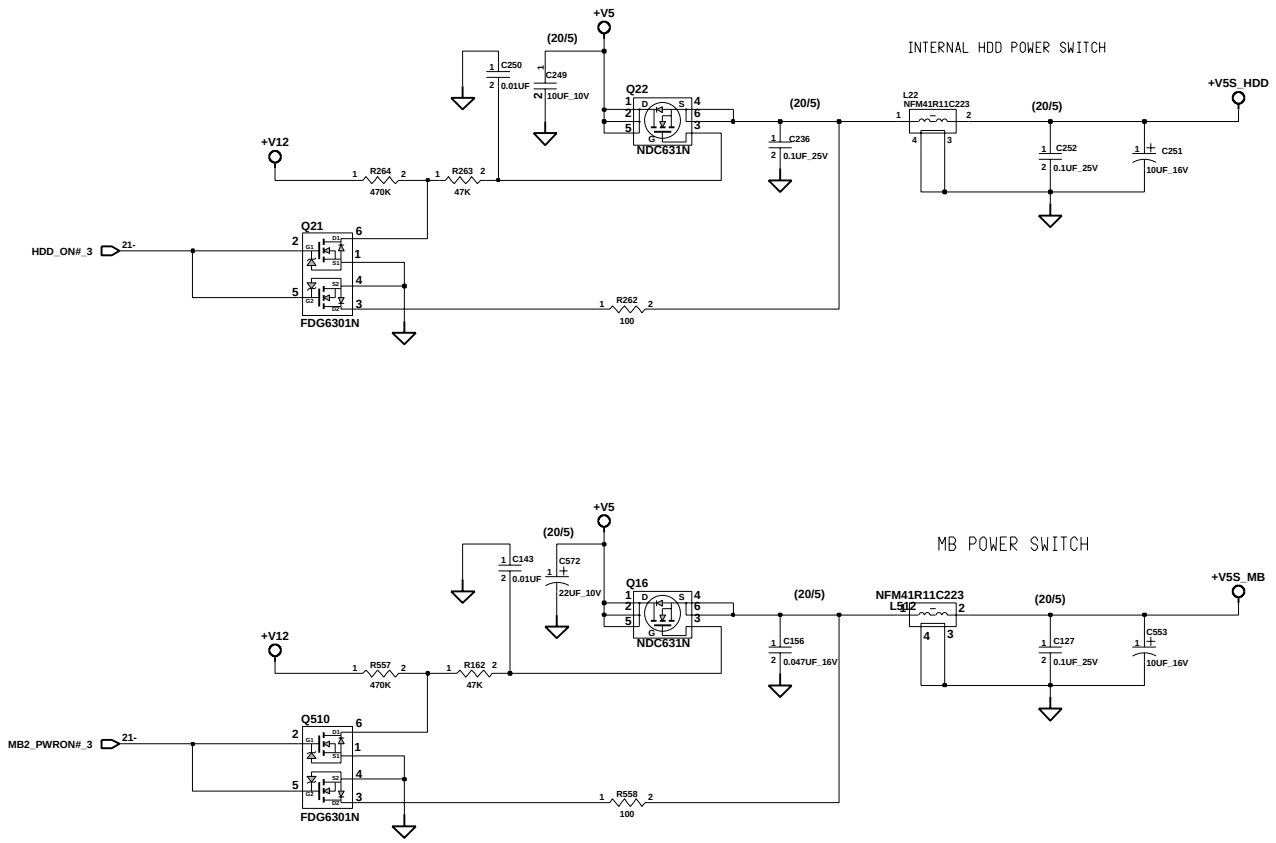
Engineer Engr_Name	INVENTEC		
Drawn by Kevin Tseng	TITLE: Fenway2.0 PC CARD SLOT		Size A3
DOC CTRL CHK			
MFG ENGR CHK			
Changed by	Date Changed Wednesday, January 23, 2002	Time Changed 10:03:04 pm	QA CHK
REV	Drawing Number	Sheet 25 of 51	


+V12
R556
OPEN
R689
0_5%
+V5
C728
1UF_10V
C726
22UF_10V
100PF_50V
C727
U517
IN
OUT
GND
ADJ
EN
MIC_MIC5205BM5_SOT23_5P
SLP_S3#_3R
R687
0_1206_1/4W
R688
49.9K_1%
R692
143K_1%
C724
0.01UF_16V
C735
22UF_6.3V
TANTA
+V4.8S_A
(35 MILS)
(20/5)
D23
DA204K
C725
0.1UF_16V
+3VREG
C279
0.1UF_16V
L533
OPEN
L25
OPEN
L529
OPEN
L24
OPEN
VOL_UP
R394
47_5%
+V3ALWAYS
C396
0.1UF_16V
SW8
TC003_PS11BBBT
D29
BAV99
VOL_DN
R753
47_5%
C788
0.1UF_16V
SW7
TC003_PS11BBBT
D502
BAV99
+V3S
C736
10UF_10V
C734
0.1UF_16V
C737
0.1UF_16V
L531
BLM21A121S
C757
0.1UF_16V
C752
0.1UF_16V
C751
0.1UF_16V
C754
10UF_10V
C753
0.1UF_16V
C300
OPEN
U26
DVDD1
DVDD2
AVDD1
AVDD2
AVDD3
VREF
VREFOUT
VIDEO_L
VIDEO_R
CD_L
CD_GND_REF
CD_R
LINE_IN_L
LINE_IN_R
LINE_OUT_L
LINE_OUT_R
MONO_OUT
PHONE_IN
MIC1
MIC2
AUX_L
AUX_R
HP_OUT_L
HP_OUT_R
PC_BEEP
SDATA_OUT
BIT_CLK
SDATA_IN
SYNC
RESET#
XTL_IN
XTL_OUT
AFILT1
AFILT2
FILT_L
FILT_R
RX3D
CX3D
NC
ID0#
ID1#
JS0_EAPD
JS1
DVSS1
DVSS2
AVSS1
AVSS2
AVSS3
AD_1886A_TQFP_48P
SDATA_OUT_ICH
BITCLK_3_ICH
SDATA_IN0_ICH
FRAME_SYNC_ICH
CODEC_RST#_ICH
BLM11A121S1
L35
R330
R329
0_5%
C302
33PF_50V
C301
33PF_50V
X4
24.576MHZ
C358
270PF_50V
C359
270PF_50V
C385
1UF_10V
C384
1UF_10V
C360
0.047UF_10V
C361
0.1UF_16V
SPDIF
R332
10K_5%
R693
10K_5%
C357
0.1UF_16V
C356
10UF_10V
C755
2.2UF_0805_16V
R694
4.7K_5%
R709
4.7K_5%
A_CD_L
C756
2.2UF_0805_16V
R710
2.7K_5%
R708
2.7K_5%
A_CD_GND
C738
2.2UF_0805_16V
R696
4.7K_5%
R695
4.7K_5%
A_CD_R
C758
2.2UF_0805_16V
C355
2.2UF_0805_16V
R711
4.7K_5%
LINEINL
R712
1.33K_5%
A_LEFT
A_RIGHT
A_MPCI_IN
C297
0.1UF_16V
C354
1UF_10V
R328
1K_5%
PHONE
MIC
R327
1K_5%
C295
0.1UF_16V
C296
0.1UF_16V
R364
4.7K_5%
LINEINR
R363
1.33K_5%
C299
4700PF_50V
C298
0.1UF_16V
TRUE_SPK#
MPCI_PHONE
R735
330_5%
MPCI_PWM
R737
1K_5%
R738
1K_5%
R736
5.6K_5%
C770
0.033UF_16V
C765
0.033UF_16V
PHONE
PCSPKC#_3
+3VREG
D22
1N4148
R305
47K_5%
PCSPKB_3
PCSPKR_ICH_3
U24
74VHC86
R304
10K_5%
TRUE_SPK#
R686
1K_5%
3.3 V LEVEL
Engineer
Drawn by
Kevin Tseng
DOC CTRL CHK
MFG ENGR CHK
QA CHK
INVENTEC
TITLE:
Fenway2.0
AUDIO CONTROLLER
Size
A3
Changed by
Date Changed
Tuesday, June 18, 2002
Time Changed
9:06:19 am
REV
Drawing Number
Sheet 26 of 51


INT_MIC_SW
EXT_MIC
MIC
A_LEFT
A_RIGHT
C345 0.22UF_16V
C346 0.22UF_16V
R323 100K_1%
R324 10K_1%
C287 100PF_50V
R349 100K_1%
C288 33PF_50V
VREF_L
VREF_R
C347 33PF_50V
C377 33PF_50V
C350 33PF_50V
C351 33PF_50V
C292 33PF_50V
C759 33PF_50V
C761 33PF_50V
C763 33PF_50V
C764 33PF_50V
C742 33PF_50V
C380 0.33UF_Z_16V
C739 0.33UF_Z_16V
C353 0.015UF
C352 0.015UF
R351 80.6K_1%
R355 26.7K_1%
R353 8.06K_1%
R354 48.7K_1%
R356 53.6K_1%
R326 48.7K_1%
R325 5.62K_1%
C293 1500PF_50V
C294 1500PF_50V
R352 48.7K_1%
C289 680PF_50V
C290 680PF_50V
R350 60.4K_1%
U27
CMD_CMAMPM105_QSOP_16P
IN6
OUT6
OUT1
IN1
OUT2
IN2
OUT3
IN3
OUT4
IN4
OUT5
IN5
VDD
SUM_OUT
VREF
GND
+V4.8S_A
C348 0.1UF_16V
C349 0.1UF_16V
SPK_EQ_L
VREF_L
INTERNAL MIC CN
CN12
WM_64PCX
INT_MIC_CN
R725 3K_5%
R724 3K_5%
C766 1UF_10V
C767 0.22UF_16V
R728 10K_1%
C768 33PF_50V
C765 680PF_50V
R723 150K_1%
INT_MIC
R410 2.2K_5%
R411 2.2K_5%
C404 470PF_50V
C403 1UF_10V
L29 BLM21A121S
C413 470PF_50V
JACKGND
JACK2
EXT_MIC
(10/5)
L30 BLM21A121S
INT_MIC_SW
INT_MIC
FOX_JA6333L_1HT
EXTERNAL MIC JACK
C771 0.015UF
C772 0.015UF
R721 80.6K_1%
R726 26.7K_1%
R739 8.06K_1%
R727 48.7K_1%
R701 53.6K_1%
R700 48.7K_1%
R698 5.62K_1%
C743 1500PF_50V
C744 1500PF_50V
R722 48.7K_1%
C740 680PF_50V
C741 680PF_50V
R699 60.4K_1%
U518
CMD_CMAMPM105_QSOP_16P
C760 0.1UF_16V
C762 0.1UF_16V
SPK_EQ_R
VREF_R
Engineer
Drawn by Kevin Tseng
DOC CTRL CHK
MFG ENGR CHK
INVENTEC
TITLE:
Fenway2.0
EQUALIZER & MIC JACK
Size A3
Changed by
Date Changed Tuesday, June 18, 2002
Time Changed 9:08:49 am
QA CHK
REV
Drawing Number
Sheet 27 of 51

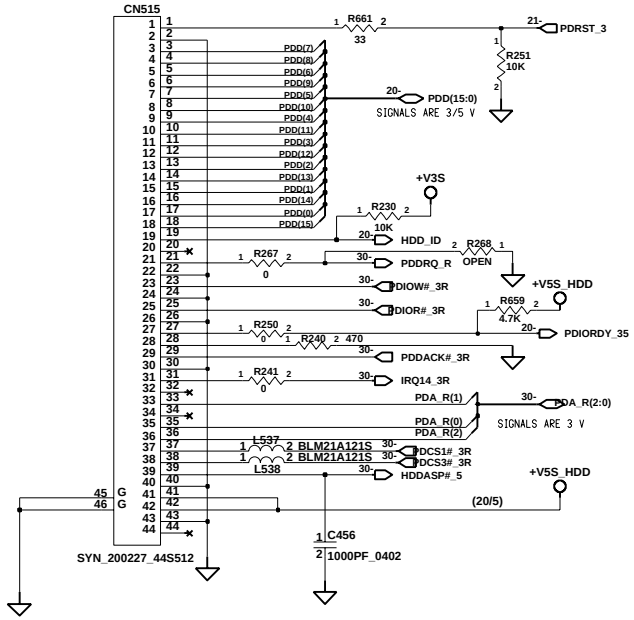


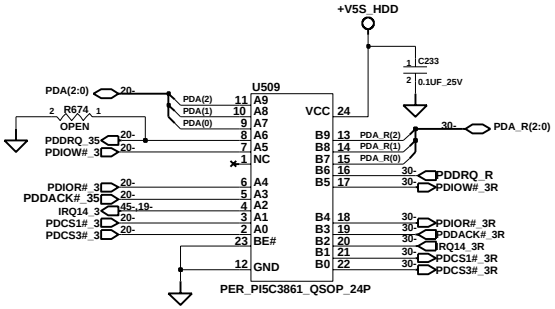
Engineer	INVENTEC		
Drawn by Kevin Tseng	TITLE: Fenway2.0		Size A3
DOC CTRL CHK	AUDIO AMP & HP JACK		
MFG ENGR CHK			
Changed by	Date Changed Friday, April 26, 2002	Time Changed 2:36:37 pm	QA CHK
REV	Drawing Number	Sheet 28 of 51	

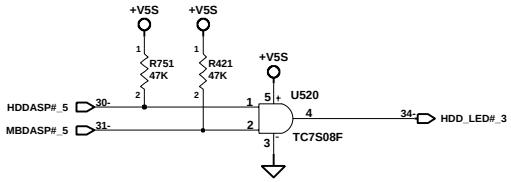


SIGNAL NAME	TRACE WIDTH (MILS)
+V5S_HDD	60
HDDPWR	60
+V5S_MB	60
MBPWR	60

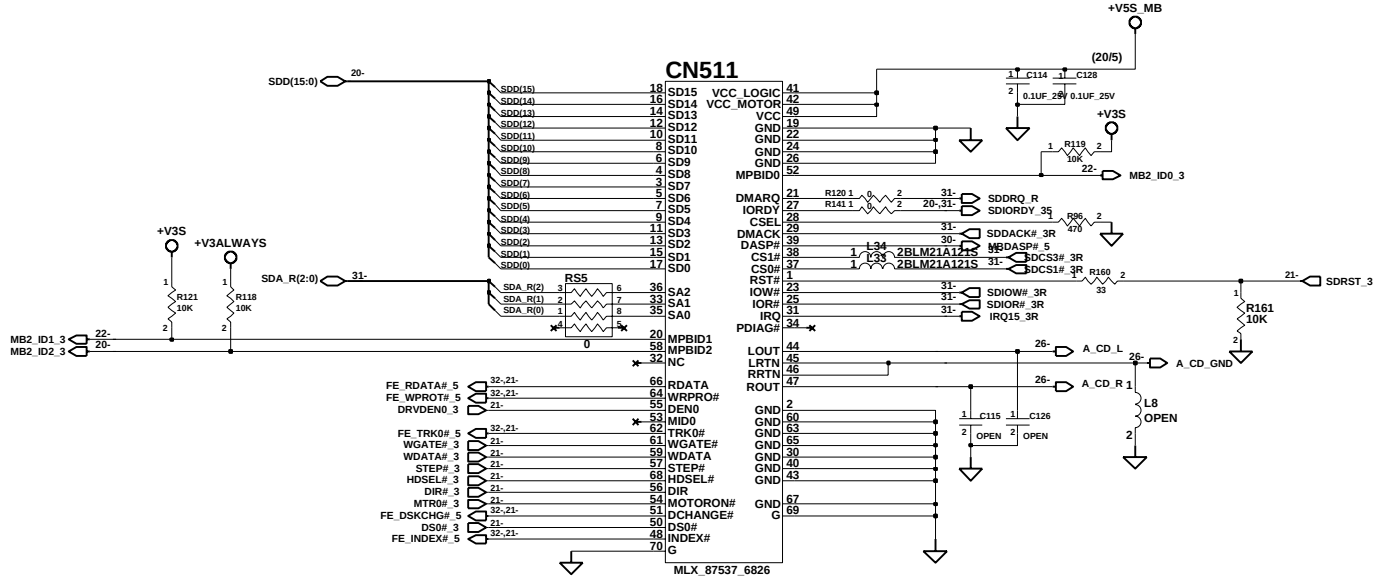
Engineer	INVENTEC				
Drawn by Kevin Tseng	TITLE: Fenway2.0				Size A3
R&D CHK	HDD & MB PWR & SWITCH				
DOC CTRL CHK					
MFG ENGR CHK					
Changed by	Date Changed Wednesday, January 23, 2002	Time Changed 10:03:24 pm	QA CHK	REV	Drawing Number	Sheet 29 of 51

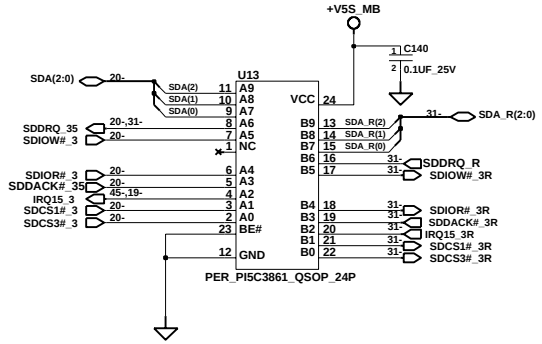


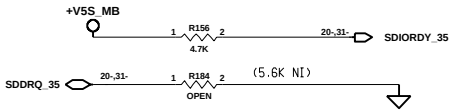




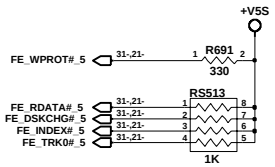
Engineer	INVENTEC				
Drawn by Kevin Tseng	TITLE: Fenway2.0 HDD CN				Size A3
R&D CHK					
DOC CTRL CHK					
MFG ENGR CHK					
Changed by	Date Changed Thursday, May 30, 2002	Time Changed 11:48:16 am	QA CHK	REV	Drawing Number	Sheet 30 of 51

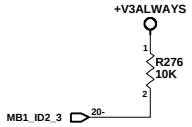






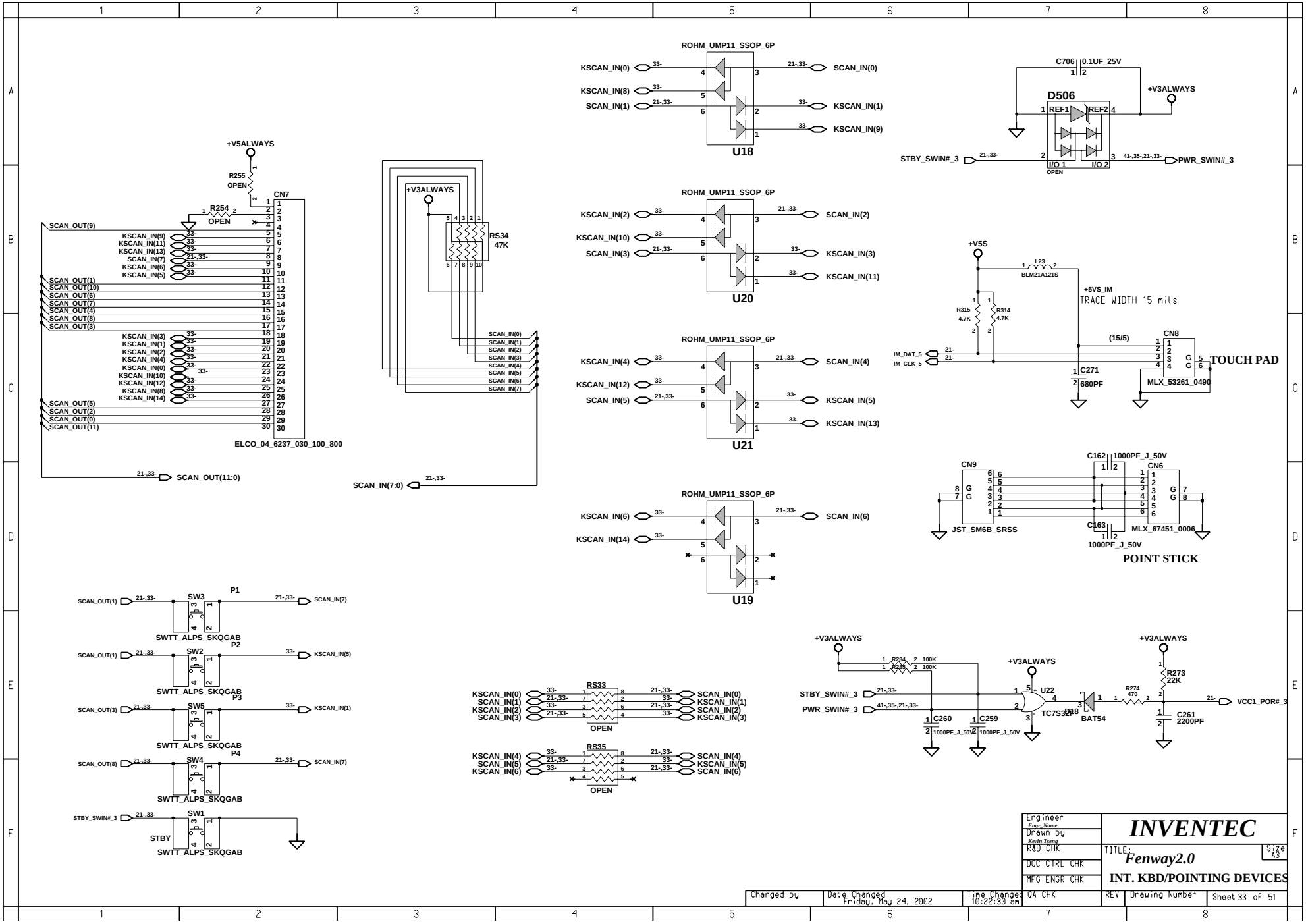
Engineer	**INVENTEC**				
Drawn by *Kevin Tseng*					
R&D CHK	TITLE: *Fenway2.0* **MULTIBAY**				Size A3
DOC CTRL CHK					
MFG ENGR CHK					
Changed by	Date Changed Thursday, May 30, 2002	Time Changed 11:50:57 am	QA CHK	REV	Drawing Number	Sheet 31 of 51



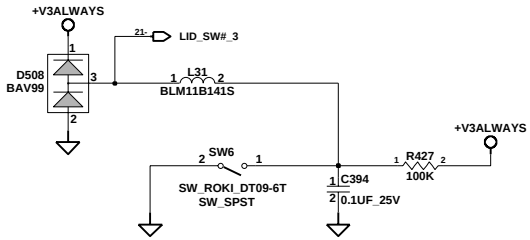


DEVICE	MB_ID2	MB_ID1	MB_ID0	FDD_ID
IDE	0	0	1	NA
FDD	0	1	0	0
NO DEVICE	1	1	1	1

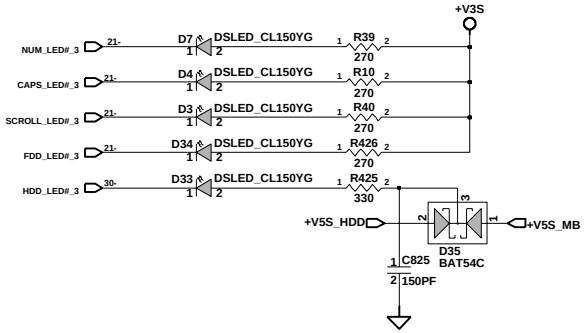
Engineer	INVENTEC		
Drawn by Kevin Tseng			
R&D CHK	TITLE: Fenway2.0 DUAL BAY		Size A3
DOC CTRL CHK			
MFG ENGR CHK			
Changed by	Date Changed Wednesday, January 23, 2002	Time Changed 10:03:42 pm	QA CHK
REV	Drawing Number	Sheet 32 of 51	

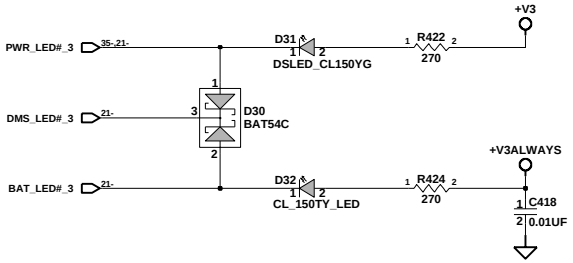


Engineer Engr_Name	INVENTEC				
Drawn by Kevin Tserna	TITLE: Fenway2.0				Size A3
R&D CHK	INT. KBD/POINTING DEVICES				
DOC CTRL CHK					
MFG ENGR CHK					
Changed by	Date Changed Friday, May 24, 2002	Time Changed 10:22:30 am	QA CHK	REV	Drawing Number	Sheet 33 of 51

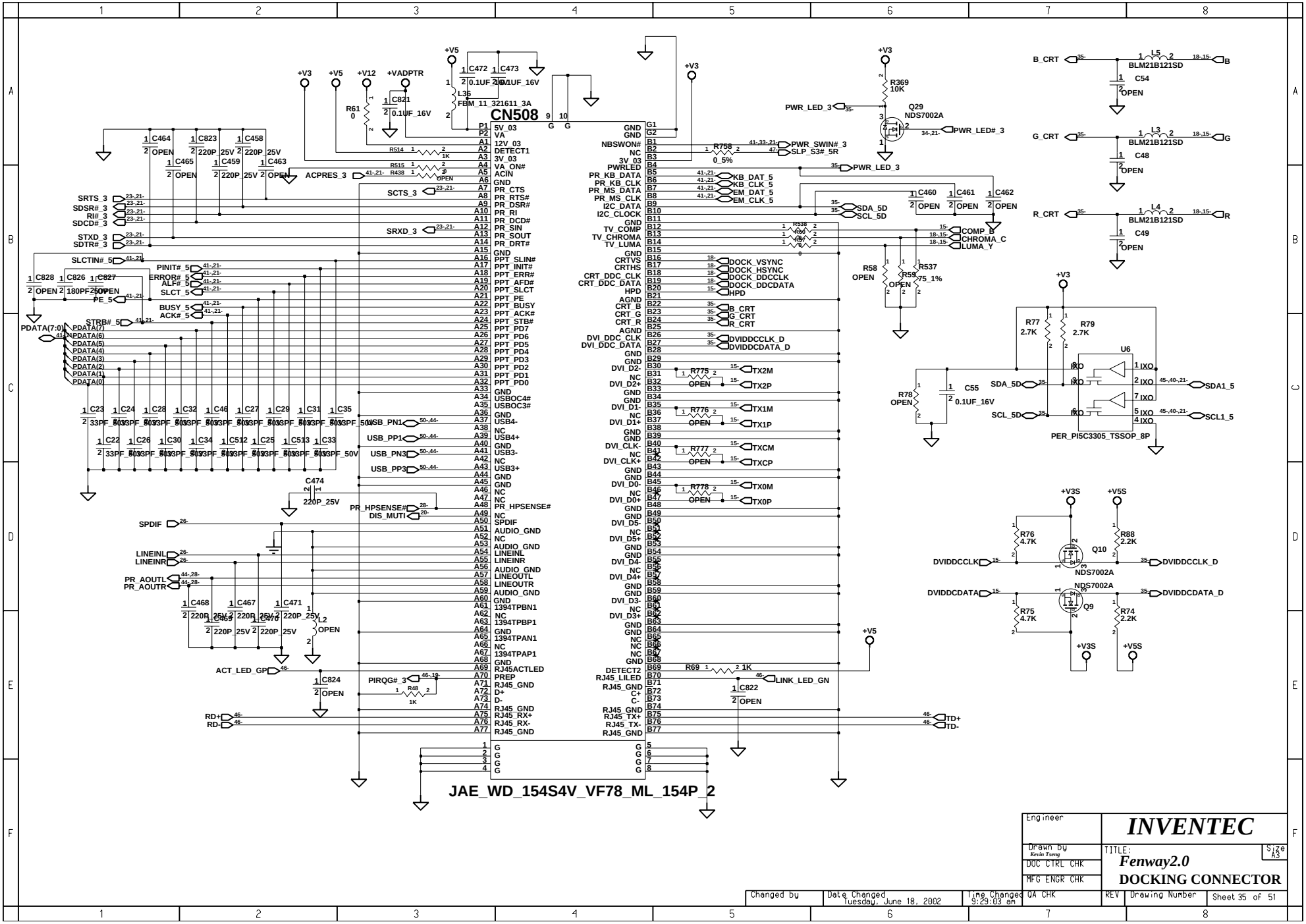


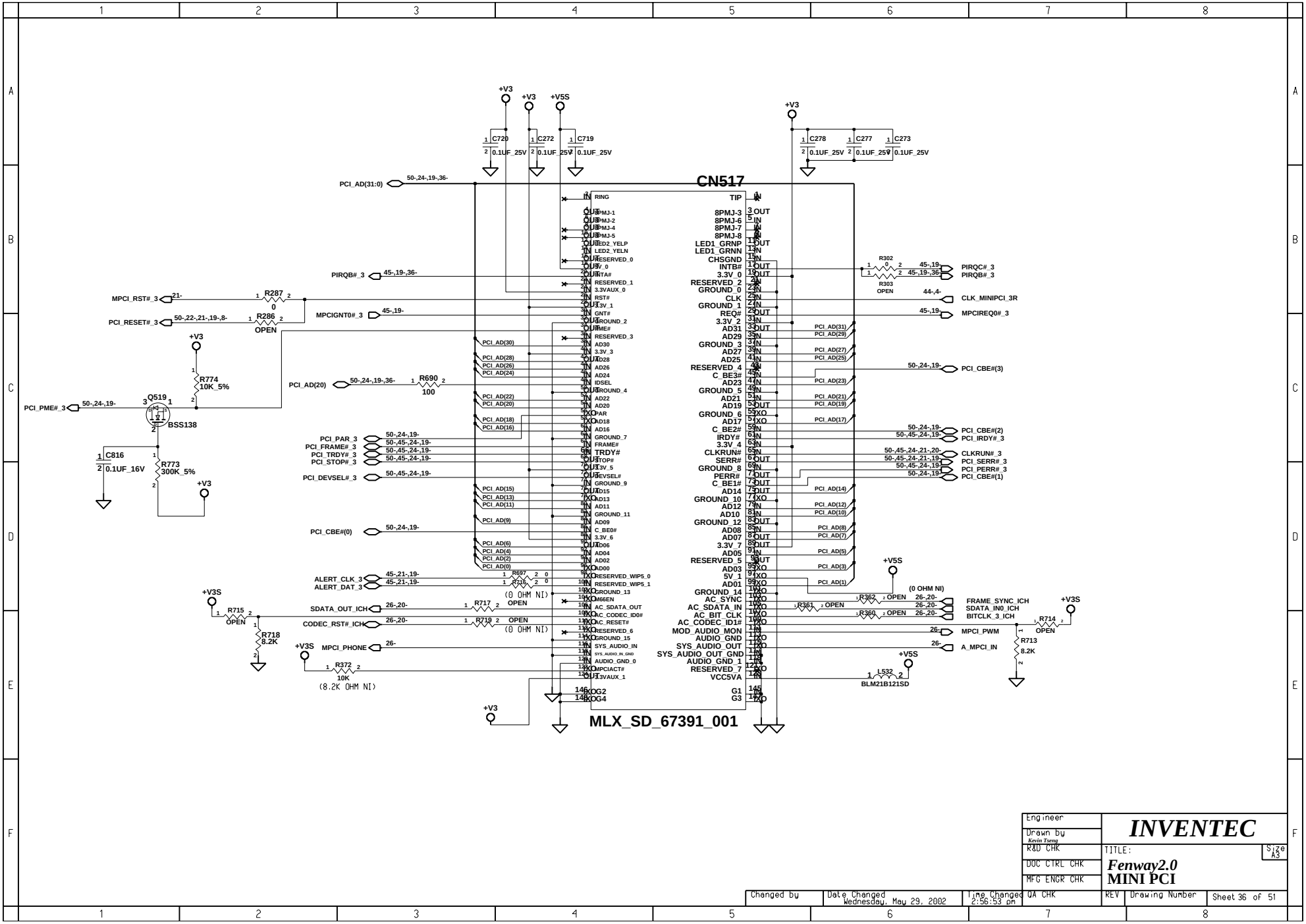
LID SWITCH



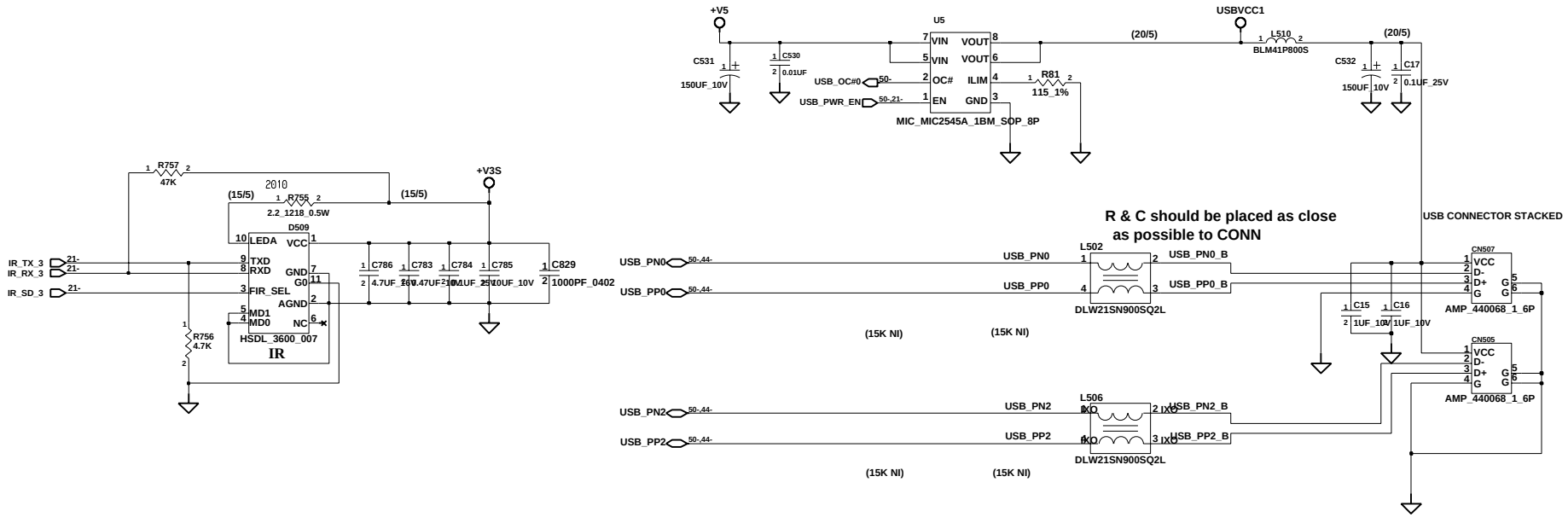


Engineer				INVENTEC	
Drawn by Kevin Tseng				TITLE: Fenway2.0	Size A3
DOC CTRL CHK				LID SWITCHES / LEDS	
MFG ENGR CHK					
Changed by	Date Changed Thursday, May 30, 2002	Time Changed 6:33:31 pm	QA CHK	REV / Drawing Number	Sheet 34 of 51

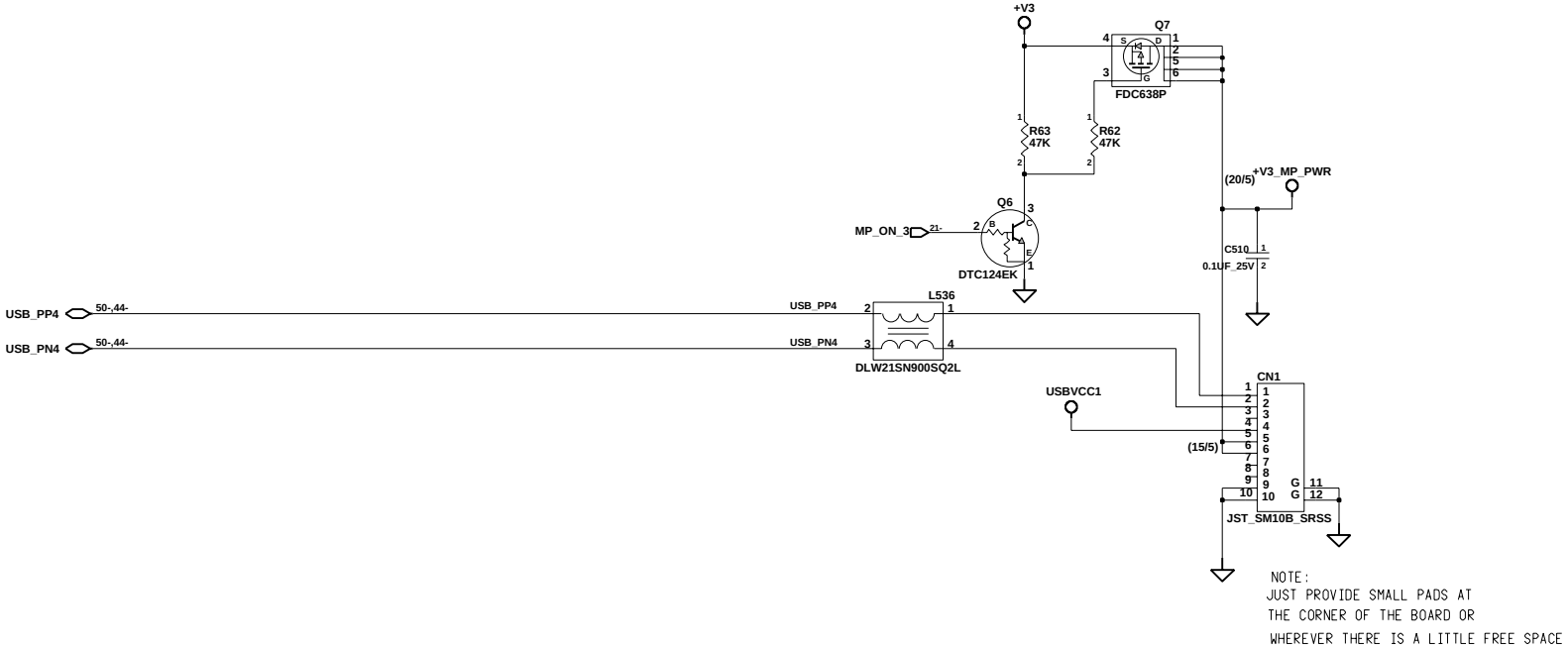

CN508
JAE_WD_154S4V_VF78_ML_154P_2
+V3
+V5
+V12
+VADPTR
+V3S
+V5S
L36
FBM_11_321611_3A
R61
0
C821
0.1UF_16V
C472
C473
0.1UF_16V
C464
C465
C823
C458
C459
C463
220P_25V
OPEN
ACPRES_3
SCTS_3
SRXD_3
SRTS_3
SDSR#_3
RI#_3
SDCD#_3
STXD_3
SDTR#_3
SLCTIN#_5
PINIT#_5
ERROR#_5
ALF#_5
SLCT_5
BUSY_5
ACK#_5
STRB#_5
PE_5
PDATA(7:0)
PDATA(7)
PDATA(6)
PDATA(5)
PDATA(4)
PDATA(3)
PDATA(2)
PDATA(1)
PDATA(0)
C828
C826
C827
180PF_50V
C474
220P_25V
SPDIF
LINEINL
LINEINR
PR_AOUTL
PR_AOUTR
C468
C467
C471
L2
ACT_LED_GP
C824
PIRQG#_3
R48
1K
RD+
RD-
USB_PN1
USB_PP1
USB_PN3
USB_PP3
PR_HPSENSE#
DIS_MUTI
5V_03
VA
12V_03
DETECT1
3V_03
VA_ON#
ACIN
GND
PR_CTS
PR_RTS#
PR_DSR#
PR_RI
PR_DCD#
PR_SIN
PR_SOUT
PR_DRT#
PPT_SLIN#
PPT_INIT#
PPT_ERR#
PPT_AFD#
PPT_SLCT
PPT_PE
PPT_BUSY
PPT_ACK#
PPT_STB#
PPT_PD7
PPT_PD6
PPT_PD5
PPT_PD4
PPT_PD3
PPT_PD2
PPT_PD1
PPT_PD0
USBOC4#
USBOC3#
USB4-
USB4+
USB3-
USB3+
PR_HPSENSE#
SPDIF
AUDIO_GND
LINEINL
LINEINR
LINEOUTL
LINEOUTR
1394TPBN1
1394TPBP1
1394TPAN1
1394TPAP1
RJ45ACTLED
PREP
RJ45_GND
D+
D-
RJ45_RX+
RJ45_RX-
NBSWON#
PWRLED
PR_KB_DATA
PR_KB_CLK
PR_MS_DATA
PR_MS_CLK
I2C_DATA
I2C_CLOCK
TV_COMP
TV_CHROMA
TV_LUMA
CRTVS
CRTHS
CRT_DDC_CLK
CRT_DDC_DATA
HPD
AGND
CRT_B
CRT_G
CRT_R
DVI_DDC_CLK
DVI_DDC_DATA
DVI_D2-
DVI_D2+
DVI_D1-
DVI_D1+
DVI_CLK-
DVI_CLK+
DVI_D0-
DVI_D0+
DVI_D5-
DVI_D5+
DVI_D4-
DVI_D4+
DVI_D3-
DVI_D3+
DETECT2
RJ45_LILED
RJ45_TX+
RJ45_TX-
R758
0_5%
PWR_SWIN#_3
SLP_S3#_5R
PWR_LED_3
KB_DAT_5
KB_CLK_5
EM_DAT_5
EM_CLK_5
SDA_5D
SCL_5D
COMP_B
CHROMA_C
LUMA_Y
DOCK_VSYNC
DOCK_HSYNC
DOCK_DDCCLK
DOCK_DDCDATA
HPD
B_CRT
G_CRT
R_CRT
DVIDDCCLK_D
DVIDDCDATA_D
TX2M
TX2P
TX1M
TX1P
TXCM
TXCP
TX0M
TX0P
R69
1K
LINK_LED_GN
C822
TD+
TD-
R369
10K
Q29
NDS7002A
PWR_LED#_3
C460
C461
C462
R538
R537
75_1%
R58
R59
B_CRT
G_CRT
R_CRT
L5
L3
L4
BLM21B121SD
C54
C48
C49
R77
2.7K
R79
2.7K
U6
R78
C55
0.1UF_16V
SDA_5D
SCL_5D
SDA1_5
SCL1_5
PER_PI5C3305_TSSOP_8P
R76
4.7K
R88
2.2K
Q10
NDS7002A
DVIDDCCLK
DVIDDCCLK_D
DVIDDCDATA
DVIDDCDATA_D
R75
4.7K
R74
2.2K
Q9
NDS7002A
INVENTEC
Engineer
Drawn By
Kevin Tseng
DOC CTRL CHK
MFG ENGR CHK
QA CHK
TITLE:
Fenway2.0
DOCKING CONNECTOR
Size
A3
REV
Drawing Number
Sheet 35 of 51
Changed by
Date Changed
Tuesday, June 18, 2002
Time Changed
9:29:03 am



Engineer		INVENTEC	
Drawn by Kevin Tseng			
R&D CHK		TITLE: Fenway2.0 MINI PCI	Size A3
DOC CTRL CHK			
MFG ENGR CHK			
Changed by	Date Changed Wednesday, May 29, 2002	Time Changed 2:56:53 pm	QA CHK
REV	Drawing Number	Sheet 36 of 51	

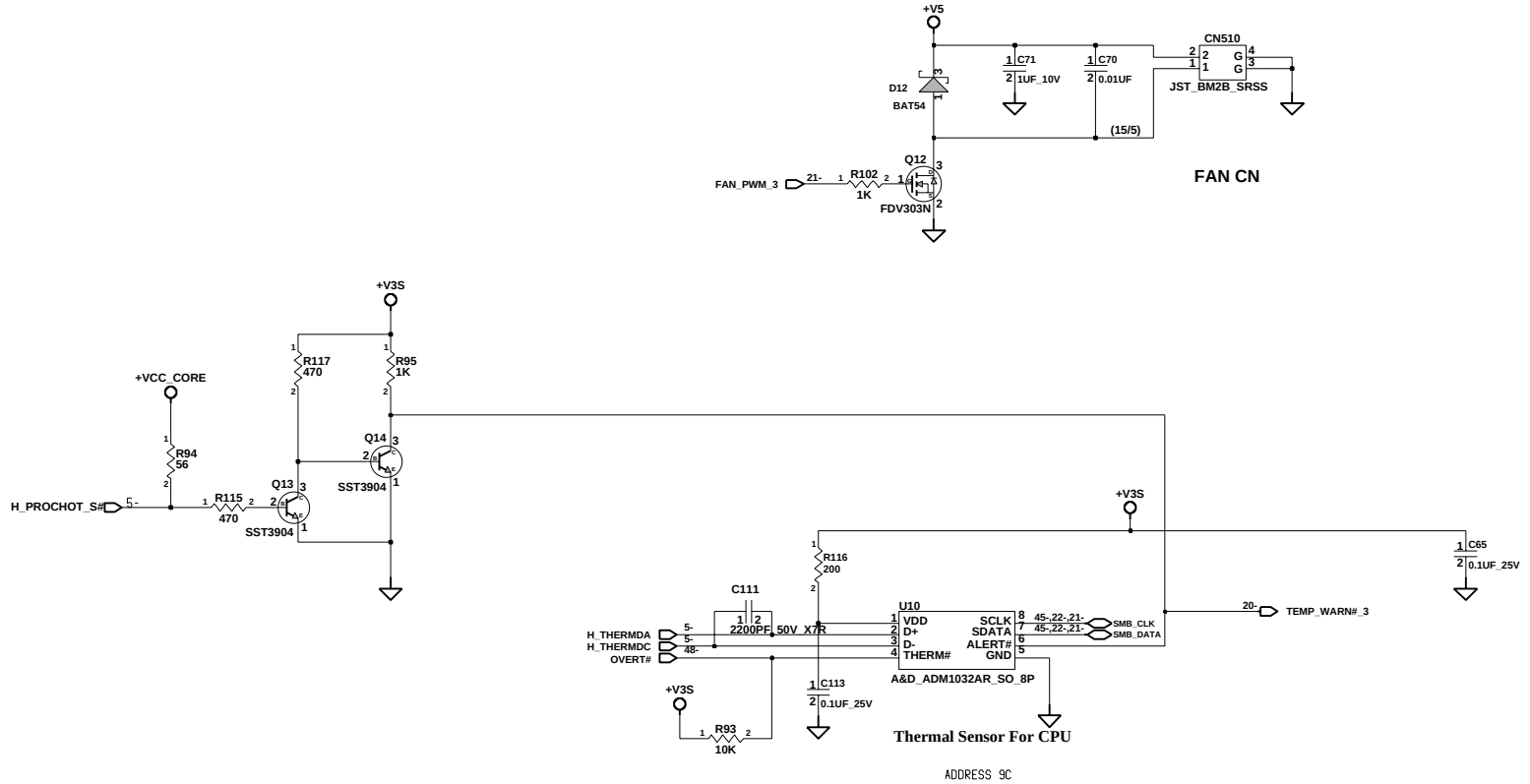


Engineer	INVENTEC				
Drawn by Kevin Tseng	TITLE: Fenway2.0				Size A3
R&D CHK	USB, IR				
DOC CTRL CHK					
MFG ENGR CHK					
Changed by	Date Changed Friday, June 21, 2002	Time Changed 3:28:46 pm	QA CHK	REV	Drawing Number	Sheet 37 of 51

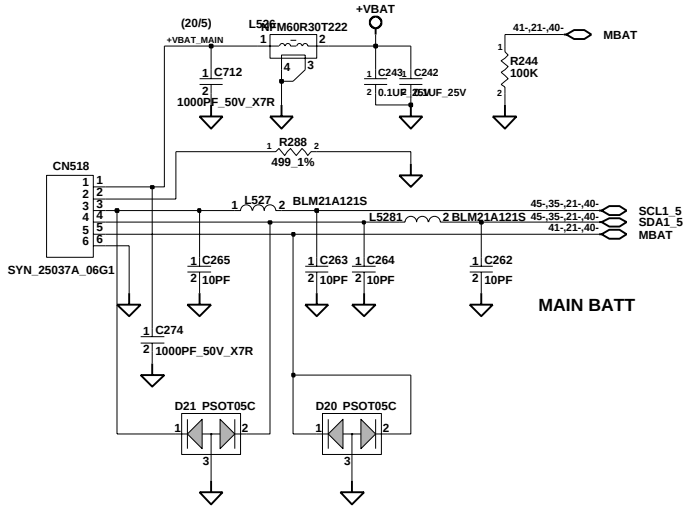


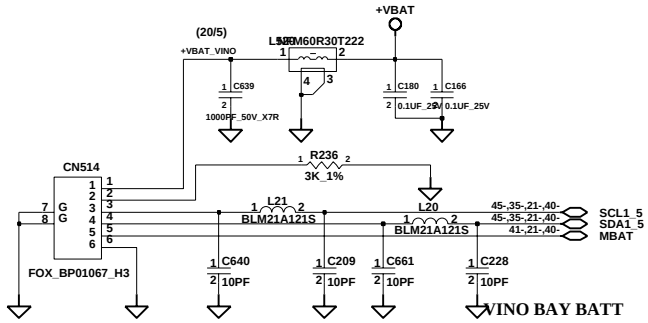
NOTE:
JUST PROVIDE SMALL PADS AT
THE CORNER OF THE BOARD OR
WHEREVER THERE IS A LITTLE FREE SPACE

Engineer	INVENTEC				
Drawn by Kevin Tseng					
R&D CHK	TITLE: Fenway2.0 BLUETOOTH				Size A3
DOC CTRL CHK					
MFG ENGR CHK					
Changed by	Date Changed Thursday, April 25, 2002	Time Changed 6:57:11 pm	QA CHK	REV	Drawing Number	Sheet 38 of 51



Engineer	INVENTEC						
Drawn by Kevin Tseng	TITLE: Fenway2.0						Size A3
R&D CHK	THERMAL SENSOR & FAN CONTROLLER						
DOC CTRL CHK							
MFG ENGR CHK							
Changed by	Date Changed Friday, May 10, 2002	Time Changed 6:33:00 pm	QA CHK	REV	Drawing Number	Sheet 39 of 51	



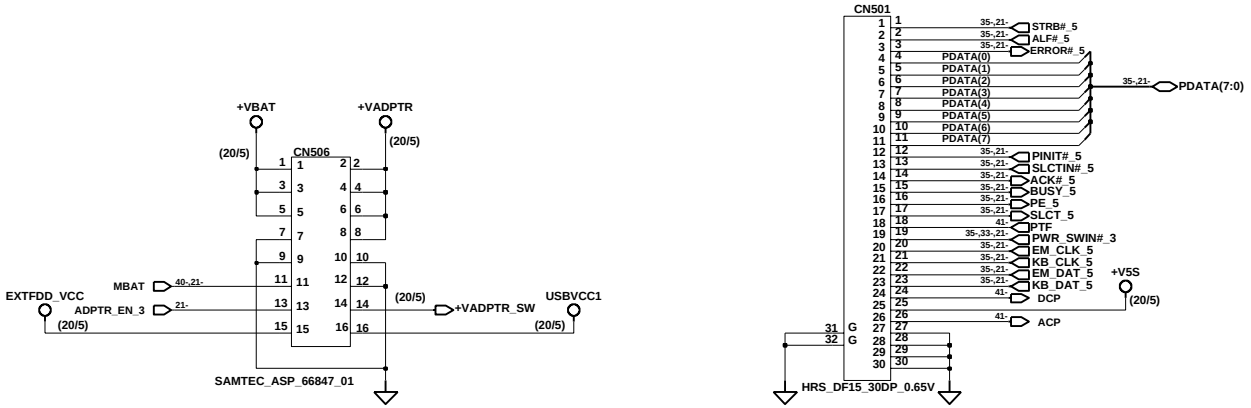


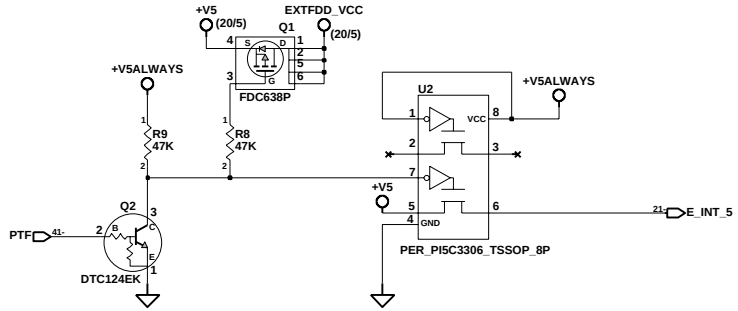
Engineer			
Drawn by Kevin Tseng			
R&D CHK			
DOC CTRL CHK			
MFG ENGR CHK			
Changed by	Date Changed Wednesday, January 23, 2002	Time Changed 10:04:27 pm	QA CHK

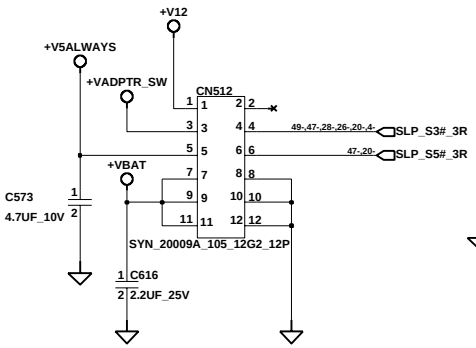
INVENTEC

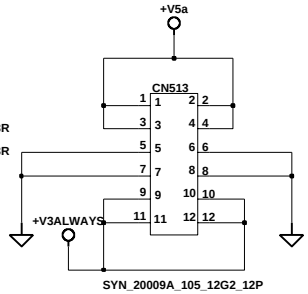
TITLE: *Fenway2.0*
ADAPTER SENSE CIRCUIT & CLAMP CIRCUIT

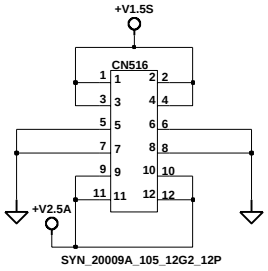
Size A3 | REV | Drawing Number | Sheet 40 of 51

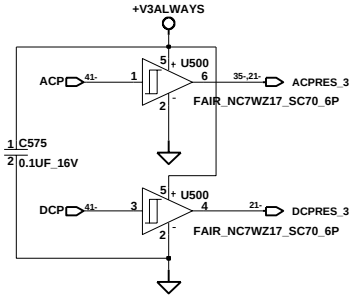






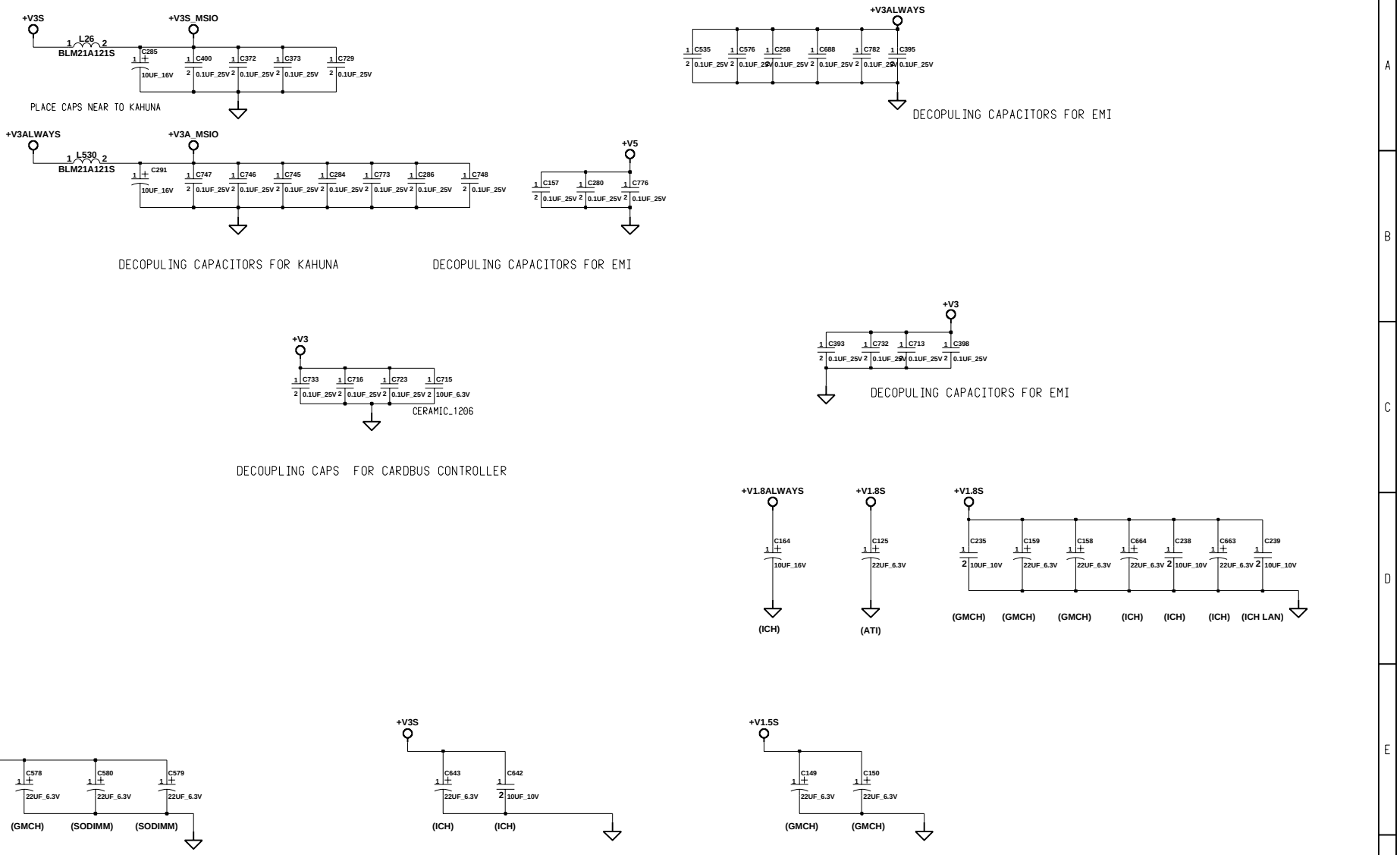




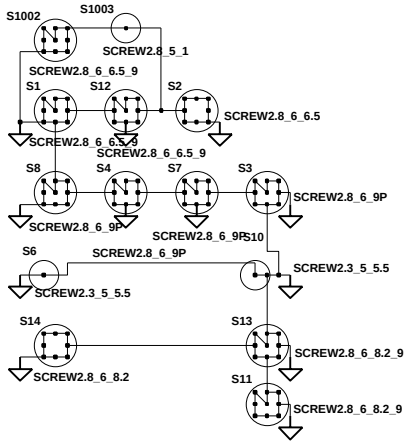


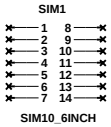
POWER BOARD CN

Engineer CHAI SONG POH	INVENTEC		
Drawn by Kevin Tseng	TITLE: Fenway2.0 PWR MODULE CONN		Size A3
DOC CTRL CHK			
MFG ENGR CHK			
Changed by	Date Changed Wednesday, April 17, 2002	Time Changed 10:15:25 am	QA CHK
REV	Drawing Number	Sheet 41 of 51	



Engineer	INVENTEC						
Drawn by Kevin Tseng							
R&D CHK	TITLE: Fenway2.0						Size A3
DOC CTRL CHK	DECOUPLING CAPS						
MFG ENGR CHK							
Changed by EE1	Date Changed Friday, April 26, 2002	Time Changed 2:43:49 pm	QA CHK	REV	Drawing Number	Sheet 42 of 51	





FOR PCB IMPEDENCE TEST

Engineer				INVENTEC	
Drawn by Kevin Tseng				TITLE: Fenway2.0 Drill Hole	Size A3
R&D CHK					
DOC CTRL CHK					
MFG ENGR CHK					
Changed by	Date Changed Wednesday, January 23, 2002	Time Changed 10:04:41 pm	QA CHK	REV / Drawing Number	Sheet 43 of 51

H_D#(0)	9-,5-
H_D#(1)	9-,5-
H_D#(2)	9-,5-
H_D#(3)	9-,5-
H_D#(4)	9-,5-
H_D#(5)	9-,5-
H_D#(6)	9-,5-
H_D#(7)	9-,5-
H_D#(8)	9-,5-
H_D#(9)	9-,5-
H_D#(10)	9-,5-
H_D#(11)	9-,5-
H_D#(12)	9-,5-
H_D#(13)	9-,5-
H_D#(14)	9-,5-
H_D#(15)	9-,5-
H_D#(16)	9-,5-
H_D#(17)	9-,5-
H_D#(18)	9-,5-
H_D#(19)	9-,5-
H_D#(20)	9-,5-
H_D#(21)	9-,5-
H_D#(22)	9-,5-
H_D#(23)	9-,5-
H_D#(24)	9-,5-
H_D#(25)	9-,5-
H_D#(26)	9-,5-
H_D#(27)	9-,5-
H_D#(28)	9-,5-
H_D#(29)	9-,5-
H_D#(30)	9-,5-
H_D#(31)	9-,5-
H_D#(32)	9-,5-
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H_D#(39)	9-,5-
H_D#(40)	9-,5-
H_D#(41)	9-,5-
H_D#(42)	9-,5-
H_D#(43)	9-,5-
H_D#(44)	9-,5-
H_D#(45)	9-,5-
H_D#(46)	9-,5-
H_D#(47)	9-,5-
H_D#(48)	9-,5-
H_D#(49)	9-,5-
H_D#(50)	9-,5-
H_D#(51)	9-,5-
H_D#(52)	9-,5-
H_D#(53)	9-,5-
H_D#(54)	9-,5-
H_D#(55)	9-,5-
H_D#(56)	9-,5-
H_D#(57)	9-,5-
H_D#(58)	9-,5-
H_D#(59)	9-,5-
H_D#(60)	9-,5-
H_D#(61)	9-,5-
H_D#(62)	9-,5-
H_D#(63)	9-,5-
H_A#(3)	9-,5-
H_A#(4)	9-,5-
H_A#(5)	9-,5-
H_A#(6)	9-,5-
H_A#(7)	9-,5-
H_A#(8)	9-,5-
H_A#(9)	9-,5-
H_A#(10)	9-,5-
H_A#(11)	9-,5-
H_A#(12)	9-,5-
H_A#(13)	9-,5-
H_A#(14)	9-,5-
H_A#(15)	9-,5-
H_A#(16)	9-,5-
H_A#(17)	9-,5-
H_A#(18)	9-,5-
H_A#(19)	9-,5-
H_A#(20)	9-,5-
H_A#(21)	9-,5-
H_A#(22)	9-,5-
H_A#(23)	9-,5-
H_A#(24)	9-,5-
H_A#(25)	9-,5-
H_A#(26)	9-,5-
H_A#(27)	9-,5-
H_A#(28)	9-,5-
H_A#(29)	9-,5-
H_A#(30)	9-,5-
H_A#(31)	9-,5-

H_TRDY#	9-,5-
H_LOCK#	9-,5-
H_HITM#	9-,5-
H_HIT#	9-,5-
H_DRDY#	9-,5-
H_DEFER#	9-,5-
H_DBSY#	9-,5-
H_BPRI#	9-,5-
H_BNR#	9-,5-
H_ADS#	9-,5-
H_RESET#	
H_REQ#(0)	9-,5-
H_REQ#(1)	9-,5-
H_REQ#(2)	9-,5-
H_REQ#(3)	9-,5-
H_REQ#(4)	9-,5-
H_RS#(0)	9-,5-
H_RS#(1)	9-,5-
H_RS#(2)	9-,5-
H_A20M#	19-,5-
H_FERR#	19-
H_IGNNE#	19-,5-
H_SMI#	19-,5-
H_PWRGD	19-,5-
H_STPCLK#	19-,5-
H_DPSLP#	19-,5-
H_INTR	19-,5-
H_NMI	19-,5-
H_INIT#	19-,5-
H_PICD0	
H_PICD1	
ITP_PREQ#	
ITP_PRDY#	
CLK_BCLK	
CLK_BCLK_R	
CLK_BCLK#	
CLK_BCLK#_R	
CLK_HT	
CLK_HT_R	
CLK_HT#	
CLK_HT#_R	
CLK_ITP	6-,4-
CLK_ITP_R	
CLK_ITP#	6-,4-
CLK_ITP#_R	
CLK_GBOUT	
CLK_AGPCONN	15-,4-
CLK_AGPCONN_R	
CLK_GBIN	
CLK_GBIN_R	
CLK_ICHHUB	19-,4-
CLK_ICHHUB_R	
CLK_ICHPCI_3R	19-,4-
CLK_ICHPCI_3	4-
CLK_CPU_APIC	
CLK_CPU_APICR	
CLK_CPU_APIC_R	
CLK_ICHAPIC_2.5R	
CLK_ICHAPICR	
CLK_ICHAPIC_R	
CLK_CBPCI_3R	24-,4-
CLK_CBPCI_3	4-
CLK_AUDPCI_3R	
CLK_AUDPCI_3	36-,4-
CLK_MINIPCI_3R	
CLK_MINIPCI_3	4-
CLK_DCKPCI_3R	
CLK_DCKPCI_3	22-,4-
CLK_FWHPCI_3R	
CLK_FWHPCI_3	4-
CLK_MSIOPCI_3R	21-,4-
CLK_MSIOPCI_3	
CLK_ICH48_3R	20-,4-
CLK_ICH48_3	4-
CLK_MSIO14_3R	4-
CLK_MSIO14_3	20-,4-
CLK_ICH14_3R	

EXP_PCICLK_3	
USB_PP0	50-,37-
USB_PP0_R	
USB_PP0_B	37-
USB_PN0	50-,37-
USB_PN0_R	
USB_PN0_B	37-
USB_PP1	50-,35-
EUSB_1P_3R	
USB_PN1	50-,35-
EUSB_1N_3R	
USB_PP2	50-,37-
USB_PP2_R	
USB_PP2_B	37-
USB_PN2	50-,37-
USB_PN2_R	
USB_PN2_B	37-
USB_PP3	50-,35-
USB_PN3	50-,35-
USB_PP4	50-,38-
USB_PN4	50-,38-
USB_PP4_R	
USB_PN4_R	
USB_PP5	
USB_PP5_3R	
USB_PN5	
USB_PN5_3R	

AGP_SBA(0)	15-,8-
AGP_SBA(1)	15-,8-
AGP_SBA(2)	15-,8-
AGP_SBA(3)	15-,8-
AGP_SBA(4)	15-,8-
AGP_SBA(5)	15-,8-
AGP_SBA(6)	15-,8-
AGP_SBA(7)	15-,8-
AGP_ST0	45-,15-,8-
AGP_ST1	45-,15-,8-
AGP_ST2	45-,15-,8-
AGP_CBE#(0)	15-,8-
AGP_CBE#(1)	15-,8-
AGP_CBE#(2)	15-,8-
AGP_CBE#(3)	15-,8-
AGP_AD(0)	15-,8-
AGP_AD(1)	15-,8-
AGP_AD(2)	15-,8-
AGP_AD(3)	15-,8-
AGP_AD(4)	15-,8-
AGP_AD(5)	15-,8-
AGP_AD(6)	15-,8-
AGP_AD(7)	15-,8-
AGP_AD(8)	15-,8-
AGP_AD(9)	15-,8-
AGP_AD(10)	15-,8-
AGP_AD(11)	15-,8-
AGP_AD(12)	15-,8-
AGP_AD(13)	15-,8-
AGP_AD(14)	15-,8-
AGP_AD(15)	15-,8-
AGP_AD(16)	15-,8-
AGP_AD(17)	15-,8-
AGP_AD(18)	15-,8-
AGP_AD(19)	15-,8-
AGP_AD(20)	15-,8-
AGP_AD(21)	15-,8-
AGP_AD(22)	15-,8-
AGP_AD(23)	15-,8-
AGP_AD(24)	15-,8-
AGP_AD(25)	15-,8-
AGP_AD(26)	15-,8-
AGP_AD(27)	15-,8-
AGP_AD(28)	15-,8-
AGP_AD(29)	15-,8-
AGP_AD(30)	15-,8-
AGP_AD(31)	15-,8-
AGP_PIPE#	45-,8-
AGP_RBF#	45-,15-,8-
AGP_WBF#	45-,15-,8-
AGP_FRAME#	45-,15-,8-
AGP_IRDY#	45-,15-,8-
AGP_TRDY#	45-,15-,8-
AGP_STOP#	45-,15-,8-
AGP_DEVSEL#	45-,15-,8-
AGP_REQ#	45-,15-,8-
AGP_GNT#	45-,15-,8-
AGP_PAR	45-,15-,8-
AGP_ADSTB0	45-,15-,8-
AGP_ADSTB0#	45-,15-,8-
AGP_ADSTB1	45-,15-,8-
AGP_ADSTB1#	45-,15-,8-
AGP_SBSTB	45-,15-,8-
AGP_SBSTB#	45-,15-,8-

HUB_PSTRB	19-,8-
HUB_PSTRB#	19-,8-
HUB_PD(0)	19-,8-
HUB_PD(1)	19-,8-
HUB_PD(2)	19-,8-
HUB_PD(3)	19-,8-
HUB_PD(4)	19-,8-
HUB_PD(5)	19-,8-
HUB_PD(6)	19-,8-
HUB_PD(7)	19-,8-
HUB_PD(8)	19-,8-
HUB_PD(9)	19-,8-
HUB_PD(10)	19-,8-
A_LEFT	28-,27-,26-
A_RIGHT	28-,27-,26-
PR_AOUTR	35-,28-
PR_AOUTL	35-,28-
INT_MIC_SW	27-
INT_MIC_CN	27-
TXOUTL0-	18-,15-
TXOUTL0+	18-,15-
TXOUTL1-	18-,15-
TXOUTL1+	18-,15-
TXOUTL2-	18-,15-
TXOUTL2+	18-,15-
TXCLKOUTL-	18-,15-
TXCLKOUTL+	18-,15-
TXOUTU0-	18-,15-
TXOUTU0+	18-,15-
TXOUTU1-	18-,15-
TXOUTU1+	18-,15-
TXOUTU2-	18-,15-
TXOUTU2+	18-,15-
TXCLKOUTU-	18-,15-
TXCLKOUTU+	18-,15-

Engineer	
Drawn by	Kevin Tseng
R&D CHK	
DOC CTRL CHK	
MFG ENGR CHK	
QA CHK	

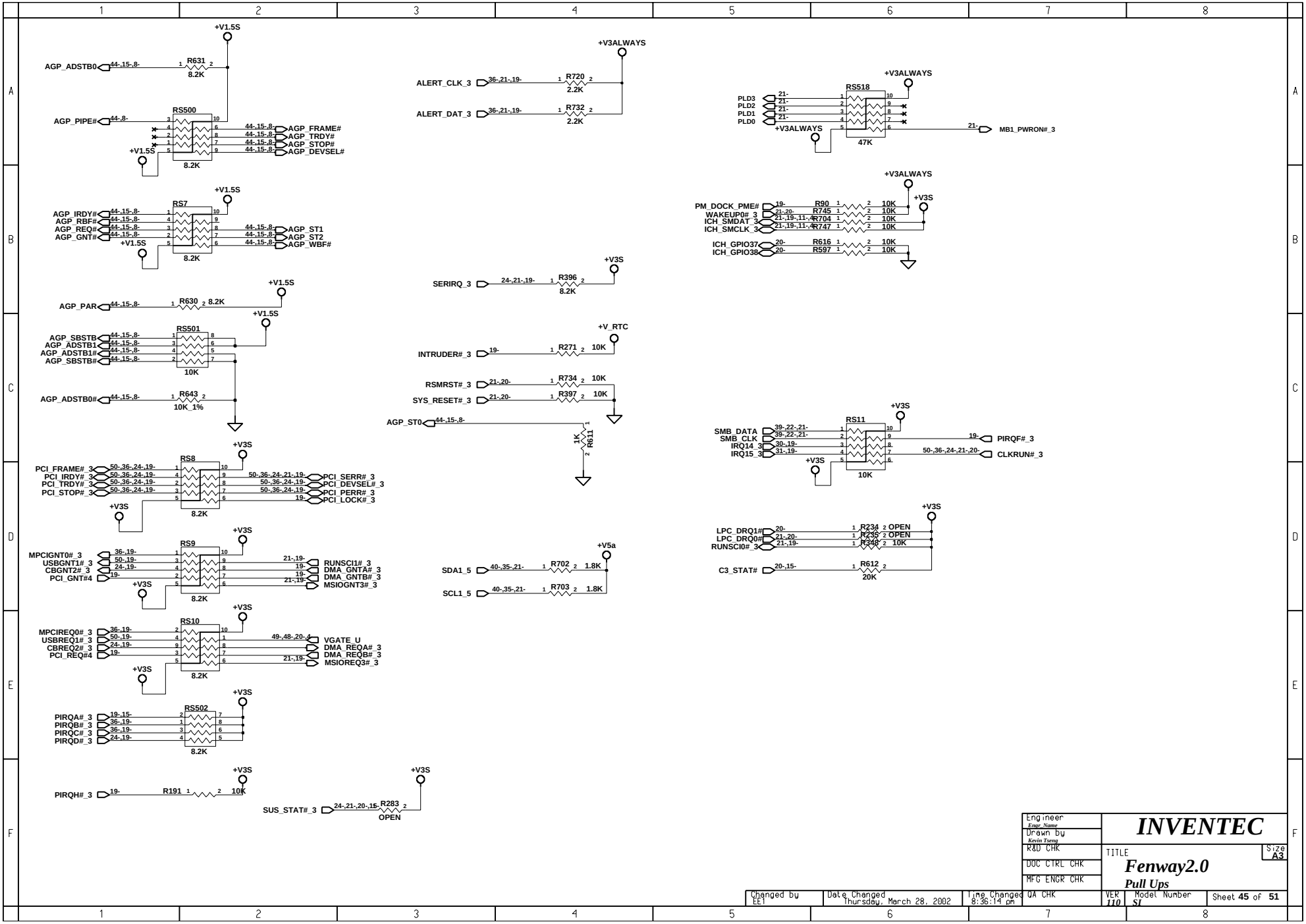
INVENTEC

TITLE **Fenway2.0**

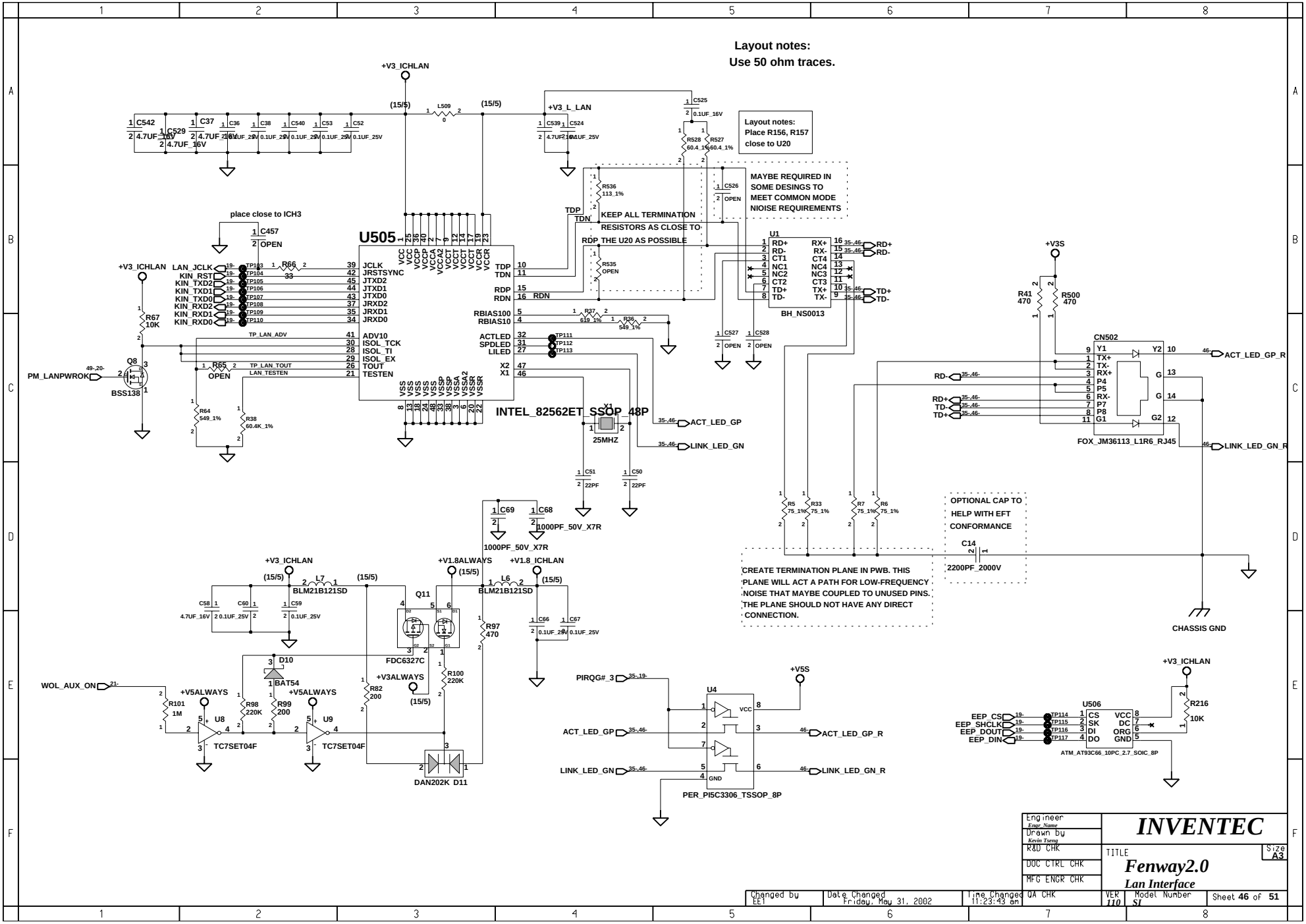
High-speed

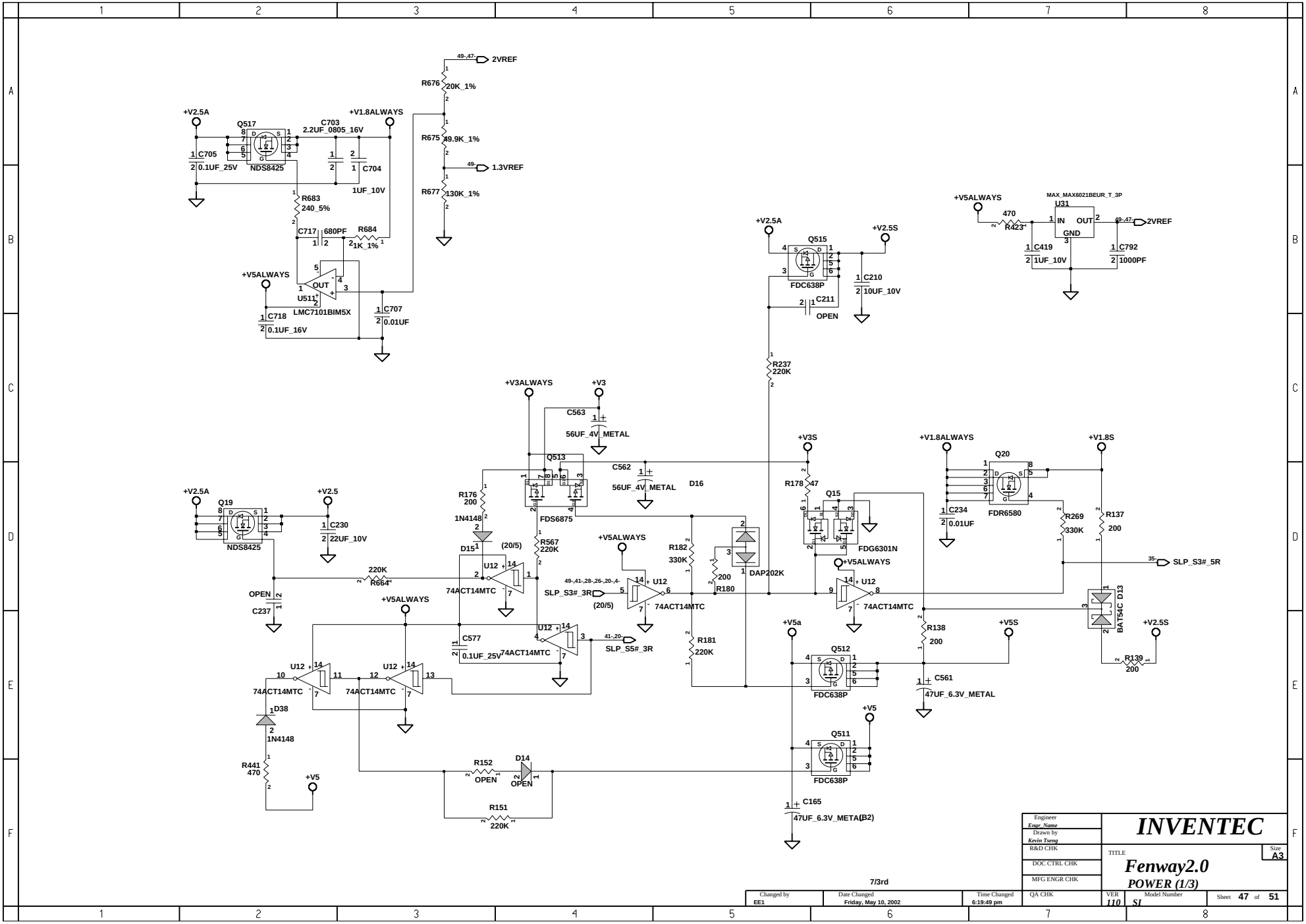
Size **A3**

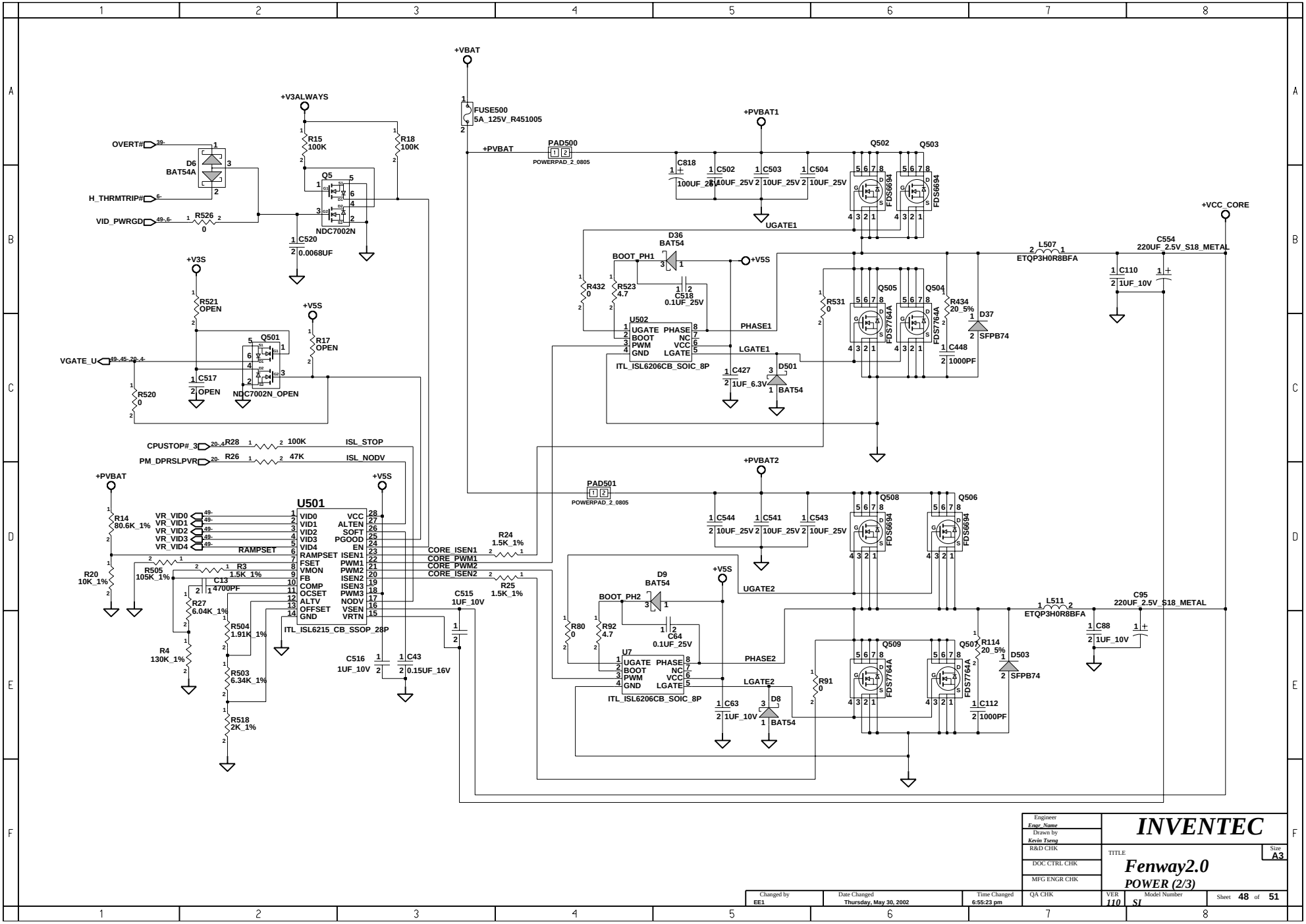
Changed by	Date Changed	Time Changed	VER	Model Number	Sheet 44 of 51
EE1	Friday, April 19, 2002	10:13:32 am		SI	



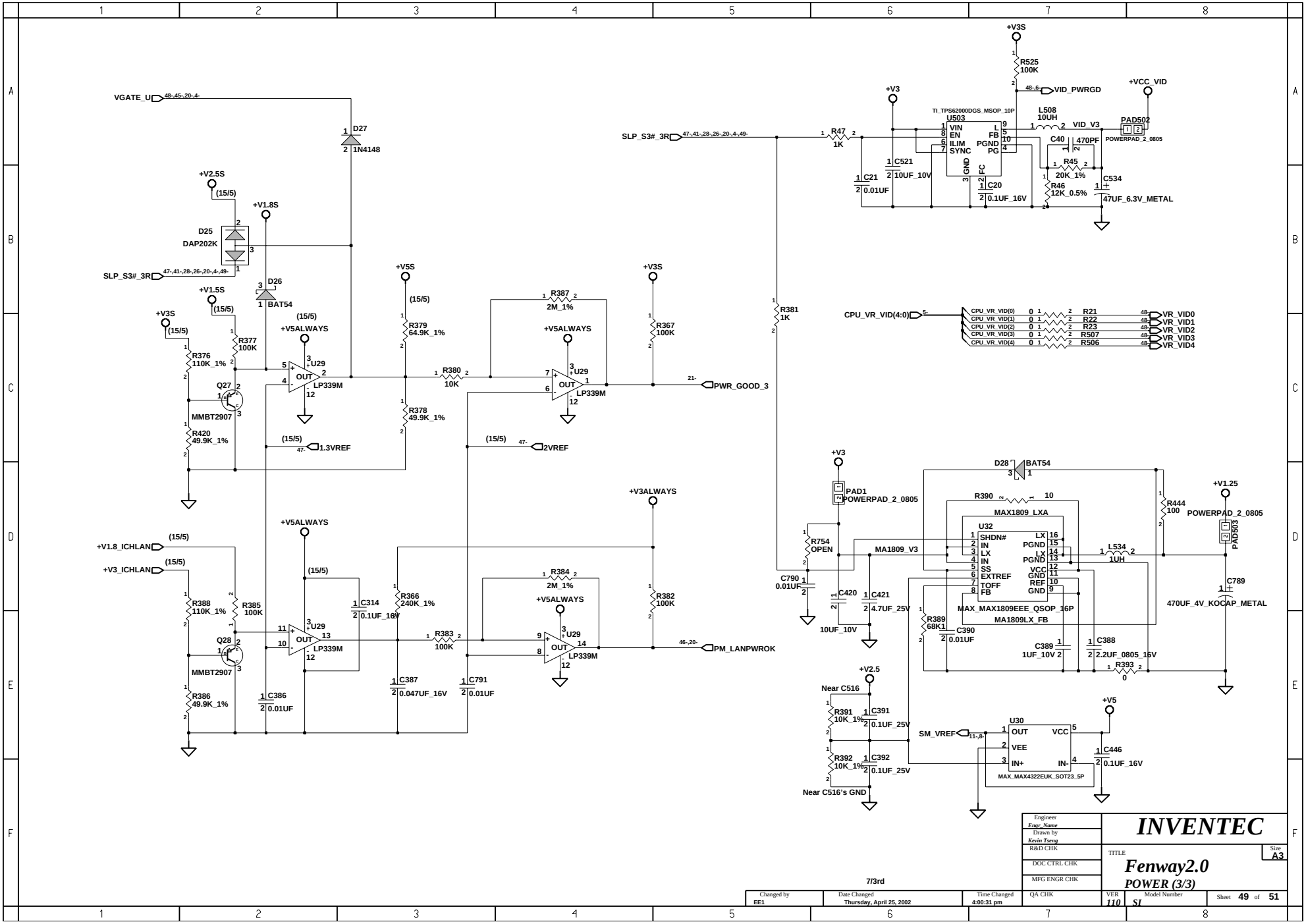
Engineer Engr_Name	INVENTEC				
Drawn by Kevin Tseng					
R&D CHK	TITLE Fenway2.0				Size A3
DOC CTRL CHK	Pull Ups				
MFG ENGR CHK					
Changed by EE1	Date Changed Thursday, March 28, 2002	Time Changed 8:36:14 pm	QA CHK	VER 110	Model Number SI	Sheet 45 of 51

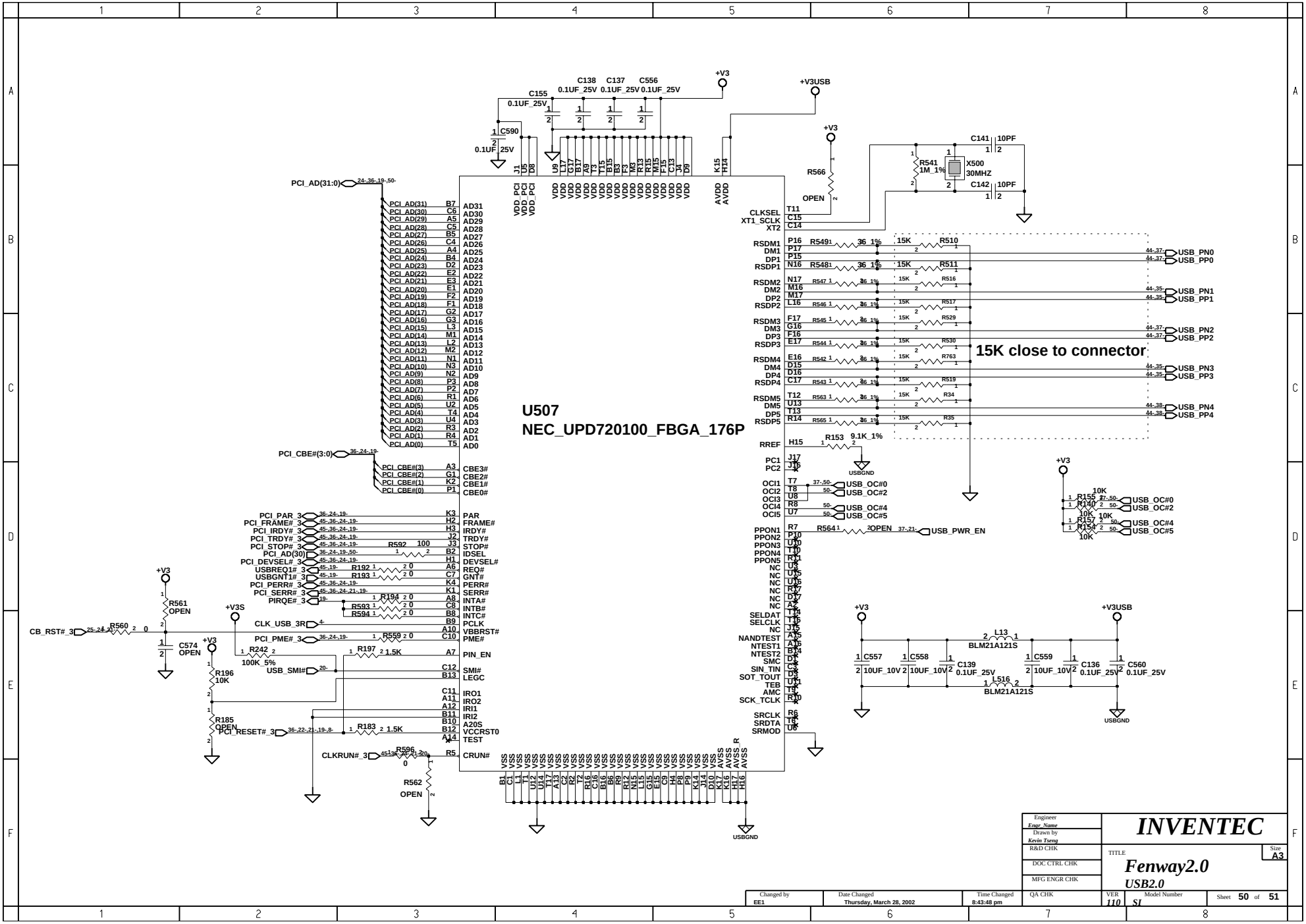

Layout notes:
Use 50 ohm traces.
Layout notes:
Place R156, R157
close to U20
MAYBE REQUIRED IN
SOME DESINGS TO
MEET COMMON MODE
NIOISE REQUIREMENTS
KEEP ALL TERMINATION
RESISTORS AS CLOSE TO
RDP THE U20 AS POSSIBLE
place close to ICH3
U505
INTEL_82562ET_SSOP_48P
BH_NS0013
FOX_JM36113_L1R6_RJ45
OPTIONAL CAP TO
HELP WITH EFT
CONFORMANCE
CREATE TERMINATION PLANE IN PWB. THIS
PLANE WILL ACT A PATH FOR LOW-FREQUENCY
NOISE THAT MAYBE COUPLED TO UNUSED PINS.
THE PLANE SHOULD NOT HAVE ANY DIRECT
CONNECTION.
CHASSIS GND
TC7SET04F
FDC6327C
DAN202K_D11
PER_PI5C3306_TSSOP_8P
ATM_AT93C66_10PC_2.7_SOIC_8P
INVENTEC
Fenway2.0
Lan Interface
Engineer
Drawn by
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
QA CHK
Size A3
Changed by EE1
Date Changed Friday, May 31, 2002
Time Changed 11:23:43 am
VER 110
Model Number SI
Sheet 46 of 51


+V2.5A
Q517
NDS8425
C705
0.1UF_25V
C703
2.2UF_0805_16V
+V1.8ALWAYS
C704
1UF_10V
R683
240_5%
C717
680PF
R684
1K_1%
+V5ALWAYS
U511
OUT
LMC7101BIM5X
C718
0.1UF_16V
C707
0.01UF
R676
20K_1%
R675
49.9K_1%
R677
130K_1%
2VREF
1.3VREF
+V2.5A
Q515
FDC638P
+V2.5S
C210
10UF_10V
C211
OPEN
R237
220K
+V5ALWAYS
470
R423
MAX_MAX6021BEUR_T_3P
U31
IN
OUT
GND
C419
1UF_10V
C792
1000PF
2VREF
+V3ALWAYS
+V3
C563
56UF_4V_METAL
Q513
FDS6875
C562
56UF_4V_METAL
D16
R176
200
1N4148
D15
(20/5)
R567
220K
+V3S
R178
47
Q15
FDG6301N
+V1.8ALWAYS
Q20
FDR6580
C234
0.01UF
+V1.8S
R269
330K
R137
200
SLP_S3#_5R
+V2.5A
Q19
NDS8425
+V2.5
C230
22UF_10V
OPEN
C237
220K
R664
74ACT14MTC
+V5ALWAYS
SLP_S3#_3R
(20/5)
R182
330K
200
R180
DAP202K
+V5ALWAYS
U12
74ACT14MTC
R181
220K
+V5ALWAYS
C577
0.1UF_25V
74ACT14MTC
SLP_S5#_3R
+V5a
Q512
FDC638P
R138
200
+V5S
C561
47UF_6.3V_METAL
BAT54C
D13
+V2.5S
R139
200
D38
1N4148
R441
470
+V5
R152
OPEN
D14
OPEN
R151
220K
Q511
FDC638P
+V5
C165
47UF_6.3V_METAL
INVENTEC
Engineer
Engr_Name
Drawn by
Kevin Tseng
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
QA CHK
TITLE
Fenway2.0
POWER (1/3)
Size
A3
7/3rd
Changed by
EE1
Date Changed
Friday, May 10, 2002
Time Changed
6:19:49 pm
VER
110
Model Number
SI
Sheet 47 of 51

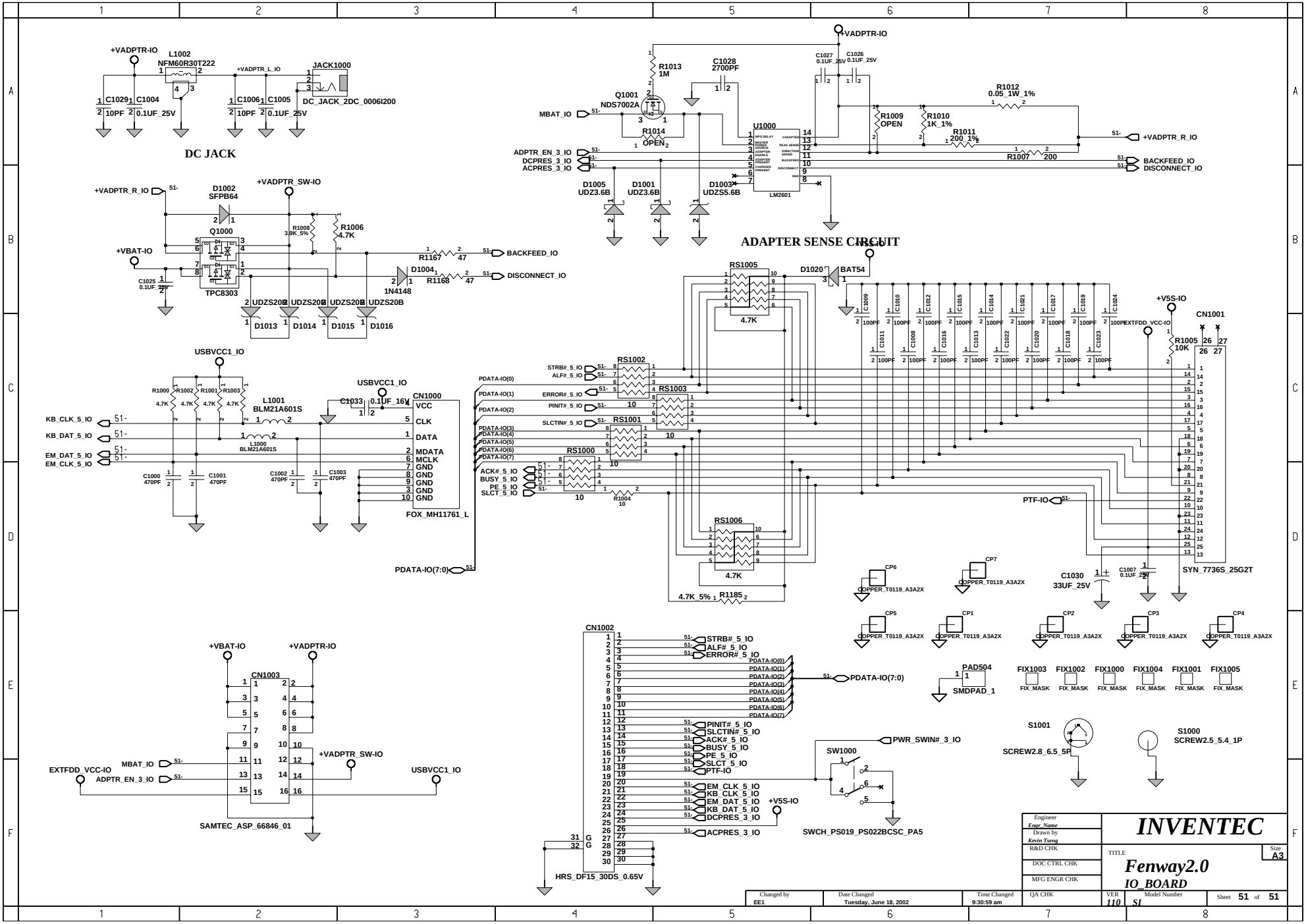


Engineer *Engr_Name*	**INVENTEC**					
Drawn by *Kevin Tseng*						
R&D CHK	TITLE *Fenway2.0*					Size A3
DOC CTRL CHK	*POWER (2/3)*					
MFG ENGR CHK						
Changed by EE1	Date Changed Thursday, May 30, 2002	Time Changed 6:55:23 pm	QA CHK	VER *110*	Model Number *SI*	Sheet 48 of 51


VGATE_U
D27
1N4148
+V2.5S
+V1.8S
D25
DAP202K
SLP_S3#_3R
D26
BAT54
+V1.5S
+V3S
R377
100K
R376
110K_1%
Q27
MMBT2907
R420
49.9K_1%
+V5ALWAYS
U29
LP339M
1.3VREF
+V5S
R379
64.9K_1%
R378
49.9K_1%
R380
10K
R387
2M_1%
2VREF
R367
100K
PWR_GOOD_3
+V1.8_ICHLAN
+V3_ICHLAN
R388
110K_1%
R385
100K
Q28
R386
49.9K_1%
C314
0.1UF_16V
C386
0.01UF
R366
240K_1%
R383
100K
C387
0.047UF_16V
C791
0.01UF
R384
2M_1%
+V3ALWAYS
R382
100K
PM_LANPWROK
R381
1K
SLP_S3#_3R
R47
1K
C21
0.01UF
C521
10UF_10V
U503
TI_TPS62000DGS_MSOP_10P
VIN
EN
ILIM
SYNC
GND
FC
L
FB
PGND
PG
C20
0.1UF_16V
R525
100K
VID_PWRGD
+VCC_VID
L508
10UH
VID_V3
PAD502
POWERPAD_2_0805
C40
470PF
R45
20K_1%
R46
12K_0.5%
C534
47UF_6.3V_METAL
CPU_VR_VID(4:0)
CPU_VR_VID(0)
CPU_VR_VID(1)
CPU_VR_VID(2)
CPU_VR_VID(3)
CPU_VR_VID(4)
R21
R22
R23
R507
R506
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
PAD1
POWERPAD_2_0805
R754
OPEN
C790
0.01UF
C420
10UF_10V
C421
4.7UF_25V
D28
BAT54
R390
10
MAX1809_LXA
U32
SHDN#
IN
LX
IN
SS
EXTREF
TOFF
FB
PGND
LX
PGND
VCC
GND
REF
GND
MAX_MAX1809EEE_QSOP_16P
MA1809_V3
MA1809LX_FB
R389
68K1
C390
0.01UF
C389
1UF_10V
C388
2.2UF_0805_16V
R393
0
L534
1UH
R444
100
+V1.25
POWERPAD_2_0805
PAD503
C789
470UF_4V_KOCAP_METAL
+V2.5
Near C516
R391
10K_1%
C391
0.1UF_25V
R392
10K_1%
C392
0.1UF_25V
Near C516's GND
SM_VREF
U30
OUT
VEE
IN+
VCC
IN-
MAX_MAX4322EUK_SOT23_5P
C446
0.1UF_16V
INVENTEC
Engineer
Engr_Name
Drawn by
Kevin Tseng
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
TITLE
Fenway2.0
POWER (3/3)
Size
A3
7/3rd
Changed by
EE1
Date Changed
Thursday, April 25, 2002
Time Changed
4:00:31 pm
QA CHK
VER
110
Model Number
SI
Sheet 49 of 51



Engineer: Engr_Name	INVENTEC		
Drawn by: Kevin Tseng			
R&D CHK	TITLE: Fenway2.0 USB2.0	Size: A3	
DOC CTRL CHK			
MFG ENGR CHK			
Changed by: EE1	Date Changed: Thursday, March 28, 2002	Time Changed: 8:43:48 pm	QA CHK
VER: 110	Model Number: SI	Sheet 50 of 51	


DC JACK
ADAPTER SENSE CIRCUIT
+VADPTR-IO
L1002
NFM60R30T222
JACK1000
DC_JACK_2DC_0006I200
C1029 10PF
C1004 0.1UF_25V
C1006 10PF
C1005 0.1UF_25V
+VADPTR_L_IO
+VADPTR_R_IO
D1002
SFPB64
+VADPTR_SW-IO
Q1000
TPC8303
R1008 3.9K_5%
R1006 4.7K
+VBAT-IO
C1025 0.1UF_25V
R1167 47
R1168 47
D1004
1N4148
BACKFEED_IO
DISCONNECT_IO
UDZS20B
D1013
D1014
D1015
D1016
R1013 1M
C1028 2700PF
Q1001
NDS7002A
MBAT_IO
R1014 OPEN
U1000
LM2601
ADPTR_EN_3_IO
DCPRES_3_IO
ACPRES_3_IO
D1005 UDZ3.6B
D1001 UDZ3.6B
D1003 UDZS5.6B
C1027 0.1UF_25V
C1026 0.1UF_25V
R1009 OPEN
R1010 1K_1%
R1011 200_1%
R1012 0.05_1W_1%
R1007 200
+VADPTR_R_IO
BACKFEED_IO
DISCONNECT_IO
D1020
BAT54
RS1005
4.7K
+V5S-IO
EXTFDD_VCC-IO
R1005 10K
CN1001
SYN_7736S_25G2T
USBVCC1_IO
R1000 4.7K
R1002 4.7K
R1001 4.7K
R1003 4.7K
L1001
BLM21A601S
C1033 0.1UF_16V
CN1000
FOX_MH11761_L
KB_CLK_5_IO
KB_DAT_5_IO
EM_DAT_5_IO
EM_CLK_5_IO
C1000 470PF
C1001 470PF
C1002 470PF
C1003 470PF
VCC
CLK
DATA
MDATA
MCLK
GND
PDATA-IO(7:0)
RS1002
RS1003
RS1001
RS1000
RS1006
STRB#_5_IO
ALF#_5_IO
ERROR#_5_IO
PINIT#_5_IO
SLCTIN#_5_IO
ACK#_5_IO
BUSY_5_IO
PE_5_IO
SLCT_5_IO
R1004 10
R1185 4.7K_5%
PTF-IO
C1030 33UF_25V
C1007 0.1UF_25V
CP6
CP7
CP5
CP1
CP2
CP3
CP4
COPPER_T0119_A3A2X
PAD504
SMDPAD_1
FIX1003
FIX1002
FIX1000
FIX1004
FIX1001
FIX1005
FIX_MASK
S1001
SCREW2.8_6.5_5P
S1000
SCREW2.5_5.4_1P
+VBAT-IO
+VADPTR-IO
CN1003
EXTFDD_VCC-IO
MBAT_IO
ADPTR_EN_3_IO
+VADPTR_SW-IO
USBVCC1_IO
SAMTEC_ASP_66846_01
CN1002
PDATA-IO(0)
PDATA-IO(1)
PDATA-IO(2)
PDATA-IO(3)
PDATA-IO(4)
PDATA-IO(5)
PDATA-IO(6)
PDATA-IO(7)
PINIT# 5 IO
SLCTIN# 5 IO
ACK# 5 IO
BUSY 5 IO
PE 5 IO
SLCT 5 IO
PTF-IO
EM_CLK_5_IO
KB_CLK_5_IO
EM_DAT_5_IO
KB_DAT_5_IO
DCPRES_3_IO
ACPRES_3_IO
PWR_SWIN#_3_IO
SW1000
SWCH_PS019_PS022BCSC_PA5
HRS_DF15_30DS_0.65V
INVENTEC
Engineer
Engr_Name
Drawn by
Kevin Tseng
R&D CHK
DOC CTRL CHK
MFG ENGR CHK
TITLE
Fenway2.0
IO_BOARD
Size
A3
Changed by
EE1
Date Changed
Tuesday, June 18, 2002
Time Changed
9:30:59 am
QA CHK
VER
110
Model Number
SI
Sheet 51 of 51