PROJECT : CHICAGO (For Intel Huron River Platform)

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P. Leader	Check by	Design by

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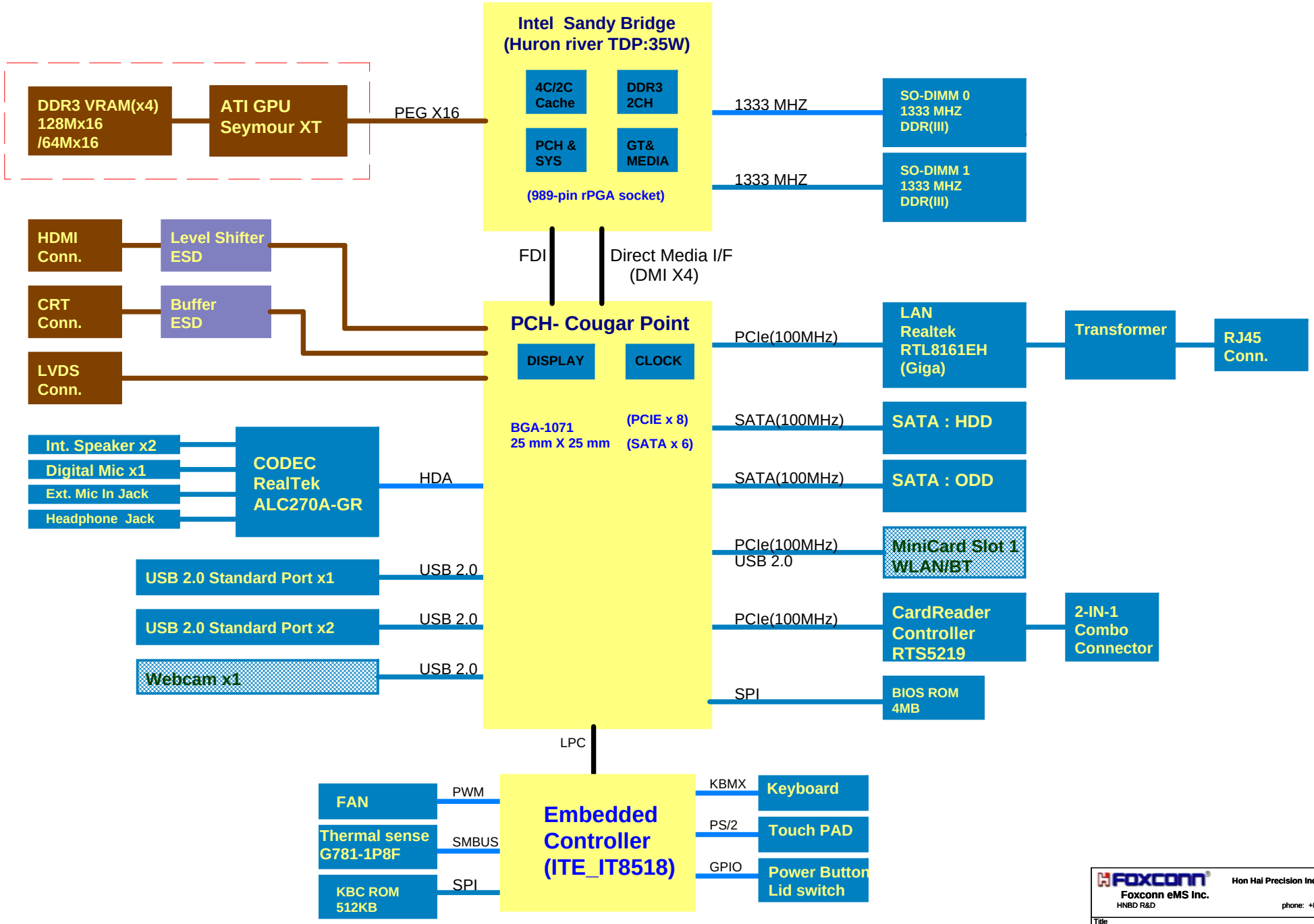

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Title: SYSTEM BLOCK DIAGRAM

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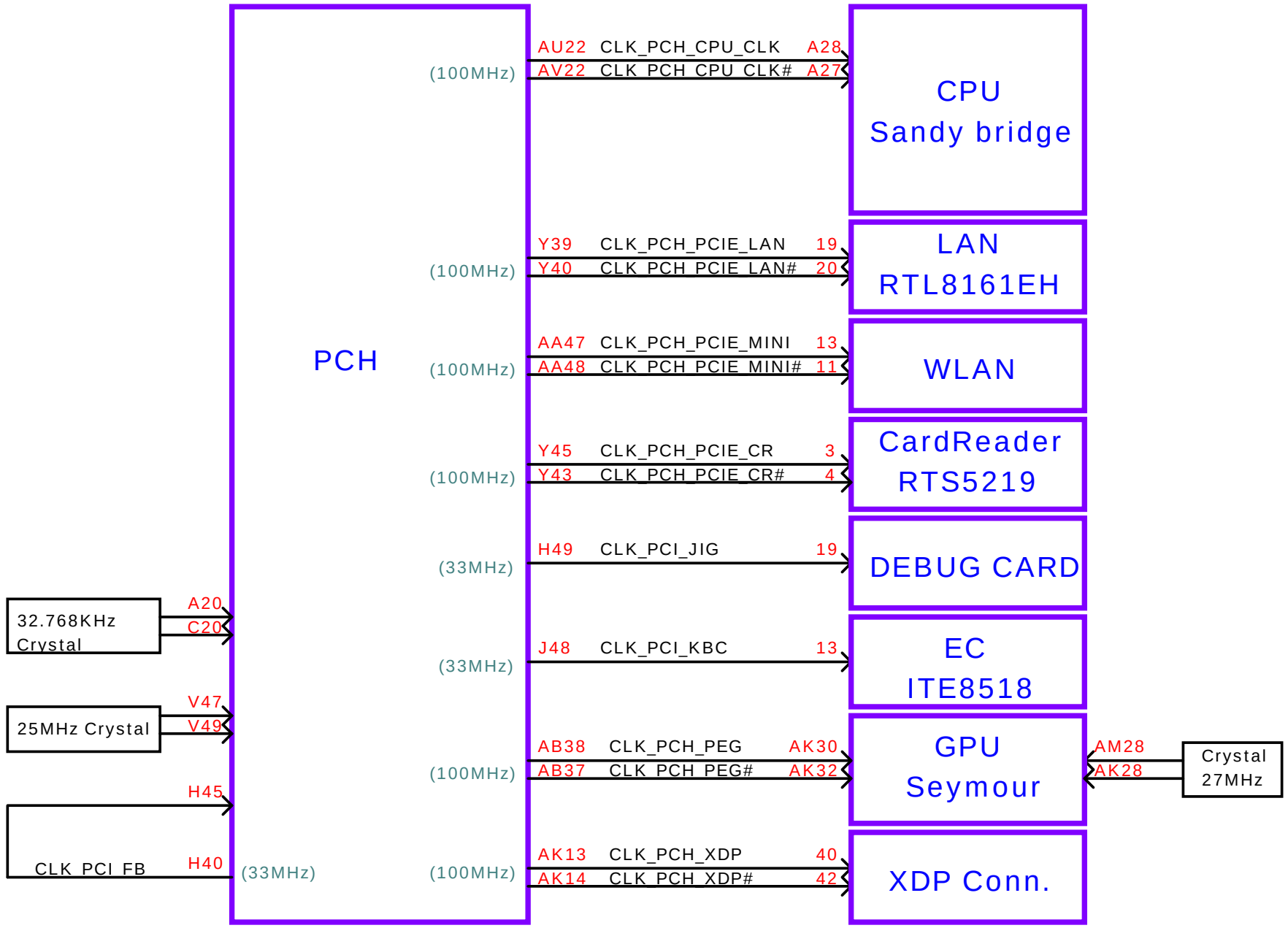

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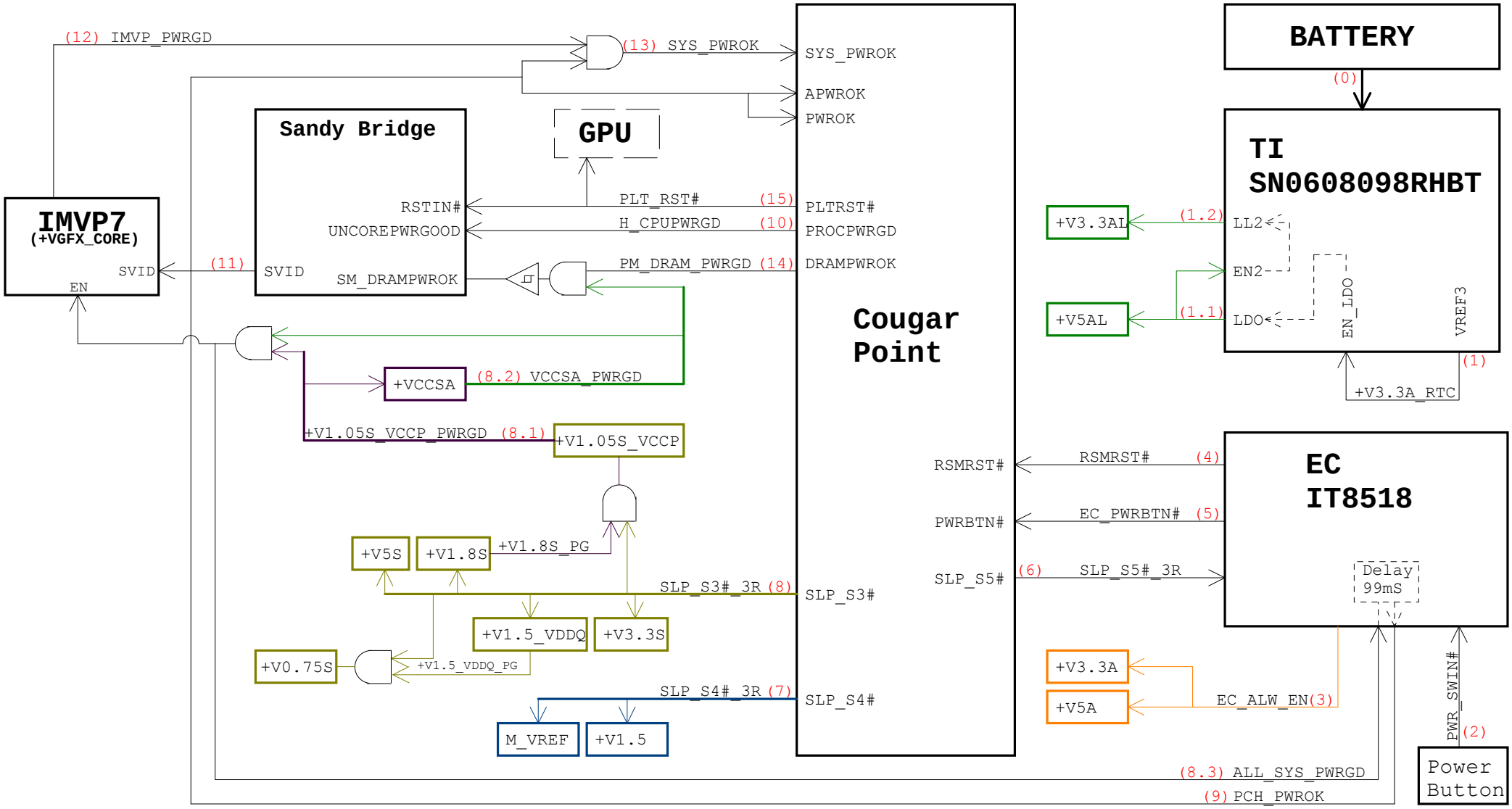

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Title: POWER SEQUENCY DIAGRAM

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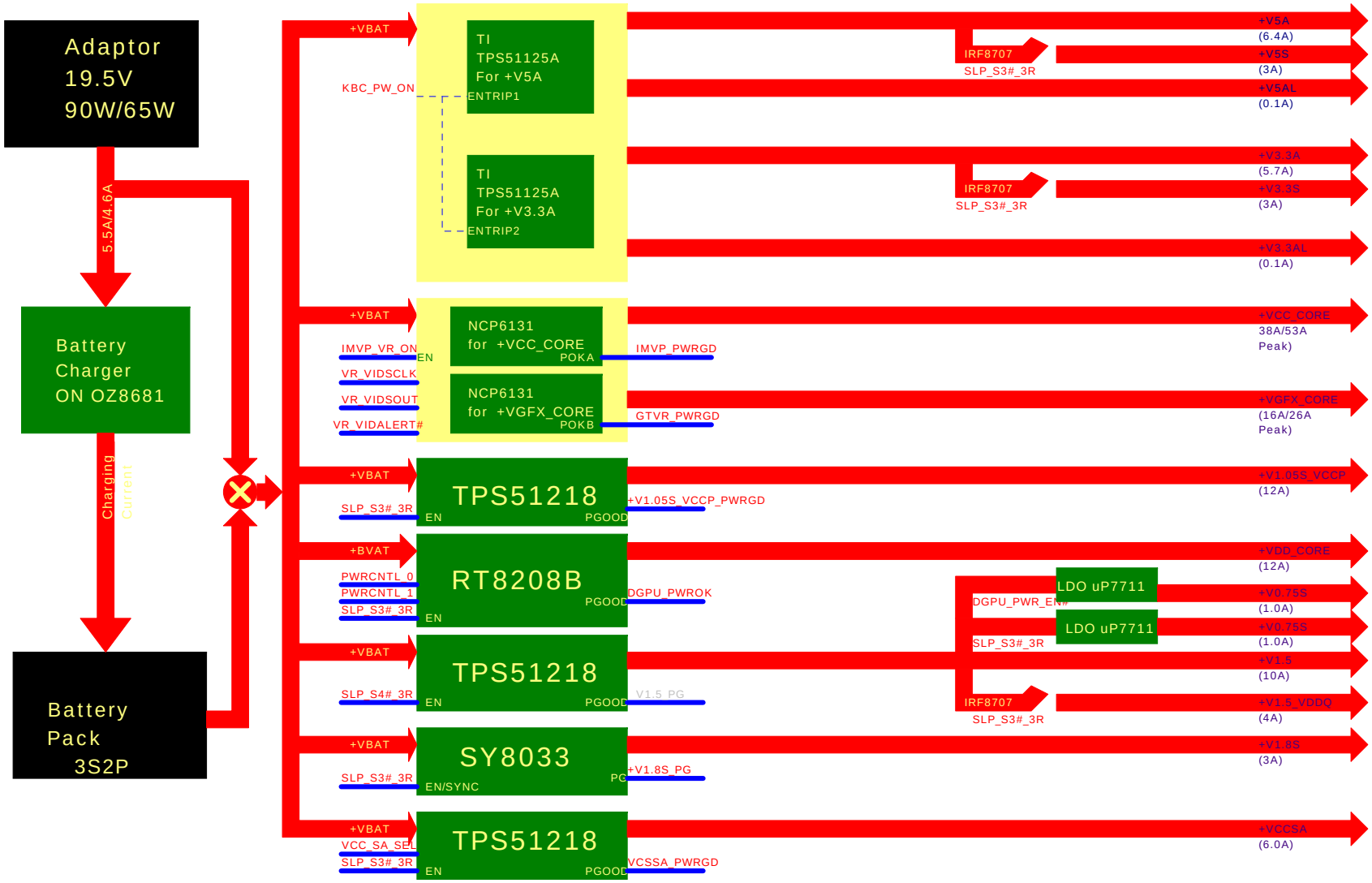
POWER MAP



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POWER MAP		
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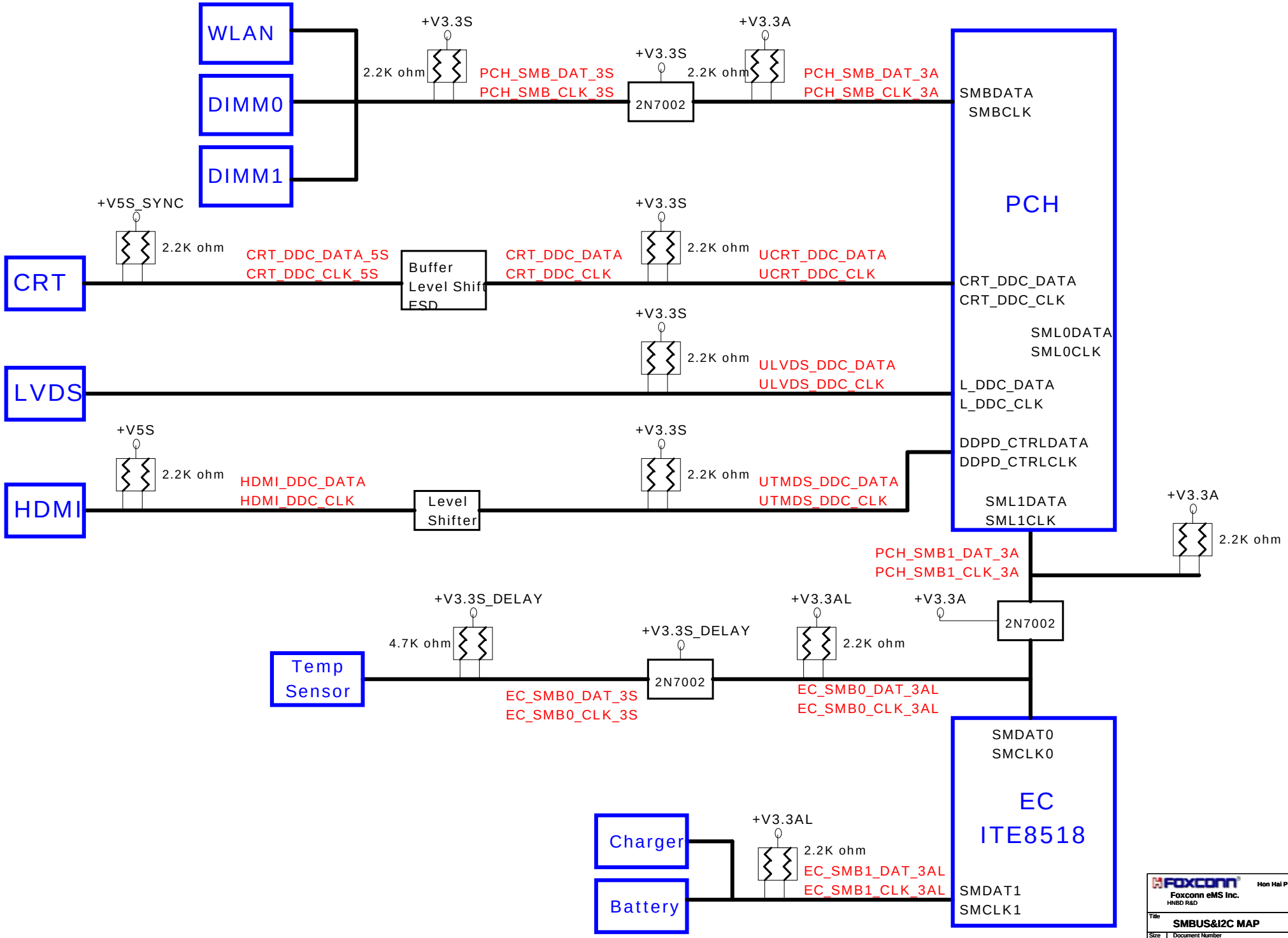
WLAN
DIMM0
DIMM1
+V3.3S
2.2K ohm
PCH_SMB_DAT_3S
PCH_SMB_CLK_3S
+V3.3S
2N7002
+V3.3A
2.2K ohm
PCH_SMB_DAT_3A
PCH_SMB_CLK_3A
SMBDATA
SMBCLK
PCH
+V5S_SYNC
2.2K ohm
CRT
CRT_DDC_DATA_5S
CRT_DDC_CLK_5S
Buffer
Level Shift
ESD
CRT_DDC_DATA
CRT_DDC_CLK
+V3.3S
2.2K ohm
UCRT_DDC_DATA
UCRT_DDC_CLK
CRT_DDC_DATA
CRT_DDC_CLK
SML0DATA
SML0CLK
LVDS
+V3.3S
2.2K ohm
ULVDS_DDC_DATA
ULVDS_DDC_CLK
L_DDC_DATA
L_DDC_CLK
+V5S
2.2K ohm
HDMI
HDMI_DDC_DATA
HDMI_DDC_CLK
Level
Shifter
+V3.3S
2.2K ohm
UTMDS_DDC_DATA
UTMDS_DDC_CLK
DDPD_CTRLDATA
DDPD_CTRLCLK
SML1DATA
SML1CLK
+V3.3A
2.2K ohm
PCH_SMB1_DAT_3A
PCH_SMB1_CLK_3A
+V3.3S_DELAY
4.7K ohm
Temp
Sensor
EC_SMB0_DAT_3S
EC_SMB0_CLK_3S
+V3.3S_DELAY
2N7002
+V3.3AL
2.2K ohm
EC_SMB0_DAT_3AL
EC_SMB0_CLK_3AL
+V3.3A
2N7002
SMDAT0
SMCLK0
EC
ITE8518
Charger
Battery
+V3.3AL
2.2K ohm
EC_SMB1_DAT_3AL
EC_SMB1_CLK_3AL
SMDAT1
SMCLK1
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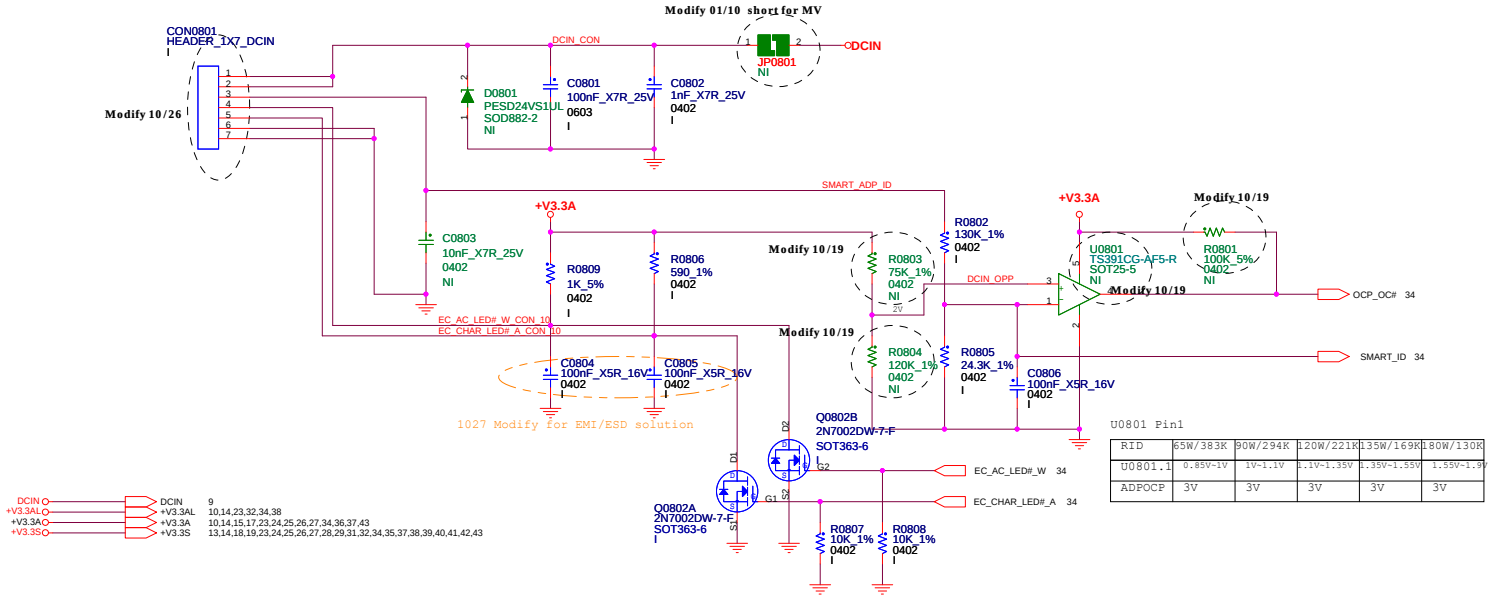
DC_JACK WIRE to BOARD CONNECTOR

2010.1203.0

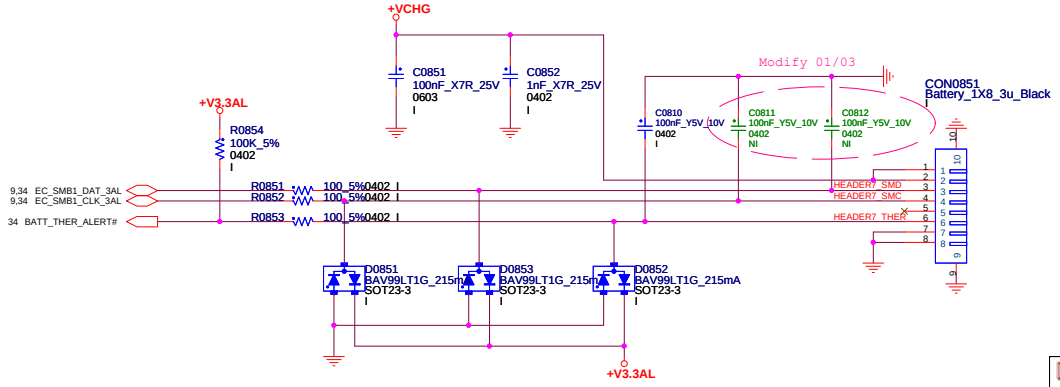


U0801 Pin1

RID	65W/383K	90W/294K	120W/221K	135W/169K	180W/130K
U0801.1	0.85V~1V	1V~1.1V	1.1V~1.35V	1.35V~1.55V	1.55V~1.9V
ADPOCP	3V	3V	3V	3V	3V

BATTERY CONNECTOR

2010.0914.0



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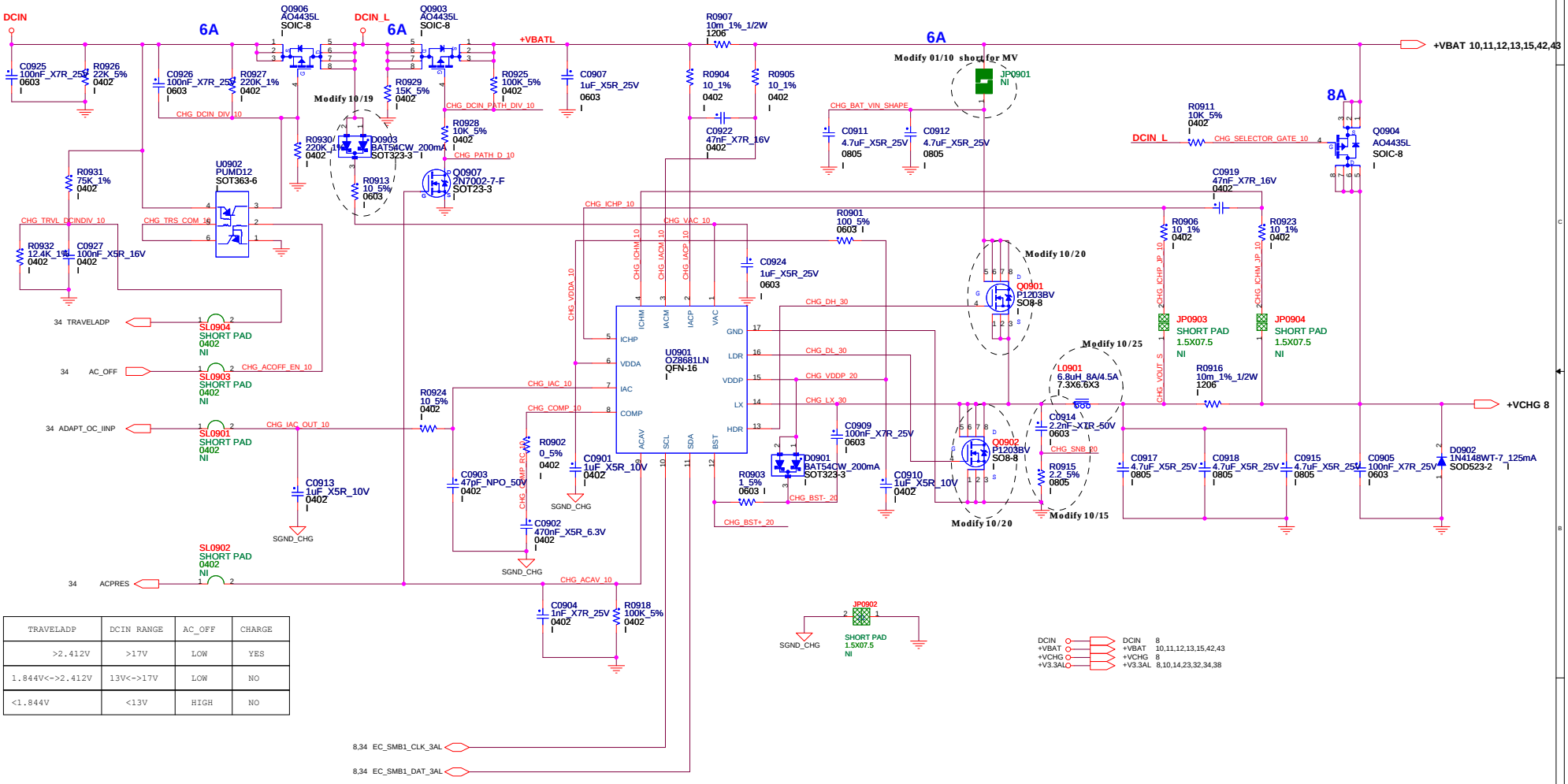
BATTERY CHARGER



TRAVELADP	DCIN RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

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+V5A / +V3.3A POWER SUPPLY

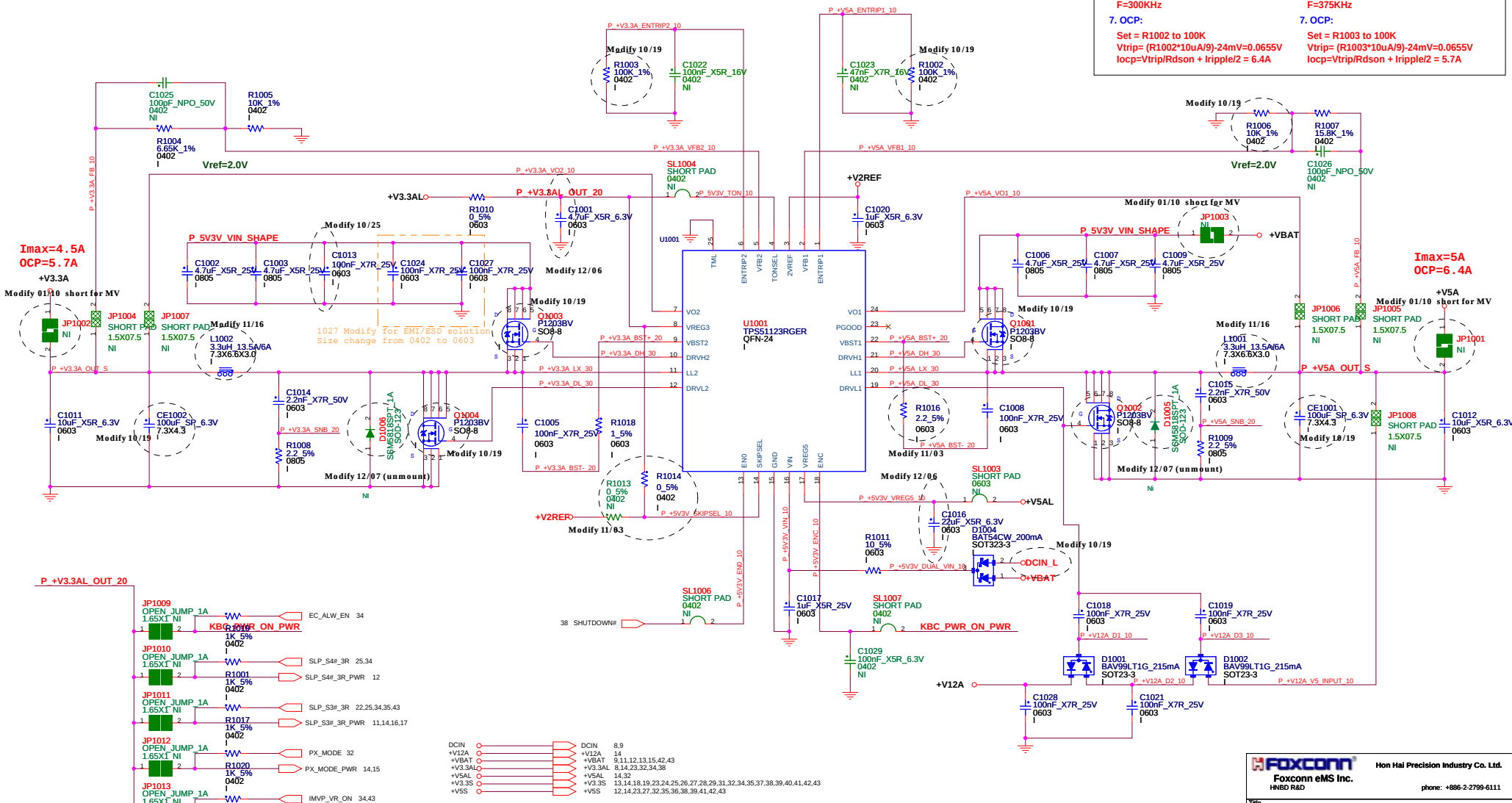
2010.1103.0

+V5A:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=3.7A
2. Ripple Current:
   Irip=3.72A
3. Ripple Voltage:
   ESR/1=15mohm
   Vrip=55.8mV
4. Inductor Spec:
   Isat=13.5A
   Idc=6A
   DCR=30mohm
5. MOSFET Spec:
   H-side MOSFET: IRF8707PBF
   Rds(ON)=17.5mohm (Vgs=4.5 V)
   I cont = 11A (T =25 ℃)
   I peak = 88A (Pause =10 us)
6. Frequency:
   F=300KHz
7. OCP:
   Set = R1002 to 100K
   Vtrip= (R1002*10uA/9)-24mV=0.0655V
   Iocp=Vtrip/Rdson + Iripple/2 = 6.4A

+V3.3A:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.2A
2. Ripple Current:
   Irip=2.21A
3. Ripple Voltage:
   ESR/1=15mohm
   Vrip=33.15mV
4. Inductor Spec:
   Isat=13.5A
   Idc=6A
   DCR=30mohm
5. MOSFET Spec:
   L-side MOSFET: IRF8707PBF
   Rds(ON)=17.5mohm (Vgs=4.5 V)
   I cont = 11A (T =25 ℃)
   I peak = 88A (Pause =10 us)
6. Frequency:
   F=375KHz
7. OCP:
   Set = R1003 to 100K
   Vtrip= (R1003*10uA/9)-24mV=0.0655V
   Iocp=Vtrip/Rdson + Iripple/2 = 5.7A



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Title	5V/3.3V
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+VTT POWER SUPPLY

2010.1103.0

+V1.05S_VCCP:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.24A

2. Ripple Current:

Irip=3.42A

3. Ripple Voltage:

ESR/1=9mohm
Vrip=30.78mV

4. Inductor Spec:

Isat=36A
Idc=18A
DCR=3.3mohm

5.MOSFET Spec:

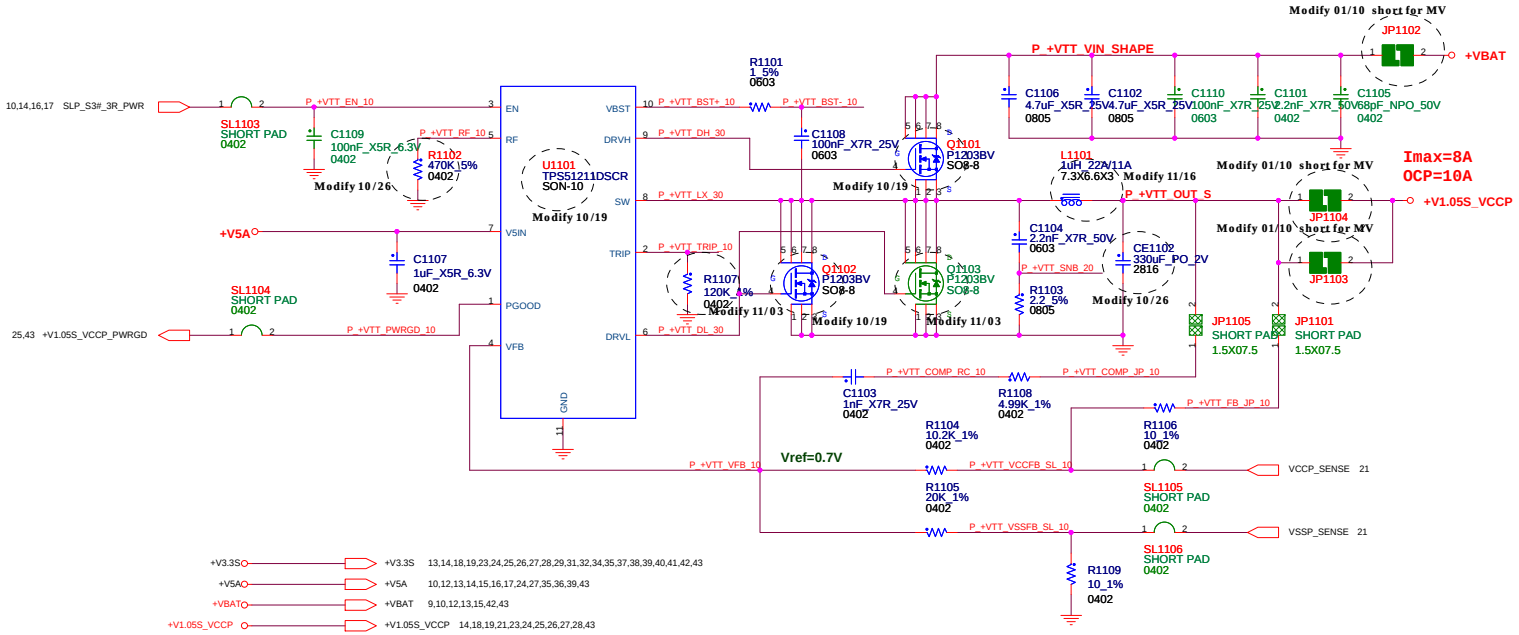
H-side MOSFET: IRF8707PBF		L-side MOSFET: IRF8707PBF	
Rds(ON)=17.5mohm	(Vgs=4.5 V)	Rds(ON)=17.5mohm	(Vgs=4.5 V)
I cont = 11A	(T =25 ℃)	I cont = 11A	(T =25 ℃)
I peak = 88A	(Pause =10 us)	I peak = 88A	(Pause =10 us)

6. Frequency:

F=290KHz (R1102=0ohm)

7. OCP:

Set = R1107 to 120K
Vtrip= R1107*10uA=1.2V
Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A



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Title: +VTT			
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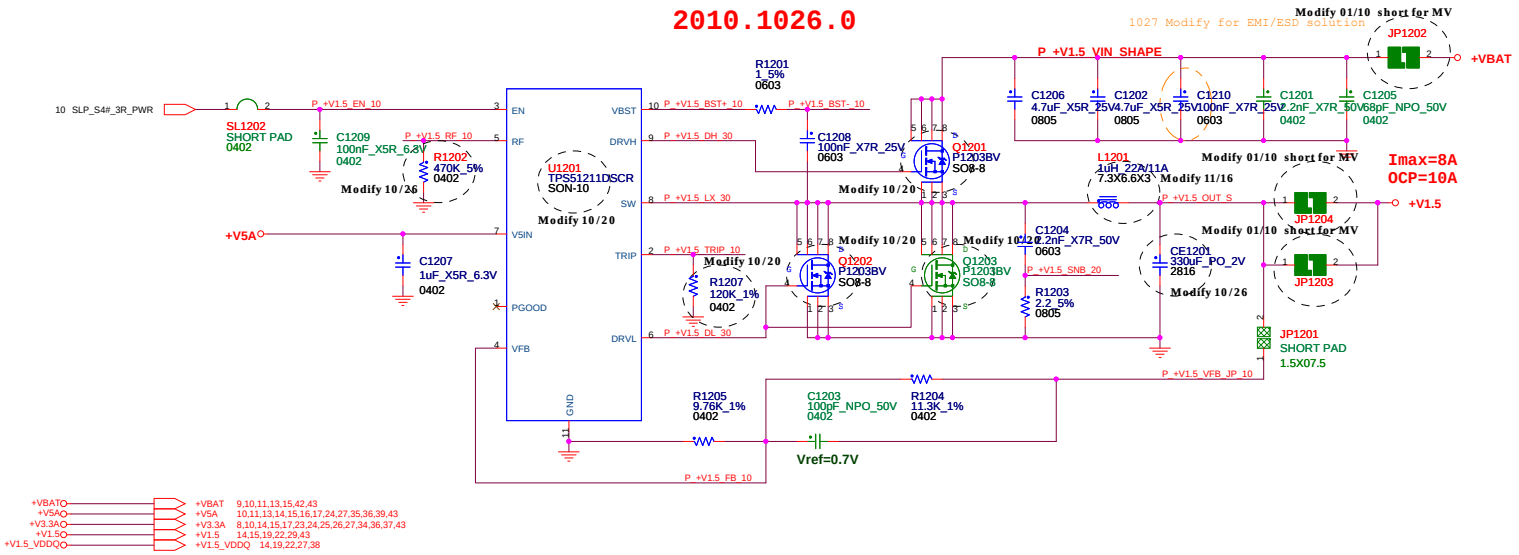
+V1.5 POWER SUPPLY

2010.1026.0



+V1.5:

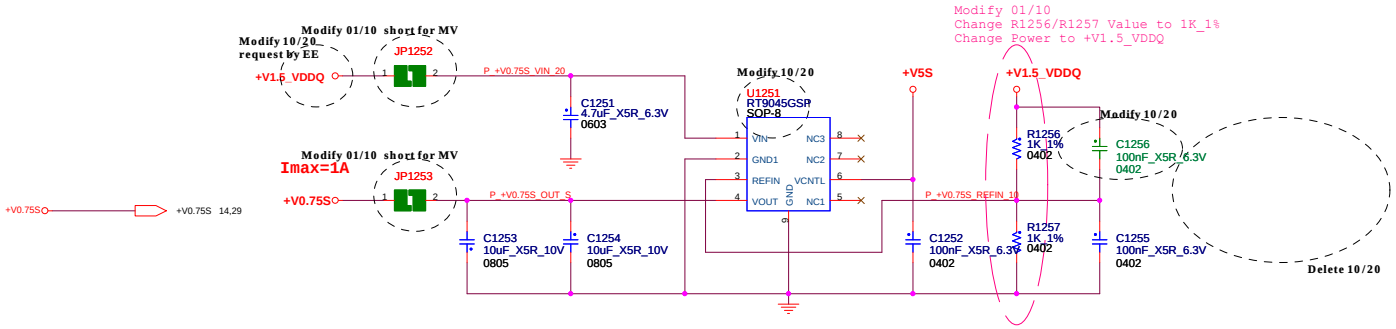
1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.78A
2. Ripple Current:
   Irip=3.34A
3. Ripple Voltage:
   ESR/1=9mohm
   Vrip=30.6mV
4. Inductor Spec:
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. MOSFET Spec:

H-side MOSFET: IRF8707PBF		L-side MOSFET: IRF8707PBF	
Rds(ON)=17.5mohm	(Vgs=4.5 V)	Rds(ON)=17.5mohm	(Vgs=4.5 V)
I cont = 11A	(T =25 ℃)	I cont = 11A	(T =25 ℃)
I peak = 88A	(Pause =10 us)	I peak = 88A	(Pause =10 us)

6. Frequency:
   F=290KHz (R0902=0ohm)
7. OCP:
   Set = R1207 to 120K
   Vtrip= R1207*10uA=1.2V
   Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A

+V0.75S POWER SUPPLY

2010.1026.0



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Title: 1.5VDDR3/0.75V			
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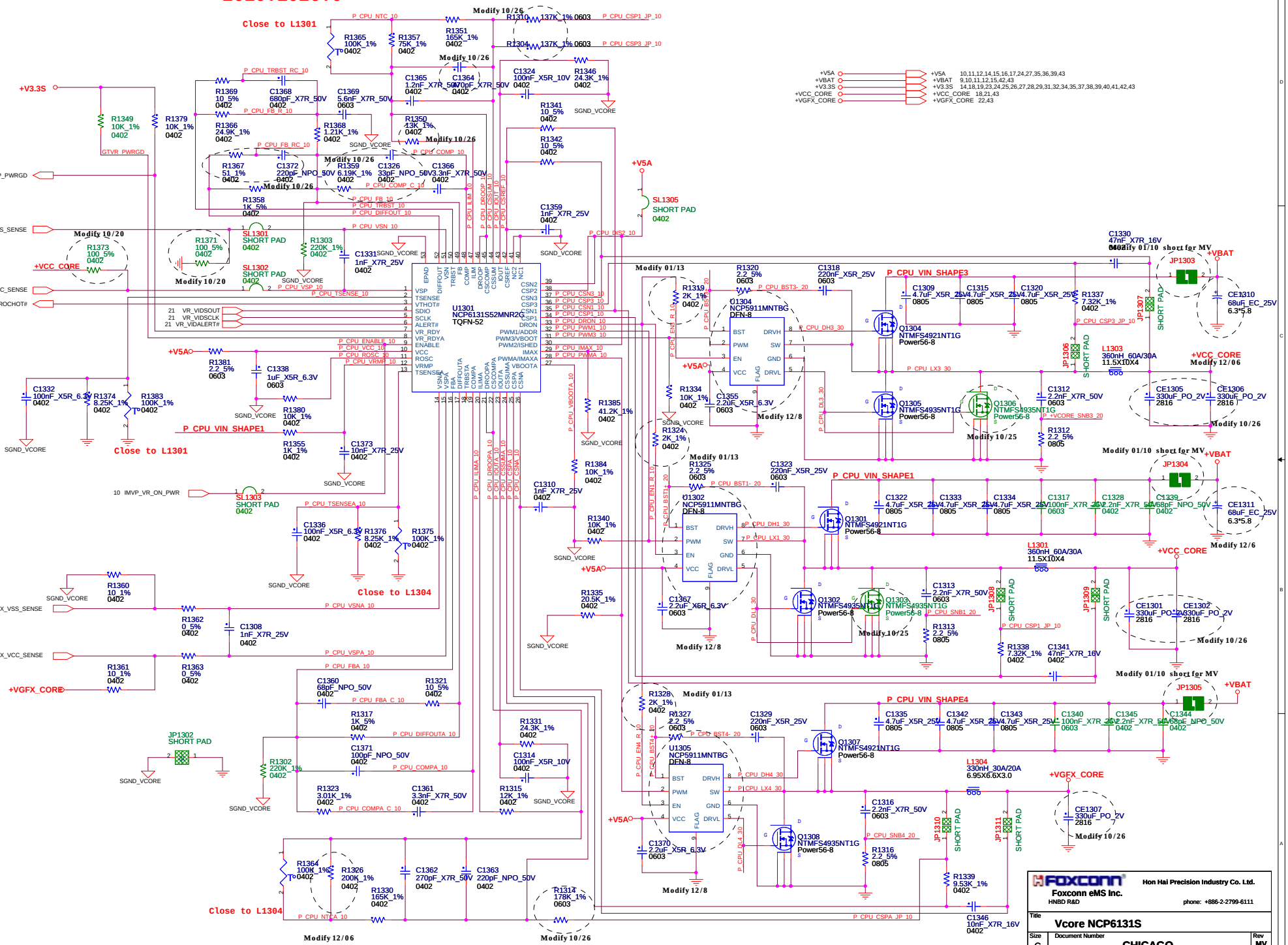
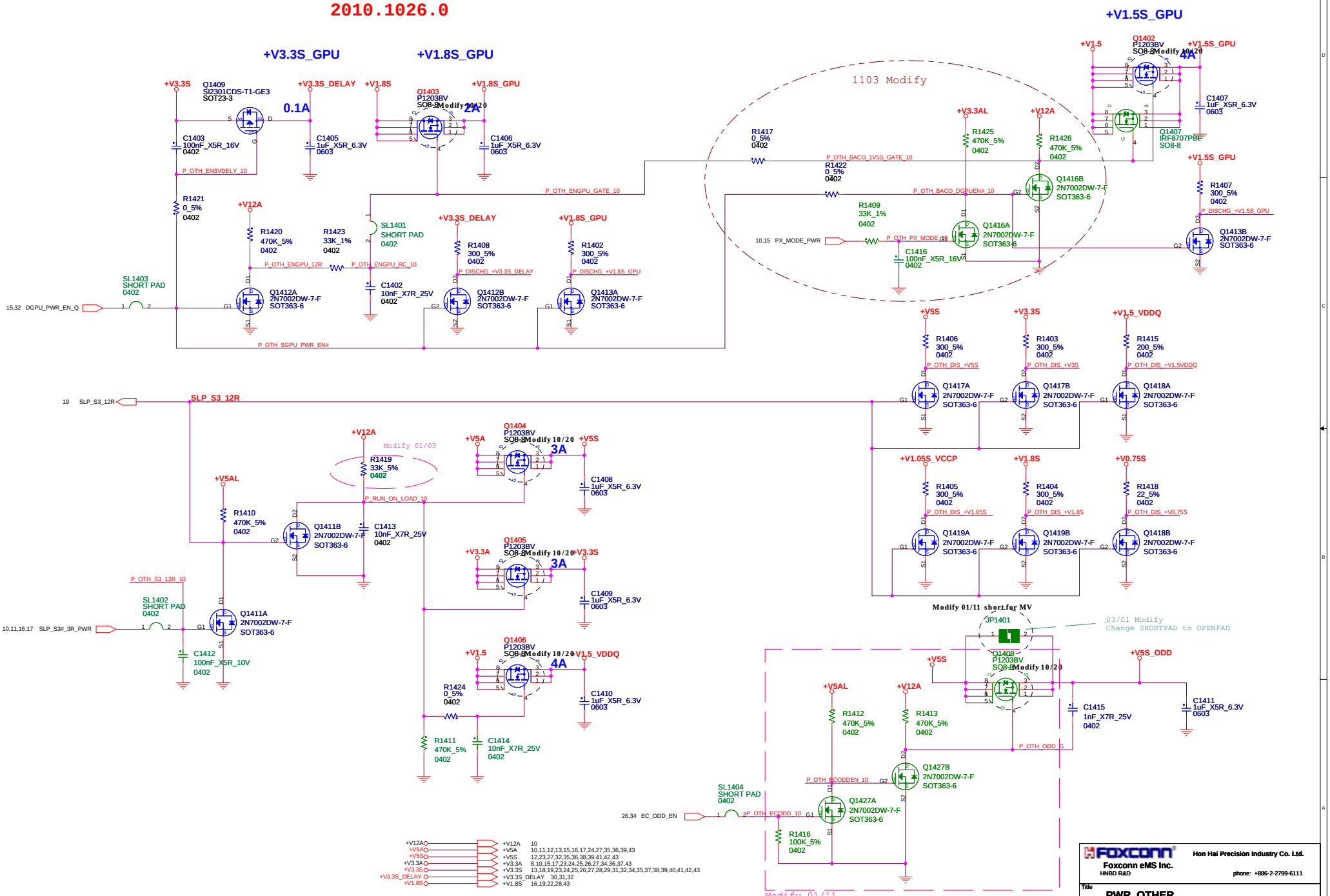
2010.1026.0

IMVP7 CPU VCORE POWER SUPPLY



OTHER POWER / DISCHARGE CIRCUITS

2010.1026.0



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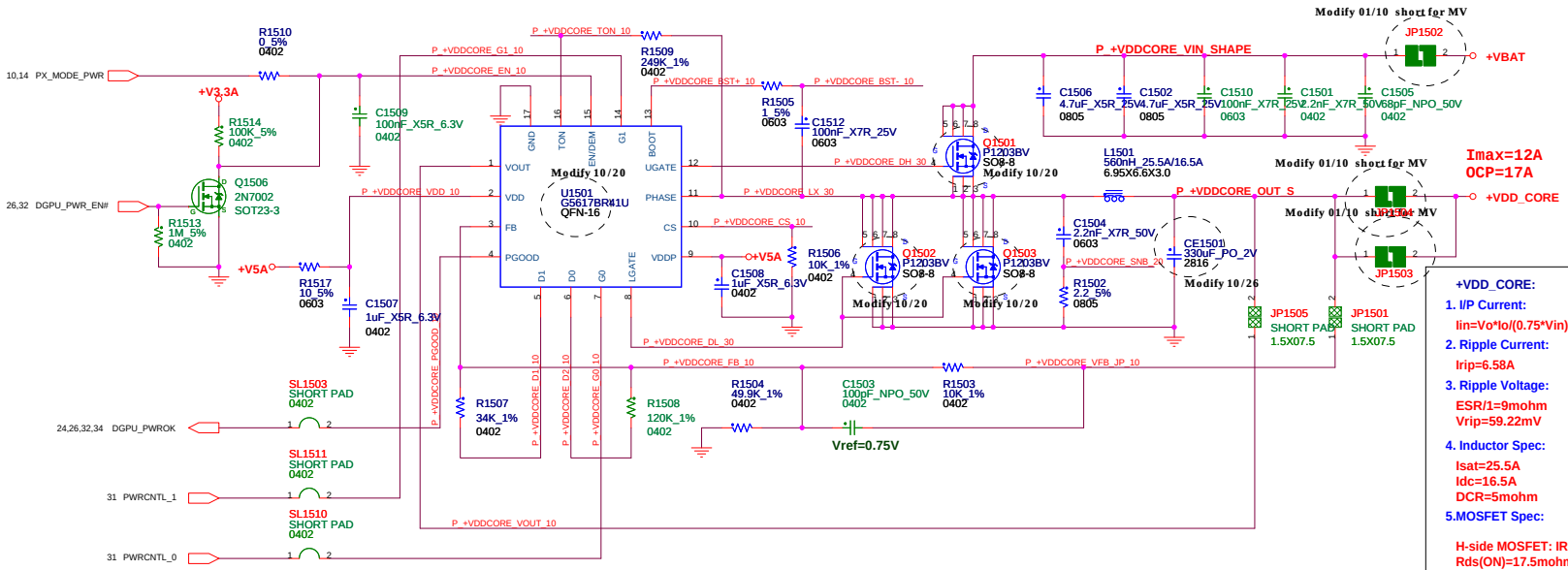
+VDD_CORE POWER SUPPLY

2010.1026.0



PWRCNTL_1	PWRCNTL_0	VDD_CORE
0	---	1.121V
---	---	---
1	---	0.9V
---	---	---

+VDD_CORE:

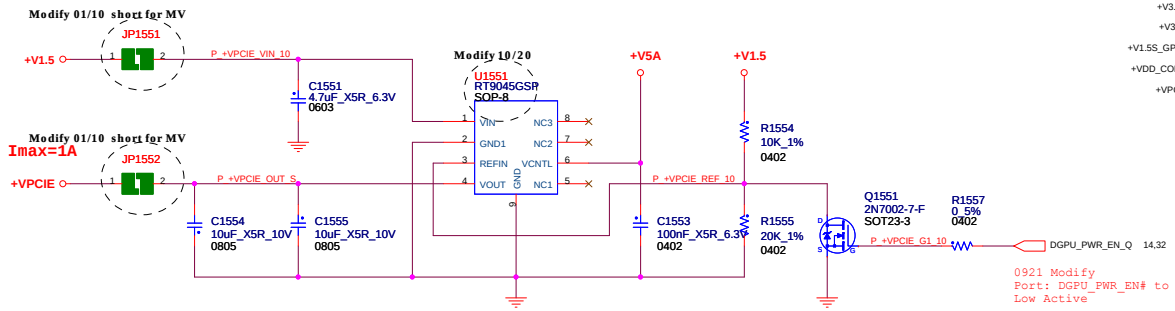
1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.48A
2. Ripple Current:
   Irip=6.58A
3. Ripple Voltage:
   ESR/1=9mohm
   Vrip=59.22mV
4. Inductor Spec:
   Isat=25.5A
   Idc=16.5A
   DCR=5mohm
5. MOSFET Spec:

H-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)

L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)

6. Frequency:
   TON=9.6P*R1509*(VOUT+0.1) / (VIN-0.3)+50ns=206ns
   F=VOUT/(VIN*TON)=286KHz
7. OCP:
   Set = R1506 to 10K
   Vtrip= R1206*10uA=0.1V
   Iocp=(Vtrip/Rdson) + Iripple/2 = 17A

2010.1020.0 +VPCIE POWER SUPPLY



+VBAT	+VBAT	9,10,11,12,13,42,43
+V5A	+V5A	10,11,12,13,14,16,17,24,27,35,36,39,43
+V3.3A	+V3.3A	8,10,14,17,23,24,25,26,27,34,36,37,43
+V3.3S	+V3.3S	13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.5S_GPU	+V1.5S_GPU	14,30,32,33,43
+VDD_CORE	+VDD_CORE	32,43
+VPCIE	+VPCIE	30,31,32,43

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+V1.8S POWER SUPPLY

2010.1025.0

+V1.8S:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.44A

2. Ripple Current:

Irip=0.53A

3. Ripple Voltage:

ESR/3=3.3mohm
Vrip=1.75mV

4. Inductor Spec:

Isat=14A
Idc=8A
DCR=20mohm

5.MOSFET Spec:

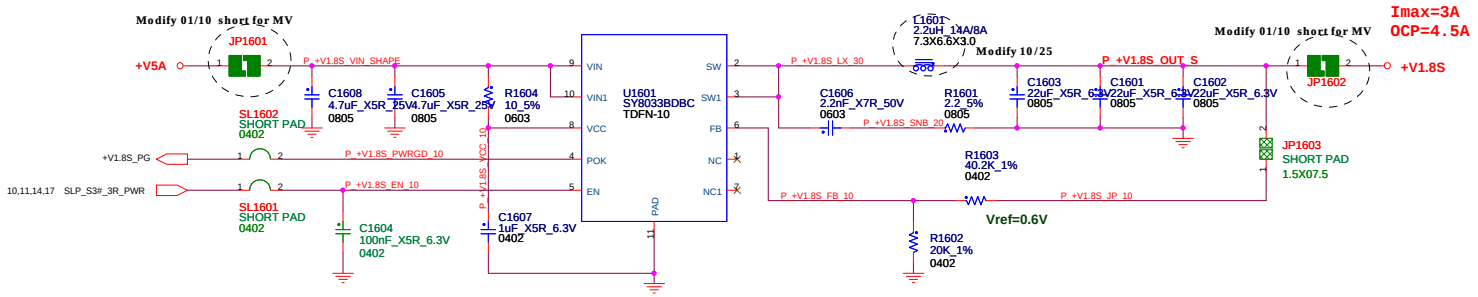
H-side P-MOSFET:	L-side N-MOSFET:
Rds(ON)=110mohm (Vgs=4.5 V)	Rds(ON)=75mohm (Vgs=4.5 V)

6. Frequency:

F=1MHz (min=800KHz, max=1.2MHz)

7. OCP:

Iocp=4A(min)/4.5A(typ)/5A(max)



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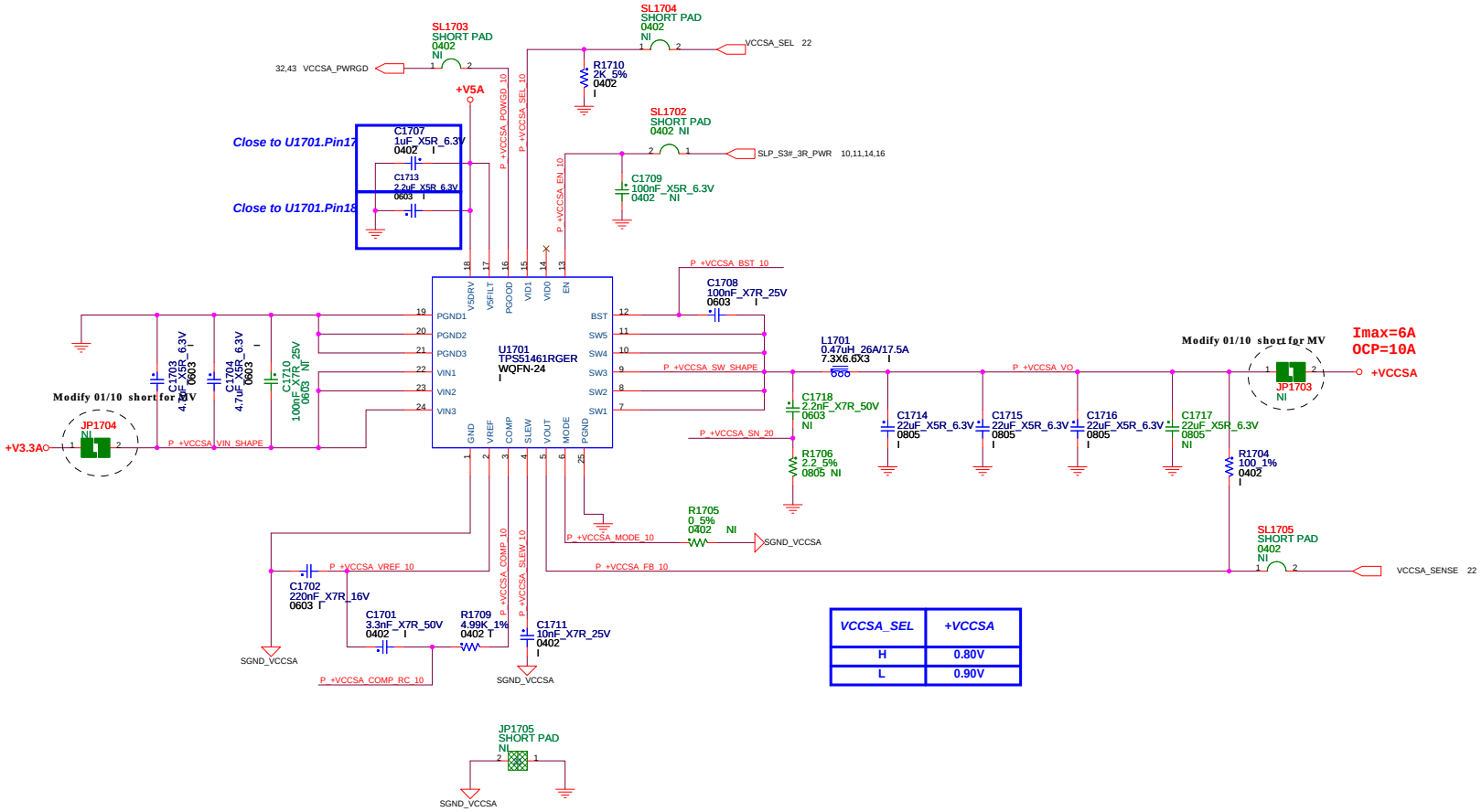
+VCCSA POWER SUPPLY

2010.1026.0

+VCCSA:
1. I/P Current:
Iin=Vo*Io/(0.75*Vin)=2.18A
2. Ripple Current:
Irip=1.39A
3. Ripple Voltage:
ESR/4=1mohm
Vrip=1.39mV
4. Inductor Spec:
Isat=26A
Idc=17.5A
DCR=4.2mohm
5.MOSFET Spec:

6. Frequency:
F=1MHz (R1705=Open)
7. OCP:
Min : 6A / Typ : 7.5A



VCCSA_SEL	+VCCSA
H	0.80V
L	0.90V

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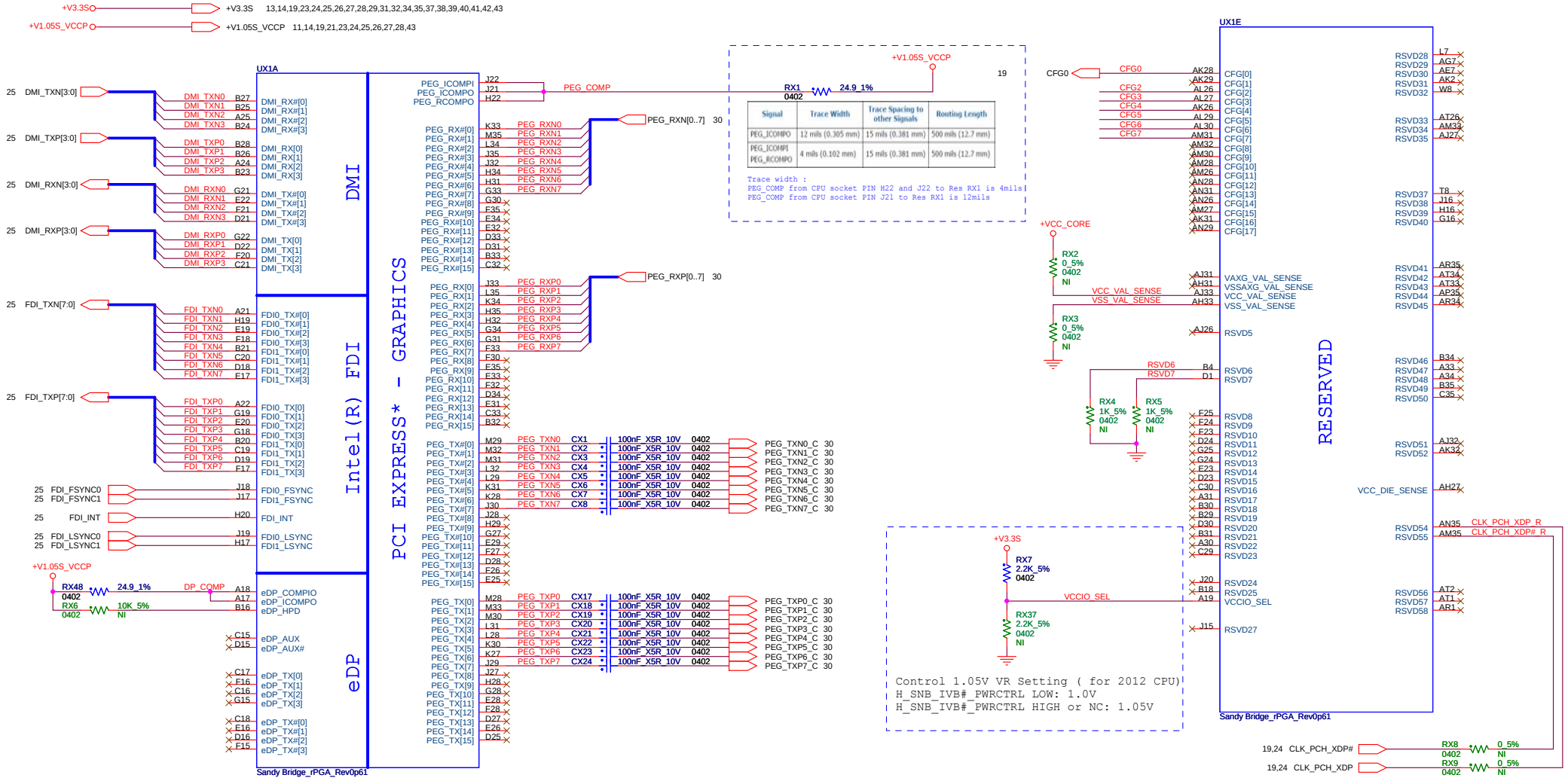

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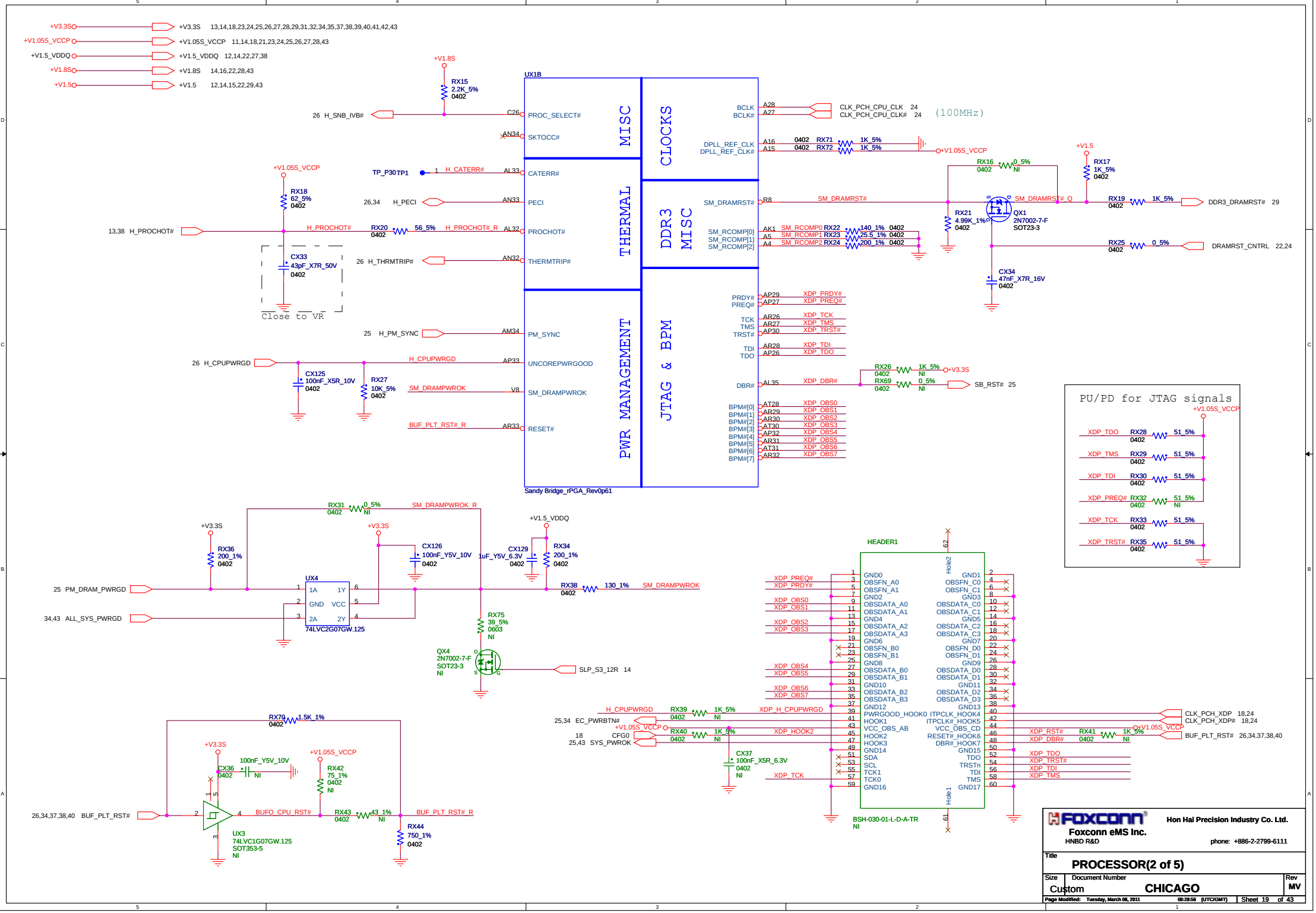
+V3.3S 13,14,18,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP +V1.05S_VCCP 11,14,18,21,23,24,25,26,27,28,43
+V1.5_VDDQ +V1.5_VDDQ 12,14,22,27,38
+V1.8S +V1.8S 14,16,22,28,43
+V1.5 +V1.5 12,14,15,22,29,43
UX1B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
PROC_SELECT#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_CLK
DPLL_REF_CLK#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
Sandy Bridge_rPGA_Rev0p61
CLK_PCH_CPU_CLK 24
CLK_PCH_CPU_CLK# 24
(100MHz)
26 H_SNB_IVB#
RX15 2.2K_5% 0402
TP_P30 TP1
H_CATERR#
26,34 H_PECI
13,38 H_PROCHOT#
H_PROCHOT#
RX20 0402 56_5% H_PROCHOT# R
CX33 43pF_X7R_50V 0402
Close to VR
26 H_THRMTRIP#
RX18 62_5% 0402
25 H_PM_SYNC
26 H_CPUPWRGD
H_CPUPWRGD
CX125 100nF_X5R_10V 0402
RX27 10K_5% 0402
SM_DRAMPWROK
BUF_PLT_RST# R
RX16 0402 0_5% NI
RX17 1K_5% 0402
SM_DRAMRST# Q
RX19 0402 1K_5%
DDR3_DRAMRST# 29
RX21 4.99K_1% 0402
QX1 2N7002-7-F SOT23-3
RX22 140_1% 0402
RX23 25.5_1% 0402
RX24 200_1% 0402
RX25 0402 0_5%
DRAMRST_CNTRL 22,24
CX34 47nF_X7R_16V 0402
XDP_PRDY#
XDP_PREQ#
XDP_TCK
XDP_TMS
XDP_TRST#
XDP_TDI
XDP_TDO
XDP_DBR#
RX26 0402 1K_5% NI
RX69 0402 0_5% NI
SB_RST# 25
XDP_OBS0
XDP_OBS1
XDP_OBS2
XDP_OBS3
XDP_OBS4
XDP_OBS5
XDP_OBS6
XDP_OBS7
PU/PD for JTAG signals
RX28 0402 51_5%
RX29 0402 51_5%
RX30 0402 51_5%
RX32 0402 51_5% NI
RX33 0402 51_5%
RX35 0402 51_5%
RX31 0402 0_5% NI
SM_DRAMPWROK_R
RX36 200_1% 0402
CX126 100nF_Y5V_10V 0402
1uF_Y5V_6.3V
CX129 0402
RX34 200_1% 0402
25 PM_DRAM_PWRGD
34,43 ALL_SYS_PWRGD
UX4
74LVC2G07GW.125
RX38 0402 130_1% SM_DRAMPWROK
RX75 39_5% 0603 NI
QX4 2N7002-7-F SOT23-3 NI
SLP_S3_12R 14
HEADER1
BSH-030-01-L-D-A-TR NI
H_CPUPWRGD
RX39 0402 1K_5% NI
XDP_H_CPUPWRGD
25,34 EC_PWRBTN#
RX40 0402 1K_5% NI
XDP_HOOK2
18 CFG0
25,43 SYS_PWROK
CX37 100nF_X5R_6.3V 0402 NI
CLK_PCH_XDP 18,24
CLK_PCH_XDP# 18,24
RX41 0402 1K_5% NI
BUF_PLT_RST# 26,34,37,38,40
XDP_DBR#
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
RX70 0402 1.5K_1%
CX36 0402 100nF_Y5V_10V NI
RX42 75_1% 0402 NI
26,34,37,38,40 BUF_PLT_RST#
BUFO_CPU_RST#
RX43 0402 43_1% NI
BUF_PLT_RST# R
RX44 750_1% 0402
UX3 74LVC1G07GW.125 SOT353-5 NI
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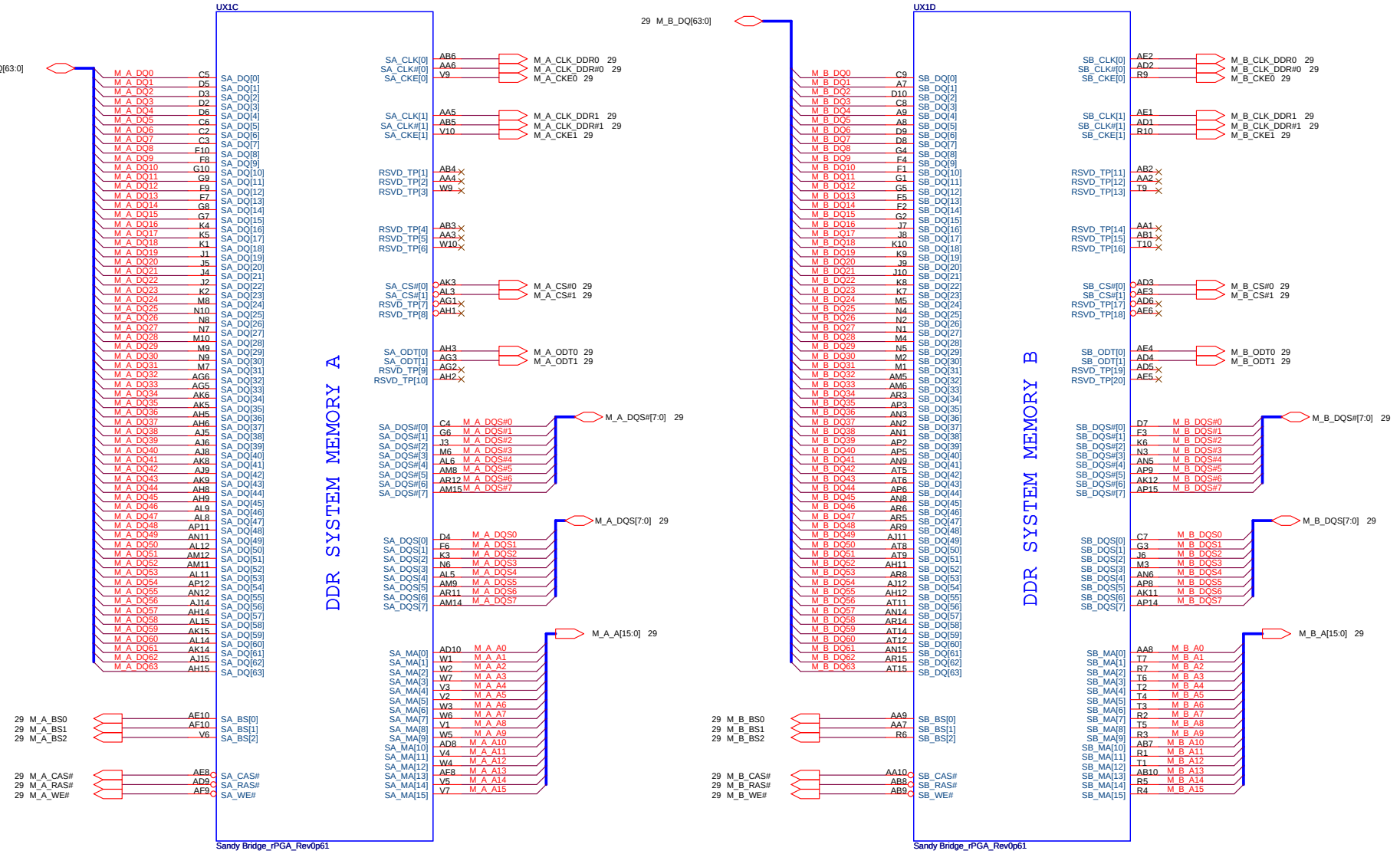

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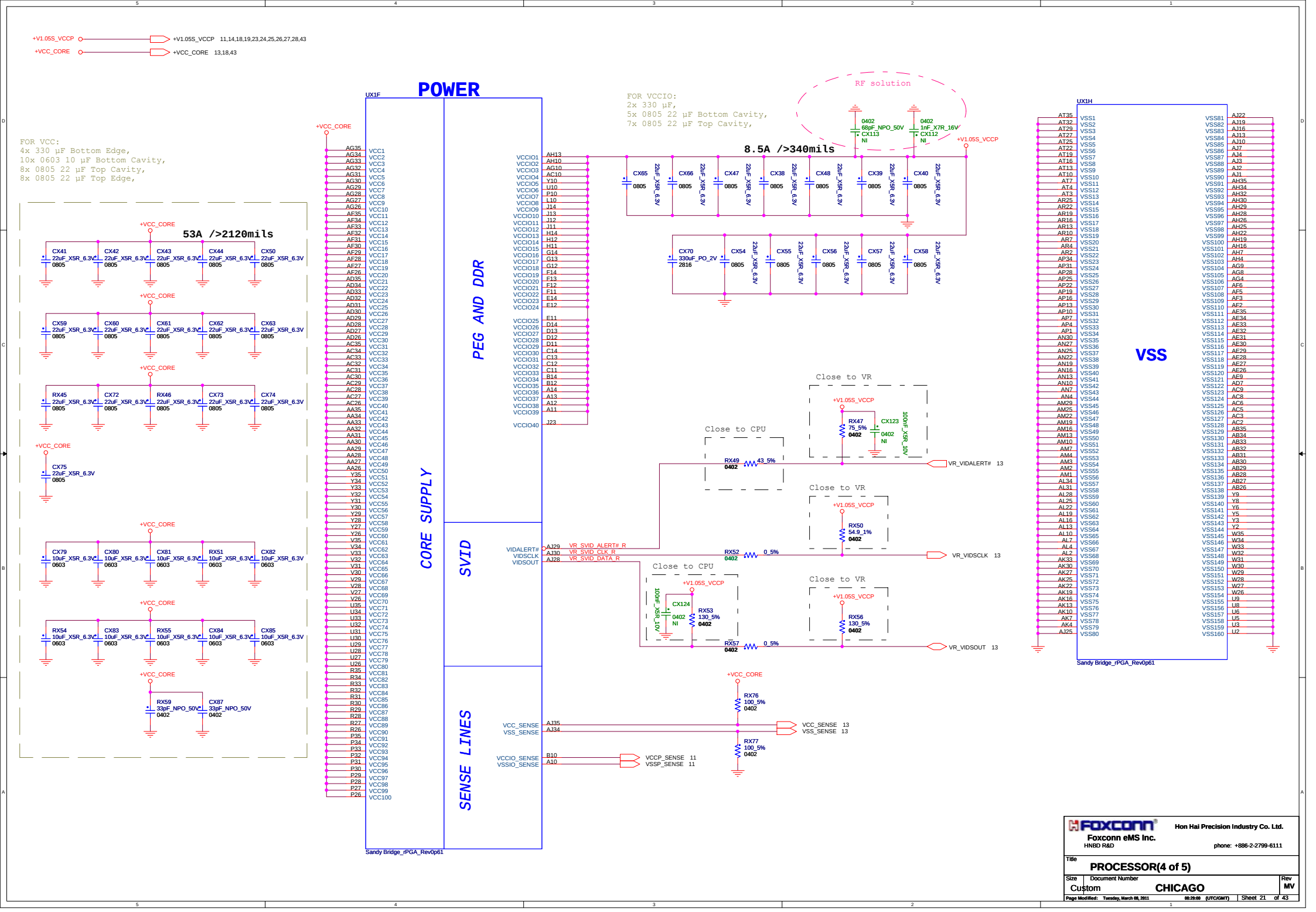
POWER
UX1F
PEG AND DDR
CORE SUPPLY
SVID
SENSE LINES
Sandy Bridge_rPGA_Rev0p61
FOR VCC:
4x 330 µF Bottom Edge,
10x 0603 10 µF Bottom Cavity,
8x 0805 22 µF Top Cavity,
8x 0805 22 µF Top Edge,
53A />2120mils
FOR VCCIO:
2x 330 µF,
5x 0805 22 µF Bottom Cavity,
7x 0805 22 µF Top Cavity,
RF solution
8.5A />340mils
Close to VR
Close to CPU
VR_VIDALERT# 13
VR_VIDSCLK 13
VR_VIDSOUT 13
VCC_SENSE 13
VSS_SENSE 13
VCCP_SENSE 11
VSSP_SENSE 11
UX1H
VSS
Sandy Bridge_rPGA_Rev0p61
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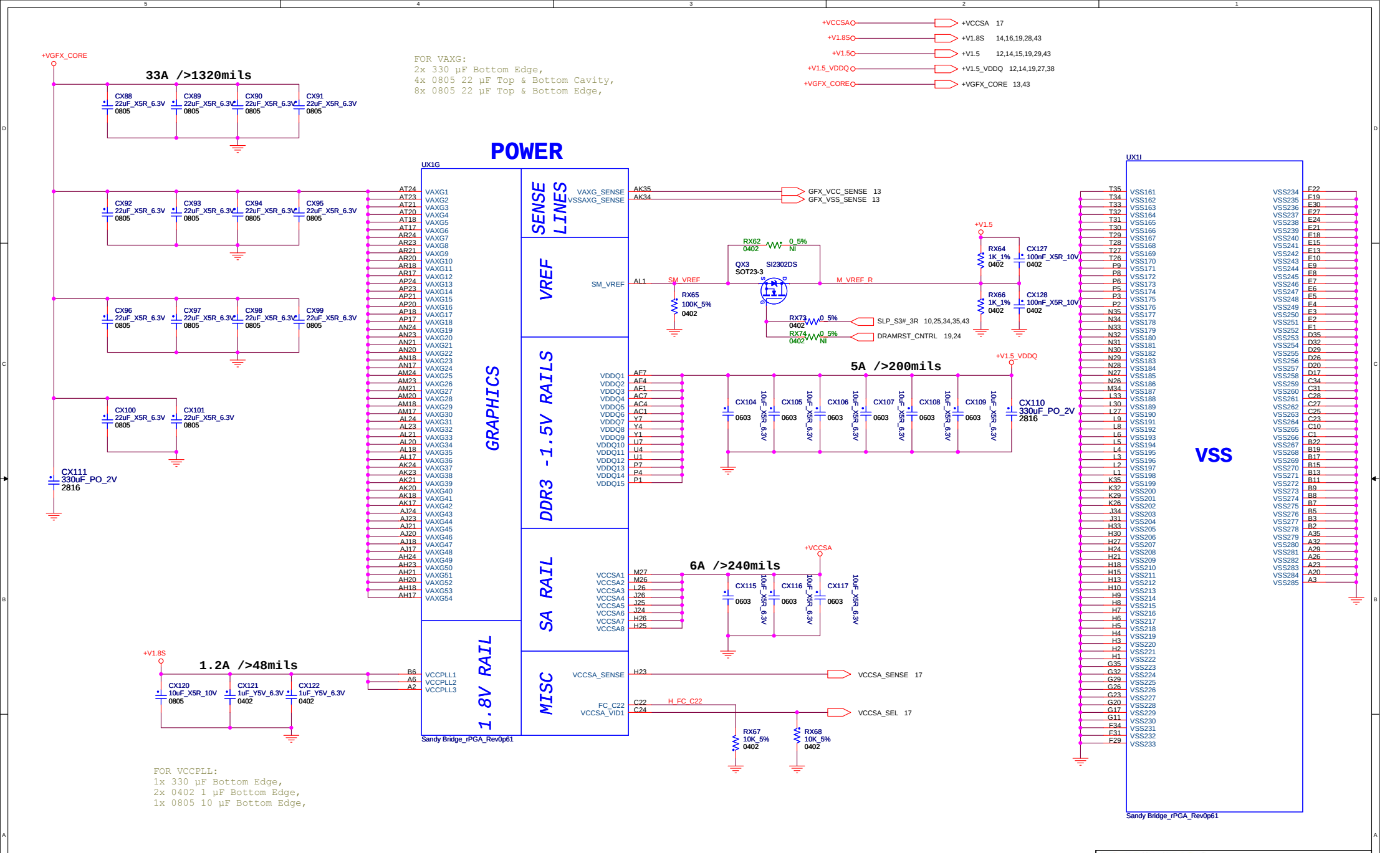

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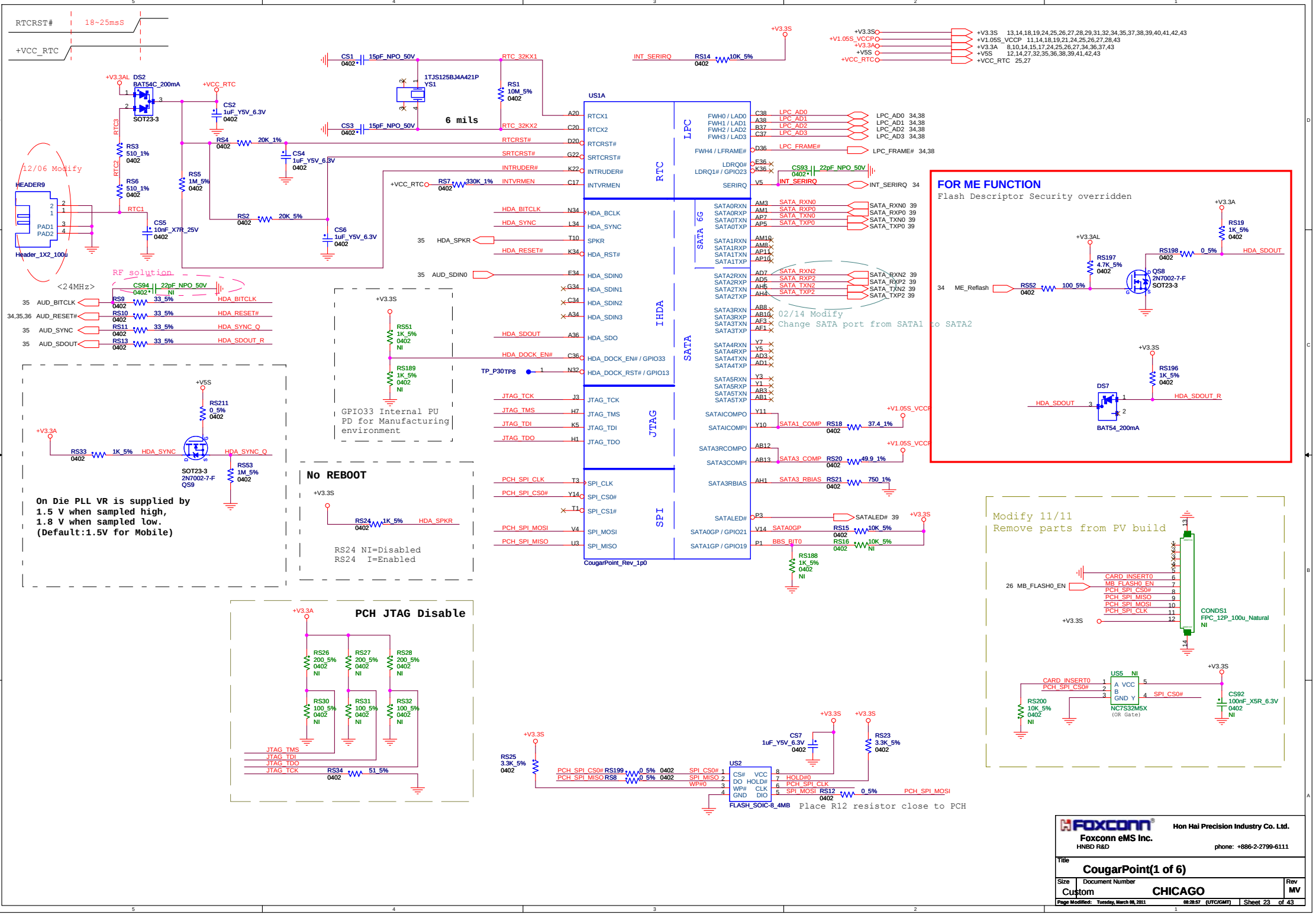
RTCRST#
18~25msS
+VCC_RTC
12/06 Modify
HEADER9
Header_1X2_100u
RF solution
<24MHz>
CS94 22pF_NPO_50V
RS9 33_5%
RS10 33_5%
RS11 33_5%
RS13 33_5%
35 AUD_BITCLK
34,35,36 AUD_RESET#
35 AUD_SYNC
35 AUD_SDOUT
HDA_BITCLK
HDA_RESET#
HDA_SYNC_Q
HDA_SDOUT_R
On Die PLL VR is supplied by
1.5 V when sampled high,
1.8 V when sampled low.
(Default:1.5V for Mobile)
RS211 0_5%
RS33 1K_5%
RS53 1M_5%
SOT23-3
2N7002-7-F
QS9
GPIO33 Internal PU
PD for Manufacturing
environment
RS51 1K_5%
RS189 1K_5%
No REBOOT
RS24 1K_5%
HDA_SPKR
RS24 NI=Disabled
RS24 I=Enabled
PCH JTAG Disable
RS26 200_5%
RS27 200_5%
RS28 200_5%
RS30 100_5%
RS31 100_5%
RS32 100_5%
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TCK
RS34 51_5%
US1A
RTC
LPC
IHDA
SATA
JTAG
SPI
CougarPoint_Rev_1p0
6 mils
1TJS125BJ4A421P
YS1
RS1 10M_5%
RS14 10K_5%
INT_SERIRQ
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
CS93 22pF_NPO_50V
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN2
SATA_RXP2
SATA_TXN2
SATA_TXP2
02/14 Modify
Change SATA port from SATA1 to SATA2
SATA1_COMP RS18 37.4_1%
SATA3_COMP RS20 49.9_1%
SATA3_RBIAS RS21 750_1%
SATA0GP RS15 10K_5%
BBS_BIT0 RS16 10K_5%
RS188 1K_5%
SATALED#
FOR ME FUNCTION
Flash Descriptor Security overridden
RS19 1K_5%
RS197 4.7K_5%
RS198 0_5%
RS52 100_5%
34 ME_Reflash
QS8
2N7002-7-F
SOT23-3
RS196 1K_5%
DS7
BAT54_200mA
Modify 11/11
Remove parts from PV build
26 MB_FLASH0_EN
CARD_INSERT0
MB_FLASH0_EN
PCH_SPI_CS0#
PCH_SPI_MISO
PCH_SPI_MOSI
PCH_SPI_CLK
CONDS1
FPC_12P_100u_Natural
NI
US5 NI
NC7S32M5X
(OR Gate)
RS200 10K_5%
CS92 100nF_X5R_6.3V
RS25 3.3K_5%
PCH_SPI_CS0# RS199 0_5%
PCH_SPI_MISO RS8 0_5%
SPI_CS0#
SPI_MISO
WP#0
US2
FLASH_SOIC-8_4MB
CS7 1uF_Y5V_6.3V
RS23 3.3K_5%
HOLD#0
PCH_SPI_CLK
SPI_MOSI RS12 0_5%
PCH_SPI_MOSI
Place R12 resistor close to PCH
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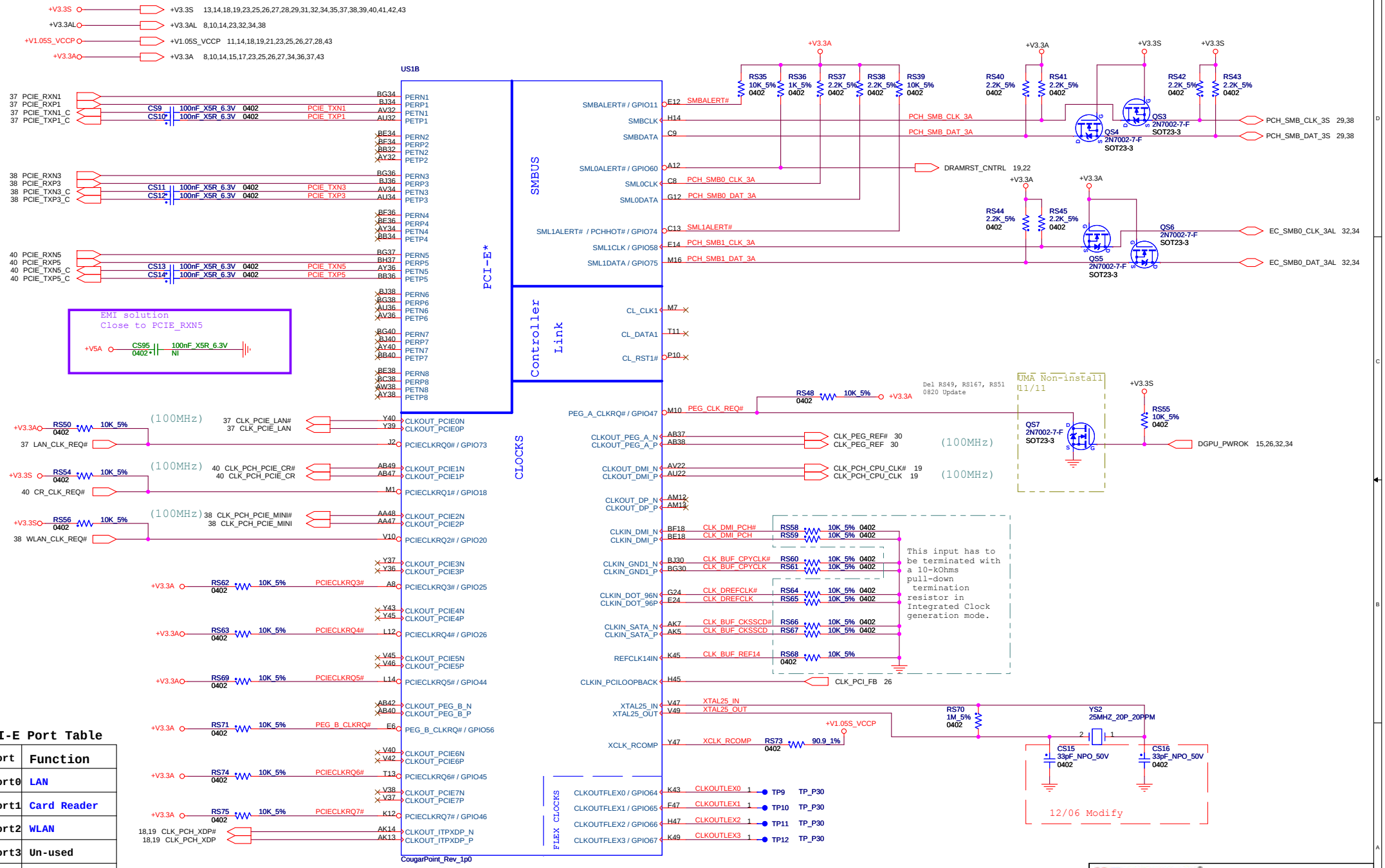

PCI-E Port Table

Port	Function
Port0	LAN
Port1	Card Reader
Port2	WLAN
Port3	Un-used
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used

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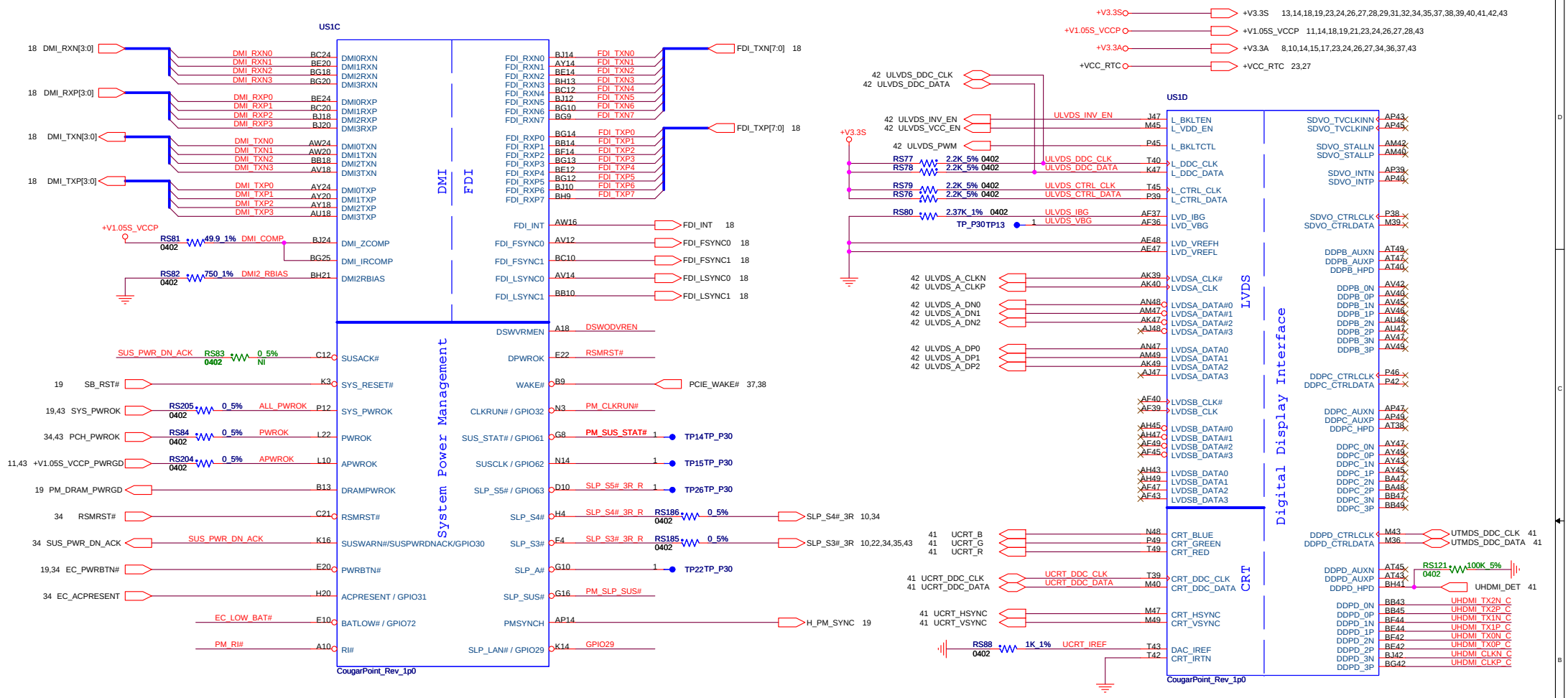
US1C
DMI
FDI
System Power Management
CougarPoint_Rev_1p0
US1D
LVDS
Digital Display Interface
CRT
CougarPoint_Rev_1p0
+V3.3S 13,14,18,19,23,24,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP 11,14,18,19,21,23,24,26,27,28,43
+V3.3A 8,10,14,15,17,23,24,26,27,34,36,37,43
+VCC_RTC 23,27
18 DMI_RXN[3:0]
18 DMI_RXP[3:0]
18 DMI_TXN[3:0]
18 DMI_TXP[3:0]
FDI_TXN[7:0] 18
FDI_TXP[7:0] 18
FDI_INT 18
FDI_FSYNC0 18
FDI_FSYNC1 18
FDI_LSYNC0 18
FDI_LSYNC1 18
PCIE_WAKE# 37,38
SLP_S4#_3R 10,34
SLP_S3#_3R 10,22,34,35,43
H_PM_SYNC 19
UTMDS_DDC_CLK 41
UTMDS_DDC_DATA 41
UHDMI_DET 41
UHDMI_CLKP 41
UHDMI_CLKN 41
UHDMI_TX2P 41
UHDMI_TX2N 41
UHDMI_TX1P 41
UHDMI_TX1N 41
UHDMI_TX0P 41
UHDMI_TX0N 41
+V3.3A
+V3.3S
+V1.05S_VCCP
+VCC_RTC
DSWODVREN
RS97 0402 330K_1% +VCC_RTC
RS103 0402 330K_1% NI
DSWODVREN - on Die DSW VR Enable
RS97 RS103
I NI Enabled
NI I Disabled
12/06 Modify
Modify CS30/CS53/CS101 to non-stuff on 01/11
Place resistor close to PCH
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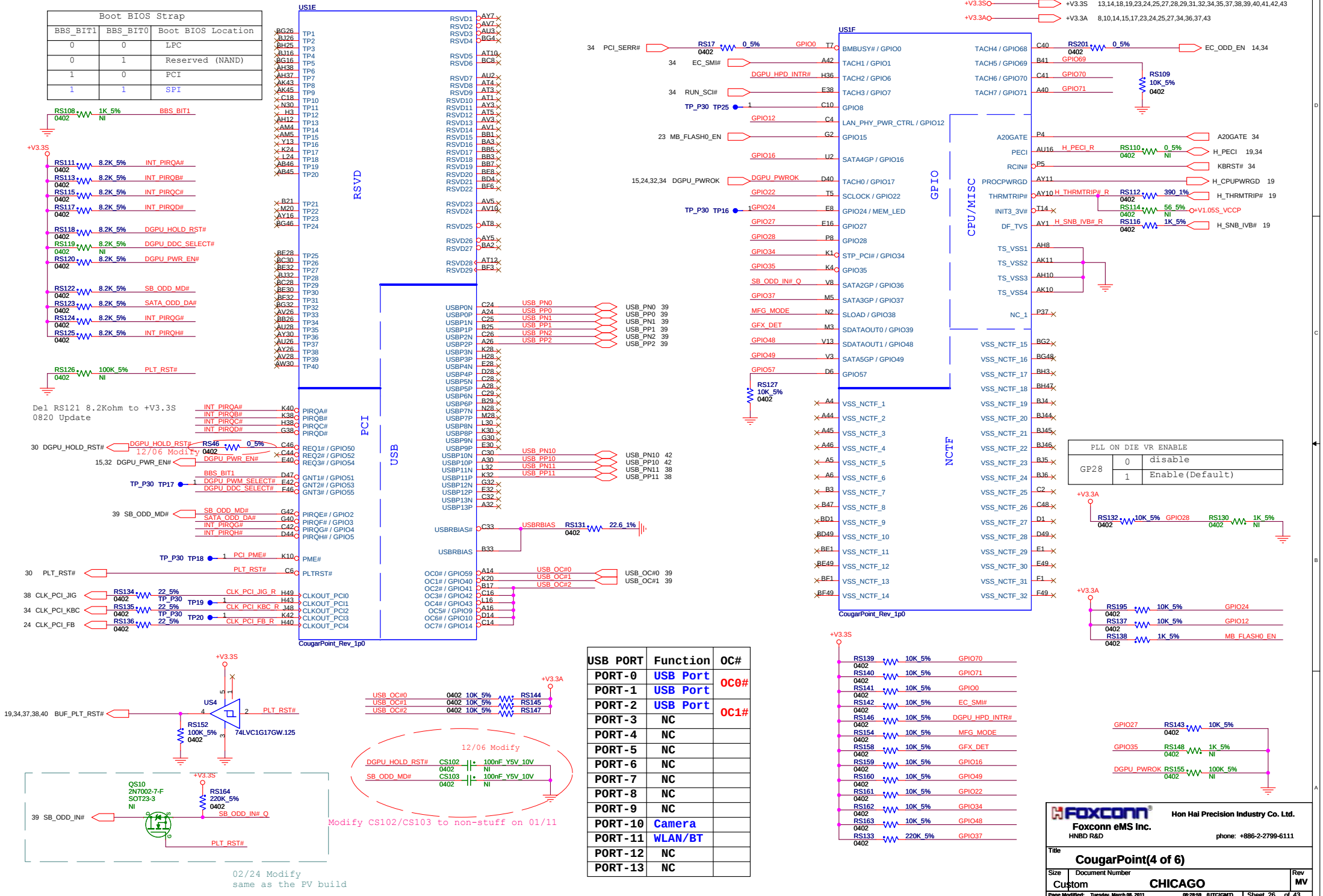
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



USB PORT	Function	OC#
PORT-0	USB Port	OC0#
PORT-1	USB Port	
PORT-2	USB Port	OC1#
PORT-3	NC	
PORT-4	NC	
PORT-5	NC	
PORT-6	NC	
PORT-7	NC	
PORT-8	NC	
PORT-9	NC	
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12	NC	
PORT-13	NC	

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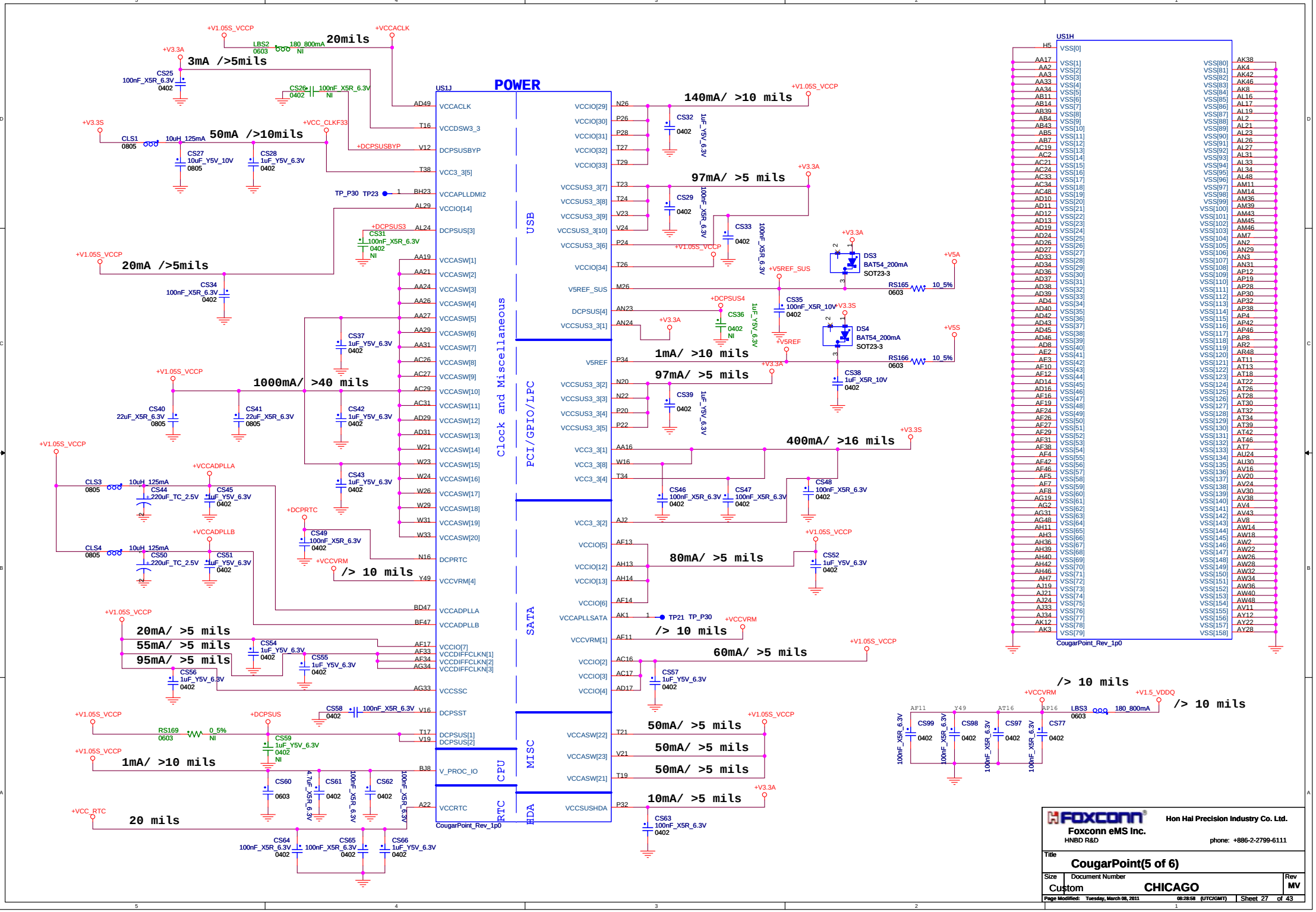
POWER
US1J
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
CougarPoint_Rev_1p0
US1H
CougarPoint_Rev_1p0
20mils
3mA />5mils
50mA />10mils
20mA />5mils
1000mA/ >40 mils
/> 10 mils
20mA/ >5 mils
55mA/ >5 mils
95mA/ >5 mils
1mA/ >10 mils
20 mils
140mA/ >10 mils
97mA/ >5 mils
1mA/ >10 mils
97mA/ >5 mils
400mA/ >16 mils
80mA/ >5 mils
/> 10 mils
60mA/ >5 mils
50mA/ >5 mils
50mA/ >5 mils
50mA/ >5 mils
10mA/ >5 mils
/> 10 mils
/> 10 mils
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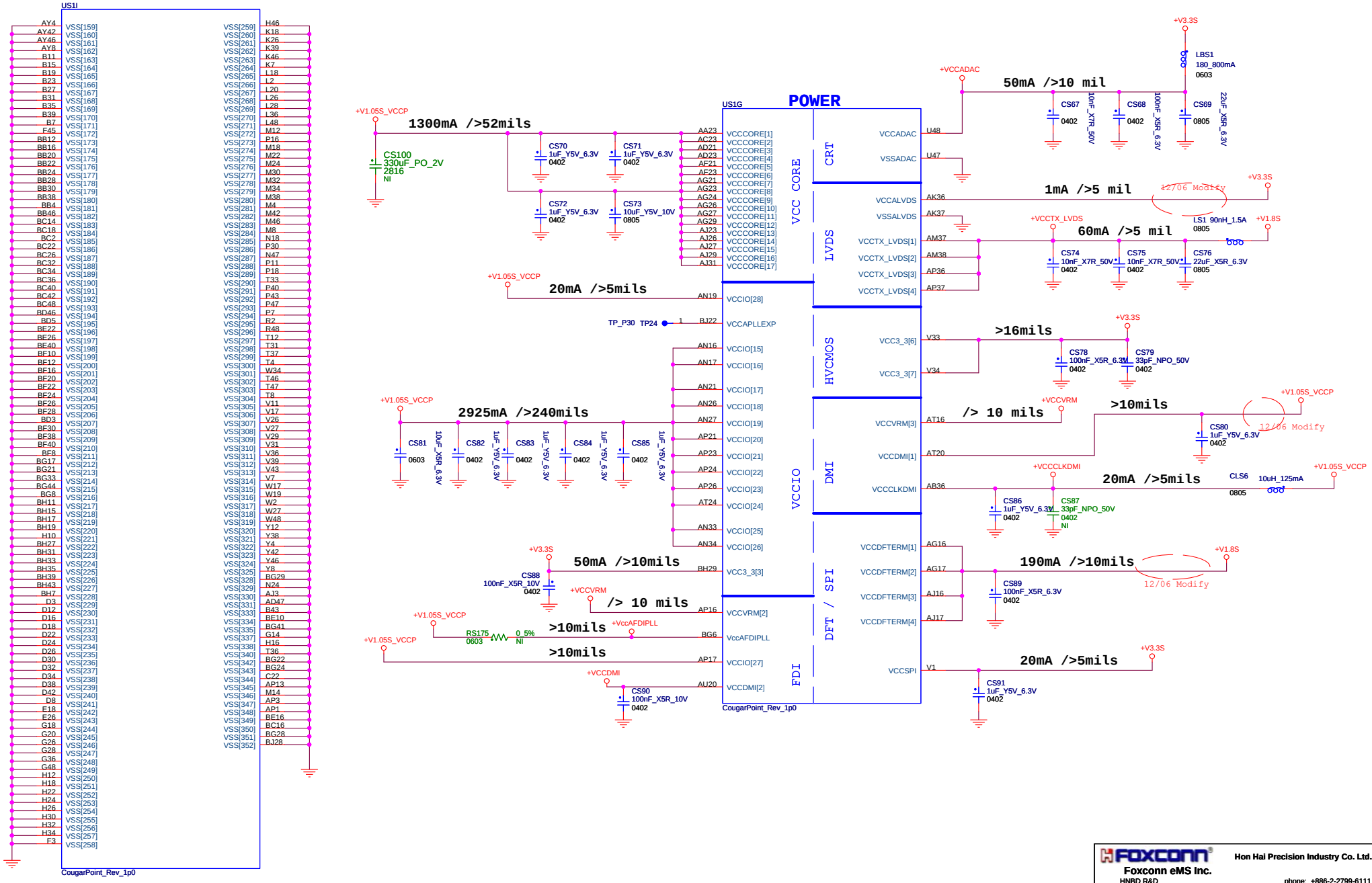

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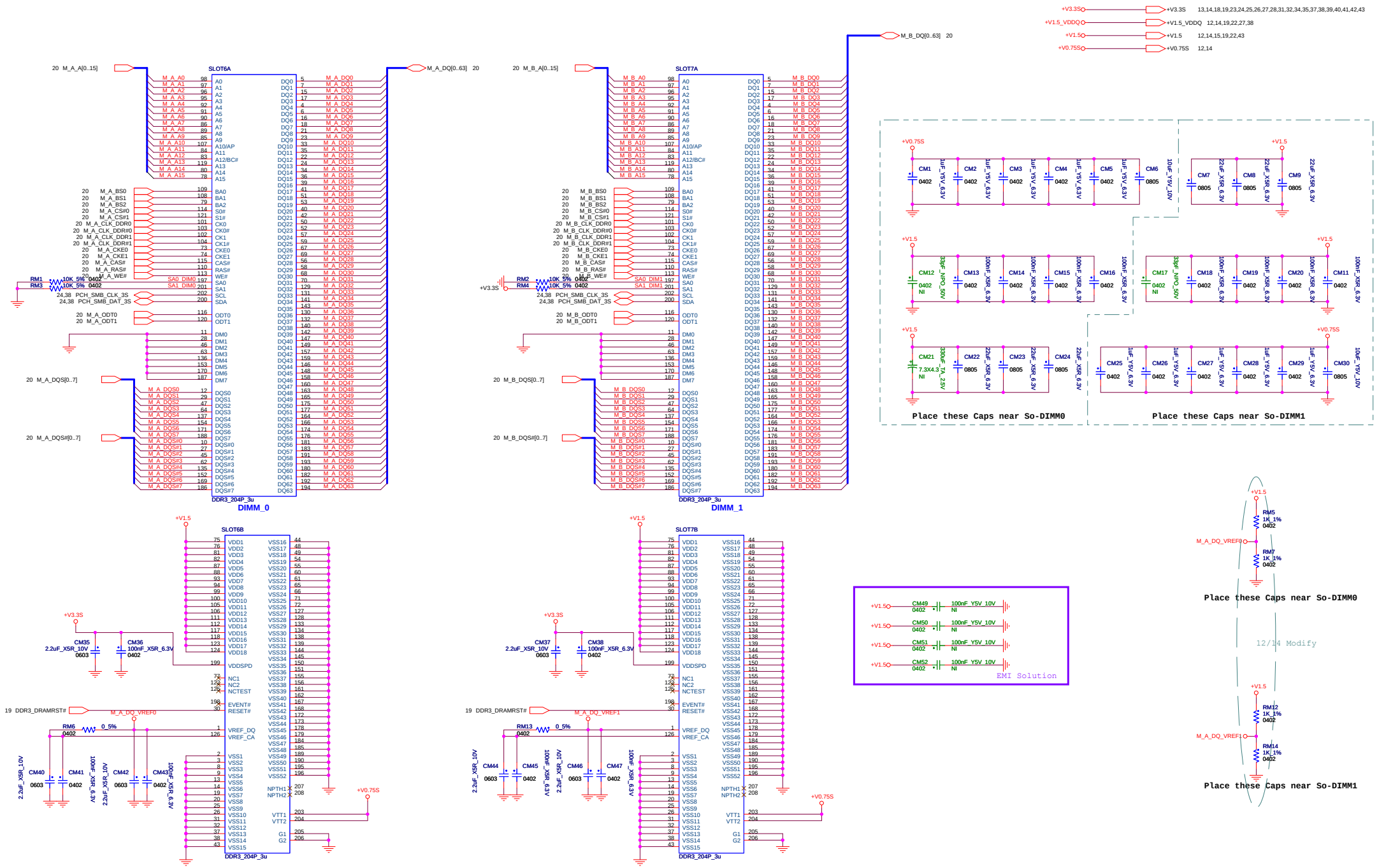
SLOT6A
DDR3_204P_3u
DIMM_0
SLOT7A
DIMM_1
SLOT6B
SLOT7B
M_A_DQ[0..63] 20
M_B_DQ[0..63] 20
+V3.3S 13,14,18,19,23,24,25,26,27,28,31,32,34,35,37,38,39,40,41,42,43
+V1.5_VDDQ 12,14,19,22,27,38
+V1.5 12,14,15,19,22,43
+V0.75S 12,14
Place these Caps near So-DIMM0
Place these Caps near So-DIMM1
EMI Solution
M_A_DQ_VREF0
M_A_DQ_VREF1
12/14 Modify
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Title
DDR3 SO-DIMM_0/SO-DIMM_1
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Document Number
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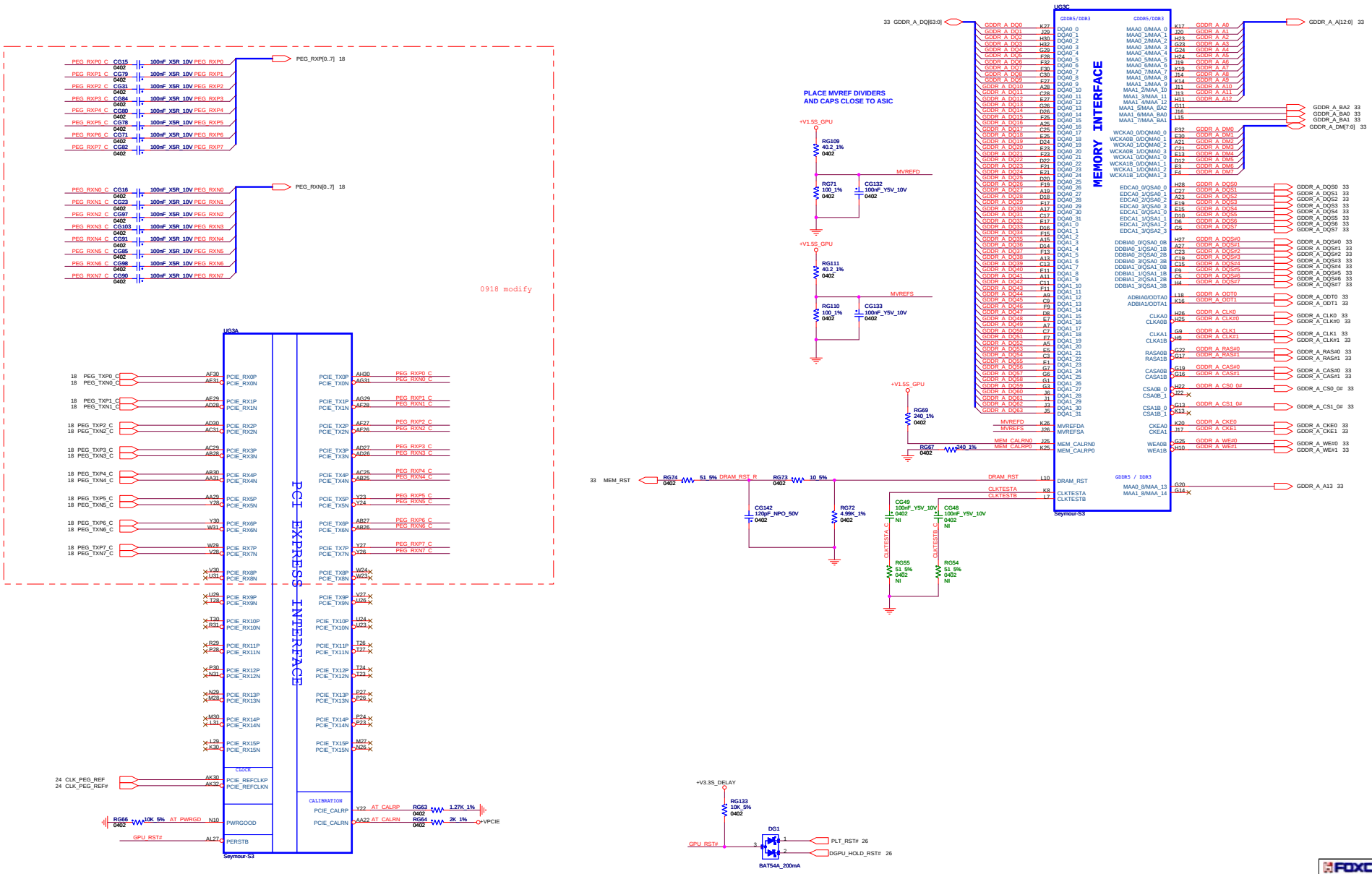

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Title: VGA_S3 (PCI-E) 1/3

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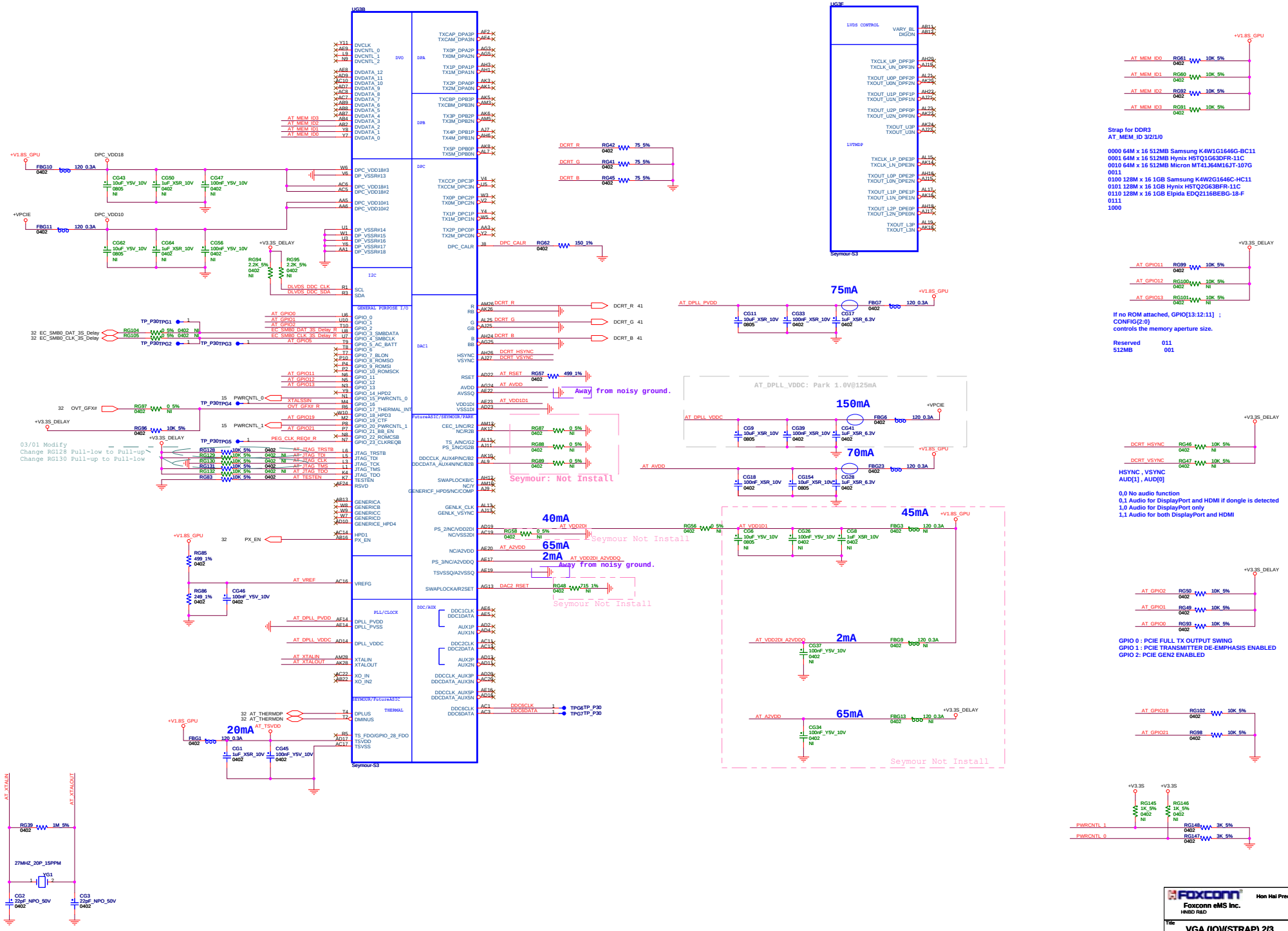
UG3B
Seymour-S3
UG3F
LVDS CONTROL
LVTMDP
Strap for DDR3
AT_MEM_ID 3/2/1/0
0000 64M x 16 512MB Samsung K4W1G1646G-BC11
0001 64M x 16 512MB Hynix H5TQ1G63DFR-11C
0010 64M x 16 512MB Micron MT41J64M16JT-107G
0011
0100 128M x 16 1GB Samsung K4W2G1646C-HC11
0101 128M x 16 1GB Hynix H5TQ2G63BFR-11C
0110 128M x 16 1GB Elpida EDQ2116BEBG-18-F
0111
1000
If no ROM attached, GPIO[13:12:11] ;
CONFIG{2:0}
controls the memory aperture size.
Reserved 011
512MB 001
HSYNC , VSYNC
AUD[1] , AUD[0]
0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI
GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2: PCIE GEN2 ENABLED
75mA
150mA
70mA
45mA
40mA
65mA
2mA
20mA
Away from noisy ground.
Seymour: Not Install
Seymour Not Install
AT_DPLL_VDDC: Park 1.0V@125mA
03/01 Modify
Change RG128 Pull-low to Pull-up
Change RG130 Pull-up to Pull-low
27MHZ_20P_15PPM
Foxconn
Foxconn eMS Inc.
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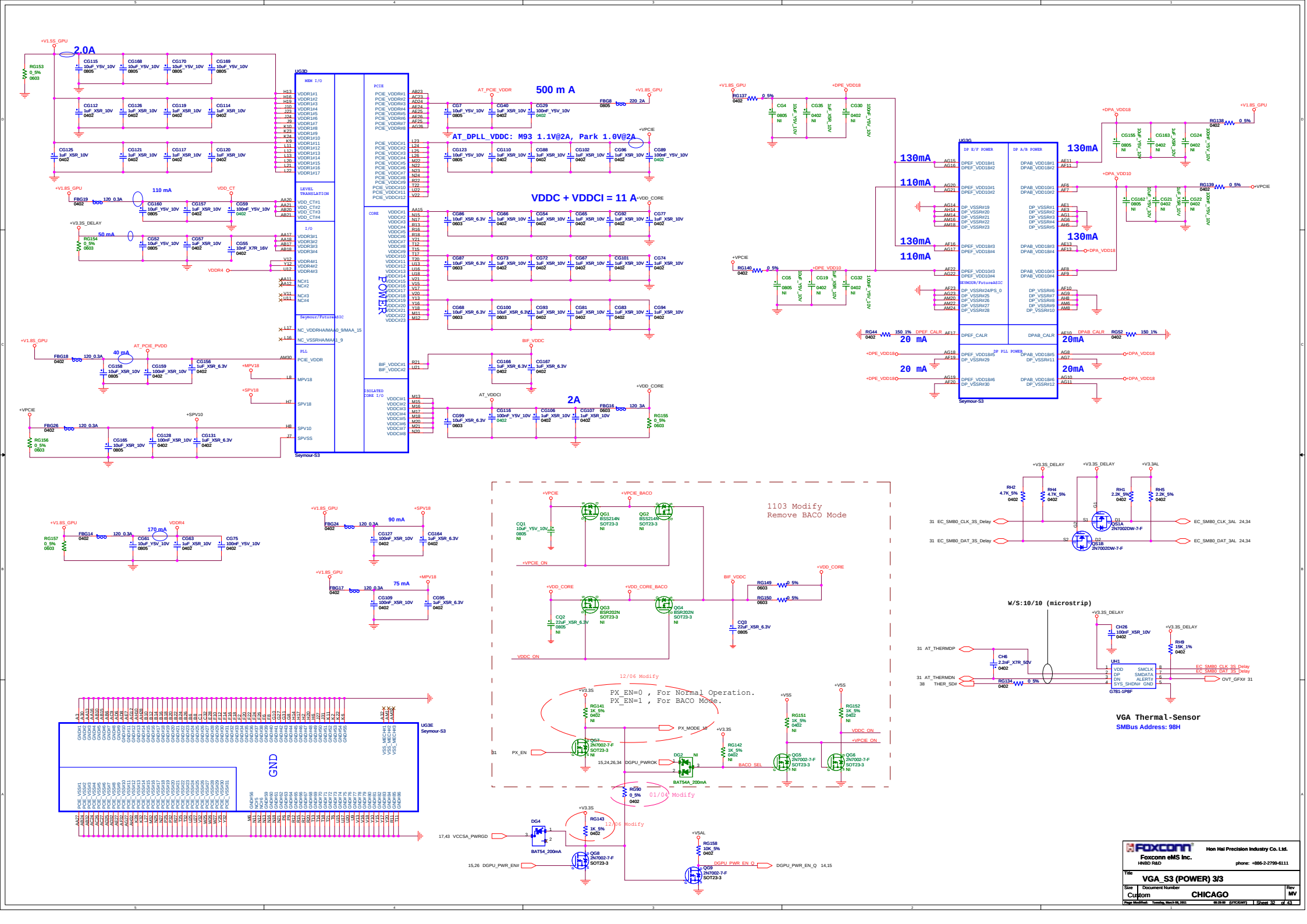
Title
VGA (IO)/(STRAP) 2/3
Size
Document Number
Rev
Custom
CHICAGO
MV
Page Modified: Tuesday, March 09, 2021
Sheet 31 of 43


2.0A
500 m A
AT_PCIE_VDDR
AT_DPLL_VDDC: M93 1.1V@2A, Park 1.0V@2A
VDDC + VDDCI = 11 A
110 mA
50 mA
40 mA
AT_PCIE_PVDD
BIF_VDDC
2A
AT_VDDCI
170 mA
90 mA
75 mA
130mA
110mA
20 mA
UG3D
Seymour-S3
UG3G
UG3E
1103 Modify
Remove BACO Mode
PX_EN=0 , For Normal Operation.
PX_EN=1 , For BACO Mode.
12/06 Modify
01/04 Modify
W/S:10/10 (microstrip)
VGA Thermal-Sensor
SMBus Address: 98H
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VGA_S3 (POWER) 3/3
Size: Custom
Document Number: CHICAGO
Rev: MV
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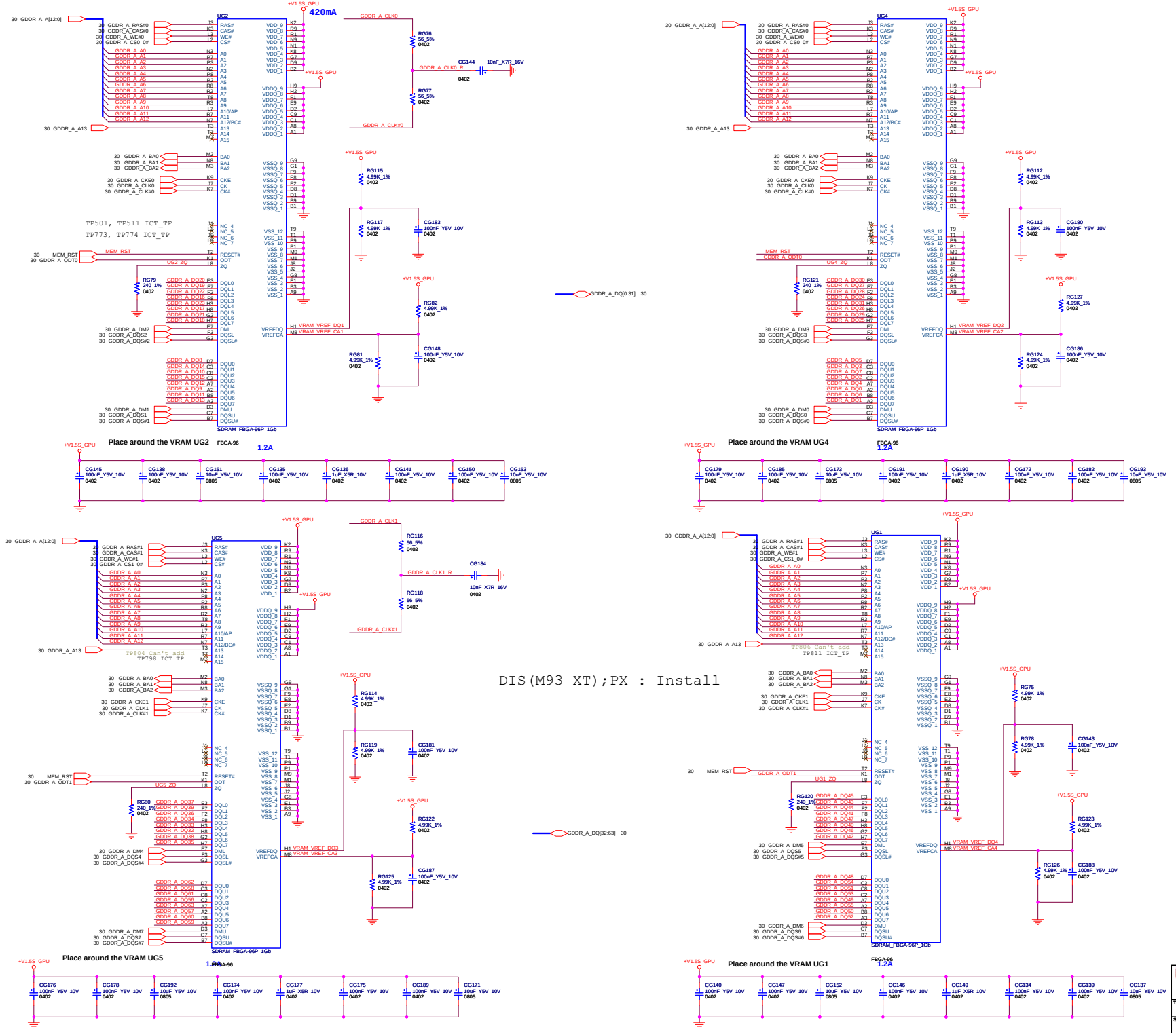

DIS(M93 XT);PX : Install

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Title: VRAM (DDR3)

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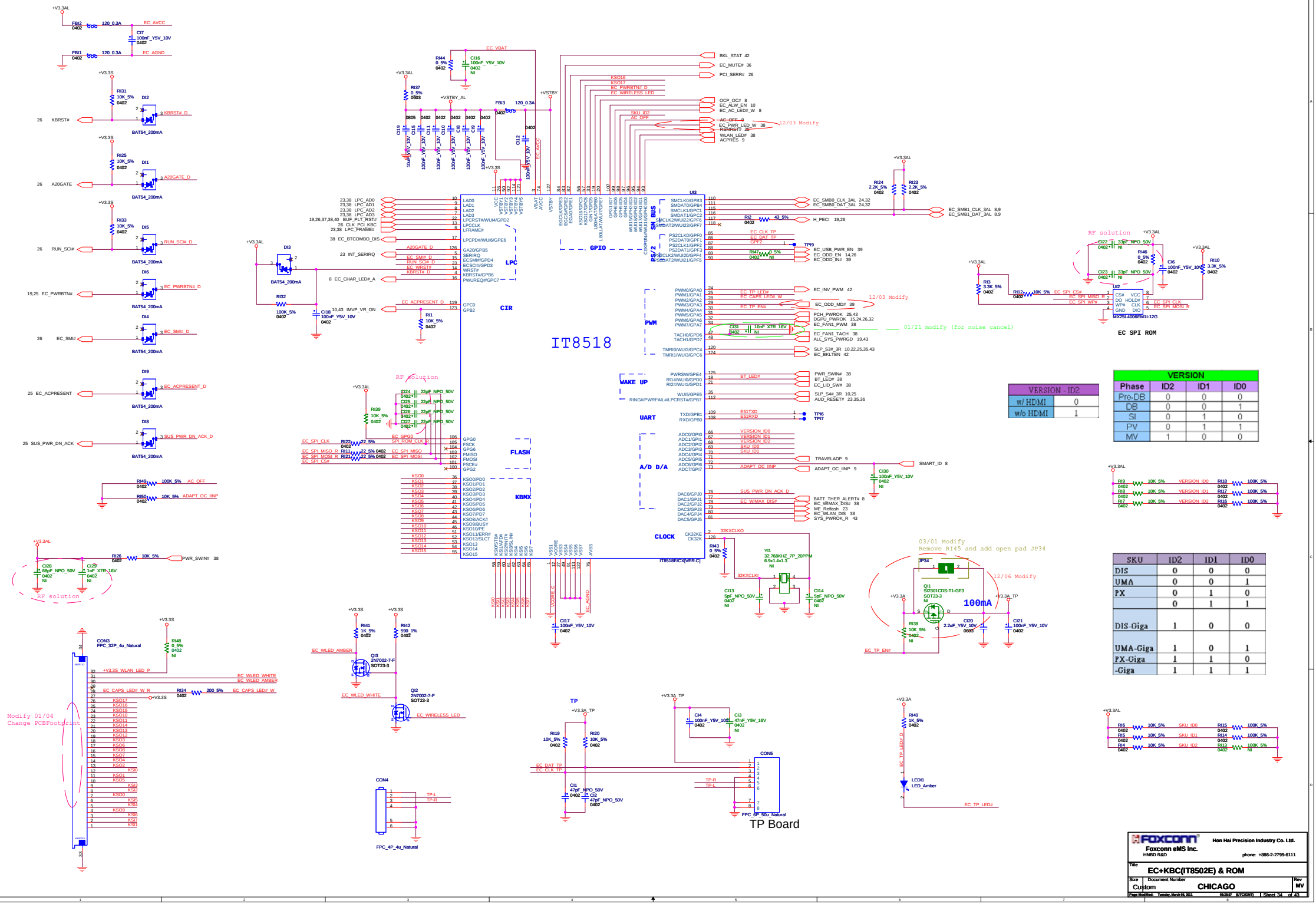
IT8518
LPC
CIR
FLASH
KBMX
GPIO
SMB BUS
PWM
WAKE UP
UART
A/D D/A
CLOCK
EC SPI ROM
TP Board
RF solution
12/03 Modify
01/21 modify (for noise cancel)
03/01 Modify
Remove RI45 and add open pad JP34
12/06 Modify
100mA
Modify 01/04
Change PCBFootprint
VERSION - ID2
w/ HDMI 0
w/o HDMI 1
VERSION
Phase ID2 ID1 ID0
Pre-DB 0 0 0
DB 0 0 1
SI 0 1 0
PV 0 1 1
MV 1 0 0
SKU ID2 ID1 ID0
DIS 0 0 0
UMA 0 0 1
PX 0 1 0
0 1 1
DIS-Giga 1 0 0
UMA-Giga 1 0 1
PX-Giga 1 1 0
-Giga 1 1 1
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Title
EC+KBC(IT8502E) & ROM
Size Document Number Rev
Custom CHICAGO MV
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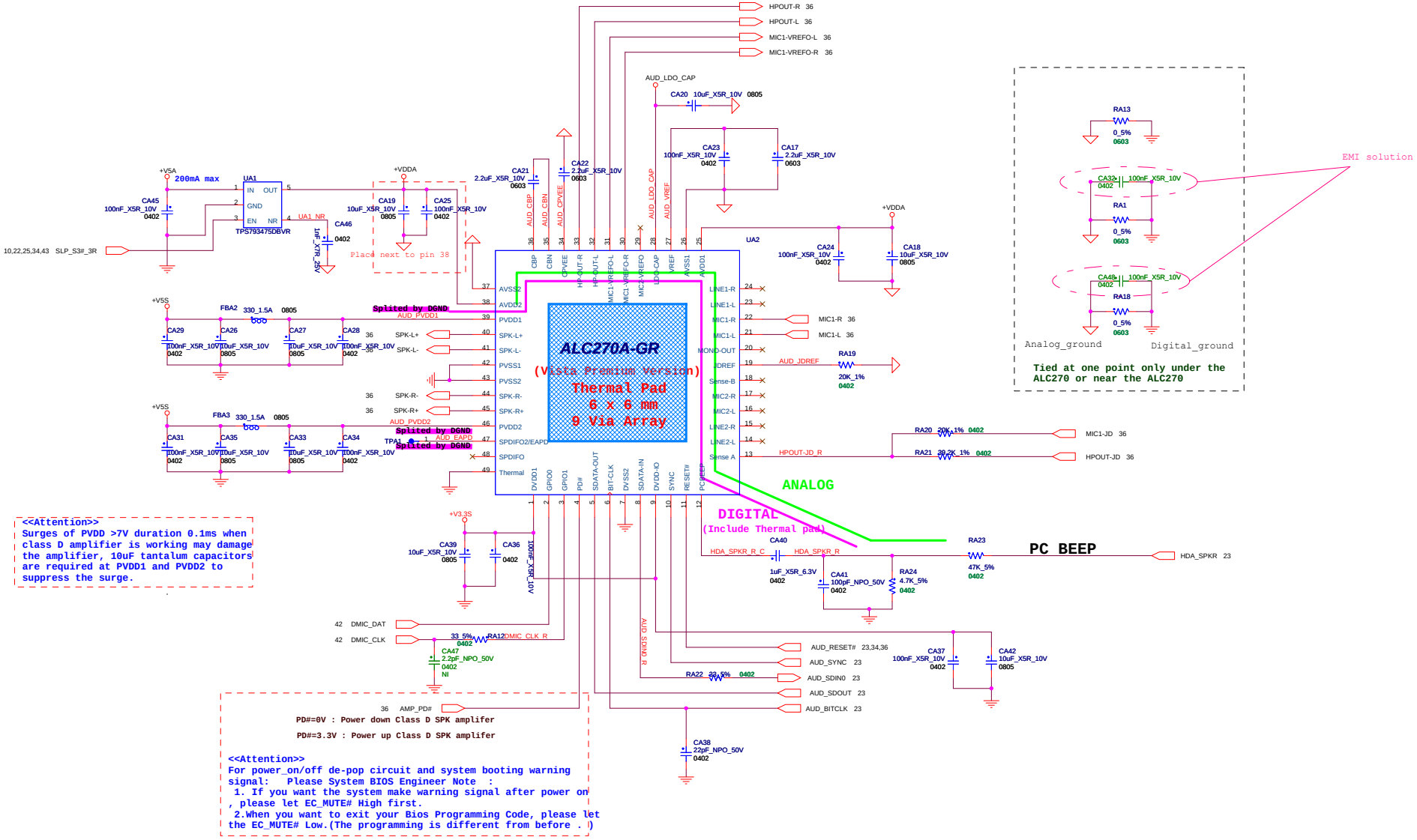

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Title: Audio (CODEC_ALC270A)

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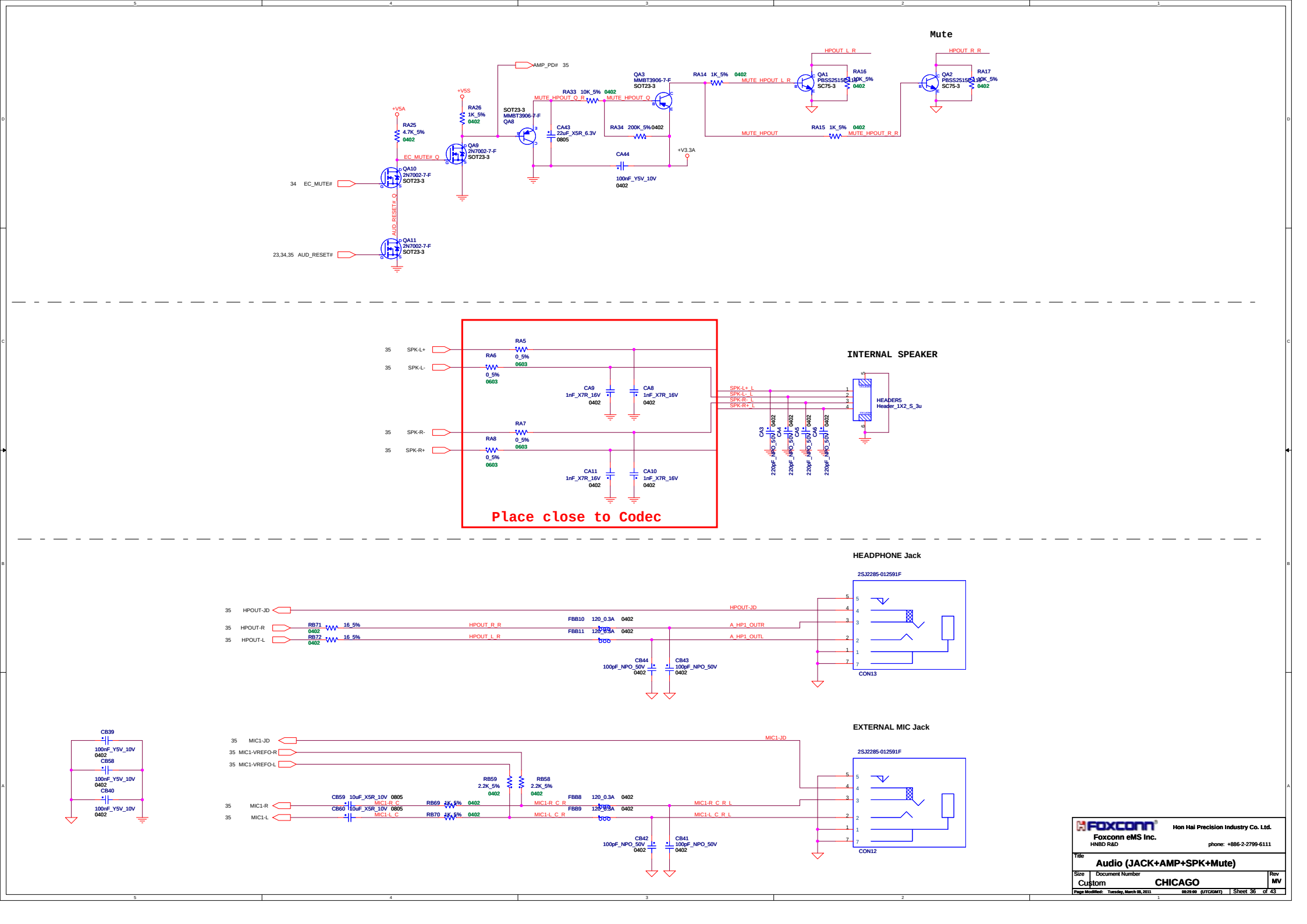
Mute
AMP_PD# 35
+V5S
+V5A
RA26 1K_5% 0402
RA25 4.7K_5% 0402
EC_MUTE# Q
QA9 2N7002-7-F SOT23-3
QA10 2N7002-7-F SOT23-3
34 EC_MUTE#
AUD_RESET# Q
QA11 2N7002-7-F SOT23-3
23,34,35 AUD_RESET#
SOT23-3 MMBT3906-7-F QA8
RA33 10K_5% 0402
MUTE_HPOUT_Q_R
MUTE_HPOUT_Q
CA43 22uF_X5R_6.3V 0805
QA3 MMBT3906-7-F SOT23-3
RA34 200K_5% 0402
CA44 100nF_Y5V_10V 0402
+V3.3A
RA14 1K_5% 0402
MUTE_HPOUT_L_R
HPOUT_L_R
QA1 PBSS2515E-115 SC75-3
RA16 10K_5% 0402
MUTE_HPOUT
RA15 1K_5% 0402
MUTE_HPOUT_R_R
HPOUT_R_R
QA2 PBSS2515E-115 SC75-3
RA17 10K_5% 0402
INTERNAL SPEAKER
35 SPK-L+
35 SPK-L-
35 SPK-R-
35 SPK-R+
RA5 0_5% 0603
RA6 0_5% 0603
RA7 0_5% 0603
RA8 0_5% 0603
CA9 1nF_X7R_16V 0402
CA8 1nF_X7R_16V 0402
CA11 1nF_X7R_16V 0402
CA10 1nF_X7R_16V 0402
Place close to Codec
SPK-L+_L
SPK-L-_L
SPK-R-_L
SPK-R+_L
CA3 220pF_NPO_50V 0402
CA4 220pF_NPO_50V 0402
CA5 220pF_NPO_50V 0402
CA6 220pF_NPO_50V 0402
HEADER5 Header_1X2_S_3u
HEADPHONE Jack
2SJ2285-012591F
35 HPOUT-JD
35 HPOUT-R
35 HPOUT-L
RB71 0402 16_5%
RB72 0402 16_5%
HPOUT_R_R
HPOUT_L_R
FBB10 120_0.3A 0402
FBB11 120_0.3A 0402
HPOUT-JD
A_HP1_OUTR
A_HP1_OUTL
CB44 100pF_NPO_50V 0402
CB43 100pF_NPO_50V 0402
CON13
CB39 100nF_Y5V_10V 0402
CB58 100nF_Y5V_10V 0402
CB40 100nF_Y5V_10V 0402
EXTERNAL MIC Jack
2SJ2285-012591F
35 MIC1-JD
35 MIC1-VREFO-R
35 MIC1-VREFO-L
35 MIC1-R
35 MIC1-L
RB59 2.2K_5% 0402
RB58 2.2K_5% 0402
CB59 10uF_X5R_10V 0805
CB60 10uF_X5R_10V 0805
MIC1-R_C
MIC1-L_C
RB69 1K_5% 0402
RB70 1K_5% 0402
FBB8 120_0.3A 0402
FBB9 120_0.3A 0402
MIC1-R_C_R
MIC1-L_C_R
MIC1-JD
MIC1-R_C_R_L
MIC1-L_C_R_L
CB42 100pF_NPO_50V 0402
CB41 100pF_NPO_50V 0402
CON12
FOXCONN
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Title
Audio (JACK+AMP+SPK+Mute)
Size Custom
Document Number CHICAGO
Rev MV
Page Modified: Tuesday, March 08, 2011 08:29:00 (UTC/GMT)
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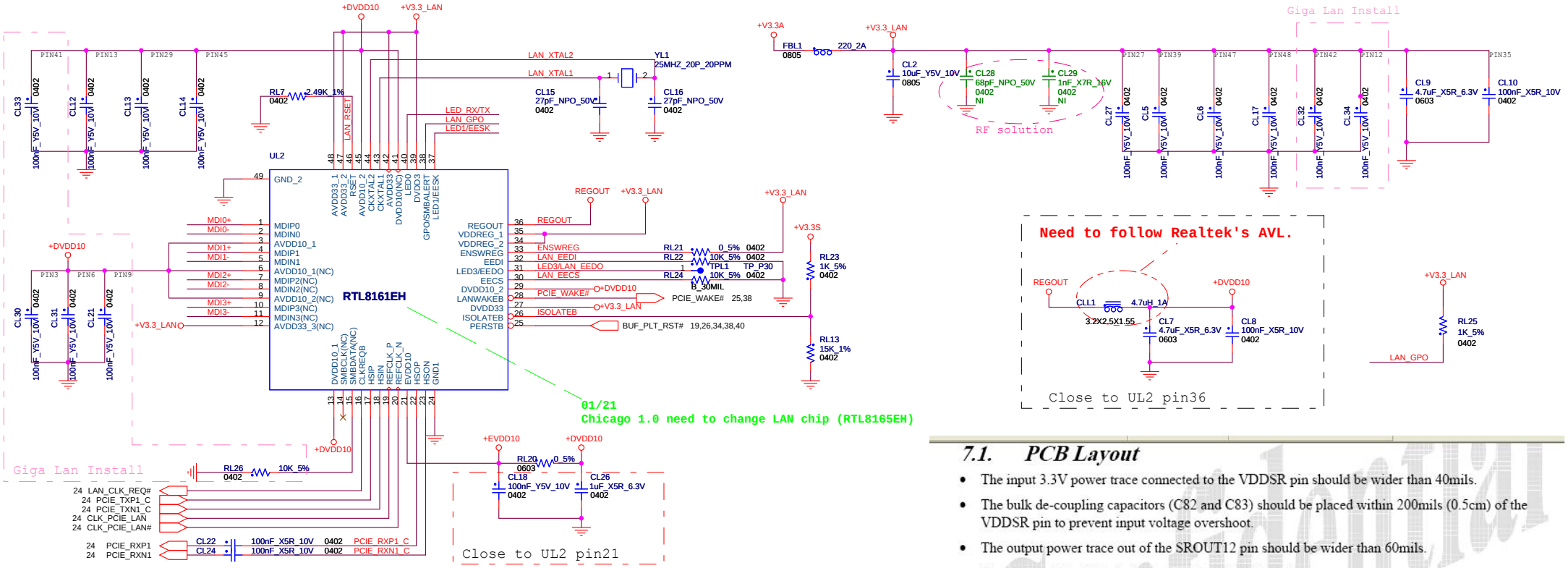
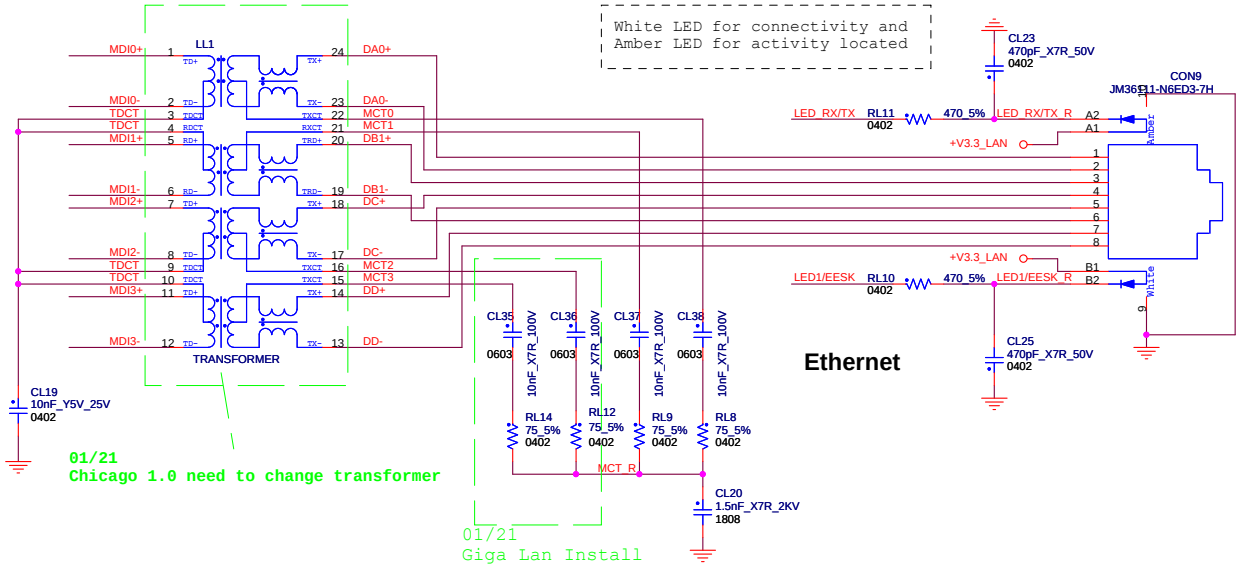
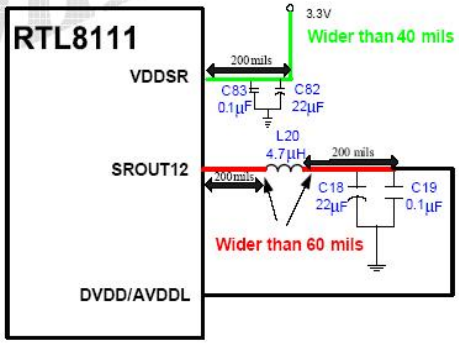




7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

Note: Violation of the above rules will damage the IC.



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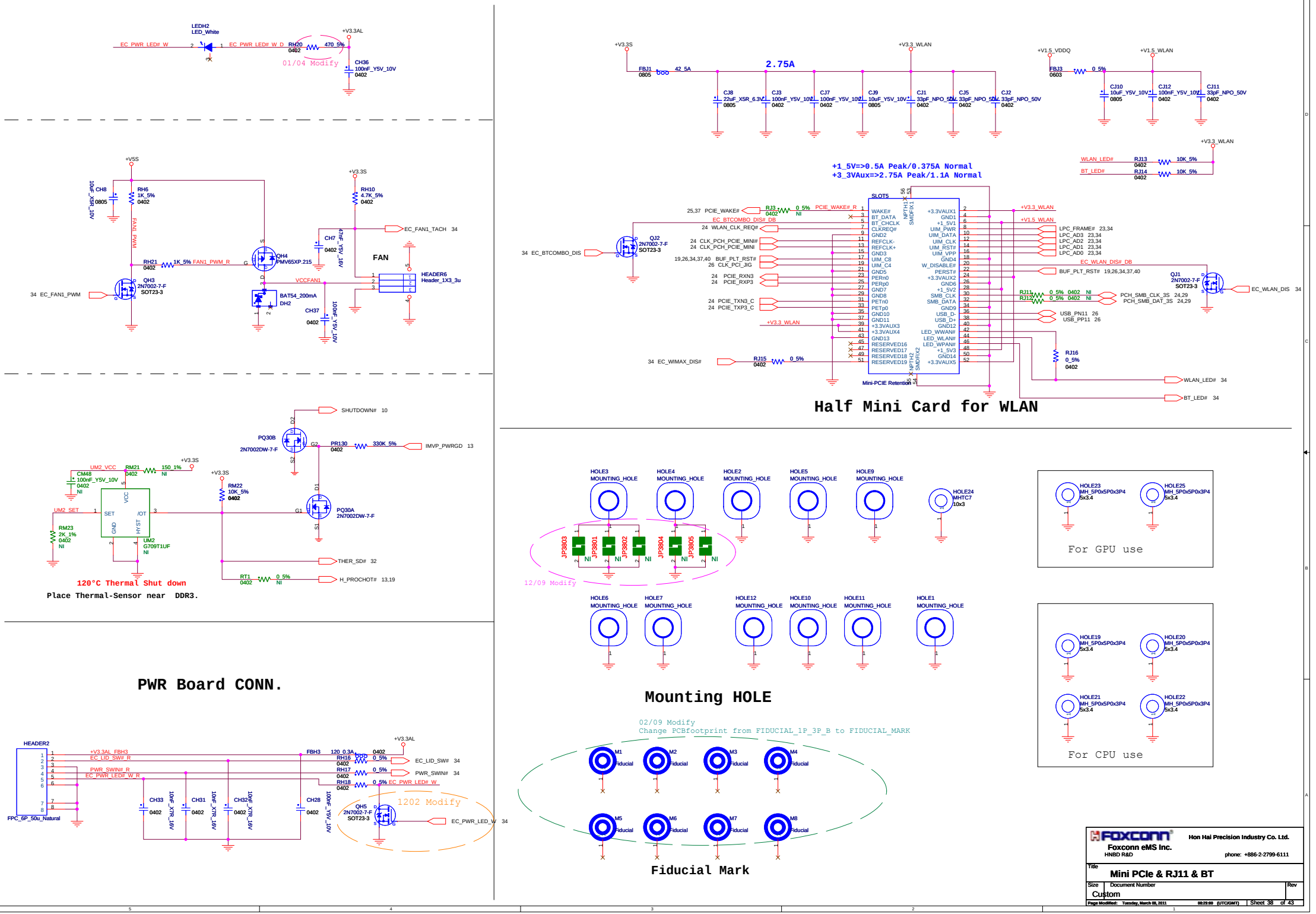
LEDH2
LED_White
EC_PWR_LED# W
EC_PWR_LED# W_D
RH20
0402
470 5%
+V3.3AL
CH36
100nF_Y5V_10V
0402
01/04 Modify
+V5S
CH8
10uF_X5R_10V
0805
RH6
1K_5%
0402
FAN1_PWM
RH21
0402
1K 5% FAN1_PWM_R
QH3
2N7002-7-F
SOT23-3
34 EC_FAN1_PWM
QH4
PMV65XP.215
BAT54_200mA
DH2
+V3.3S
RH10
4.7K_5%
0402
CH7
0402
47nF_Y5V_16V
VCCFAN1
CH37
0402
100nF_Y5V_10V
EC_FAN1_TACH 34
FAN
HEADER6
Header_1X3_3u
+V3.3S
FBJ1
0805
42_5A
2.75A
CJ8
22uF_X5R_6.3V
0805
CJ3
100nF_Y5V_10V
0402
CJ7
100nF_Y5V_10V
0402
CJ9
10uF_Y5V_10V
0805
+V3.3_WLAN
CJ1
33pF_NPO_50V
0402
CJ5
33pF_NPO_50V
0402
CJ2
33pF_NPO_50V
0402
+V1.5_VDDQ
FBJ3
0603
0 5%
+V1.5_WLAN
CJ10
10uF_Y5V_10V
0805
CJ12
100nF_Y5V_10V
0402
CJ11
33pF_NPO_50V
0402
+V3.3_WLAN
WLAN_LED#
RJ13
0402
10K 5%
BT_LED#
RJ14
0402
10K 5%
+1_5V=>0.5A Peak/0.375A Normal
+3_3VAux=>2.75A Peak/1.1A Normal
SLOT5
25,37 PCIE_WAKE#
RJ3
0402
0 5%
NI
PCIE_WAKE#_R
EC_BTCOMBO_DIS# DB
24 WLAN_CLK_REQ#
QJ2
2N7002-7-F
SOT23-3
34 EC_BTCOMBO_DIS
24 CLK_PCH_PCIE_MINI#
24 CLK_PCH_PCIE_MINI
19,26,34,37,40 BUF_PLT_RST#
26 CLK_PCI_JIG
24 PCIE_RXN3
24 PCIE_RXP3
24 PCIE_TXN3_C
24 PCIE_TXP3_C
+V3.3_WLAN
34 EC_WIMAX_DIS#
RJ15
0402
0 5%
WAKE#
BT_DATA
BT_CHCLK
CLKREQ#
GND2
REFCLK-
REFCLK+
GND3
UIM_C8
UIM_C4
GND5
PERn0
PERp0
GND7
GND8
PETn0
PETp0
GND10
GND11
+3.3VAUX3
+3.3VAUX4
GND13
RESERVED16
RESERVED17
RESERVED18
RESERVED19
+3.3VAUX1
GND1
+1_5V1
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RST#
UIM_VPP
GND4
W_DISABLE#
PERST#
+3.3VAUX2
GND6
+1_5V2
SMB_CLK
SMB_DATA
GND9
USB_D-
USB_D+
GND12
LED_WWAN#
LED_WLAN#
LED_WPAN#
+1_5V3
GND14
+3.3VAUX5
Mini-PCIE Retention
+V3.3_WLAN
+V1.5_WLAN
LPC_FRAME# 23,34
LPC_AD3 23,34
LPC_AD2 23,34
LPC_AD1 23,34
LPC_AD0 23,34
EC_WLAN_DIS# DB
BUF_PLT_RST# 19,26,34,37,40
QJ1
2N7002-7-F
SOT23-3
EC_WLAN_DIS 34
RJ11
RJ12
0 5% 0402 NI
PCH_SMB_CLK_3S 24,29
PCH_SMB_DAT_3S 24,29
USB_PN11 26
USB_PP11 26
RJ16
0 5%
0402
WLAN_LED# 34
BT_LED# 34
Half Mini Card for WLAN
SHUTDOWN# 10
PQ30B
2N7002DW-7-F
PR130
0402
330K 5%
IMVP_PWRGD 13
UM2_VCC
RM21
0402
150_1%
NI
+V3.3S
CM48
100nF_Y5V_10V
0402
NI
UM2_SET
RM23
2K_1%
0402
NI
UM2
G709T1UF
NI
+V3.3S
RM22
10K_5%
0402
PQ30A
2N7002DW-7-F
THER_SD# 32
RT1
0402
0 5%
NI
H_PROCHOT# 13,19
120°C Thermal Shut down
Place Thermal-Sensor near DDR3.
HOLE3
MOUNTING_HOLE
HOLE4
MOUNTING_HOLE
HOLE2
MOUNTING_HOLE
HOLE5
MOUNTING_HOLE
HOLE9
MOUNTING_HOLE
HOLE24
MHTC7
10x3
JP3803
JP3801
JP3802
JP3804
JP3805
NI
12/09 Modify
HOLE6
MOUNTING_HOLE
HOLE7
MOUNTING_HOLE
HOLE12
MOUNTING_HOLE
HOLE10
MOUNTING_HOLE
HOLE11
MOUNTING_HOLE
HOLE1
MOUNTING_HOLE
Mounting HOLE
HOLE23
MH_5P0x5P0x3P4
5x3.4
HOLE25
MH_5P0x5P0x3P4
5x3.4
For GPU use
HOLE19
MH_5P0x5P0x3P4
5x3.4
HOLE20
MH_5P0x5P0x3P4
5x3.4
HOLE21
MH_5P0x5P0x3P4
5x3.4
HOLE22
MH_5P0x5P0x3P4
5x3.4
For CPU use
PWR Board CONN.
HEADER2
FPC_6P_50u_Natural
+V3.3AL_FBH3
EC_LID_SW# R
PWR_SWIN# R
EC_PWR_LED# W_R
FBH3
120_0.3A
0402
+V3.3AL
RH16
0402
0 5%
EC_LID_SW# 34
RH17
0402
0 5%
PWR_SWIN# 34
RH18
0402
0 5%
EC_PWR_LED# W
CH33
0402
10nF_X7R_16V
CH31
0402
10nF_X7R_16V
CH32
0402
10nF_X7R_16V
CH28
0402
100nF_Y5V_10V
QH5
2N7002-7-F
SOT23-3
EC_PWR_LED_W 34
1202 Modify
02/09 Modify
Change PCBfootprint from FIDUCIAL_1P_3P_B to FIDUCIAL_MARK
M1
Fiducial
M2
Fiducial
M3
Fiducial
M4
Fiducial
M5
Fiducial
M6
Fiducial
M7
Fiducial
M8
Fiducial
Fiducial Mark
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Title
Mini PCIe & RJ11 & BT
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Document Number
Rev
Custom
Page Modified: Tuesday, March 08, 2011 08:29:00 (UTC/GMT)
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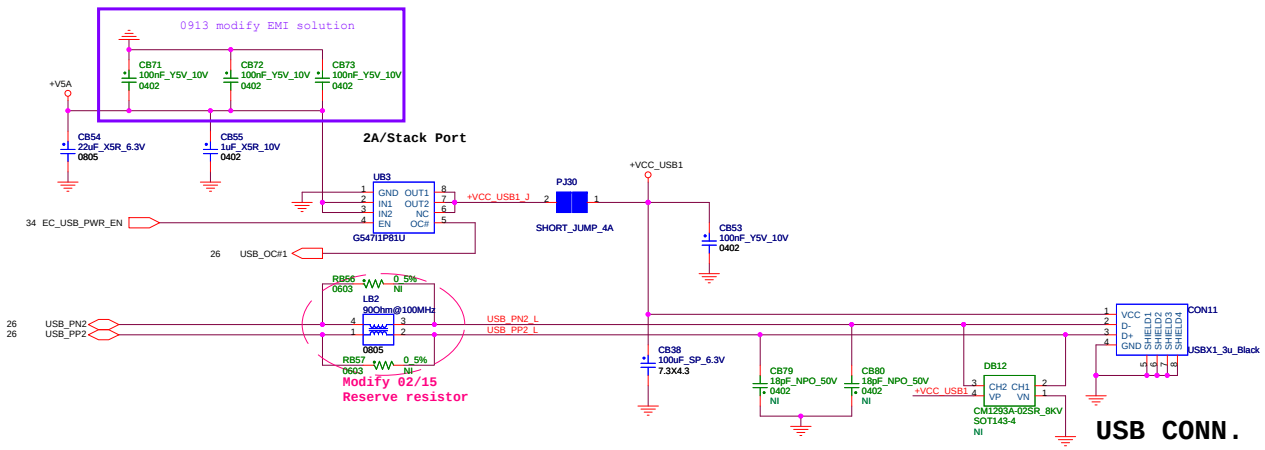
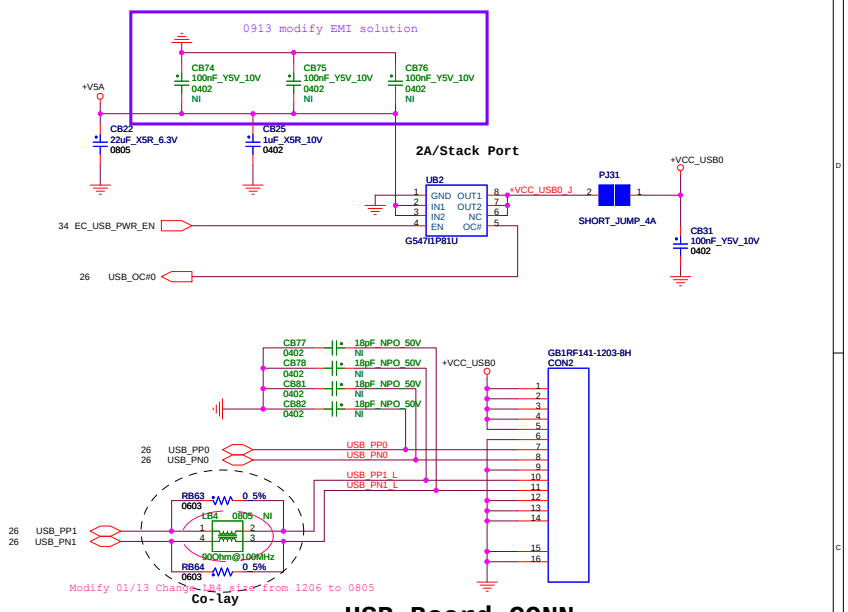
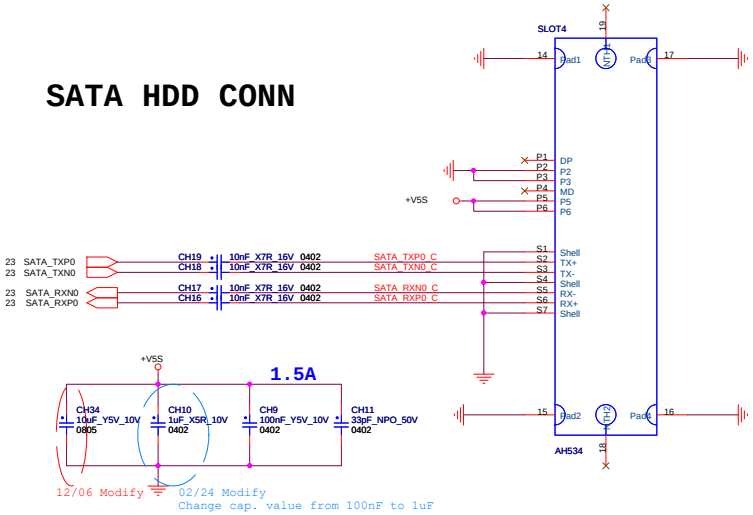
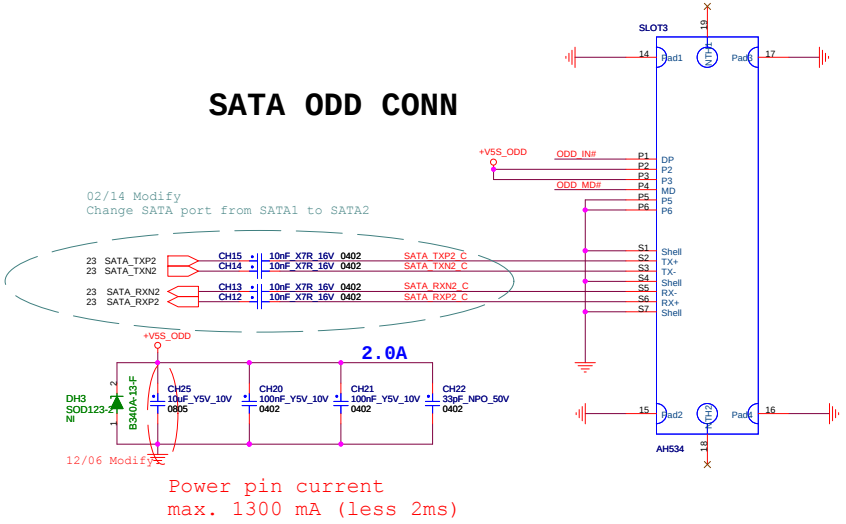




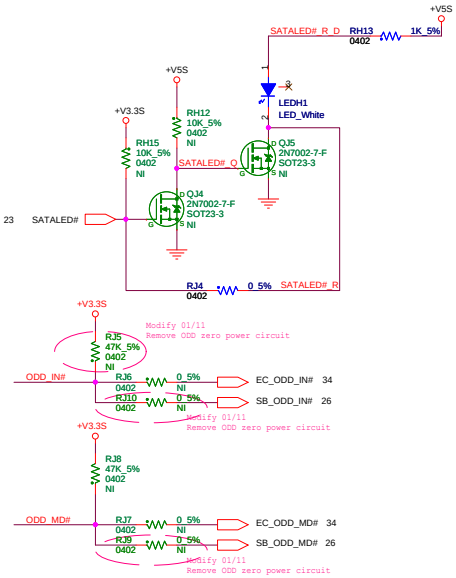
SATA HDD CONN



SATA ODD CONN



HDD/ODD Status LED



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Title: USBX2/USB DB CONN./SATA CONN.		
Size: Custom	Document Number: CHICAGO	Rev: MV
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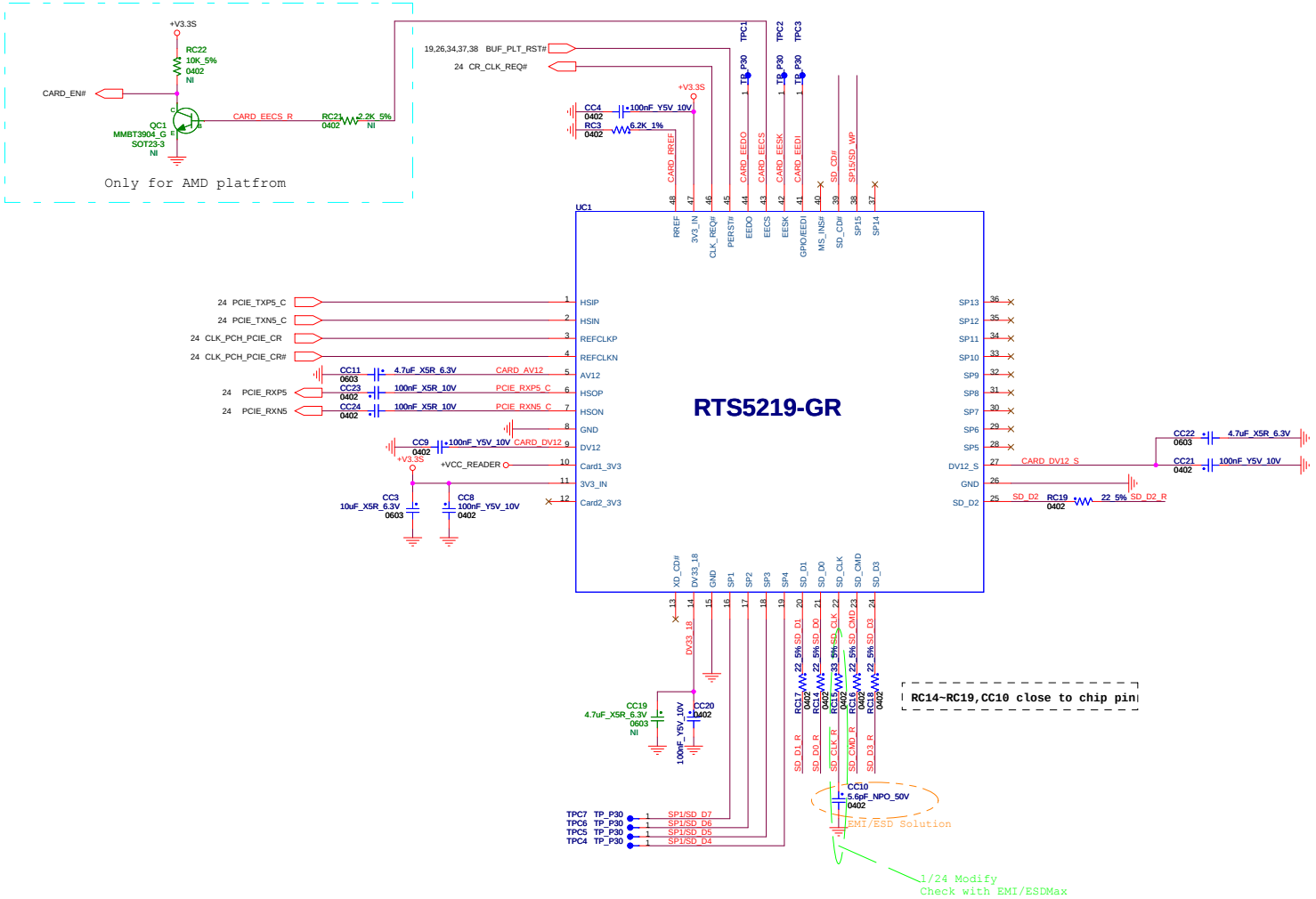

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Title: Card Reader

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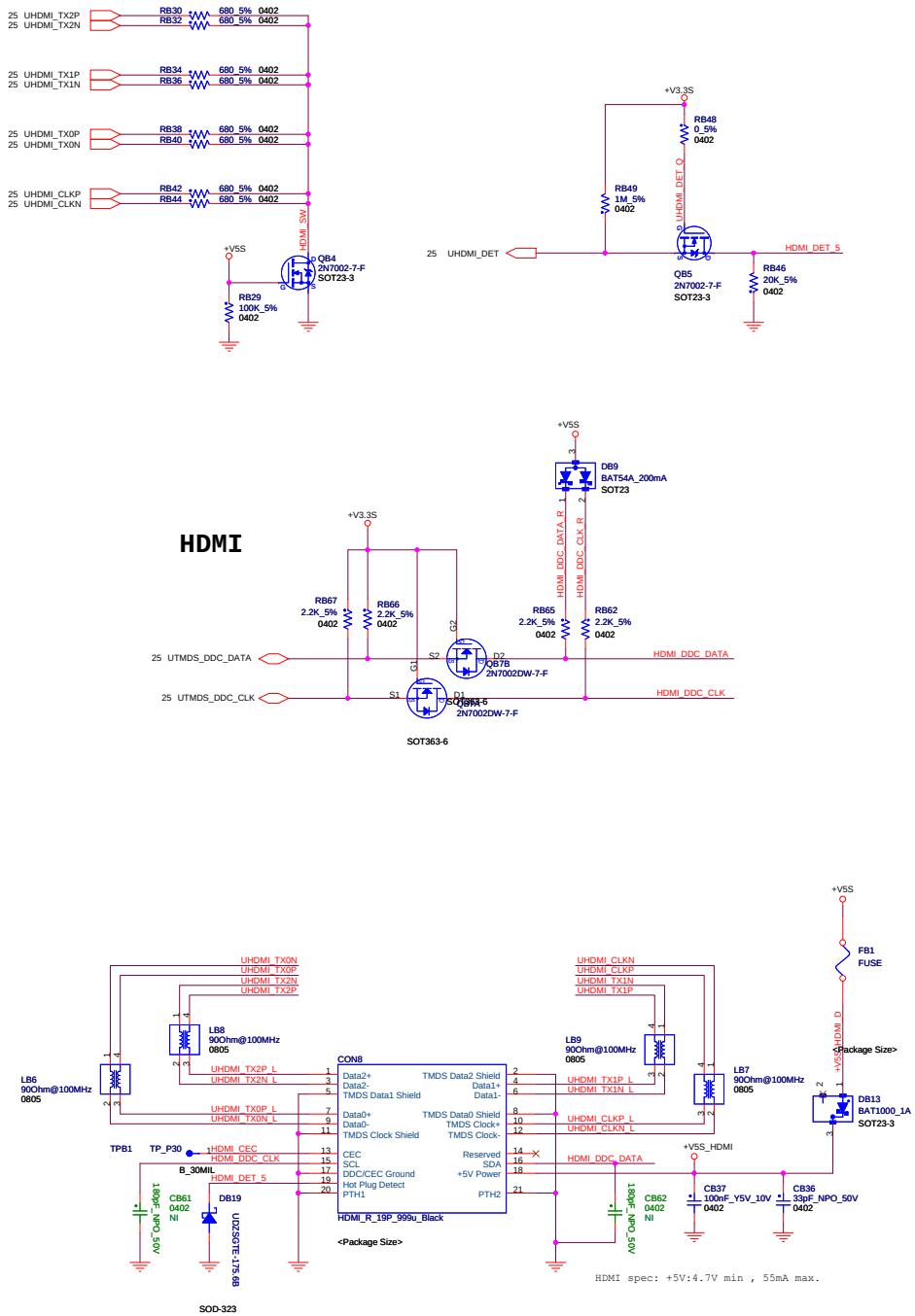

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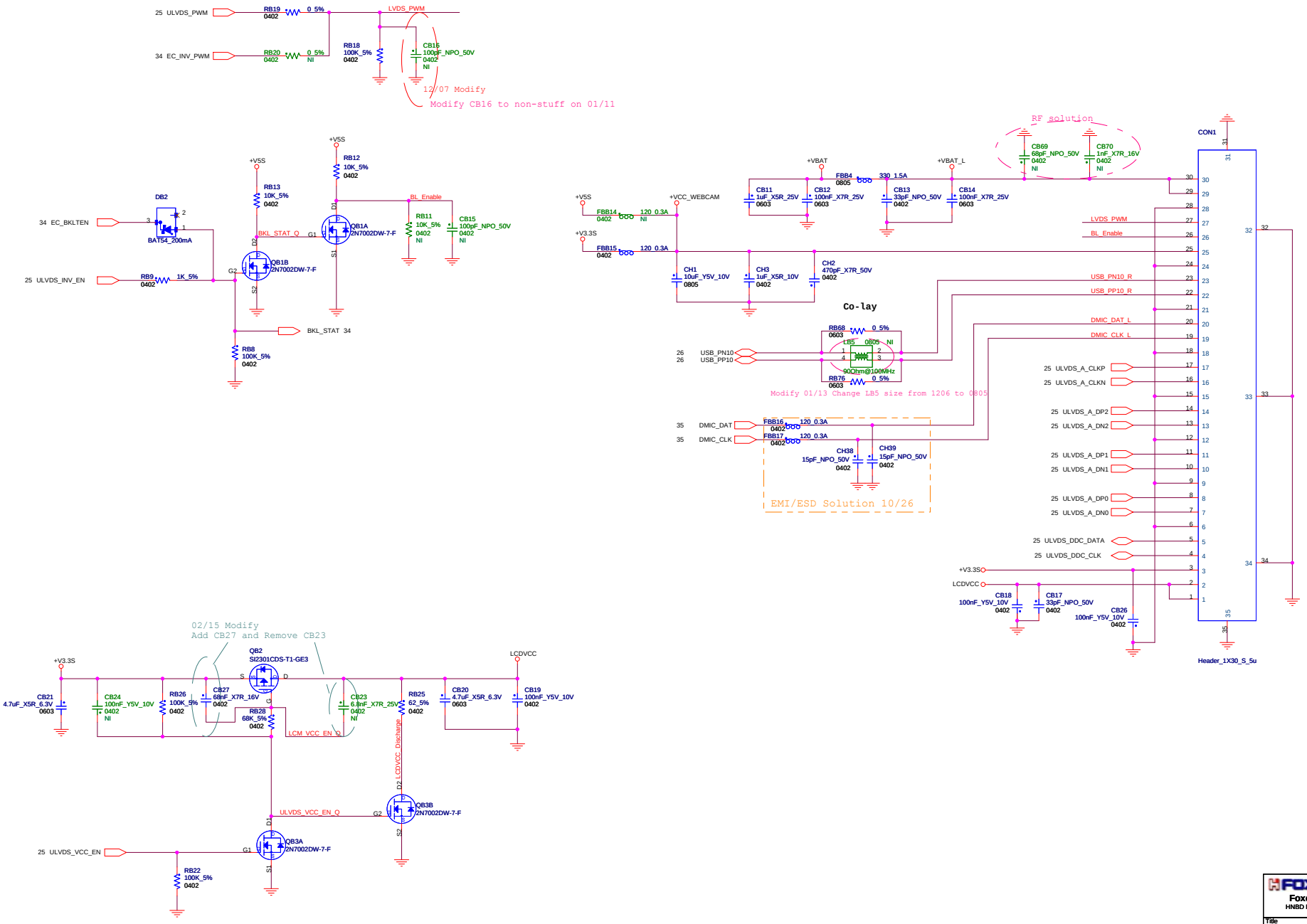
Title: HDMI & CRT		
Size: Custom	Document Number	Rev
Page Modified: Tuesday, March 08, 2011 08:28:59 (UTC/GMT)	Sheet 41 of 43	



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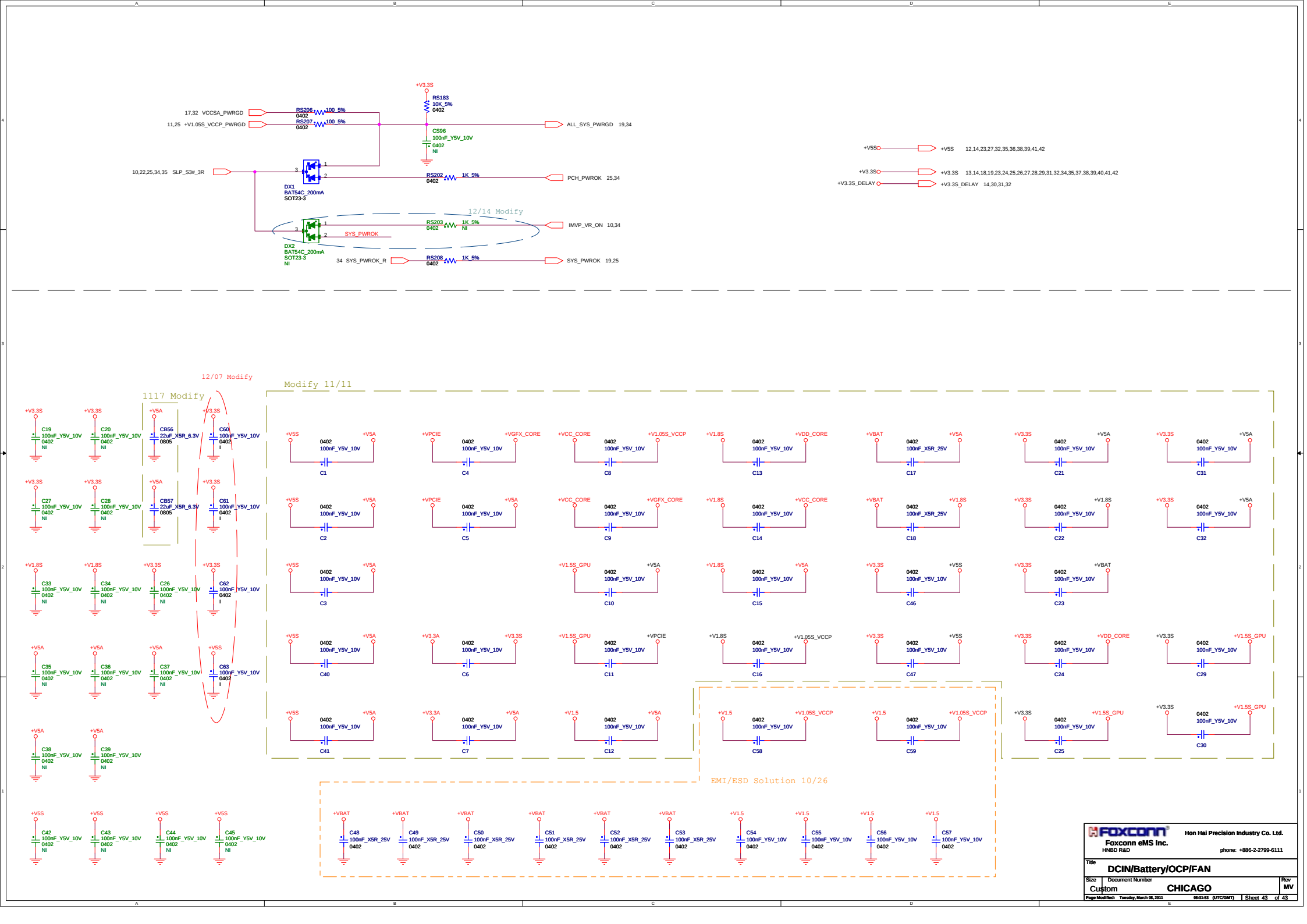
Title: LVDS&Webcam

Size: Custom | Document Number: CHICAGO | Rev: MV

Page Modified: Tuesday, March 08, 2011 08:28:57 (UTC/GMT) | Sheet 42 of 43


+V3.3S
RS183 10K_5% 0402
17,32 VCCSA_PWRGD
11,25 +V1.05S_VCCP_PWRGD
RS206 100_5% 0402
RS207 100_5% 0402
ALL_SYS_PWRGD 19,34
CS96 100nF_Y5V_10V 0402 NI
10,22,25,34,35 SLP_S3#_3R
DX1 BAT54C_200mA SOT23-3
RS202 1K_5% 0402
PCH_PWROK 25,34
12/14 Modify
RS203 1K_5% 0402 NI
IMVP_VR_ON 10,34
SYS_PWROK
DX2 BAT54C_200mA SOT23-3 NI
34 SYS_PWROK_R
RS208 1K_5% 0402
SYS_PWROK 19,25
+V5S
+V5S 12,14,23,27,32,35,36,38,39,41,42
+V3.3S
+V3.3S 13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42
+V3.3S_DELAY
+V3.3S_DELAY 14,30,31,32
12/07 Modify
1117 Modify
Modify 11/11
C19 100nF_Y5V_10V 0402 NI
C20 100nF_Y5V_10V 0402 NI
CB56 22uF_X5R_6.3V 0805
C60 100nF_Y5V_10V 0402 I
C27 100nF_Y5V_10V 0402 NI
C28 100nF_Y5V_10V 0402 NI
CB57 22uF_X5R_6.3V 0805
C61 100nF_Y5V_10V 0402 I
C33 100nF_Y5V_10V 0402 NI
C34 100nF_Y5V_10V 0402 NI
C26 100nF_Y5V_10V 0402 NI
C62 100nF_Y5V_10V 0402 I
C35 100nF_Y5V_10V 0402 NI
C36 100nF_Y5V_10V 0402 NI
C37 100nF_Y5V_10V 0402 NI
C63 100nF_Y5V_10V 0402 I
C38 100nF_Y5V_10V 0402 NI
C39 100nF_Y5V_10V 0402 NI
C42 100nF_Y5V_10V 0402 NI
C43 100nF_Y5V_10V 0402 NI
C44 100nF_Y5V_10V 0402 NI
C45 100nF_Y5V_10V 0402 NI
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C21 C22 C23 C24 C25 C29 C30 C31 C32 C40 C41 C46 C47 C58 C59
0402 100nF_Y5V_10V
0402 100nF_X5R_25V
EMI/ESD Solution 10/26
C48 C49 C50 C51 C52 C53 100nF_X5R_25V 0402
C54 C55 C56 C57 100nF_Y5V_10V 0402
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Title
DCIN/Battery/OCP/FAN
Size Custom
Document Number CHICAGO
Rev MV
Page Modified: Tuesday, March 08, 2011 08:31:53 (UTC/GMT)
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