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Design of an Asynchronous Flash Analog-to-Digital Converter

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Abstract

The proliferation of Internet of Things (IoT) nodes and biomedical sensors has created a stringent demand for ultra-low-power signal processing interfaces. In many of these applications, the signals of interest are sparse or bursty, characterized by long periods of inactivity. Classical synchronous Analog-to-Digital Converters (ADCs) are inherently inefficient in such scenarios, as they consume dynamic power continuously due to the global clock, regardless of the input signal activity.

This dissertation proposes the design and implementation of an Asynchronous Flash ADC. By removing the clock, the proposed architecture aligns power consumption with the input signal activity, theoretically achieving near-zero power dissipation during idle periods. However, the removal of the clock introduces design challenges, particularly regarding the accuracy of continuous-time comparators, which are prone to offset voltages due to transistor mismatch in scaled CMOS technologies.

To address this, an offline trimming strategy is proposed to calibrate the comparator offsets without compromising the high-speed operation of the flash topology. The work encompasses the theoretical analysis, schematic design, and validation of the system through Analog/Mixed-Signal (A/MS) co-simulation. The expected outcome is a robust, clockless ADC architecture that offers a superior Figure of Merit (FoM) for sparse signal applications compared to traditional synchronous counterparts.

Keywords: Analog-to-Digital Converter, Asynchronous Design, Flash ADC, Level-Crossing Sampling, Offset Trimming, Low Power, IoT.

UN Sustainable Development Goals

The United Nations Sustainable Development Goals (SDGs) provide a global framework to achieve a better and more sustainable future for all. It includes 17 goals to address the world's most pressing challenges, including poverty, inequality, climate change, environmental degradation, peace, and justice.

Electronic systems play a pivotal role in modern society, acting as the backbone for smart infrastructure, healthcare monitoring, and environmental sensing. However, the massive deployment of battery-operated devices poses a significant challenge regarding energy consumption and electronic waste. This dissertation contributes directly to the efficiency and sustainability of these systems.

The specific Sustainable Development Goals addressed by this work are:

SDG 7 Affordable and Clean Energy: Ensure access to affordable, reliable, sustainable and modern energy for all. By optimizing the power consumption of data converters, we extend the battery life of devices and reduce the overall energy footprint of IoT networks.

SDG 9 Industry, Innovation and Infrastructure: Build resilient infrastructure, promote inclusive and sustainable industrialization and foster innovation. This work advances the state-of-the-art in microelectronics by proposing novel asynchronous architectures that enable smarter and more efficient industrial sensors.

SDG	**Target**	**Contribution**	**Performance Indicators and Metrics**
7	7.3	By double the global rate of improvement in energy efficiency, this work reduces the power waste in standby modes of electronic sensors.	Reduction in Energy per Conversion (fJ/conv) compared to synchronous architectures.
	7.a	Facilitate access to clean energy research and technology, including energy efficiency and advanced and cleaner fossil-fuel technology.	Development of ultra-low-power IP blocks for energy-harvesting systems.
9	9.5	Enhance scientific research, upgrade the technological capabilities of industrial sectors, encouraging innovation.	Successful validation of the proposed calibration algorithm and circuit topology.

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“Our greatest glory is not in never falling, but in rising every time we fall”

Confucius

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List of Acronyms

ADT	Abstract Data Type
ANDF	Architecture-Neutral Distribution Format
API	Application Programming Interface
CAD	Computer-Aided Design
CASE	Computer-Aided Software Engineering
CORBA	Common Object Request Broker Architecture
UNCOL	UNiversal COmpiler-oriented Language
Loren	Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Sed vehicula lorem commodo dui
WWW	*World Wide Web*

Chapter 1

Introduction

This chapter introduces the research topic, establishing the context of analog-to-digital conversion in modern electronic systems and defining the motivation for investigating asynchronous architectures.

1.1 Context

1.2 Motivation and Problem Statement

1.3 Objectives and Contribution

Chapter 2

Literature Review

This chapter presents the state-of-the-art in Analog-to-Digital Converters, reviewing theoretical foundations and analyzing survey data to justify the proposed architecture.

2.1 Fundamentals of Analog-to-Digital Conversion

This section provides the theoretical background required to understand the operation and performance characterization of data converters. It covers the fundamental steps of the conversion process—sampling, quantization, and coding—and details the metrics used to evaluate both static and dynamic performance, which serve as a universal baseline for any ADC architecture.

2.1.1 The Data Conversion Process

2.1.1.1 Ideal Data Conversion

The analog-to-digital conversion process acts as the bridge between the continuous physical world and the discrete digital domain. Conceptually, it involves two distinct operations: discretization in time (sampling) and discretization in amplitude (quantization). Ideally, this process should be instantaneous and lossless within the signal bandwidth of interest.

2.1.1.2 The Sampling Operation

Sampling converts a continuous-time signal $x(t)$ into a discrete-time sequence $x[n]$. Mathematically, this is modeled as the multiplication of the input signal by a periodic train of Dirac delta functions with period T_s.

[Image of sampling theorem time frequency domain]

Sampling Theorem: According to the Nyquist-Shannon sampling theorem, a band-limited signal with maximum frequency B can be perfectly reconstructed if the sampling frequency f_s satisfies:

$$f_s \geq 2B \tag{2.1}$$

Violating this condition results in *aliasing*, where high-frequency spectral components fold back into the baseband, becoming indistinguishable from the original signal.

Sampling of Bandpass Signals: For signals centered at a high intermediate frequency (f_{IF}) but with a narrow bandwidth ($B \ll f_{IF}$), direct baseband sampling is inefficient. Bandpass sampling (or undersampling) allows the use of $f_s < 2f_{IF}$, provided that $f_s > 2B$ and the spectral replicas do not overlap.

2.1.1.3 The Reconstruction Operation

Reconstruction is the inverse operation, converting the digital sequence back into a continuous signal. In an ideal scenario, this corresponds to convolving the discrete samples with a sinc function (ideal low-pass filter), which perfectly removes the spectral images generated during sampling, leaving only the original baseband content.

2.1.1.4 The Quantization Operation

While sampling discretizes time, quantization maps the continuous amplitude of each sample to one of a finite number of levels. An N-bit ADC divides the input range (V_{ref}) into 2^N discrete levels. The step size between adjacent levels is the Least Significant Bit (LSB):

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{2.2}$$

Unlike sampling, quantization is non-reversible and introduces a deterministic error. This error is typically modeled as additive white noise (*quantization noise*) with a uniform probability distribution. For an ideal quantizer, the Signal-to-Quantization-Noise Ratio (SQNR) is given by the well-known formula:

$$SQNR_{dB} \approx 6.02N + 1.76 \tag{2.3}$$

2.1.1.5 Coding

The final stage is encoding the quantized level into a binary format. The choice of coding scheme (e.g., straight binary, two's complement, Gray code) depends on the system requirements for data processing and transmission, but does not affect the fundamental analog performance.

2.1.1.6 Undersampling and Oversampling

- **Undersampling:** Intentionally violates the Nyquist criterion for the carrier frequency to down-convert RF signals directly.
- **Oversampling:** Involves sampling at a rate much higher than the Nyquist rate ($f_s \gg 2B$). This technique spreads the fixed quantization noise power over a wider frequency range. A subsequent digital filter can then remove the out-of-band noise, effectively increasing the SNR and resolution beyond the intrinsic bit-depth of the hardware.

2.1.1.7 Decimation and Interpolation

- **Decimation:** Reduces the sampling rate of an oversampled signal by filtering and down-sampling, trading speed for resolution.
- **Interpolation:** Increases the effective sampling rate in the digital domain (zero-stuffing and filtering), often used in DACs to relax the requirements of the analog reconstruction filter.

2.1.2 Performance Metrics

To evaluate and compare different data converters objectively, a standard set of metrics is used. These are categorized into dynamic and static parameters.

2.1.2.1 Resolution and Sampling Rate

Resolution defines the theoretical dynamic range, while the sampling rate determines the maximum signal bandwidth. However, these are nominal values; real-world performance is limited by noise and non-linearities.

2.1.2.2 Signal-to-Noise-and-Distortion Ratio (SNDR)

SNDR (or SINAD) is the primary dynamic metric. It is the ratio of the signal power to the total power of all noise and harmonic distortion components. From SNDR, the Effective Number of Bits (ENOB) is derived:

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \tag{2.4}$$

This value represents the true resolution of the converter at a specific input frequency.

2.1.2.3 Spurious-Free Dynamic Range (SFDR)

SFDR is defined as the ratio between the fundamental signal power and the power of the largest spurious component in the spectrum (typically a harmonic). A high SFDR is crucial in communication systems to detect small signals in the presence of strong interferers.

2.1.2.4 Harmonic Distortion (HD) and IMD

- **HD2/HD3:** The second and third harmonic distortions quantify the linearity of the transfer function. Differential signaling is commonly employed to suppress even-order harmonics (HD2).
- **Inter-Modulation Distortion (IMD):** When two tones are present, system non-linearities generate sum and difference frequencies (intermodulation products). Third-order products ($2f_1 - f_2$) are particularly troublesome as they often fall near the fundamental tones.

2.1.2.5 Differential and Integral Non-Linearity (DNL and INL)

Static linearity is characterized by measuring the deviation of code transition levels from their ideal positions.

- **DNL:** Measures the deviation of a single step width from the ideal $1LSB$. A DNL less than -1 LSB implies a missing code in the transfer function.
- **INL:** Is the cumulative sum of DNL errors, representing the deviation of the transfer curve from a straight line. Specific INL patterns (like "S-curves" or "saw-tooth" shapes) can reveal systematic errors in the architecture, such as gain mismatch or non-linear biasing.

2.1.2.6 Offset and Gain Error

These are linear errors. Offset is a constant shift of the transfer characteristic, while gain error is a deviation in the slope. Unlike non-linearity, these errors preserve the signal shape and can often be calibrated out simply.

2.1.2.7 Jitter

Jitter refers to the short-term variation in the sampling instants. It introduces phase noise and limits the maximum achievable SNR, especially for high-frequency input signals. The SNR limitation due to jitter is independent of resolution and is given by:

$$SNR_{jitter} = -20\log(2\pi f_{in}\sigma_t) \tag{2.5}$$

2.1.2.8 Bit Error Rate (BER)

BER quantifies the probability of the converter producing an incorrect digital code. This is often caused by metastability, a phenomenon where internal decision circuits fail to resolve a valid logic level within the allocated time when the input is extremely close to a decision threshold.

2.2 Synchronous Architectures

2.3 Asynchronous Architectures

2.4 Calibration and Trimming Techniques

In high-speed Flash ADCs, the accuracy of the system is fundamentally limited by the precision of the comparators. While the architecture fundamentals were established in the previous sections, practical implementations must address the non-idealities of the fabrication process, specifically the Input Offset Voltage (V_{os}).

2.4.1 The Component Mismatch Problem

In deep sub-micron CMOS technologies, transistors that are drawn with identical dimensions on the layout will exhibit slight differences in their electrical parameters after fabrication. This phenomenon, known as **mismatch**, affects the threshold voltage (V_{th}) and the current gain factor (β) of the differential pair in a comparator.

According to Pelgrom's Law [**johns_martin_analog**], the standard deviation of the threshold voltage mismatch (σ_{Vth}) is inversely proportional to the square root of the transistor area ($W \cdot L$):

$$\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{W \cdot L}} \tag{2.6}$$

Where $A_{V_{th}}$ is a technology-dependent constant. This creates a critical trade-off: to minimize offset without calibration, transistors must be made very large, which increases parasitic capacitance and drastically degrades the ADC speed and power efficiency. Therefore, small transistors are used for speed, and calibration is employed to correct the resulting offset.

2.4.2 Calibration Classifications

Calibration techniques can be broadly categorized by their timing and domain:

- **Timing:** *Foreground* (Offline) calibration interrupts normal operation to measure and correct errors, while *Background* (Online) calibration operates continuously but adds significant complexity.
- **Domain:** *Digital* calibration corrects the output code mathematically, whereas *Analog* calibration adjusts the circuit biasing or load conditions to nullify the offset at the source.

For an asynchronous architecture, avoiding continuous clock activity is crucial to maintain low power during idle periods. Thus, **Analog Foreground Calibration** (Trimming) is the preferred approach.

2.4.3 Resistive Trimming Techniques

Resistive trimming aims to compensate for the imbalance in the input differential pair (M_1, M_2) by intentionally creating an opposing imbalance in the load resistance or the reference path.

2.4.3.1 Internal Resistive Loading

This method involves placing a variable resistive network in parallel (or series) with the output loads of the comparator's pre-amplifier stage.

- **Mechanism:** By digitally switching small resistors (or MOS switches operating in the triode region) in parallel with the load branch, the effective resistance R_L is modulated.

- **Effect:** Since the gain of the pre-amplifier is $A_v = g_m R_L$, changing R_L on one side adjusts the output DC level. If the differential pair has an offset $+\Delta V$, the trimming network is adjusted to introduce $-\Delta V$, effectively zeroing the error.

- **Implementation:** A binary-weighted bank of PMOS transistors is typically used as the variable resistance. The digital code to control these switches is determined at startup and stored in a register.

2.4.3.2 Reference Ladder Trimming

Alternatively, instead of modifying the comparator internally, the reference voltages (V_{ref}) supplied to the comparators can be adjusted.

- **Mechanism:** The main resistive reference ladder is tapped using a local switching network that allows fine-tuning of the tap voltage connected to each comparator input.

- **Context:** This technique was successfully demonstrated in asynchronous Flash ADCs, such as in the work of Chen et al. [**chen_async_2006**], where the reference ladder itself acts as the calibration DAC.

2.4.4 Advantages of Resistive Trimming for Asynchronous ADCs

Compared to dynamic techniques like Auto-Zeroing (which requires accurate clock phases ϕ_1, ϕ_2 and storage capacitors), resistive trimming offers distinct advantages for the proposed work:

1. **Static Operation:** Once the calibration bits are set (during the offline phase), the trimming network becomes static. It does not switch and does not require a clock, preserving the "event-driven" nature of the ADC.

2. **No Switching Noise:** Since the calibration is constant during conversion, it introduces no injection noise or clock feedthrough.

3. **Speed Preservation:** It does not add significant capacitive load to the high-speed nodes of the comparator, allowing for maximum bandwidth.

2.5 Summary

Chapter 3

Future Work Planning, Methodologies and Tools

This chapter outlines the development strategy for the dissertation, detailing the methodologies, tools, and the schedule for the remaining phases.

3.1 Methodologies and Tools

3.2 Work Plan

Chapter 4

Conclusions

This document presented the preparatory work for the design of an Asynchronous Flash ADC with calibration. The literature review confirmed that asynchronous architectures offer superior energy efficiency for sparse signal processing, validating the research direction. The identified challenge of comparator offset will be addressed through the proposed trimming methodology, as outlined in the work plan.

Chapter 5

Apendix

After the conclusions and bibliographical references, the text used to complete the dissertation is presented in this numbered annex.