FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Design of an Asynchronous Flash Analog-to-Digital Converter

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Abstract

The proliferation of Internet of Things and biomedical sensors has created a high demand for low-power signal processing interfaces. In many of these applications, the signals of interest are sparse, characterized by long periods of inactivity. Classical synchronous Analog-to-Digital Converters are inherently inefficient in such scenarios, as they consume dynamic power continuously due to the global clock, regardless of the input signal activity.

This dissertation proposes the design and implementation of an Asynchronous Flash ADC. By removing the clock, the proposed architecture aligns power consumption with the input signal activity, theoretically achieving a much lower power consuption. However, the removal of the clock introduces design challenges (acrescentar aqui problemas)

To address this, an offline trimming strategy is proposed to calibrate the comparator offsets without compromising the high-speed operation of the flash topology. The work encompasses the theoretical analysis, schematic design, and validation of the system through Analog/Mixed-Signal co-simulation. The expected outcome is a robust, clockless ADC architecture that offers a superior Figure of Merit for sparse signal applications in compared to conventional synchronous architectures.

Keywords: Analog-to-Digital Converter, Asynchronous Design, Flash ADC, Level-Crossing Sampling, Offset Trimming, Low Power, IoT.

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Chapter 1

Introduction

This chapter provides a brief introduction to the topic associated with the work carried out during the dissertation period. Firstly, a contextualization is given, followed by a presentation of the research question and the main motivations for carrying out this study. The main objectives of this dissertation will also be outlined, as well as the methodology used to achieve them. Finally, the structure of the dissertation is presented.

We live in an era where smart devices are everywhere, known as the Internet of Things, IoT. While the processing and storage of information are inherently digital, benefiting from the scaling of Moore's Law, the physical world remains fundamentally analogic. Physical variables such as temperature, sound and biological potentials are continuous in both time and amplitude. Consequently, the Analog-to-Digital Converter, ADC, serves as the critical interface bridging these two domains, enabling digital systems to interact with the real world [15].

Energy efficiency has shifted from being a secondary performance metric to a primary design constraint, many of the sensors operate on limited battery or rely on energy harvesting, where every Joule of power dissipation has a direct effect on the system's autonomy. In this landscape, the data conversion block almost always takes place as the most spender in this field, especially in sensor interfaces where the digital transmission is duty-cycled.

However, a fundamental characteristic of many environmental and physiological signals is sparsity in between pulses. Signals such as electrocardiograms, voice activity, or environmental monitoring data are spread in bursts in nature: they contain short periods of high information content followed by long intervals of inactivity.

Traditional data conversion approaches, based on uniform sampling and dictated by the Nyquist-Shannon theorem [26], treat these silence periods with the same computational power and energetic waste as the active periods. This creates a paradigm of inefficiency the system dissipates power to generate redundant digital samples that carry no new information. Recognizing and exploiting this sparsity is the key to unlocking ultra-low-power electronic interfaces.

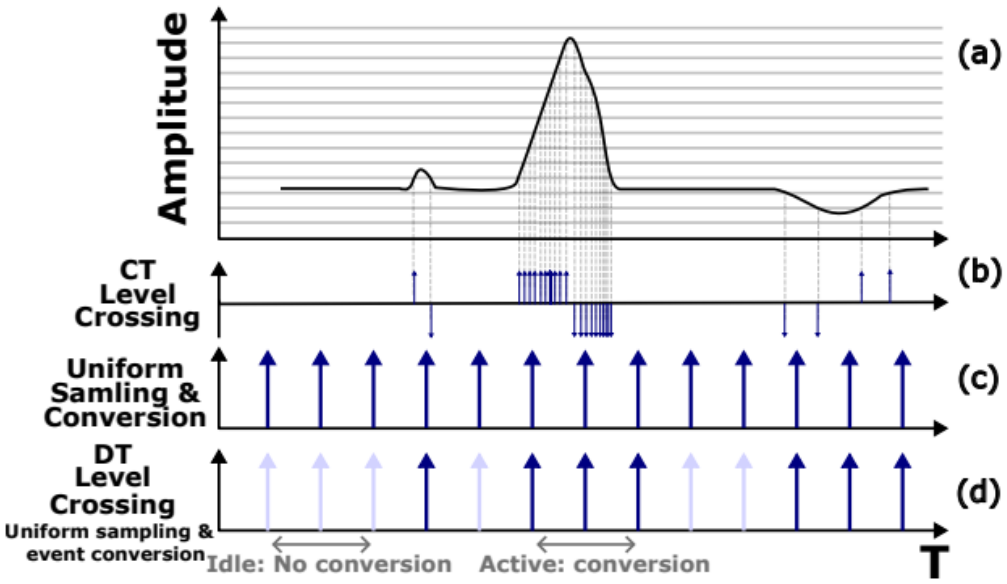

Figure 1.1: Time-sparse signal representation and sampling strategies. (a) Time-sparse signal example showing burst activity with periods of inactivity. (b) Continuous-time event-driven sampling and conversion, which responds to signal changes. (c) Conventional uniform sampling operating at fixed Nyquist rate regardless of signal activity. (d) Discrete-time sampling with event-driven conversion, combining periodic and event-based approaches. This illustration demonstrates the efficiency of adaptive sampling methods for sparse signals compared to uniform sampling at the Nyquist rate [17].

1.1 Motivation and Problem Statement

The energy waste in massive-scale IoT deployments and the inefficiency of conventional synchronous architectures when processing sparse data shows the need for a fundamental shift toward architectures that activate only when meaningful data events occur.

1.1.1 Inefficiency of Synchronous Sampling

Traditional Analog-to-Digital Converters operate under a fixed-rate sampling rate, dictated by a global clock signal (f_s). As established by the Nyquist-Shannon sampling theorem [26], this rate is determined by the maximum possible bandwidth of the signal, $f_s \geq 2B$. However, in many real-world applications, the signal is often active for only a fraction of the time, meaning the true information content is much lower than the theoretical maximum bandwidth suggests.

This leads to a massive waste of energy due to the fundamental relationship governing dynamic power consumption in CMOS circuits [2]:

$$P_{dynamic} = \alpha \cdot f \cdot C_L \cdot V_{DD}^2 \tag{1.1}$$

where:

- $P_{dynamic}$ is the dynamic power dissipated.
- α is the activity factor (or switching factor).
- f is the clock frequency.
- C_L is the load capacitance being switched (e.g., in the clock tree).

1.1.2 Architectural Problem: Flash ADCs

While the Flash ADC architecture is highly attractive due to its single-cycle, high-speed conversion capability [15], it suffers from severe limitations regarding power and area, particularly when reaching medium-to-high resolution. The number of required comparators scales exponentially with resolution (2^N). This exponential scaling leads directly to an increase in input capacitance and static power dissipation.

Even in low-power, synchronous designs, the dynamic power of the comparator switching is the dominant factor in the power budget.

Therefore, combining the high speed of the Flash architecture with the high power efficiency required for IoT demands a radical shift away from the synchronous clocking scheme.

1.1.3 Device Limitation: The Mismatch Problem

To mitigate the power and area issues mentioned above, designers are compelled to minimize the physical dimensions of the core devices, particularly the transistors within the comparators. However, this introduces a fundamental physical constraint:

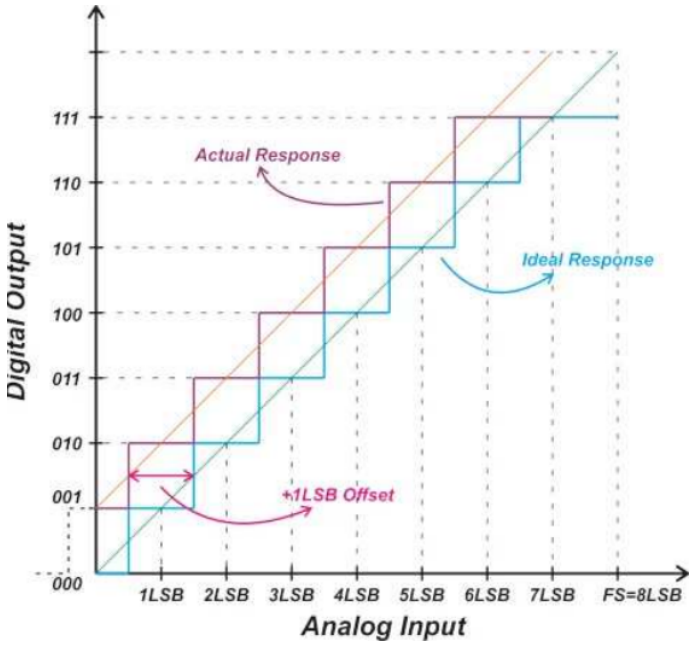

Figure 1.2: Input offset voltage (V_{os}) generation in CMOS comparators due to transistor mismatch. The figure illustrates how random variations in threshold voltage (V_{th}) and gain factor (β) in the differential input pair result in an offset voltage that shifts the trip point of the comparator [15]. This mismatch-induced offset becomes the primary limitation for converter accuracy in deep-submicron technologies.

The reduction of transistor size, while increasing speed and reducing capacitance, drastically increases random variations in parameters like the threshold voltage (V_{th}), leading to a significant Input Offset Voltage (V_{os}) in the comparators [2].

1.2 Objectives and Contribution

Based on the limitations identified in traditional synchronous data conversion when dealing with sparse sensor signals, the primary objective of this work is to design and implement an energy-efficient ADC architecture, so this ADC must exploit signal inactivity to achieve a significant reduction in power consumption.

1.2.1 Specific Objectives

To achieve the overall goal of developing an efficient ADC, the following specific objectives are defined for this dissertation:

1. Asynchronous Architecture Design: To develop the circuit-level design of an asynchronous Flash ADC, minimizing dynamic power consumption by ensuring that power is only dissipated when an input signal event occurs.

2. Offline Trimming Implementation: To implement an offline trimming mechanism capable of detecting and compensating for the input offset voltage of the comparators.

3. Mixed-Signal Validation: To validate the complete system through analog and digital co-simulation. This validation must confirm the functionality and accuracy of both the asynchronous core and the trimming logic.

4. Performance Benchmarking: To quantify the energy efficiency of the proposed design using well known figures of merit. The results must be compared against the current state of the art synchronous ADCs and relevant asynchronous solutions.

Chapter 2

Literature Review

This chapter presents the state-of-the-art in Analog-to-Digital Converters, reviewing theoretical foundations and analyzing survey data to justify the proposed architecture.

2.1 Fundamentals of Analog-to-Digital Conversion

This section provides the theoretical background required to understand the operation and performance characterization of data converters. It covers the fundamental steps of the conversion process such as sampling, quantization, and coding.

2.1.1 The Data Conversion Process

2.1.1.1 Ideal Data Conversion

The analog-to-digital conversion process acts as the bridge between the continuous physical world and the discrete digital domain. Conceptually, it involves two distinct operations: discretization in time, sampling, and discretization in amplitude, quantization. Ideally, this process should be instantaneous and lossless within the signal bandwidth of interest [15].

2.1.1.2 The Sampling Operation

Sampling converts a continuous-time signal $x(t)$ into a discrete-time sequence $x[n]$ [15].

According to the Nyquist-Shannon sampling theorem [26], a band-limited signal with maximum frequency B can be perfectly reconstructed if the sampling frequency f_s satisfies:

$$f_s \geq 2B \tag{2.1}$$

Violating this condition results in aliasing, where high-frequency spectral components mixes into the baseband, becoming indistinguishable from the original signal [15].

2.1.1.3 The Quantization Operation

While sampling transforms continuous time in discrete values, quantization maps the continuous amplitude of each sample to one of a finite number of levels [15]. An N-bit ADC divides the input range (V_{ref}) into 2^N discrete levels. The step size between adjacent levels is the Least Significant Bit (LSB):

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{2.2}$$

Unlike sampling, quantization is non-reversible and introduces a deterministic error. This error is typically modeled as white noise added, the quantization noise with a uniform probability distribution. For an ideal quantizer, the Signal-to-Quantization-Noise Ratio (SQNR) is given by the formula [15]:

$$SQNR_{dB} \approx 6.02N + 1.76 \tag{2.3}$$

2.1.1.4 Coding

The final stage is encoding the quantized level into a binary format. The choice of coding scheme being the most common straight binary and gray code which depends on the system requirements for data processing and transmission, but does not affect the fundamental analog performance [2].

2.1.2 Performance Metrics

To evaluate and compare different data converters objectively, a standard set of metrics is used [15]. These are categorized into dynamic and static parameters.

2.1.2.1 Resolution and Sampling Rate

Resolution defines the theoretical dynamic range, while the sampling rate determines the maximum signal bandwidth. However, these are nominal values the actual performance is limited by noise and non-linearities [15].

2.1.2.2 Signal-to-Noise-Distortion Ratio (SNDR)

Signal to noise ratio adding distortion ratio or SNDR is the primary dynamic metric [15]. It is the ratio of the signal power to the total power of all noise and harmonic distortion components. From SNDR, the Effective Number of Bits, ENOB, is derived [15]:

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \tag{2.4}$$

This value represents the true resolution of the converter at a specific input frequency.

2.1.2.3 Differential and Integral Non-Linearity (DNL and INL)

Static linearity is characterized by measuring the deviation of code transition levels from their ideal positions [15]. The DNL measures the deviation of a single step width from the ideal 1 LSB. A DNL less than -1 LSB implies a missing code in the transfer function.

The INL is the cumulative sum of DNL errors, representing the deviation of the transfer curve from a straight line. Specific INL patterns like saw-tooth shapes can reveal systematic errors in the architecture, such as gain mismatch or non-linear biasing [22].

2.1.2.4 Offset and Gain Error

These are linear errors, offset is a constant shift of the transfer characteristic as seen before in section 1.2.3, while gain error is a deviation in the slope [15]. Unlike non-linearity, these errors preserve the signal shape and can often be calibrated out simply.

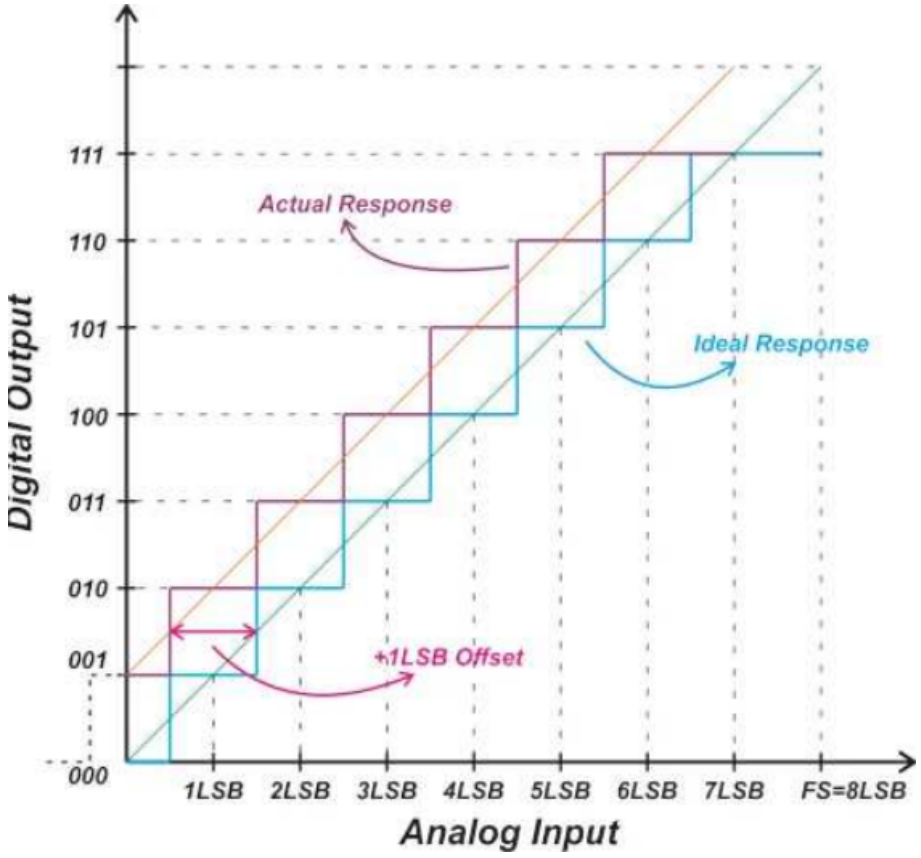

Figure 2.1: ADC transfer function showing offset and gain errors. Offset error represents a constant DC shift applied uniformly across all codes, while gain error modifies the slope of the transfer function. Both are linear errors that can be calibrated using digital post-processing techniques [15].

2.1.2.5 Bit Error Rate (BER)

BER quantifies the probability of the converter producing an incorrect digital code [2]. This is often caused by metastability, a phenomenon where internal decision circuits fail to resolve a valid logic level within the allocated time when the input is extremely close to a decision threshold.

2.1.3 State-of-the-Art Comparative Analysis

The performance benchmarks and comparative trends presented in this section were derived from a comprehensive survey of the IEEE International Solid-State Circuits Conference (ISSCC) data from 1997 to 2022. The ISSCC was chosen as the primary data source because it is widely regarded as the premier forum for solid-state circuit design, requiring experimental silicon-measured results for every publication. This ensures that the comparison is based on proven hardware rather than theoretical simulations.

The analytical plots and tables presented below incorporate data from an exhaustive list of state-of-the-art works. The comparative baseline for Flash architectures is established by [4, 7, 19]. The boundaries for energy efficiency and high-resolution performance (the "survey envelopes") are defined by the record-holders described in [5, 9, 12, 14, 16, 20, 28] for power efficiency, and [1, 6, 8, 13] for high resolution and dynamic range. Collectively, these references [1, 4–9, 12–14, 16, 19, 20, 28] represent the performance frontier across all major ADC architectures.

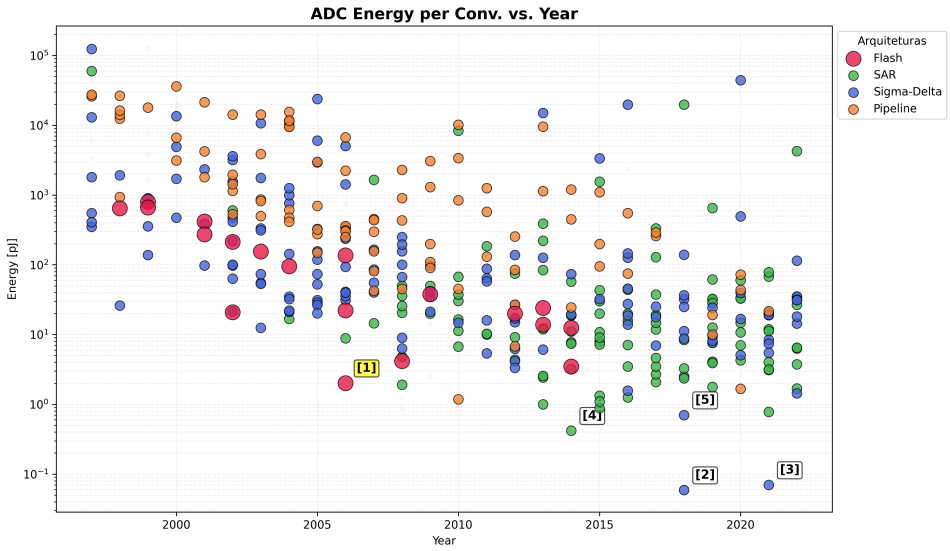

Figure 2.2: Energy per conversion step vs. Year of publication (ISSCC dataset).

Table 2.1: Energy per Conversion vs. Year (Flash reference [1] highlighted)

Ref.	Architecture	Publication	Energy [pJ]
[1]	**Flash**	**Chen [4]**	**2.02**
[2]	Sigma-Delta	Jiang [14]	0.059
[3]	Sigma-Delta	Veldhoven [28]	0.070
[4]	SAR	Ginsburg [9]	0.420
[5]	Sigma-Delta	Kim [16]	0.703

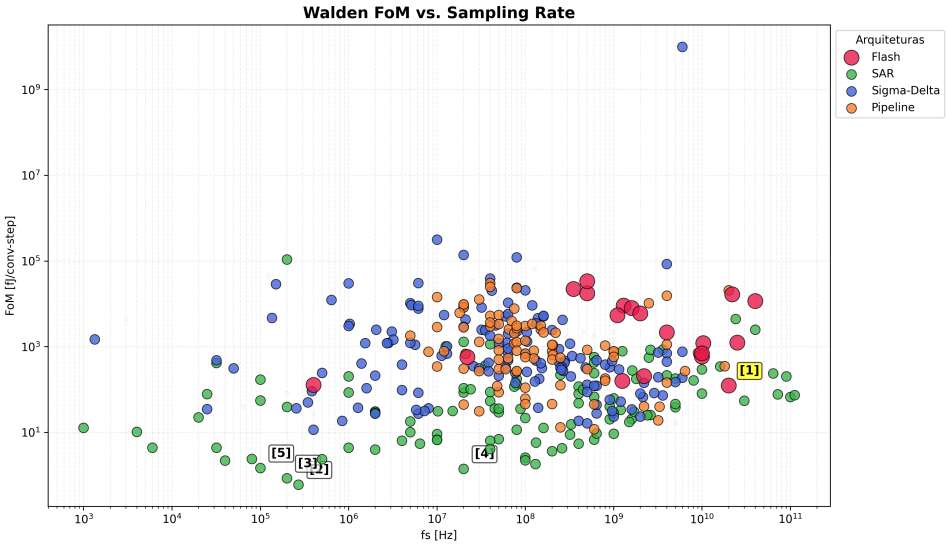

Figure 2.3: Walden FoM vs. Sampling Rate (f_s).

2.2 Synchronous Architectures

To address asynchronous ADCs we first need to address synchronous ADCs, they have a global clock signal that dictates sampling instances and synchronizes internal operations. While these

Table 2.2: Walden FoM vs. Sampling Frequency (Flash reference [1] highlighted)

Ref.	Architecture	Publication	f_s [Hz]
[1]	**Flash**	**Lukas [19]**	**20G**
[2]	SAR	Jang [12]	270k
[3]	SAR	Ginsburg [9]	200k
[4]	SAR	Cano [5]	20M
[5]	SAR	Muller [20]	200

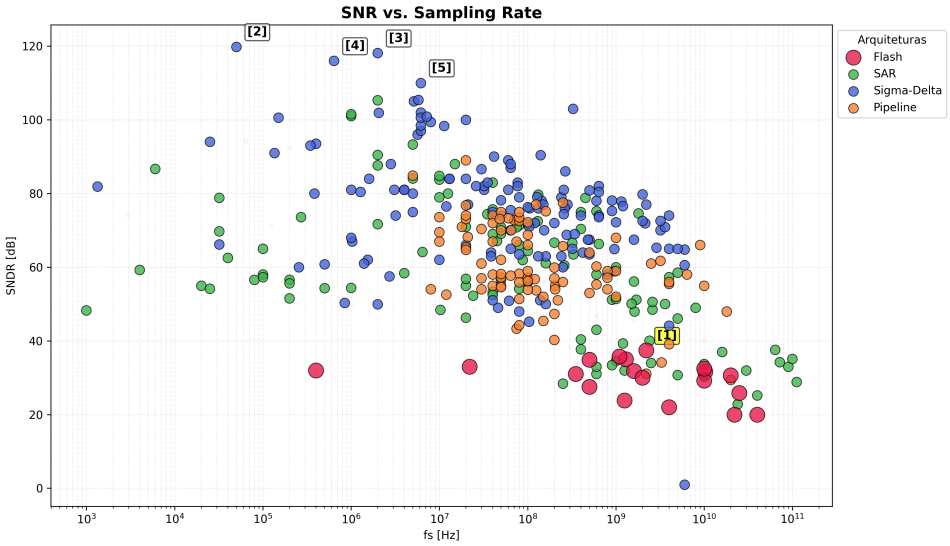

Figure 2.4: SNDR vs. Sampling Frequency (f_s) comparison.

Table 2.3: SNDR vs. Sampling Frequency (Flash reference [1] highlighted)

Ref.	Architecture	Publication	SNDR [dB]
[1]	**Flash**	**Draxelmayr [7]**	**37.4**
[2]	Sigma-Delta	Delic [6]	120.0
[3]	Sigma-Delta	Jang [13]	118.0
[4]	Sigma-Delta	Abe [1]	116.0
[5]	Sigma-Delta	Geelen [8]	110.0

architectures are highly mature and widely used, they face fundamental power efficiency trade-offs, particularly when operating at high frequencies or processing sparse data [15].

2.2.1 Synchronous Flash ADC

The Flash ADC is conceptually the simplest and fastest architecture, performing a complete conversion in a single clock cycle [2]. It utilizes a resistive ladder to generate $2^N - 1$ reference voltages, which are compared simultaneously to the input signal by a large bank of comparators. This parallel comparison produces a thermometer code, that a digital logic block then converts into a standard binary output. Its primary limitation is the exponential increase in hardware complexity, area, and power consumption as resolution increases.

The thermometer term refers to the parallel output from the Flash ADC comparators, where '1's run up to the input voltage level like mercury in a thermometer, indicating signal strength before being converted to standard binary by an encoder.

2.2.2 The Power Bottleneck

The primary drawback of the synchronous Flash architecture is its exponential scaling. Survey data clearly illustrates that high speed translates into high power in these designs. For example, a 6-bit 500 MS/s CMOS Flash ADC reported in 1999 already consumed 400 mW [27].

More extreme cases, such as a 22 GS/s 5-bit design, can consume up to 1.2 W [25].

The continuous clocking of a massive comparator bank creates a significant energy dissipation even when the input signal is static. This lack of adaptivity makes synchronous Flash architectures increasingly unsuitable for battery-powered or energy-harvesting applications.

2.2.3 SAR (Successive Approximation Register)

The SAR ADC operates using a binary search algorithm [22], for each sample the internal logic tests one bit at a time, starting from the most significant bit (MSB). A single comparator compares the input to the output of an internal digital to analog converter (DAC), if the input is higher, the bit is set to '1' otherwise, it is set to '0'. This process repeats for N cycles. Because it uses very few active components, it is the most energy efficient choice for low speeds.

2.2.4 Pipeline

The Pipeline ADC breaks the conversion into several sequential stages [15], each stage resolves a few bits of information, quantizes them, and passes the remaining error, the residue, to the next stage after amplification. This approach allows the ADC to work on multiple samples concurrently, obtaining very high throughput and high resolution, the problem relies in the inherent processing latency.

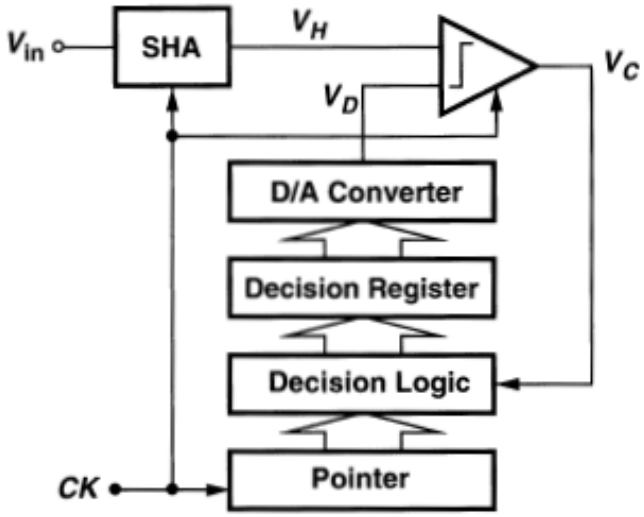

Figure 2.5: Successive Approximation Register (SAR) ADC architecture showing the binary search algorithm implementation. The architecture consists of a DAC, a single comparator, and binary search logic that successively tests each bit from MSB to LSB, resulting in N clock cycles for an N-bit conversion. The main advantage is energy efficiency due to the use of a single comparator and minimal active circuitry [22].

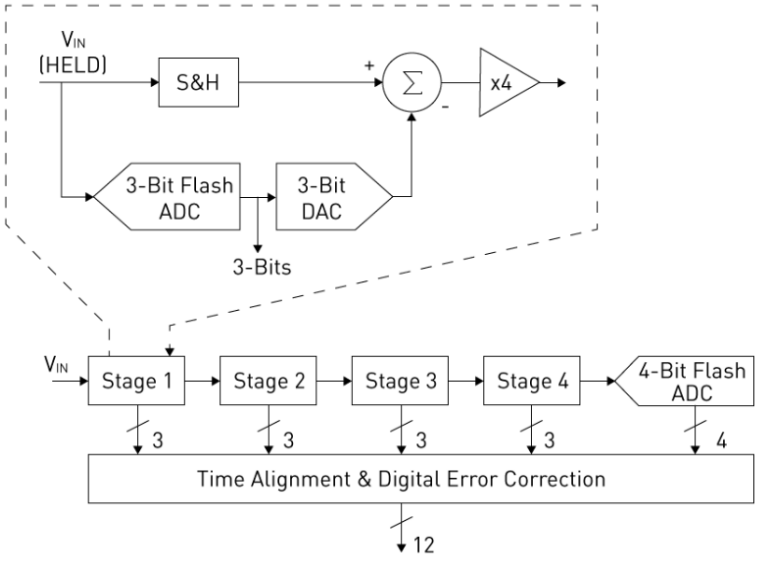

Figure 2.6: Pipeline ADC architecture showing multiple conversion stages operating in parallel on different input samples. Each stage resolves a portion of the bits and amplifies the residual error to the next stage. The pipelined structure enables high-throughput operation at the expense of increased latency and circuit complexity [15].

2.2.5 Sigma-Delta (ΣΔ)

The ΣΔ architecture relies on oversampling, sampling much faster than the Nyquist rate [3], and noise-modulation. A modulator integrates the difference between the input signal and a feedback version of the quantized output. This process pushes the quantization noise into higher frequencies, outside the signal band of interest, a digital filter then removes the high-frequency noise, resulting in high resolution and precision [24].

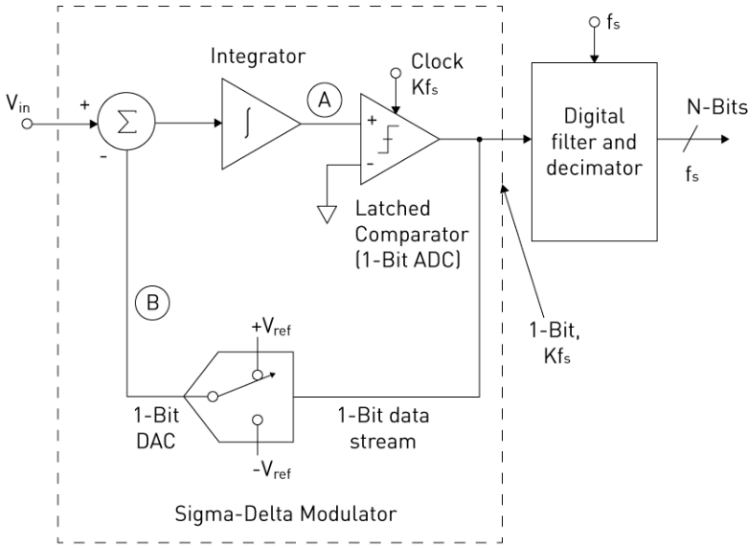

Figure 2.7: First-order Sigma-Delta modulator architecture showing the integrator, quantizer, and feedback path. The modulator operates at a clock frequency much higher than the Nyquist rate, and the quantization noise is shaped to frequencies outside the signal band, allowing digital filtering to recover high-resolution signals [3].

2.2.6 Dual-slope

This integrating architecture [23] measures the time required for a capacitor to charge and discharge, in the first phase, the capacitor is charged by the input voltage for a fixed period then for the second phase, it is discharged by a known reference voltage. The time it takes to return to zero is proportional to the average value of the input signal it's highly accurate and immune to high-frequency noise but is much slower than other architectures.

2.3 Asynchronous Architectures

Asynchronous, or event-driven, architectures represent a fundamental paradigm shift in data conversion [17], unlike synchronous ADCs, which are bound by a global clock and the Nyquist-Shannon sampling theorem, asynchronous ADCs operate based on the signal's activity. This approach offers a more efficient alternative for processing sparse signals.

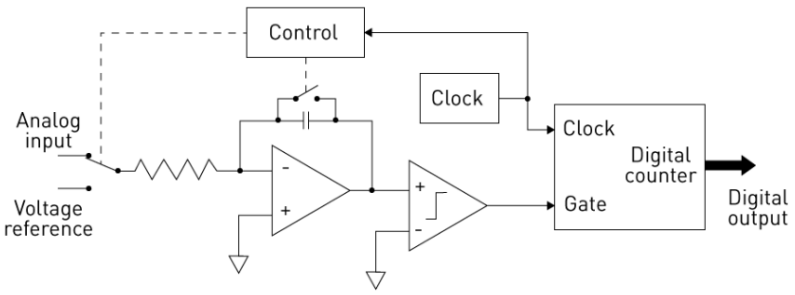

Figure 2.8: Dual-slope (integrating) ADC architecture showing the charging phase where an unknown input signal is integrated for a fixed time, and the discharge phase where a precise reference voltage drives the capacitor back to zero. The conversion time is proportional to the input voltage, providing excellent accuracy and noise rejection at the expense of low throughput [23].

2.3.1 Level-Crossing Sampling (LCS)

The core principle behind many asynchronous ADCs is Level-Crossing Sampling (LCS) [17]. In traditional uniform sampling, the signal is captured at fixed time intervals (T_s), and the amplitude is quantized. In LCS, the process is inverted: the amplitude levels are fixed (quantization thresholds), and the ADC records the exact time at which the input signal crosses these thresholds.

This method is particularly powerful for signals that remain constant or change slowly over long periods. Instead of generating redundant samples that capture no new information, the LCS ADC remains idle, only producing a digital event when the signal effectively changes by more than the defined threshold.

2.3.2 Asynchronous Flash ADC

The Asynchronous Flash ADC adapts the parallel structure of a standard Flash ADC but removes the sampling clock entirely. In this architecture, the comparators are not latched by a clock, they operate in continuous time, constantly monitoring the input voltage V_{in} against the reference ladder. The event generation happens when the input signal crosses a threshold, the corresponding comparator changes its output state immediately, this transition triggers an asynchronous logic to generate a digital output pulse.

2.4 Calibration and Trimming Techniques

In high-speed Flash ADCs, the accuracy of the system is fundamentally limited by the precision of the comparators. While the architecture fundamentals were established in the previous sections, practical implementations must address the non-idealities of the fabrication process, specifically the Input Offset Voltage (V_{os}).

2.4.1 The Component Mismatch Problem

In deep sub-micron CMOS technologies, transistors that are drawn with identical dimensions on the layout will exhibit slight differences in their electrical parameters after fabrication. This phenomenon, known as mismatch, affects the threshold voltage (V_{th}) and the current gain factor (β) of the differential pair in a comparator [2].

According to Pelgrom's Law cited in section 2.3.3 of [15], the standard deviation of the threshold voltage mismatch (σ_{Vth}) is inversely proportional to the square root of the transistor area ($W \cdot L$):

$$\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{W \cdot L}} \tag{2.5}$$

Where $A_{V_{th}}$ is a technology-dependent constant. This creates a critical trade-off, to minimize offset without calibration, transistors must be made large, which increases parasitic capacitance and degrades the ADC speed and power efficiency. Therefore, small transistors are used for speed, and calibration is needed to correct the resulting offset.

2.4.2 Calibration Classifications

Calibration techniques can be broadly categorized by their timing and domain [2]. In terms of timing there can be derived two types foreground calibration which interrupts normal operation to measure and correct errors and background calibration which operates continuously but adds significant complexity. In terms of domain there is digital calibration that corrects the output code mathematically, whereas analog calibration adjusts the circuit biasing or load conditions to nullify the offset at the source.

For an asynchronous architecture, avoiding continuous clock activity is crucial to maintain low power during idle periods. Thus, Analog Foreground Calibration is the preferred approach.

2.4.3 Resistive Trimming Techniques

Resistive trimming aims to compensate for the imbalance in the input differential pair (M_1, M_2) by intentionally creating an opposing imbalance in the load resistance or the reference path [2].

2.4.3.1 Internal Resistive Loading

The internal resistive loading method involves placing a variable resistive network in parallel or series with the output loads of the comparator pre-amplifier stage. By digitally switching small resistors or MOS switches operating in the triode region in parallel with the load branch, the effective resistance R_L is modulated. Since the gain of the pre-amplifier is defined as $A_v = g_m R_L$, changing R_L on one side of the differential pair adjusts the output DC level. If the differential pair has an offset, the trimming network is adjusted to introduce an equal and opposite value to effectively zero the error. This technique is typically implemented using a binary-weighted bank

of PMOS transistors as the variable resistance, where the digital control code is determined at startup and stored in a register.

2.4.3.2 Resistive Reference Ladder Trimming

The resistive reference ladder trimming technique corrects comparator offset by utilizing the main reference ladder as a calibration source [30]. In this architecture, a switching network selects specific voltage taps from the resistor ladder and applies them to the bulk terminals of the input transistors M1 and M2. This approach leverages the body effect to shift the threshold voltage (V_{th}) of the differential pair, thereby nullifying the input-referred offset caused by process mismatch.

As demonstrated in the simulation results of the threshold voltage ($|V_t|$) versus the ladder tap voltage (LT), the threshold voltage of transistors M1 and M2 increases linearly from approximately 356.5 mV to 372 mV as the calibration voltage is adjusted. In contrast, the threshold voltage of transistors M3 and M4 remains constant at approximately 356.5 mV because their bulk terminals are not connected to the tuning network. This targeted adjustment of the bulk potential for the input differential pair provides a tuning range sufficient to compensate for random process variations and ensure the accuracy of the comparator trip points.

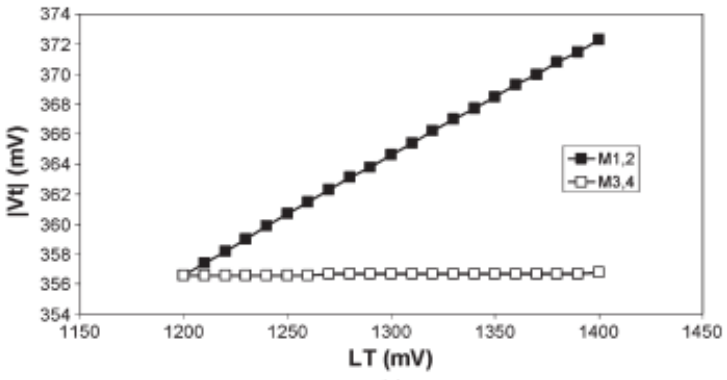

Figure 2.9: Threshold voltage ($|V_t|$) variation of input differential pair transistors (M1, M2) and load transistors (M3, M4) as a function of the resistive ladder tap voltage (LT). The graph demonstrates the body effect: as the bulk potential of M1 and M2 is modulated via the reference ladder, their threshold voltage increases linearly, providing a calibration range to compensate for process-induced mismatch. In contrast, M3 and M4 maintain constant V_{th} since their bulk terminals are connected to fixed substrate potential. This selective tuning is the basis of the proposed resistive ladder trimming mechanism [30].

2.4.4 Advantages of Resistive Trimming for Asynchronous ADCs

Compared to dynamic techniques like Auto-Zeroing which requires accurate clock phases ϕ_1, ϕ_2 and storage capacitors [2], resistive trimming offers distinct advantages for the proposed work:

1. Static Operation: Once the calibration bits are set (during the offline phase), the trimming network becomes static. It does not switch and does not require a clock, preserving the "event-driven" nature of the ADC.

2. Speed Preservation: It does not add significant capacitive load to the high-speed nodes of the comparator, allowing for maximum bandwidth.

2.5 Related Works

As high-speed and low-power Analog-to-Digital Converters become increasingly critical for modern integrated systems, the Flash architecture remains a preferred choice due to its parallel operation and low latency. However, at high resolutions and speeds, transistor mismatch in the comparator array poses a significant challenge, leading to increased offset voltages. To address these limitations, various research efforts have focused on current-mode techniques and optimized comparator structures.

The research proposed in this dissertation differs from the established literature by focusing on an asynchronous level-crossing sampling Flash ADC, which deviates from the synchronous current-mode architectures. While most current-mode designs rely on specialized conveyors or algorithmic cycles, the approach developed here utilizes a bulk-driven offset trimming mechanism. By modulating the threshold voltage (V_{th}) via the body effect through a resistive reference ladder [30], this work achieves precise offset nullification without the high power overhead of complex biasing or the speed penalties of synchronous clocking.

2.6 Asynchronous vs. Synchronous

2.6.1 Advantage

The primary motivation for adopting asynchronous architectures is the direct relationship between signal activity and power consumption [17].

In a synchronous system, the clock tree and the comparators switch at every clock cycle, regardless of whether the input is changing, the power consumption is dominated by the fixed clock frequency [2]:

$$P_{sync} \approx f_{clk} \cdot C_{total} \cdot V_{DD}^2 \tag{2.6}$$

In an asynchronous ADC, the switching frequency is replaced by the event rate. If the signal is constant or slowly varying, the comparators and digital logic remain static, leading to the following proportionality:

$$P_{async} \propto Activity \times V_{DD}^2 \tag{2.7}$$

This property ensures that the energy consumed is always proportional to the information content of the signal which makes these ADCs significantly more efficient for sparse signal environments, where they can achieve near-zero power during periods of inactivity.

2.6.2 Comparative Evaluation

An analysis of state-of-the-art converters shows that asynchronous ADCs excel in energy efficiency across a wide range of sampling rates, particularly for low-to-medium bandwidths [17].

While Synchronous Flash ADCs are designed for peak performance at a specific frequency and suffer from a much higher power consumption caused by the continuous clocking, asynchronous designs scale their power consumption linearly with the input activity.

Table 2.4: Comparison of Power Consumption between Synchronous and Asynchronous Flash ADCs. Simulation results from this work showing the power advantage of asynchronous operation for sparse signals.

Topology	**Average power (P [W])**	**No of samples**
Synchronous	0.1016	145
Asynchronous	0.0314	23

The impact of this architectural difference on long-term technology trends is illustrated in Figure 2.10. The plot depicts the energy per conversion (P/f_s) over the last two decades. While both paradigms show a downward trend due to process node scaling, asynchronous designs (indicated by triangular markers) consistently occupy the lower bound of the energy envelope. This suggests that eliminating the global clock is a key enabler for breaking the power efficiency barriers in modern designs.

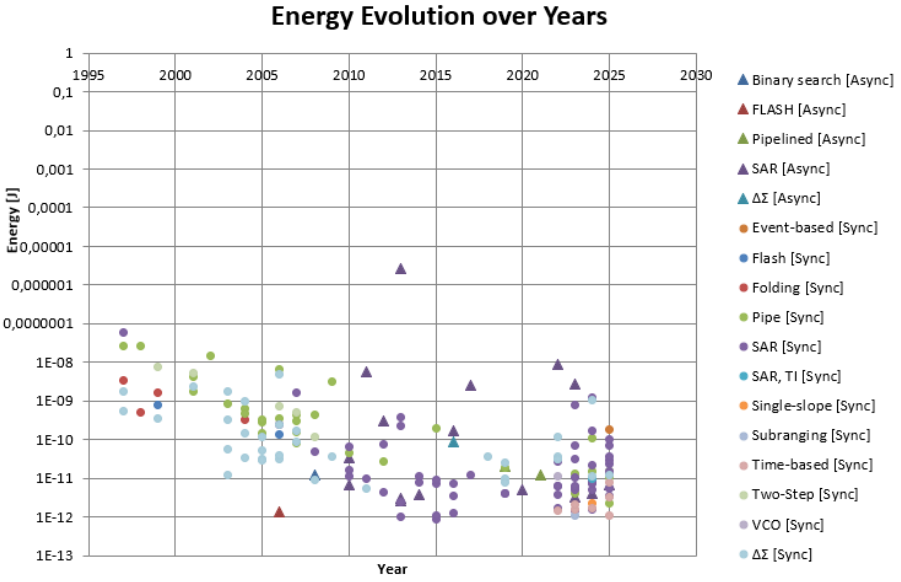

Figure 2.10: Energy per conversion evolution (P/f_s) over the years, highlighting the lower energy floor achieved by asynchronous designs. The triangular markers represent asynchronous ADC implementations, while circular markers represent synchronous designs. The plot demonstrates that asynchronous architectures consistently achieve lower energy consumption across multiple technology nodes compared to their synchronous counterparts, validating the energy efficiency advantage of event-driven operation. Data compiled from ISSCC publications (1997-2025) [10, 11, 17, 18, 21, 25, 27, 29, 31].

Bibliography

[1] S. Abe et al. “A 22.3b 1kHz 12.7mW Switched-Capacitor Delta-Sigma Modulator”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2016.

[2] R. Jacob Baker. *CMOS: Circuit Design, Layout, and Simulation*. 3rd. John Wiley & Sons, 2010.

[3] J. C. Candy and G. C. Temes. “Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation”. In: *IEEE Transactions on Circuits and Systems* CAS-32.12 (1985), pp. 1306–1318.

[4] S.-W. Chen and R. W. Brodersen. “A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-um CMOS”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006, pp. 574–583. DOI: 10.1109/ISSCC.2006.1695276.

[5] P. De Cano-Garcia et al. “A 1.41fJ/conv-step 20MS/s SAR ADC in 14nm CMOS”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2019.

[6] M. Delic-Ibuspachic et al. “A 120dB SNDR Audio Sigma-Delta Modulator”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2013.

[7] D. Draxelmayr et al. “A 2.2-GS/s 7-bit ADC with 37.4 dB SNDR”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2014. DOI: 10.1109/ISSCC.2014.6757514.

[8] G. Geelen. “A 5V, 118dB Delta-Sigma ADC for Wideband Digital Audio”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1997.

[9] B. P. Ginsburg et al. “A 0.42-pJ/step SAR ADC in 28nm CMOS”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2014.

[10] C. Hammerschmied and Qiuting Huang. “A MOSFET-only, 10 b, 200 ksample/s A/D converter capable of 12 b untrimmed linearity”. In: *1997 IEEE International Solids-State Circuits Conference. Digest of Technical Papers*. ISSCC-97. IEEE, pp. 132–133. DOI: 10.1109/isscc.1997.585301. URL: http://dx.doi.org/10.1109/ISSCC.1997.585301.

[11] J. Ingino and B. Wooley. “A continuously-calibrated 10 M sample/s 12 b 3.3 V ADC”. In: *1998 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, ISSCC. First Edition (Cat. No.98CH36156)*. ISSCC-98. IEEE, pp. 144–145. DOI: 10.1109/isscc.1998.672409. URL: http://dx.doi.org/10.1109/ISSCC.1998.672409.

[12] T. Jang et al. “A 0.61fJ/conv-step 270kS/s SAR ADC with Charge-Average-Loop-Preset Technique”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2018. DOI: 10.1109/ISSCC.2018.8310276.

[13] T. Jang et al. “A 118dB DR Delta-Sigma Modulator for Audio Applications”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2018.

[14] H. Jiang et al. “A 0.059-pJ/conv-step Sigma-Delta ADC”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2018.

[15] David A. Johns and Ken Martin. *Analog Integrated Circuit Design*. 2nd. John Wiley & Sons, 2012.

[16] G. Kim et al. “A 0.3V Biofuel-Cell-Powered Glucose/Lactate Biosensing System Integrating a 142nW ADC”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2018. DOI: 10.1109/ISSCC.2018.8310240.

[17] Y. Lim, S. Salehi, et al. “Asynchronous Level-Crossing Sampling ADC for Bio-Signals”. In: *IEEE Transactions on Biomedical Circuits and Systems* 7.3 (2013).

[18] Wenbo Liu, Pingli Huang, and Yun Chiu. “A 12b 22.5/45MS/s 3.0mW 0.059mm² CMOS SAR ADC achieving over 90dB SFDR”. In: *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*. IEEE, Feb. 2010, 380â€“381. DOI: 10.1109/isscc.2010.5433830. URL: http://dx.doi.org/10.1109/ISSCC.2010.5433830.

[19] C. Lukas et al. “A 20-GS/s 6-bit Interleaved ADC with 1.2-V Supply”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2014. DOI: 10.1109/ISSCC.2014.6757512.

[20] R. Muller et al. “A 3nW Signal-Acquisition IC Integrating an Amplifier and a 1.5fJ/conv-step ADC”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2015.

[21] Yong-In Park et al. “A 10 b 100 MSample/s CMOS pipelined ADC with 1.8 V power supply”. In: *2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177)*. ISSCC-01. IEEE, pp. 130–131. DOI: 10.1109/isscc.2001.912573. URL: http://dx.doi.org/10.1109/ISSCC.2001.912573.

[22] R. J. van de Plassche. “Integrated Analog-to-Digital and Digital-to-Analog Converters”. In: (1994).

[23] Behzad Razavi. *Microelectronics*. Prentice Hall, 1998.

[24] R. Schreier and G. C. Temes. “Understanding Delta-Sigma Data Converters”. In: (2005).

[25] P. Schvan et al. “A 22GS/s 5b adc in 0.13/spl mu/m SiGe BiCMOS”. In: *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*. IEEE, 2006, 2340â€“2349. DOI: 10.1109/isscc.2006.1696297. URL: http://dx.doi.org/10.1109/ISSCC.2006.1696297.

[26] C. E. Shannon. *Communication in the Presence of Noise*. Vol. 37. 1. 1949, pp. 10–21.

[27] Y. Tamba and K. Yamakido. “A CMOS 6 b 500 MSample/s ADC for a hard disk drive read channel”. In: *1999 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC. First Edition (Cat. No.99CH36278)*. ISSCC-99. IEEE, 324â€“325. DOI: 10.1109/isscc.1999.759272. URL: http://dx.doi.org/10.1109/ISSCC.1999.759272.

[28] E. Van Veldhoven et al. “A Sub-pJ Energy-Efficient ADC for IoT”. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2021.

[29] P. Vorenkamp and R. Roovers. “A 12 b 50 M sample/s cascaded folding and interpolating ADC”. In: *1997 IEEE International Solids-State Circuits Conference. Digest of Technical Papers*. ISSCC-97. IEEE, pp. 134–135. DOI: 10.1109/isscc.1997.585303. URL: http://dx.doi.org/10.1109/ISSCC.1997.585303.

[30] L. Yao. “Bulk-Driven Switched-Opamp Integrator for Low-Voltage Low-Power Data Converters”. In: *IEEE Journal of Solid-State Circuits* 46.10 (2011).

[31] Masato Yoshioka et al. “A 10b 50MS/s 820µW SAR ADC with on-chip digital calibration”. In: *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*. IEEE, Feb. 2010, 384â€“385. DOI: 10.1109/isscc.2010.5433965. URL: http://dx.doi.org/10.1109/ISSCC.2010.5433965.