FACULDADE DE ENGENHARIA DA UNIVERSIDADE DO PORTO

Design of an Asynchronous Flash Analog-to-Digital Converter

Gonçalo Pinto Monteiro

INTRODUCTION TO RESEARCH

U.PORTO
FEUP FACULDADE DE ENGENHARIA
UNIVERSIDADE DO PORTO

Mestrado em Engenharia Eletrotécnica e de Computadores

Supervisor: Prof. Manuel Cândido Duarte dos Santos

Second Supervisor: João Pedro Santos

January 12, 2026

© Gonçalo Pinto Monteiro, 2025

Abstract

The proliferation of internet of things and biomedical sensors has created a high demand for low-power signal processing interfaces. In many of these applications, the signals of interest are sparse, characterized by long periods of inactivity. Classical synchronous analog to digital converters are inherently inefficient in such scenarios, as they consume dynamic power continuously due to the global clock, regardless of the input signal activity. Ideally the sampling rate should dynamically be adapted to the signal properties, so that power consumption due to the clock activity could be minimized. However, an adaptive sampling rate is not straightforward. As such, the use of an asynchronous ADC is a natural approach to sample non-uniform signals. Asynchronous ADCs require architectural changes, to allow proper operations without a global clock. The adoption of asynchronous control in Flash architectures is primarily motivated by the need to eliminate power consumption high-speed clock distribution networks, thereby improving energy efficiency. Furthermore, asynchronous operation offers intrinsic benefits in handling comparator metastability and reducing latency, making it particularly attractive for high-speed, event-driven applications where signal activity varies significantly over time. This dissertation proposes the design and implementation of an asynchronous Flash ADC. By removing the clock, the proposed architecture aligns power consumption with the input signal activity, theoretically achieving a much lower power consuption.

To address this, an offline trimming strategy is proposed to calibrate the comparator offsets without compromising the high-speed operation of the flash topology. The work encompasses the theoretical analysis, schematic design, and validation of the system through analog/mixed-signal co-simulation. The expected outcome is a robust, clockless ADC architecture that offers a superior figure of merit for sparse signal applications in compared to conventional synchronous architectures.

Keywords: Analog-to-Digital Converter, Asynchronous Design, Flash ADC, Level-Crossing Sampling, Offset Trimming, Low Power, IoT.

Contents

1 Introduction **1**
1.1 Motivation and Problem Statement . . . 3
1.1.1 Inefficiency of Synchronous Sampling . . . 3
1.1.2 Architectural Problem: Flash ADCs . . . 4
1.1.3 Device Limitation: The Mismatch Problem . . . 4
1.2 Objectives . . . 5

2 Literature Review **7**
2.1 Fundamentals of Analog-to-Digital Conversion . . . 7
2.1.1 The Data Conversion Process . . . 7
2.1.2 Performance Metrics . . . 8
2.1.3 State-of-the-Art Comparative Analysis . . . 10
2.2 Synchronous Architectures . . . 12
2.2.1 Synchronous Flash ADC . . . 12
2.2.2 The Power Bottleneck . . . 12
2.2.3 SAR (Successive Approximation Register) . . . 12
2.2.4 Pipeline . . . 13
2.2.5 Sigma-Delta ($\Sigma\Delta$) . . . 14
2.2.6 Dual-slope . . . 14
2.3 Asynchronous Architectures . . . 16
2.3.1 Level-Crossing Sampling (LCS) . . . 16
2.3.2 Asynchronous Flash ADC . . . 17
2.4 Calibration and Trimming Techniques . . . 17
2.4.1 The Component Mismatch Problem . . . 17
2.4.2 Calibration Classifications . . . 18
2.4.3 Resistive Trimming Techniques . . . 18
2.4.4 Advantages of Resistive Trimming for Asynchronous ADCs . . . 20
2.5 Related Works . . . 21
2.6 Asynchronous vs. Synchronous . . . 23
2.6.1 Advantage . . . 23
2.6.2 Comparative Evaluation . . . 23

3 Future Work Planning, Methodologies and Tools **26**
3.1 Work Plan . . . 26
3.2 Methodologies and Tools . . . 28

4 Conclusions **29**

List of Figures

1.1 Time-sparse signal and sampling strategies 2
1.2 Effect of DNL on ADC transfer characteristic 4

2.1 Offset and gain errors in ADC transfer function 9
2.2 Walden FoM versus sampling frequency for representative ADCs 10
2.3 SNR versus sampling frequency for representative ADCs 11
2.4 SAR ADC architecture 13
2.5 Pipeline ADC architecture 13
2.6 First-order sigma-delta ADC architecture 14
2.7 Dual-slope integrating ADC architecture 15
2.8 Digital logic for level-crossing asynchronous ADC 16
2.9 Bulk-driven resistive ladder trimming for comparator offset calibration 19
2.10 Bulk-driven trimming effect on input pair threshold voltage 20
2.11 Current-conveyor-based comparator used in [104] 22
2.12 CC-II-based current comparator used in [107] 22
2.13 Energy per conversion versus publication year for representative ADCs 24

3.1 Gantt chart of dissertation work plan 27

List of Tables

2.1 Walden FoM vs. Sampling Frequency (Flash reference [1] highlighted) 11
2.2 SNR vs. Sampling Frequency (Flash reference [1] highlighted) 11
2.3 Comparison of Power Consumption between Synchronous and Asynchronous Flash ADCs. Simulation results from this work showing the power advantage of asynchronous operation for sparse signals. 24
2.4 Energy per Conversion vs. Year (Flash reference [1] highlighted) 25

List of Acronyms

IoT	Internet of Things
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
CMOS	Complementary Metal-Oxide-Semiconductor
LSB	Least Significant Bit
MSB	Most Significant Bit
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SQNR	Signal-to-Quantization-Noise Ratio
ENOB	Effective Number of Bits
DNL	Differential Non-Linearity
INL	Integral Non-Linearity
BER	Bit Error Rate
FoM	Figure of Merit
SAR	Successive Approximation Register
LCS	Level-Crossing Sampling
GS/s	Giga-Samples per Second
MS/s	Mega-Samples per Second
SHA	Sample-and-Hold Amplifier
V_{th}	Threshold Voltage
V_{OS}	Input Offset Voltage
V_{DD}	Supply Voltage
INC	Increment event signal (upper level crossing)
DEC	Decrement event signal (lower level crossing)
DOUT	Digital output code
DOUT+	Upper digital threshold code
DOUT-	Lower digital threshold code
LC	Level Crossing
LFP	Local Field Potential
AP	Action Potential
RMSE	Root-Mean-Square Error

Chapter 1

Introduction

This chapter provides a brief introduction to the topic associated with the work carried out during the dissertation period. A contextualization is given, followed by a presentation of the research question and the main motivations for carrying out this study. The main objectives of this dissertation will also be outlined, as well as the methodology used to achieve them. Finally, the structure of the dissertation is presented.

We live in an era where smart devices are everywhere, known as the Internet of Things, IoT. While the processing and storage of information are inherently digital, benefiting from the scaling of Moore's Law, the physical world remains fundamentally analog. Physical variables such as temperature, sound and biological potentials are continuous in both time and amplitude. Consequently, the Analog-to-Digital Converter, ADC, serves as the critical interface bridging these two domains, enabling digital systems to interact with the real world [70].

Energy efficiency has shifted from being a secondary performance metric to a primary design constraint, many of the sensors operate on limited battery or rely on energy harvesting, where every Joule of power dissipation has a direct effect on the system's autonomy. In this landscape, the data conversion block almost always takes place as the most spender in this field, especially in sensor interfaces where the digital transmission is duty-cycled.

However, a fundamental characteristic of many environmental and physiological signals is sparsity in between pulses. Signals such as electrocardiograms, voice activity, or environmental monitoring data are spread in bursts, they contain short periods of high information content followed by long intervals of inactivity.

Traditional data conversion approaches, based on uniform sampling and dictated by the Nyquist-Shannon theorem [121], treat these silence periods with the same computational power and energetic waste as the active periods. This creates a paradigm of inefficiency, the system dissipates power to generate redundant digital samples that carry no new information. Recognizing and exploiting this sparsity is the key to unlocking ultra-low-power electronic interfaces.

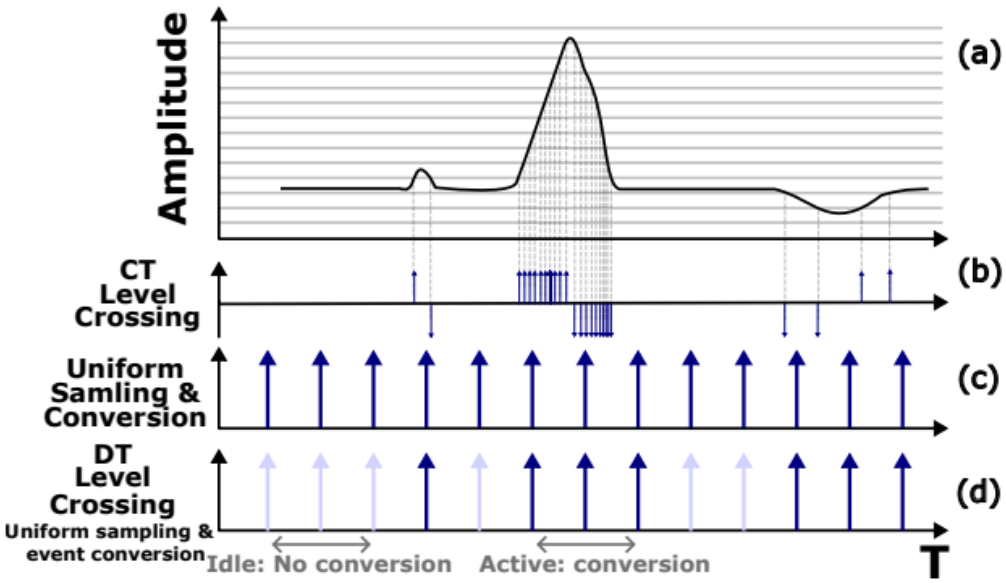

Figure 1.1: Time-sparse signal representation and sampling strategies. (a) Time-sparse signal example showing burst activity with periods of inactivity. (b) Continuous-time event-driven sampling and conversion, which responds to signal changes. (c) Conventional uniform sampling operating at fixed Nyquist rate regardless of signal activity. (d) Discrete-time sampling with event-driven conversion, combining periodic and event-based approaches. This illustration demonstrates the efficiency of adaptive sampling methods for sparse signals compared to uniform sampling at the Nyquist rate [86].

The time-sparse nature of many signals can be observed in the burst waveform where information is concentrated in short intervals separated by long idle periods, as was demonstrated in 1.1. In particular, subfigures (b) and (d) highlight how continuous-time and discrete-time event-driven strategies avoid generating samples during inactivity, in contrast with conventional uniform sampling which keeps operating at a fixed Nyquist rate regardless of the signal content.

1.1 Motivation and Problem Statement

The energy waste in massive-scale IoT deployments and the inefficiency of conventional synchronous architectures when processing sparse data shows the need for a fundamental shift toward architectures that activate only when meaningful data events occur.

1.1.1 Inefficiency of Synchronous Sampling

Traditional Analog-to-Digital Converters operate under a fixed-rate sampling rate, dictated by a global clock signal (f_s). As established by the Nyquist-Shannon sampling theorem [121], this rate is determined by the maximum possible bandwidth of the signal, $f_s \geq 2B$. However, in many real-world applications, the signal is often active for only a fraction of the time, meaning the true information content is much lower than the theoretical maximum bandwidth suggests.

This leads to a massive waste of energy due to the fundamental relationship governing dynamic power consumption in CMOS circuits [10]:

$$P_{dynamic} = \alpha \cdot f \cdot C_L \cdot V_{DD}^2 \tag{1.1}$$

where:

- $P_{dynamic}$ is the dynamic power dissipated.
- α is the activity factor (or switching factor).
- f is the clock frequency.
- C_L is the load capacitance being switched (e.g., in the clock tree).

In a uniformly clocked ADC, f is fixed by the Nyquist criterion and the clock network toggles every cycle, so α remains high even when the input signal is almost static. As a result, the converter continues to charge and discharge large clock and comparator capacitances at every period, dissipating dynamic power to generate redundant samples that do not carry new information. For example, if a sensor signal is active only 10% of the time but the ADC samples continuously, 90% of the switching events are spent tracking intervals where the input is essentially constant, directly illustrating how synchronous operation leads to massive energy waste for non synchronous signals.

1.1.2 Architectural Problem: Flash ADCs

While the Flash ADC architecture is highly attractive due to its single-cycle, high-speed conversion capability [70], it suffers from severe limitations regarding power and area, particularly when reaching higher resolutions. The number of required comparators scales exponentially with resolution (2^N). This exponential scaling leads directly to an increase in input capacitance and static power dissipation.

Even in low-power, synchronous designs, the dynamic power of the comparator switching is the dominant factor in the power budget.

Therefore, combining the high speed of the Flash architecture with the high power efficiency required for IoT demands a radical shift away from the synchronous clocking scheme.

1.1.3 Device Limitation: The Mismatch Problem

To mitigate the power and area issues mentioned above, designers are compelled to minimize the physical dimensions of the core devices, particularly the transistors within the comparators. However, this introduces a fundamental physical constraint:

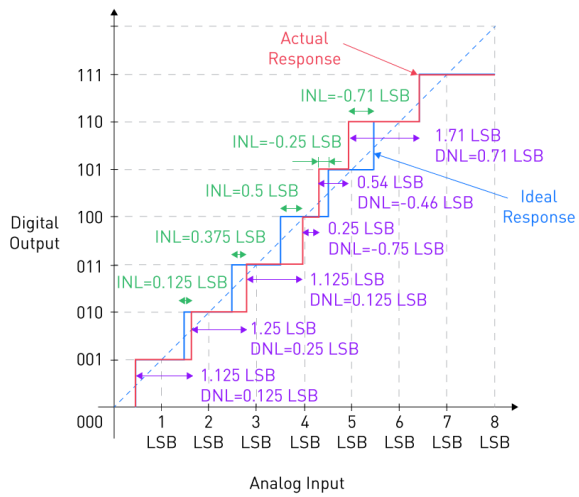

Figure 1.2: Adapted from [102]. ADC transfer function illustrating Differential Non-Linearity (DNL) errors. The graph compares the ideal staircase response (blue) with the actual response (red), highlighting varying step widths and a missing code.

The impact of device mismatch on the ADC transfer characteristic is illustrated by the deviation between the ideal and actual staircase curves, as shown in Fig. 1.2. In this figure, varying step widths and the presence of a missing output code clearly demonstrate how Differential Non-Linearity (DNL) errors distort the ideal 1 LSB step profile. The reduction of transistor size, while increasing speed and reducing capacitance, drastically increases random variations in parameters like the threshold voltage (V_{th}), leading to a significant Input Offset Voltage (V_{os}) in the comparators [10].

Linearity errors arise from several factors, starting with component mismatches where DNL and INL faults are caused by discrepancies in resistor values within ladders or capacitors in arrays. Nonlinearities in analog components such as amplifiers and other parts of the ADC also influence these mistakes [102]. Furthermore, variations in temperature and supply voltage can cause component values to drift, thereby contributing to linearity problems.

1.2 Objectives

Based on the limitations identified in traditional synchronous data conversion when dealing with asynchronous sensor signals, the primary objective of this work is to design and implement an energy-efficient ADC architecture, so this ADC must exploit signal inactivity to achieve a significant reduction in power consumption.

To achieve the overall goal of developing an efficient ADC, the following specific objectives are defined for this dissertation:

1. Asynchronous Architecture Design: To develop the circuit-level design of an asynchronous Flash ADC, minimizing dynamic power consumption by ensuring that power is only dissipated when an input signal event occurs.

2. Offline Trimming Implementation: To implement an offline trimming mechanism capable of detecting and compensating for the input offset voltage of the comparators.

3. Mixed-Signal Validation: To validate the complete system through analog and digital co-simulation. This validation must confirm the functionality and accuracy of both the asynchronous core and the trimming logic.

4. Performance Benchmarking: To quantify the energy efficiency of the proposed design using well known figures of merit. The results must be compared against the current state of the art synchronous ADCs and relevant asynchronous solutions.

In order to support these objectives, the state-of-the-art review is structured to progressively narrow the focus from general data-conversion theory to the specific asynchronous Flash architecture and trimming techniques addressed in this work. Chapter 2 begins by revisiting the fundamentals of sampling, quantization, and performance metrics for data converters, establishing the theoretical background required to interpret figures of merit such as SNDR, ENOB, and Walden FoM. It then surveys the main synchronous ADC architectures (Flash, SAR, Pipeline, and Sigma-Delta), highlighting their inherent power, speed and resolution trade-offs and identifying why conventional clocked Flash converters become inefficient when dealing with sparse signals.

Subsequent sections of the literature review focus on asynchronous and level-crossing sampling strategies, examining prior work on event-driven converters and their advantages for time-sparse signals, and finally discuss existing calibration and trimming techniques for comparator offset

reduction, providing the reference framework against which the proposed bulk-driven resistive trimming mechanism will be compared.

Chapter 2

Literature Review

This chapter presents the state-of-the-art in Analog-to-Digital Converters, reviewing theoretical foundations and analyzing survey data to justify the proposed architecture.

2.1 Fundamentals of Analog-to-Digital Conversion

This section provides the theoretical background required to understand the operation and performance characterization of data converters. It covers the fundamental steps of the conversion process such as sampling, quantization, and coding.

2.1.1 The Data Conversion Process

2.1.1.1 Ideal Data Conversion

The analog-to-digital conversion process acts as the bridge between the continuous physical world and the discrete digital domain. Conceptually, it involves two distinct operations: discretization in time, sampling, and discretization in amplitude, quantization. Ideally, this process should be instantaneous and lossless within the signal bandwidth of interest [70].

2.1.1.2 The Sampling Operation

Sampling converts a continuous-time signal $x(t)$ into a discrete-time sequence $x[n]$ [70].

According to the Nyquist-Shannon sampling theorem [121], a band-limited signal with maximum frequency B can be perfectly reconstructed if the sampling frequency f_s satisfies:

$$f_s \geq 2B \tag{2.1}$$

Violating this condition results in aliasing, where high-frequency spectral components mixes into the baseband, becoming indistinguishable from the original signal.

2.1.1.3 The Quantization Operation

While sampling transforms continuous time in discrete values, quantization maps the continuous amplitude of each sample to one of a finite number of levels [70]. An N-bit ADC divides the input range (V_{ref}) into 2^N discrete levels. The step size between adjacent levels is the Least Significant Bit (LSB):

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{2.2}$$

Unlike sampling, quantization is non-reversible and introduces a deterministic error. This error is typically modeled as white noise added, the quantization noise with a uniform probability distribution. For an ideal quantizer, the Signal-to-Quantization-Noise Ratio (SQNR) is given by the formula:

$$SQNR_{dB} \approx 6.02N + 1.76 \tag{2.3}$$

2.1.1.4 Coding

The final stage is encoding the quantized level into a binary format. The choice of coding scheme being the most common straight binary and gray code which depends on the system requirements for data processing and transmission, but does not affect the fundamental analog performance [10].

2.1.2 Performance Metrics

To evaluate and compare different data converters objectively, a standard set of metrics is used. These are categorized into dynamic and static parameters.

2.1.2.1 Resolution and Sampling Rate

Resolution defines the theoretical dynamic range, while the sampling rate determines the maximum signal bandwidth. However, these are nominal values the actual performance is limited by noise and non-linearities [70].

2.1.2.2 Signal-to-Noise-Distortion Ratio (SNDR)

Signal to noise ratio adding distortion ratio or SNDR is the primary dynamic metric. It is the ratio of the signal power to the total power of all noise and harmonic distortion components. From SNDR, the Effective Number of Bits, ENOB, is derived [70]:

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \tag{2.4}$$

This value represents the true resolution of the converter at a specific input frequency.

2.1.2.3 Differential and Integral Non-Linearity (DNL and INL)

Static linearity is characterized by measuring the deviation of code transition levels from their ideal positions [70]. The DNL measures the deviation of a single step width from the ideal 1 LSB. A DNL less than -1 LSB implies a missing code in the transfer function.

The INL is the cumulative sum of DNL errors, representing the deviation of the transfer curve from a straight line. Specific INL patterns like saw-tooth shapes can reveal systematic errors in the architecture, such as gain mismatch or non-linear biasing [109].

2.1.2.4 Offset and Gain Error

These are linear errors, offset is a constant shift of the transfer characteristic as seen before in section 1.2.3, while gain error is a deviation in the slope [70]. Unlike non-linearity, these errors preserve the signal shape and can often be calibrated out simply. Linear imperfections such as offset and gain error modify the global position and slope of the transfer characteristic without changing its shape, as shown in Fig. 2.1. In this representation, a constant DC shift moves the whole transfer curve up or down (offset error), while a slope deviation alters the full-scale span, the so called gain error, both of which can be compensated by simple digital calibration.

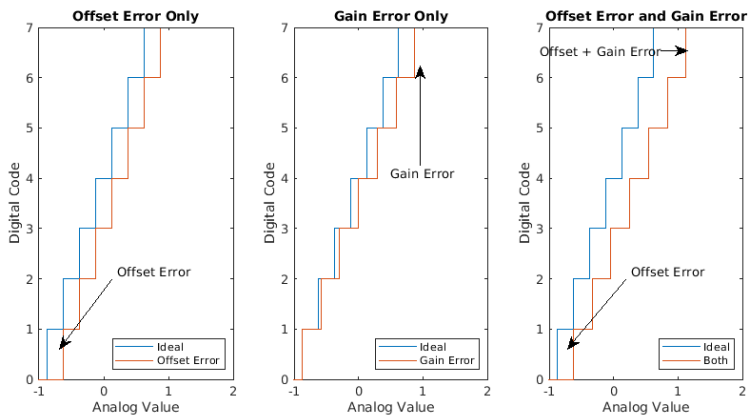

Figure 2.1: Adapted from [99] ADC transfer function showing offset and gain errors. Offset error represents a constant DC shift applied uniformly across all codes, while gain error modifies the slope of the transfer function. Both are linear errors that can be calibrated using digital post-processing techniques [70].

2.1.2.5 Bit Error Rate (BER)

BER quantifies the probability of the converter producing an incorrect digital code [10]. This is often caused by metastability, a phenomenon where internal decision circuits fail to resolve a valid logic level within the allocated time when the input is extremely close to a decision threshold.

2.1.3 State-of-the-Art Comparative Analysis

The analytical plots and tables presented below incorporate data from an exhaustive set of 140 state-of-the-art works. All entries were selected from the ISSCC and JSSC publications, due to their high prestige and stringent peer-review process in the field of data converters. Within these sources, only papers reporting both supply voltage (V_{DD}) and signal-to-noise-and-distortion ratio (SNDR) were retained, ensuring that all points in the performance envelopes are based on consistently documented electrical and dynamic performance metrics. To ensure transparency and reproducibility, the complete list of references used to generate these performance envelopes, covering Flash, SAR, Pipeline, and Sigma-Delta architectures, is provided in [2–9, 11–15, 17–22, 24–29, 32–35, 37–41, 43, 44, 46–64, 67, 68, 71, 72, 74–85, 87–96, 98, 100, 101, 105, 108, 110–113, 117–120, 123–128, 130–132, 134–148, 151–170].

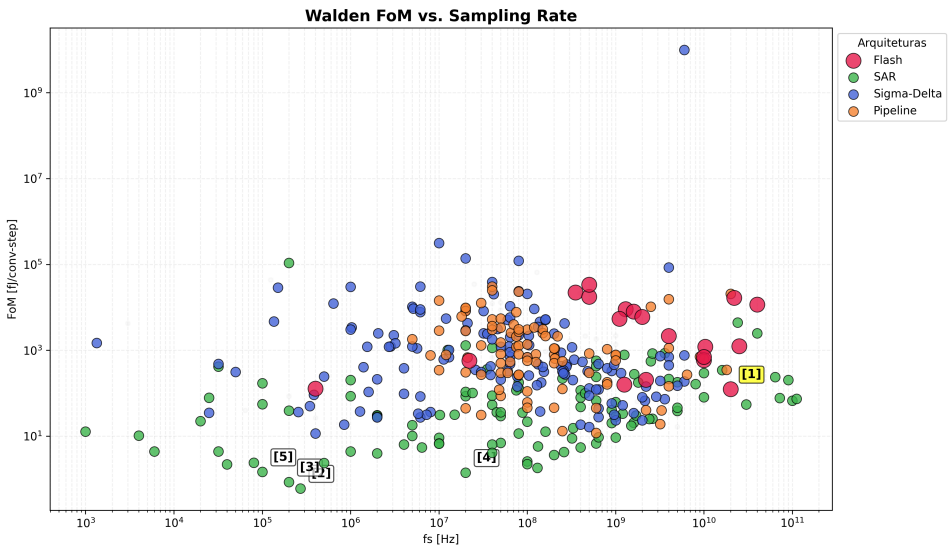

Figure 2.2: Walden FoM vs. Sampling Frequency (Flash reference [1] highlighted)

The evolution of the Walden Figure of Merit as a function of sampling rate for different ADC architectures is summarized in Fig. 2.2. This plot allows identifying the performance envelope across a wide range of f_s and highlights how specific implementations approach the energy-efficiency limit at their target bandwidth.

Table 2.1: Walden FoM vs. Sampling Frequency (Flash reference [1] highlighted)

Ref.	Architecture	Publication	f_s [Hz]
[1]	**Flash**	**Lukas [97]**	**20G**
[2]	SAR	Jang [65]	270k
[3]	SAR	Ginsburg [45]	200k
[4]	SAR	Cano [30]	20M
[5]	SAR	Muller [103]	200

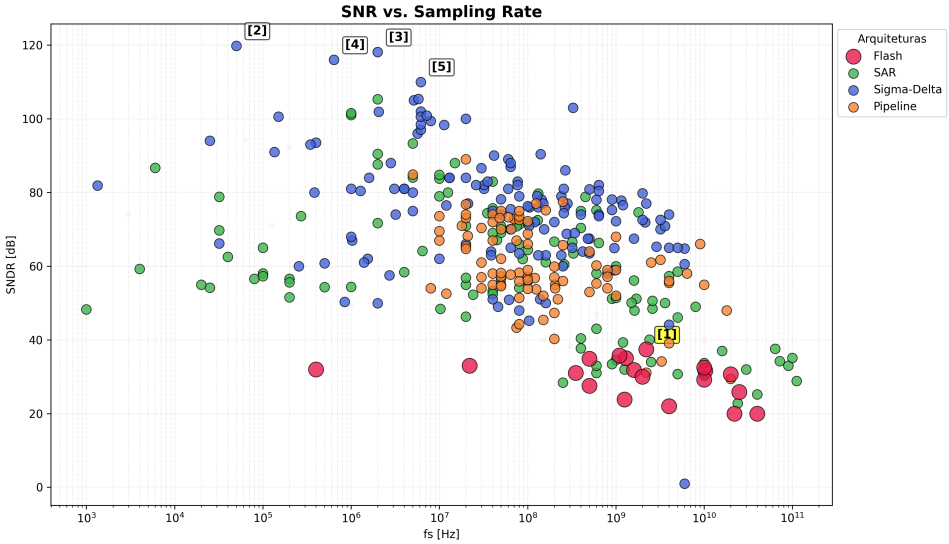

Figure 2.3: SNDR vs. Sampling Frequency (Flash reference [1] highlighted)

The dependence of SNR on the sampling frequency for several state-of-the-art designs is presented in Fig. 2.3. By comparing the trajectories of different architectures, the figure shows how high-resolution sigma-delta converters sustain very high SNDR at low f_s, whereas Flash and SAR topologies occupy regions optimized for speed or moderate resolution.

Table 2.2: SNR vs. Sampling Frequency (Flash reference [1] highlighted)

Ref.	Architecture	Publication	SNDR [dB]
[1]	**Flash**	**Draxelmayr [36]**	**37.4**
[2]	Sigma-Delta	Delic [31]	120.0
[3]	Sigma-Delta	Jang [66]	118.0
[4]	Sigma-Delta	Abe [1]	116.0
[5]	Sigma-Delta	Geelen [42]	110.0

2.2 Synchronous Architectures

To address asynchronous ADCs we first need to address synchronous ADCs, they have a global clock signal that dictates sampling instances and synchronizes internal operations. While these architectures are highly mature and widely used, they face fundamental power efficiency trade-offs, particularly when operating at high frequencies or processing sparse data [70].

2.2.1 Synchronous Flash ADC

The Flash ADC is conceptually the simplest and fastest architecture, performing a complete conversion in a single clock cycle [10]. It utilizes a resistive ladder to generate $2^N - 1$ reference voltages, which are compared simultaneously to the input signal by a large bank of comparators. This parallel comparison produces a thermometer code, that a digital logic block then converts into a standard binary output. Its primary limitation is the exponential increase in hardware complexity, area, and power consumption as resolution increases.

The thermometer term refers to the parallel output from the Flash ADC comparators, where '1's run up to the input voltage level like mercury in a thermometer, indicating signal strength before being converted to standard binary by an encoder.

2.2.2 The Power Bottleneck

The primary drawback of the synchronous Flash architecture is its exponential scaling. Survey data clearly illustrates that high speed translates into high power in these designs. For example, a 6-bit 500 MS/s CMOS Flash ADC reported in 1999 already consumed 400 mW [129].

More extreme cases, such as a 22 GS/s 5-bit design, can consume up to 3W [116].

The continuous clocking of a massive comparator bank creates a significant energy dissipation even when the input signal is static. This lack of adaptivity makes synchronous Flash architectures increasingly unsuitable for battery-powered or energy-harvesting applications.

2.2.3 SAR (Successive Approximation Register)

The SAR ADC operates using a binary search algorithm [109], for each sample the internal logic tests one bit at a time, starting from the most significant bit (MSB). A single comparator compares the input to the output of an internal digital to analog converter (DAC), if the input is higher, the bit is set to '1' otherwise, it is set to '0'. This process repeats for N cycles. Because it uses very few active components, it is the most energy efficient choice for low speeds.

The binary search operation of a SAR ADC is implemented by successively testing each bit through the interaction of the sample-and-hold amplifier (SHA), DAC, comparator, and control logic, as shown in Fig. 2.4. At every conversion step, the SAR logic updates the DAC output and the comparator decides whether the input is above or below the trial voltage, gradually converging from the MSB to the LSB towards the final digital code.

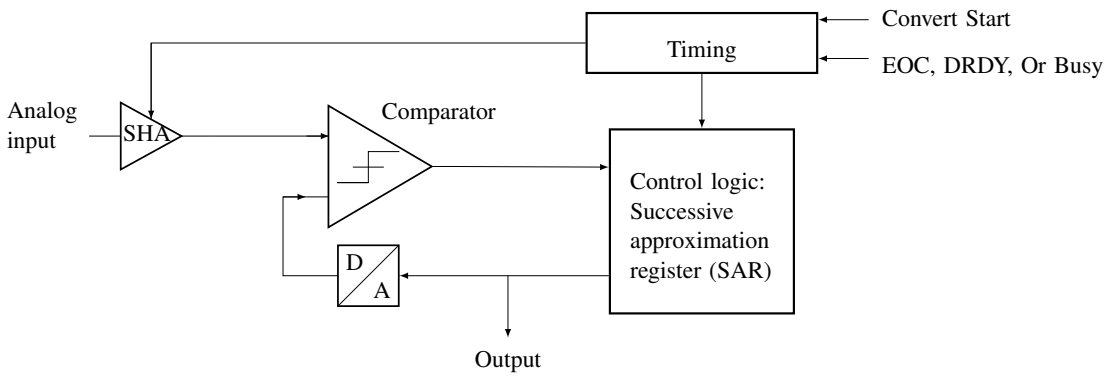

Figure 2.4: Successive Approximation Register (SAR) ADC architecture showing the sample-and-hold amplifier (SHA), comparator, digital-to-analog converter (DAC), and control logic. The SAR logic iteratively approximates the input signal by testing each bit from MSB to LSB, achieving high energy efficiency at moderate speeds [109].

2.2.4 Pipeline

The Pipeline ADC breaks the conversion into several sequential stages [70], each stage resolves a few bits of information, quantizes them, and passes the remaining error, the residue, to the next stage after amplification. This approach allows the ADC to work on multiple samples concurrently, obtaining very high throughput and high resolution, the problem relies in the inherent processing latency.

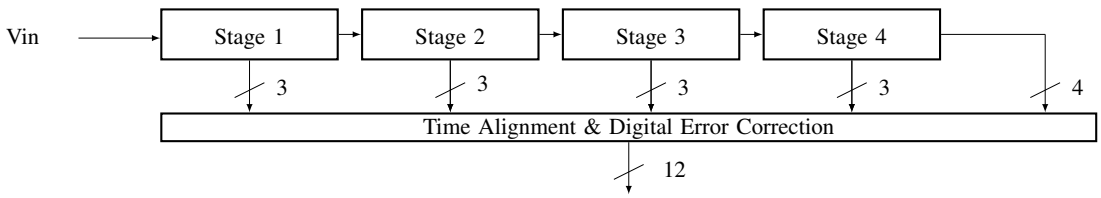

Figure 2.5: Pipeline ADC architecture showing multiple conversion stages operating in parallel on different input samples. Each stage resolves a subset of bits, generates a partial digital output, and amplifies the residue for the next stage. The pipelined structure enables high-throughput operation at the expense of increased latency and circuit complexity.

The pipelined converter processes multiple samples simultaneously by distributing the resolution across several cascaded stages, as shown in Fig. 2.5. Each stage resolves a subset of bits, generates a partial digital output, and amplifies the residue for the next stage, while a digital error-correction block aligns the timing of all stage outputs to produce the final high-throughput conversion result.

2.2.5 Sigma-Delta (ΣΔ)

The ΣΔ architecture relies on oversampling, sampling much faster than the Nyquist rate [16], and noise-modulation. A modulator integrates the difference between the input signal and a feedback version of the quantized output. This process pushes the quantization noise into higher frequencies, outside the signal band of interest, a digital filter then removes the high-frequency noise, resulting in high resolution and precision [115].

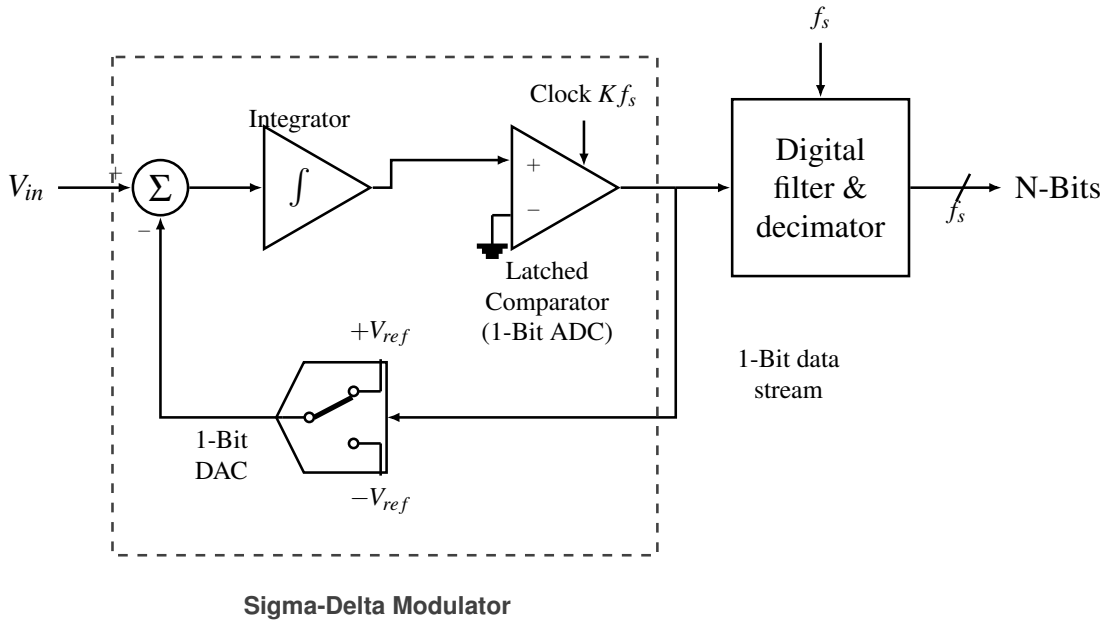

Figure 2.6: First-order sigma-delta ADC architecture illustrating the oversampling modulator with summer, integrator, 1-bit quantizer, feedback DAC, and digital decimation filter, which together implement noise shaping and high-resolution conversion [16, 115].

Oversampling and noise shaping are achieved by the feedback loop formed by summer, integrator, 1-bit quantizer, and digital decimation filter in the first-order sigma-delta architecture, as shown in Fig. 2.6. The modulator continuously integrates the difference between the analog input and the 1-bit DAC feedback, pushing most of the quantization noise to high frequencies, which are later removed by the digital filter.

2.2.6 Dual-slope

This integrating architecture [114] measures the time required for a capacitor to charge and discharge, in the first phase, the capacitor is charged by the input voltage for a fixed period then for

the second phase, it is discharged by a known reference voltage. The time it takes to return to zero is proportional to the average value of the input signal it's highly accurate and immune to high-frequency noise but is much slower than other architectures.

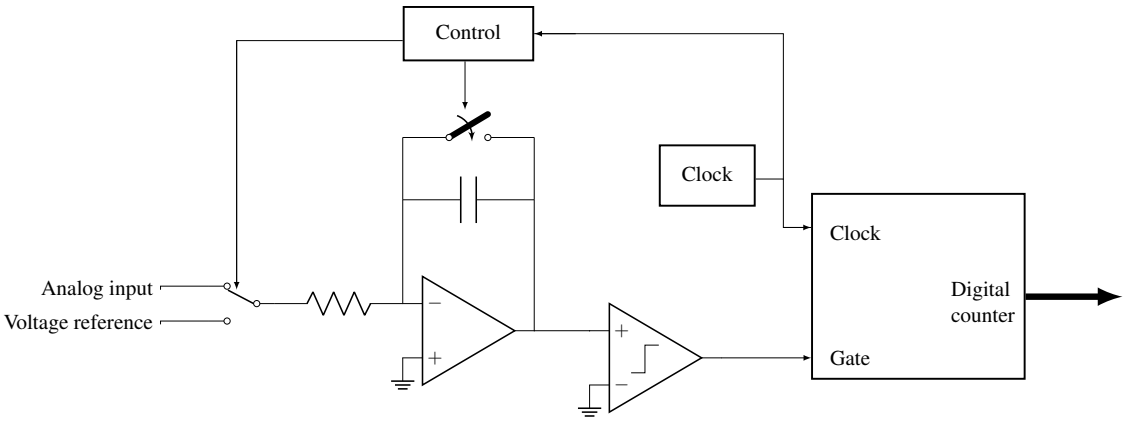

Figure 2.7: Dual-slope (integrating) ADC architecture showing the charging phase where an unknown input signal is integrated for a fixed time, and the discharge phase where a precise reference voltage drives the capacitor back to zero. The conversion time is proportional to the input voltage, providing excellent accuracy and noise rejection at the expense of low throughput.

The dual-slope architecture converts the input voltage into time by integrating it during a fixed interval and then discharging the capacitor with a known reference, as shown in Fig. 2.7. The digital counter measures the discharge interval controlled by the reference voltage, so the resulting count is proportional to the average value of the input signal and inherently rejects high-frequency noise.

2.3 Asynchronous Architectures

Asynchronous, or event-driven, architectures represent a fundamental paradigm shift in data conversion [86], unlike synchronous ADCs, which are bound by a global clock and the Nyquist-Shannon sampling theorem, asynchronous ADCs operate based on the signal's activity. This approach offers a more efficient alternative for processing sparse signals.

2.3.1 Level-Crossing Sampling (LCS)

The core principle behind many asynchronous ADCs is Level-Crossing Sampling (LCS) [86]. In traditional uniform sampling, the signal is captured at fixed time intervals (T_s), and the amplitude is quantized. In LCS, the process is inverted: the amplitude levels are fixed (quantization thresholds), and the ADC records the exact time at which the input signal crosses these thresholds.

This method is particularly powerful for signals that remain constant or change slowly over long periods. Instead of generating redundant samples that capture no new information, the LCS ADC remains idle, only producing a digital event when the signal effectively changes by more than the defined threshold.

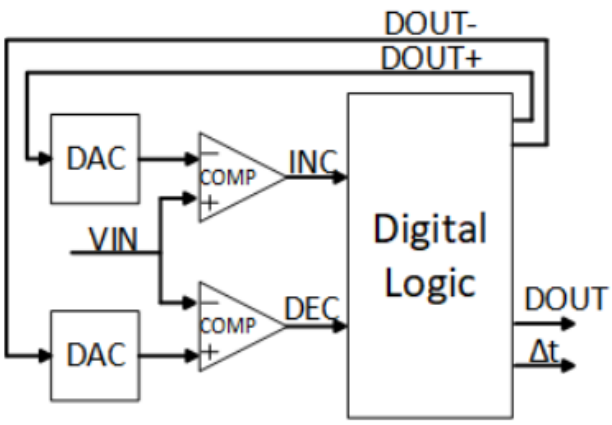

Figure 2.8: Digital logic core of a level-crossing asynchronous ADC showing the two DACs that generate upper and lower thresholds around the input signal V_{IN}, the pair of comparators that produce the INC and DEC event signals, and the digital logic that updates the output code $DOUT$ and the time-stamp Δt based on each level crossing. The feedback paths from the digital logic to the DACs keep the thresholds centered around the most recent output level, enabling event-driven tracking of the input signal instead of uniform-rate sampling [106].

The core of the proposed event-driven conversion scheme is illustrated in Fig. 2.8. In this architecture, two on-chip DACs generate a pair of voltage thresholds placed symmetrically around the analog input signal V_{IN}, while two comparators continuously monitor the crossings of V_{IN} with respect to these levels. The upper comparator asserts the INC signal whenever V_{IN} rises above the upper threshold, whereas the lower comparator asserts the DEC signal when V_{IN} falls below the lower threshold.

Upon each level-crossing event, the digital logic block updates the encoded amplitude word $DOUT$ and the control words driving the DACs so that the thresholds are recentered around the new signal level. In addition, the logic measures the elapsed time since the previous event and outputs a time-stamp Δt, thereby representing the signal as a sequence of non-uniform events $(DOUT, \Delta t)$ instead of uniformly spaced samples. This mechanism concentrates conversion activity in intervals where the input varies rapidly and naturally suppresses conversions during flat regions, enabling an asynchronous ADC operation whose power consumption scales with the actual signal dynamics rather than with a fixed global sampling clock.

2.3.2 Asynchronous Flash ADC

The Asynchronous Flash ADC adapts the parallel structure of a standard Flash ADC but removes the sampling clock entirely. In this architecture, the comparators are not latched by a clock, they operate in continuous time, constantly monitoring the input voltage V_{in} against the reference ladder. The event generation happens when the input signal crosses a threshold, the corresponding comparator changes its output state immediately, this transition triggers an asynchronous logic to generate a digital output pulse.

2.4 Calibration and Trimming Techniques

In high-speed Flash ADCs, the accuracy of the system is fundamentally limited by the precision of the comparators. While the architecture fundamentals were established in the previous sections, practical implementations must address the non-idealities of the fabrication process, specifically the Input Offset Voltage (V_{os}).

2.4.1 The Component Mismatch Problem

In deep sub-micron CMOS technologies, transistors that are drawn with identical dimensions on the layout will exhibit slight differences in their electrical parameters after fabrication. This phenomenon, known as mismatch, affects the threshold voltage (V_{th}) and the current gain factor (β) of the differential pair in a comparator [10].

According to Pelgrom's Law cited in section 2.3.3 of [70], the standard deviation of the threshold voltage mismatch (σ_{Vth}) is inversely proportional to the square root of the transistor area ($W \cdot L$):

$$\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{W \cdot L}} \tag{2.5}$$

Where $A_{V_{th}}$ is a technology-dependent constant. This creates a critical trade-off, to minimize offset without calibration, transistors must be made large, which increases parasitic capacitance and degrades the ADC speed and power efficiency. Therefore, small transistors are used for speed, and calibration is needed to correct the resulting offset.

2.4.2 Calibration Classifications

Calibration techniques can be broadly categorized by their timing and domain [10]. In terms of timing there can be derived two types foreground calibration which interrupts normal operation to measure and correct errors and background calibration which operates continuously but adds significant complexity. In terms of domain there is digital calibration that corrects the output code mathematically, whereas analog calibration adjusts the circuit biasing or load conditions to nullify the offset at the source.

For an asynchronous architecture, avoiding continuous clock activity is crucial to maintain low power during idle periods. Thus, Analog Foreground Calibration is the preferred approach.

2.4.3 Resistive Trimming Techniques

Resistive trimming aims to compensate for the imbalance in the input differential pair (M_1, M_2) by intentionally creating an opposing imbalance in the load resistance or the reference path [10].

2.4.3.1 Internal Resistive Loading

The internal resistive loading method involves placing a variable resistive network in parallel or series with the output loads of the comparator pre-amplifier stage. By digitally switching small resistors or MOS switches operating in the triode region in parallel with the load branch, the effective resistance R_L is modulated. Since the gain of the pre-amplifier is defined as $A_v = g_m R_L$, changing R_L on one side of the differential pair adjusts the output DC level. If the differential pair has an offset, the trimming network is adjusted to introduce an equal and opposite value to effectively zero the error. This technique is typically implemented using a binary-weighted bank of PMOS transistors as the variable resistance, where the digital control code is determined at startup and stored in a register.

2.4.3.2 Resistive Reference Ladder Trimming

The resistive reference ladder trimming technique corrects comparator offset by utilizing the main reference ladder as a calibration source [150]. In this architecture, a switching network selects specific voltage taps from the resistor ladder and applies them to the bulk terminals of the input transistors M1 and M2. This approach leverages the body effect to shift the threshold voltage (V_{th}) of the differential pair, thereby nullifying the input-referred offset caused by process mismatch.

As demonstrated in the simulation results of the threshold voltage ($|V_t|$) versus the ladder tap voltage (LT), the threshold voltage of transistors M1 and M2 increases linearly from approximately 356.5 mV to 372 mV as the calibration voltage is adjusted. In contrast, the threshold voltage of transistors M3 and M4 remains constant at approximately 356.5 mV because their bulk terminals are not connected to the tuning network. This targeted adjustment of the bulk potential for the input differential pair provides a tuning range sufficient to compensate for random process variations and ensure the accuracy of the comparator trip points.

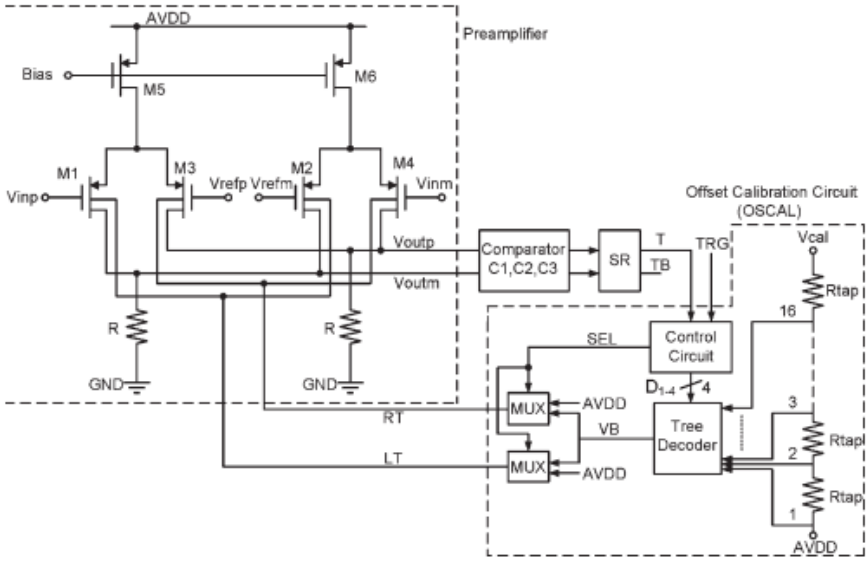

Figure 2.9: Bulk-driven resistive reference ladder trimming architecture used for comparator offset calibration. The preamplifier input pair (M1, M2) has its bulk terminals driven by a selectable tap of the main reference resistor ladder via the offset calibration circuit (OSCAL). A digital control word selects one of the ladder taps (Rtap) through a tree decoder and multiplexers, generating a calibration voltage V_{cal} that modulates the bulk node V_B. By shifting the bulk potential of M1 and M2 while keeping the load devices at a fixed substrate potential, the threshold voltage of the input pair is adjusted through the body effect, providing a tunable range to cancel process-induced input offset in high-speed Flash ADC comparators [149].

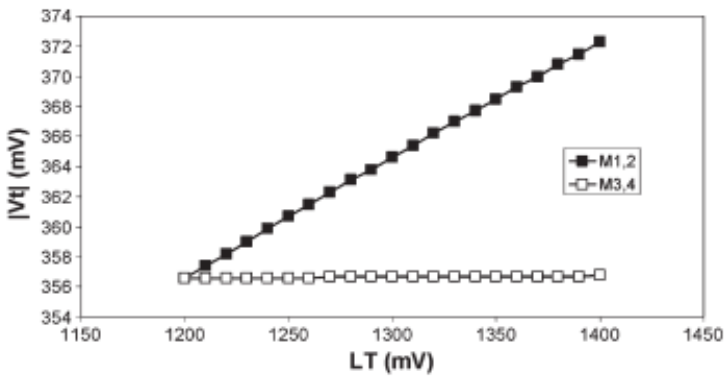

Figure 2.10: Threshold voltage V_{th} variation of input differential pair transistors M1, M2 and load transistors M3, M4 as a function of the resistive ladder tap voltage LT. The graph demonstrates the body effect as the bulk potential of M1 and M2 is modulated via the reference ladder, providing a calibration range to compensate for process-induced mismatch [149].

The effectiveness of the bulk-driven trimming mechanism is illustrated by the controlled change of the input pair threshold voltage with the ladder tap voltage, as shown in Fig. 2.10 and Fig. 2.9. As the calibration voltage LT increases, the threshold of M1 and M2 shifts linearly while M3 and M4 remain fixed, providing the tuning range required to compensate comparator offset caused by random process variations [149].

2.4.4 Advantages of Resistive Trimming for Asynchronous ADCs

Compared to dynamic offset-cancellation techniques such as auto-zeroing, which rely on accurately timed clock phases ϕ_1 ϕ_2 and additional storage capacitors that must be periodically charged and discharged [10], resistive trimming is particularly well suited to an event-driven asynchronous architecture. Once the calibration bits are determined during a dedicated foreground calibration phase, the resistive trimming network remains static, meaning that no further switching activity or clocking is required and the comparator bias conditions are held purely by DC conduction paths. This static behavior ensures that the trimming circuitry does not disturb the intrinsic event-driven operation of the ADC, which should ideally remain idle whenever the input signal is not crossing a quantization threshold.

Another important advantage is that the resistive network can be connected so as to avoid placing large additional capacitances on the high-speed nodes of the comparator, thereby preserving the original small-signal bandwidth and regeneration speed. In contrast, dynamic calibration schemes typically introduce extra sampling capacitors and switch parasitics at sensitive nodes, which can degrade the comparator's response time and limit the maximum achievable sampling rate in high-speed Flash architectures [10].

2.5 Related Works

As high-speed and low-power Analog-to-Digital Converters become increasingly critical for modern integrated systems, the Flash architecture remains a preferred choice due to its parallel operation and inherently low conversion latency. However, at high resolutions and sampling speeds, transistor mismatch in the comparator array becomes a dominant non-ideality, leading to increased input-referred offset voltages and degraded linearity. To address these limitations, various research efforts have focused on current-mode techniques, optimized comparator structures, and tailored encoding schemes that aim to improve speed and power efficiency without sacrificing accuracy. These works, while diverse in implementation, share the common constraint of operating within a synchronous, clock-driven framework and typically do not exploit the time-sparse nature of many sensor signals.

In the 3-bit design by Sharma et al., the authors compare several dynamic latch comparators and ultimately select the topology that offers the best trade-off between delay and power in 180 nm CMOS [122]. The selected comparator consists of a preamplifier stage that converts the input current differences into voltage, followed by a dynamic latch that regenerates the decision into full-swing digital levels. This separation between preamplification and latching helps to reduce kickback on the current ladder and improves decision robustness, but it also introduces additional static bias currents in the preamplifier and does not address systematic offset through any explicit calibration mechanism.

Nijhawan et al. propose a current-mode low-power Flash ADC in which the core decision element is a current comparator built around a current conveyor structure [104]. The design targets high-speed operation with very low propagation delay (on the order of 0.4 ns) at 1.8 V in 0.18 μm CMOS, achieving a reported power consumption of approximately 158 μW at 0.1 mA input current. As illustrated in Fig. 2.11, the ADC employs a current-mode front-end in which current conveyors and mirror structures realize the high-speed comparators that interface a reference ladder and a thermometer-to-binary encoder. This organization attains low input impedance and short decision time, leading to very low propagation delay and modest power, but the reliance on multiple current mirrors increases sensitivity to mismatch and temperature, and the overall converter still operates under a global sampling clock without any form of asynchronous level-crossing or on-chip offset trimming.

In the 2-bit Flash ADC by Panchal et al., the comparator is implemented using second-generation current conveyors (CC-II) combined with positive feedback to sharpen the transition between logic levels [107]. As illustrated in Fig. 2.12, the input current is processed by the CC-II core, which converts small current differences into a voltage that is then amplified by a regenerative latch, yielding fast and rail-to-rail outputs. This configuration achieves excellent linearity and very low power for the 2-bit target resolution, but the strong positive feedback and reliance on precise current matching make the structure less attractive for higher resolutions without complementary offset calibration or background trimming. [107]

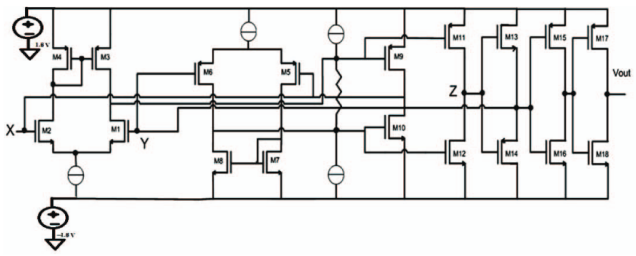

Figure 2.11: Current-mode comparator built around a current conveyor as proposed by Nijhawan et al. [104]. The conveyor provides low input impedance and mirrors the input current onto an internal sensing branch, where a decision circuit determines the sign of the current difference relative to the reference, enabling sub-nanosecond propagation delay at low power.

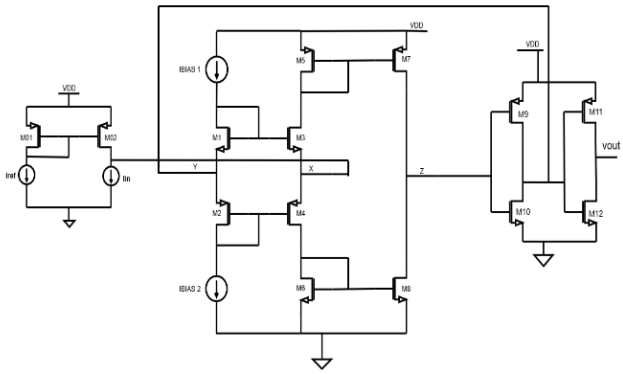

Figure 2.12: Second-generation current-conveyor (CC-II) based current comparator from the 2-bit Flash ADC of Panchal et al. [107]. The CC-II core translates small current differences into a voltage, which is further amplified by a regenerative latch with positive feedback, providing fast switching and low power at the cost of increased sensitivity to mismatch.

The research proposed in this dissertation differs from this established body of work by focusing on an asynchronous level-crossing sampling Flash ADC, which deviates fundamentally from the synchronous current-mode architectures discussed above. While most current-mode designs rely on specialized conveyors, dynamic latch structures, or algorithmic conversion cycles, the approach developed here maintains the intrinsic high-speed advantage of the Flash topology but introduces a bulk-driven offset trimming mechanism that is inherently compatible with event-driven operation. By modulating the threshold voltage V_{th} of the comparator input pair via the body effect using a resistive reference ladder that feeds the bulk terminals, as demonstrated in [**<ref148>**], the proposed architecture achieves precise offset nullification without the high power overhead of complex biasing networks or the speed penalties associated with auto-zeroing and other clock-intensive calibration schemes. In contrast to the majority of these works, which share the common constraint of operating within a synchronous, clock-driven framework and typically do not exploit the time-sparse nature of many sensor signals, the architecture developed here explicitly targets sparsity-aware power reduction while simultaneously addressing comparator mismatch in high-speed Flash ADCs.

2.6 Asynchronous vs. Synchronous

2.6.1 Advantage

The primary motivation for adopting asynchronous architectures is the direct relationship between signal activity and power consumption [86].

In a synchronous system, the clock tree and the comparators switch at every clock cycle, regardless of whether the input is changing, the power consumption is dominated by the fixed clock frequency [10]:

$$P_{sync} \approx f_{clk} \cdot C_{total} \cdot V_{DD}^2 \tag{2.6}$$

In an asynchronous ADC, the switching frequency is replaced by the event rate. If the signal is constant or slowly varying, the comparators and digital logic remain static, leading to the following proportionality:

$$P_{async} \propto Activity \times V_{DD}^2 \tag{2.7}$$

This property ensures that the energy consumed is always proportional to the information content of the signal which makes these ADCs significantly more efficient for sparse signal environments, where they can achieve near-zero power during periods of inactivity.

2.6.2 Comparative Evaluation

An analysis of state-of-the-art converters shows that asynchronous ADCs excel in energy efficiency across a wide range of sampling rates, particularly for low-to-medium bandwidths [86].

While Synchronous Flash ADCs are designed for peak performance at a specific frequency and suffer from a much higher power consumption caused by the continuous clocking, asynchronous designs scale their power consumption linearly with the input activity.

Table 2.3: Comparison of Power Consumption between Synchronous and Asynchronous Flash ADCs. Simulation results from this work showing the power advantage of asynchronous operation for sparse signals.

Topology	**Average power (P [W])**	**No of samples**
Synchronous	0.1016	145
Asynchronous	0.0314	23

The impact of this architectural difference on long-term technology trends is illustrated in Figure 2.13. The plot depicts the energy per conversion (P/f_s) over the last two decades. While both paradigms show a downward trend due to process node scaling, asynchronous designs (indicated by triangular markers) consistently occupy the lower bound of the energy envelope. This suggests that eliminating the global clock is a key enabler for breaking the power efficiency barriers in modern designs.

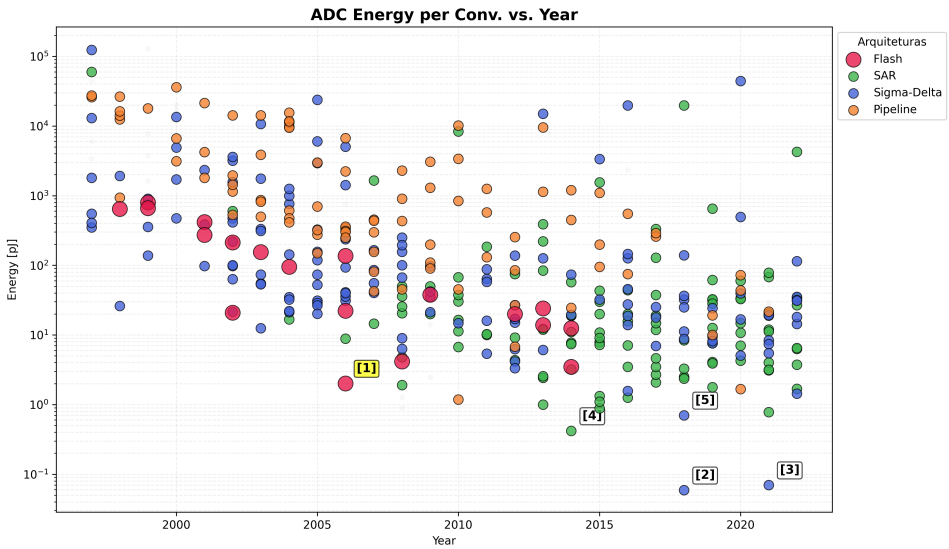

Figure 2.13: Energy per Conversion vs. Year (Flash reference [1] highlighted)

The long-term reduction in energy per conversion step driven by architectural innovation and technology scaling is depicted in Fig. 2.13. Each point in the plot corresponds to a published design, making it possible to compare how different ADC architectures fill the energy year plane

and to identify the most efficient solutions, as shown in Fig. 2.13. From the previous analy-

Table 2.4: Energy per Conversion vs. Year (Flash reference [1] highlighted)

Ref.	Architecture	Publication	Energy [pJ]
[1]	**Flash**	**Chen [23]**	**2.02**
[2]	Sigma-Delta	Jiang [69]	0.059
[3]	Sigma-Delta	Veldhoven [133]	0.070
[4]	SAR	Ginsburg [45]	0.420
[5]	Sigma-Delta	Kim [73]	0.703

sis, it becomes clear that synchronous architectures face a fundamental inefficiency when dealing with time-sparse sensor signals: the global clock forces continuous switching activity, so dynamic power remains proportional to the clock frequency even during long periods with no new information content. In contrast, event-driven schemes naturally decouple power consumption from the Nyquist rate and tie it instead to the actual rate of relevant signal transitions. Combining this observation with the survey data on state-of-the-art converters, where Flash ADCs define the speed frontier but suffer from poor Walden FoM at high sampling rates, while more energy-efficient SAR and sigma-delta architectures are optimized for lower bandwidths, motivates the choice of an asynchronous Flash topology as the core of this work. By removing the global sampling clock and operating comparators in a level-crossing, event-driven manner, the proposed asynchronous Flash ADC aims to preserve the intrinsic low-latency and high-speed advantages of the Flash architecture, while leveraging signal sparsity to significantly improve energy efficiency and close the FoM gap with the best-performing synchronous designs in the targeted operating region.

Chapter 3

Future Work Planning, Methodologies and Tools

This chapter outlines the development strategy for the dissertation, detailing the methodologies, tools, and the schedule for the remaining phases.

3.1 Work Plan

Since the work completed this far covers the introduction and the literature review, future planning focuses on the comprehensive development of the three remaining sections. Chapter 3 will be dedicated to the detailed architecture and the theoretical framework of the asynchronous level-crossing sampling and the bulk voltage trimming mechanism, establishing the necessary design parameters. Chapter 4 will involve the implementation, simulation, and discussion of the results, while Chapter 5 will present the final conclusions and suggestions for future work.

To complete the dissertation according to the established timeline and quality standards, a Gantt Chart is presented in Figure 3.1. The second semester will begin on February 18, 2026, with a deep dive into the theoretical underpinnings of bulk-driven offset compensation, specifically focusing on the threshold voltage modulation via the body effect as discussed in the literature. This initial phase is critical to define the operating limits and calibration strategy of the system before transitioning to the physical implementation. This will be followed by the design and simulation of the asynchronous Flash ADC core and the resistive trimming network in the Cadence Virtuoso environment. Documentation of the technical operating principles will run in parallel with the design phase to ensure accuracy.

Once the circuit achieves basic functionality, Monte Carlo simulations will be performed to evaluate the robustness of the trimming algorithm against random process mismatches. Furthermore, the design will be validated across different process corners to ensure reliability under varying conditions. The results will then be analyzed to quantify improvements in linearity and energy efficiency. After the first version of the dissertation is finalized, a scientific research article will be prepared for submission. Regular meetings with the supervisors will be held throughout the

process to ensure technical consistency. The provisional document will be delivered by June 30, 2026, with the defense scheduled for July 24, and the final document submission by July 31, 2026.

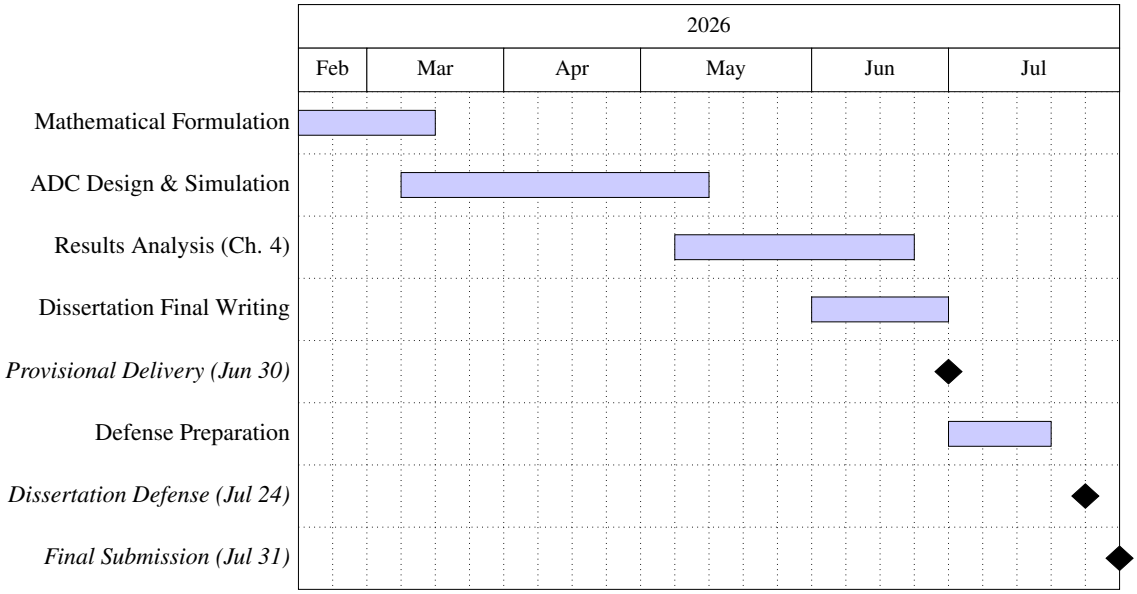

Figure 3.1: Gantt chart summarizing the planned schedule for modelling, circuit design, simulations, documentation, and dissertation milestones throughout the remaining duration of the project.

The second semester will begin on February 18, 2026, with the development of the mathematical model for bulk-driven offset compensation, specifically focusing on the threshold voltage modulation via the body effect as discussed in the literature. This will be followed by the design and simulation of the asynchronous Flash ADC core and the resistive trimming network in the Cadence Virtuoso environment. Once the circuit achieves basic functionality, Monte Carlo simulations will be performed to evaluate the robustness of the trimming algorithm against random process mismatches. The results will then be analyzed to quantify improvements in linearity and energy efficiency. After the first version of the dissertation is finalized, a scientific research article will be prepared for submission. Regular meetings with the supervisors will be held throughout the process to ensure technical consistency. The provisional document will be delivered by June 30, 2026, with the defense scheduled for July 24, and the final document submission by July 31, 2026.

3.2 Methodologies and Tools

The execution of this dissertation follows a methodology focused on academic rigor and effective project management to ensure all objectives are met. A primary practice involves the use of project management tools such as the Gantt chart presented in Figure 3.1 to establish clear milestones and monitor progress. By defining specific tasks and deadlines, it is possible to maintain a structured timeline and ensure that the research and design phases stay on schedule. Another fundamental practice consists of holding biweekly meetings with supervisors to review the work carried out and receive technical feedback. These sessions are essential for validating the circuit design choices and avoiding potential errors in the implementation of the asynchronous logic. Continuous documentation of the findings and simulation results is also prioritized to maintain transparency and facilitate the transition from the research phase to the final writing of the document.

For the development and verification of the proposed asynchronous Flash ADC, the Synopsys software will be used as the primary tool for circuit-level design and simulation.

For transistor-level design and layout implementation, this work relies on the Synopsys Custom Compiler environment, an industrial-grade custom design platform for analog, mixed-signal, and custom digital ICs. The tool provides schematic capture, SPICE-level simulation setup, and full-custom layout editing within a unified cockpit, which is particularly suitable for designing and optimizing high-speed comparator arrays and reference ladders used in Flash ADCs.

In this dissertation, Custom Compiler will be used to implement the asynchronous Flash ADC at transistor level, including device sizing, bias network design, and the resistive trimming structures required for offset calibration. The same environment will also be employed to perform physical layout, run design rule checks (DRC) and layout versus schematic (LVS) verification, and to extract parasitic elements for post-layout simulations, ensuring that the measured figures of merit accurately reflect realistic implementation constraints. This professional toolset allows for precise transistor-level modeling and the verification of the offset trimming mechanism through analog and mixed-signal simulations.

Chapter 4

Conclusions

The work conducted during the first semester has been essential for establishing the technical and theoretical foundations of this dissertation. The increasing demand for high-speed, low-power ADCs in modern system on chip applications drives the need for innovative architectures that can overcome the limitations of traditional designs. In this context, the research into an asynchronous level-crossing sampling Flash ADC with bulk-driven offset trimming can significantly contribute to the development of more efficient data conversion systems for high-bandwidth applications.

A variety of ADC architectures and comparator topologies have been deeply studied to understand their performance trade-offs. The Flash architecture is recognized for its parallel processing capabilities, but its accuracy is often limited by transistor mismatch, which necessitates effective calibration or trimming techniques. Current-mode techniques have been explored as a means to achieve higher speeds and lower power consumption compared to traditional voltage-mode designs. Furthermore, the study of dynamic latch comparators and current conveyors has provided insights into optimizing the delay profile and power dissipation of the conversion core. This research has highlighted that asynchronous level-crossing sampling can reduce the power overhead associated with global clocks, especially during periods of signal inactivity. To address the mismatch inherent in these high-speed comparators, a bulk-driven trimming mechanism utilizing the body effect is proposed, allowing for precise threshold voltage modulation without adding significant parasitic capacitance.

An extensive investigation of existing studies in this field was conducted to ensure the acquisition of the knowledge necessary to develop the mathematical formulation of the proposed system. The bibliographic review confirmed that while current-mode and inverter-based comparators offer high performance, there is a clear opportunity to integrate them into an asynchronous framework with localized trimming. Once the mathematical model for the bulk potential adjustment is finalized, the main challenge ahead will be to prove the effectiveness and robustness of the proposed approach using Synopsys simulation tools. A rigorous analysis through Monte Carlo simulations will be pursued to validate the trimming algorithm against process variations, ensuring a successful trade-off between conversion speed, power efficiency, and linearity.

Bibliography

[1] S. Abe et al. "A 22.3b 1kHz 12.7mW Switched-Capacitor Delta-Sigma Modulator". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2016.

[2] Abhishek Agrawal et al. "A 128Gb/s 1.95pJ/b D-Band Receiver with Integrated PLL and ADC in 22nm FinFET". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067439.

[3] B. Malki et al. "A 70dB DR 10b 0-80MS/s Current Integrating SAR ADC with adaptive Dynamic Range". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2012. DOI: 10.1109/ISSCC.2012.6177095.

[4] C-Y Liou et al. "A 2.4-to-5.2fJ/Conversion-step 10b 0.5-to-4MS/s SAR ADC with Charge Average Switching DAC in 90nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2013. DOI: 10.1109/ISSCC.2013.6487735.

[5] E. Janssen et al. "An 11b 3.6GS/s Time-Interleaved SAR ADC in 65nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2013. DOI: 10.1109/ISSCC.2013.6487816.

[6] P. Harpe et al. "A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with Data-Driven Noise Reduction". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2013. DOI: 10.1109/ISSCC.2013.6487730.

[7] P. Harpe et al. "A 7-to-10b 0-to-4MS/s Flexible SAR ADC with 6.5-to-16fJ/conversion-step". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2012. DOI: 10.1109/ISSCC.2012.6177096.

[8] R. Kapusta et al. "A 14-bit, 80MS/s SAR ADC with 73.6dB SNDR in 65nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2013. DOI: 10.1109/ISSCC.2013.6487820.

[9] Y. Chai et al. "A 5.37mW 10b 200MS/s Dual-Path Pipelined ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2012. DOI: 10.1109/ISSCC.2012.6177091.

[10] R. Jacob Baker. *CMOS: Circuit Design, Layout, and Simulation*. 3rd. John Wiley & Sons, 2010.

[11] P. Balmelli and Qiuting Huang. "A 25 MS/s 14 b 200 mW ΣΔ modulator in 0.18 μm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2004. DOI: 10.1109/ISSCC.2004.1332600.

[12] Rares Bodnar et al. "A 9.3nV/rtHz 20b 40MS/s 94.2dB DR Signal-Chain Friendly Precision SAR Converter". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454329.

[13] H. H. Boo, D. S. Boning, and H-S. Lee. "A 12b 250MS/s Pipelined ADC with Virtual Ground Reference Buffers". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2015. DOI: 10.1109/ISSCC.2015.7063036.

[14] L.J. Breems et al. "A 56mW CT Quadrature Cascaded ΣΔ Modulator with 77dB DR in a Near Zero-IF 20MHz Band". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2007. DOI: 10.1109/ISSCC.2007.373382.

[15] K. Bult, A. Buchwald, and J. Laskowski. "A 170 mW 10 b 50 Msample/s CMOS ADC in 1 mm²". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1997. DOI: 10.1109/ISSCC.1997.585303.

[16] J. C. Candy and G. C. Temes. "Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation". In: *IEEE Transactions on Circuits and Systems* CAS-32.12 (1985), pp. 1306–1318.

[17] Yue Cao et al. "A 1GS/s Single-Channel Pipelined ADC with a Parallel-Operation SAR Sub-Quantizer and a Dynamic-Deadzone Ring Amplifier". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904766.

[18] Yuefeng Cao et al. "A 12GS/s 12b 4× Time-Interleaved Pipelined ADC with Comprehensive Calibration of TI Errors and Linearized Input Buffer". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454350.

[19] Yuefeng Cao et al. "A Single-Channel 12b 2GS/s PVT-Robust Pipelined ADC with Ringingless Ring Amplifier and Time-Domain Quantizer". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067687.

[20] Y. Chae, I. Lee, and G. Han. "A 0.7V 36uW 85dB-DR Audio delta-sigma Modulator Using a Class-C Inverter". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2008. DOI: 10.1109/ISSCC.2008.4523271.

[21] C-H. Chan et al. "A 5.5mW 6b 5GS/s 4-times Interleaved 3b/cycle SAR ADC in 65nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2015. DOI: 10.1109/ISSCC.2015.7063128.

[22] Feng Chen, S. Ramaswamy, and B. Bakkaloglu. "A 1.5V 1mA 80dB passive ΣΔ ADC in 0.13μm digital CMOS process". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2003. DOI: 10.1109/ISSCC.2003.1234204.

[23] S.-W. Chen and R. W. Brodersen. "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-um CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006, pp. 574–583. DOI: 10.1109/ISSCC.2006.1695276.

[24] Zhuoyi Chen et al. "A 182.3dB FoMs 50MS/s Pipelined-SAR ADC using Cascode Capacitively Degenerated Dynamic Amplifier and MSB Pre-Conversion Technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454297.

[25] Zhuoyi Chen et al. "An Easy-Drive 16MS/s Pipelined-SAR ADC Using Split Coarse-Fine Input Buffer Sampling Scheme and Fast-Robust Background Inter-Stage Gain Calibration". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904526.

[26] Kai-Cheng Cheng et al. "A 94.3dB SNDR 184dB FoMs 4th-Order Noise-Shaping SAR ADC with Dynamic-Amplifier-Assisted Cascaded Integrator". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454362.

[27] Kyojin D. Choo, John Bell, and Michael P Flynn. "Area-Efficient 1GS/s 6b SAR ADC with Charge-Injection-Cell-Based DAC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2016. DOI: 10.1109/ISSCC.2016.7418106.

[28] T. Christen, T. Burger, and Qiuting Huang. "A 0.13μm CMOS EDGE/UMTS/WLAN Tri-Mode $\Delta\Sigma$ ADC with -92dB THD". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2007. DOI: 10.1109/ISSCC.2007.373383.

[29] A.L. Coban and P.E. Allen. "A 1.5 V 1.0 mW audio $\Delta\Sigma$ modulator with 98 dB dynamic range". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1999. DOI: 10.1109/ISSCC.1999.759091.

[30] P. De Cano-Garcia et al. "A 1.41fJ/conv-step 20MS/s SAR ADC in 14nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2019.

[31] M. Delic-Ibuspachic et al. "A 120dB SNDR Audio Sigma-Delta Modulator". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2013.

[32] Siddharth Devarajan et al. "A 16b 125MS/s 385mW 78.7dB SNR CMOS Pipeline ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2009. DOI: 10.1109/ISSCC.2009.4977320.

[33] A. Dezzani and E. Andre. "A 1.2-V dual-mode WCDMA/GPRS $\Sigma\Delta$ modulator". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2003. DOI: 10.1109/ISSCC.2003.1234206.

[34] M. Ding et al. "A 5.5fJ/conv.step 6.4MS/s 13b SAR ADC utilizing a redundancy facilitated background error-detection and correction scheme". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2015. DOI: 10.1109/ISSCC.2015.7063125.

[35] L. Dorrer et al. "A 3mW 74dB SNR 2MHz CT ΔΣ ADC with a tracking-ADC-quantizer in 0.13 μm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2005. DOI: 10.1109/ISSCC.2005.1494084.

[36] D. Draxelmayr et al. "A 2.2-GS/s 7-bit ADC with 37.4 dB SNDR". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2014. DOI: 10.1109/ISSCC.2014.6757514.

[37] M. Flynn and B. Sheahan. "A 400Msample/s 6b CMOS folding and interpolating ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1998. DOI: 10.1109/ISSCC.1998.672412.

[38] P. Fontaine, A.N. Mohieldin, and A. Bellaouar. "A low-noise low-voltage CT ΔΣ modulator with digital compensation of excess loop delay". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2005. DOI: 10.1109/ISSCC.2005.1494087.

[39] Y. Fujimoto et al. "An 80/100MS/s 76.3/70.1dB SNDR ΔΣ ADC for Digital TV Receivers". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006. DOI: 10.1109/ISSCC.2006.1696049.

[40] R. Gaggl, M. Inversi, and A. Wiesbauer. "A power optimized 14-bit SC ΔΣ modulator for ADSL CO applications". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2004. DOI: 10.1109/ISSCC.2004.1332604.

[41] Jihang Gao et al. "A 93.3dB SNDR, 180.4dB FoMS Calibration-Free Noise-Shaping Pipelined-SAR ADC with Cross-Stage Gain-Mismatch-Error-Shaping Technique and Negative-R-Assisted Residue Integrator". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904557.

[42] G. Geelen. "A 5V, 118dB Delta-Sigma ADC for Wideband Digital Audio". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1997.

[43] Govert Geelen and Edward Paulus. "An 8b 600MS/s 200mW CMOS folding A/D converter using an amplifier preset technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2004. DOI: 10.1109/ISSCC.2004.1332690.

[44] Govert Geelen et al. "A 90nm CMOS 1.2V 10b Power and Speed Programmable Pipelined ADC with 0.5pJ/Conversion-Step". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006. DOI: 10.1109/ISSCC.2006.1696118.

[45] B. P. Ginsburg et al. "A 0.42-pJ/step SAR ADC in 28nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2014.

[46] J. Goes et al. "A 0.9V Delta-Sigma Modulator with 80dB SNDR and 83dB DR Using a Single-Phase Technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006. DOI: 10.1109/ISSCC.2006.1696048.

[47] B. Gregoire and U-K. Moon. "An Over-60dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp with 30dB Loop Gain". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2008. DOI: 10.1109/ISSCC.2008.4523296.

[48] Mingyang Gu et al. "A 12b 3GS/s Pipelined ADC with Gated-LMS-Based Piecewise-Linear Nonlinearity Calibration". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904536.

[49] C. Hammerschmied and Q. Huang. "A MOSFET-only, 10 b, 200 ksample/s A/D converter capable of 12 b untrimmed linearity". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1997. DOI: 10.1109/ISSCC.1997.585301.

[50] Junyan Hao et al. "A Single-Channel 2.6GS/s 10b Dynamic Pipelined ADC with Time-Assisted Residue Generation Scheme Achieving Intrinsic PVT Robustness". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067822.

[51] P. Harpe, E. Cantatore, and A. van Roermund. "An Oversampled 12b/14b SAR ADC with Noise Reduction and Linearity Enhancements Achieving up to 79.1dB SNDR". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2014. DOI: 10.1109/ISSCC.2014.6757396.

[52] P. Harpe et al. "A 3nW Signal-Acquisition IC Integrating an Amplifier with 2.1 NEF and a 1.5fJ/conv-step ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2015. DOI: 10.1109/ISSCC.2015.7063086.

[53] Xiyu He et al. "A 71dB SNDR 200MHz BW Interleaved Pipe-SAR ADC with a Shared Residue Integrating Amplifier Achieving 173dB FoMs". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454431.

[54] Benjamin Hershberg et al. "A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2019. DOI: 10.1109/ISSCC.2019.8662290.

[55] M. Hesener et al. "A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13pm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2007. DOI: 10.1109/ISSCC.2007.373387.

[56] H-K. Hong et al. "A 2.6b/cycle-architecture-based 10b 1.7GS/s 15.4mW 4x Time-interleaved SAR ADC with a Multi-step Hardware Retirement Technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2015. DOI: 10.1109/ISSCC.2015.7063130.

[57] Gian Hoogzaad and Raf Roovers. "A 65 mW 10 b 40 Msample/s BiCMOS Nyquist ADC in 0.8 mm 2". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1999. DOI: 10.1109/ISSCC.1999.759268.

[58] Cheng-En Hsieh et al. "A Power- and Area-Efficient 4nm Self-Calibrated 12b/16GS/s Hierarchical Time-Interleaving ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904740.

[59] Sung-En Hsieh, Tzu-Chien Wu, and Chun-Chih Hou. "A 1.8-GHz 12-bit Pre-Sampling pipelined ADC with the reference buffer and OP power relaxations". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067258.

[60] Cheng-Chung Hsu et al. "An 11-Bit 800-MS/s Time-Interleaved ADC with Digital Background Calibration". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2007. DOI: 10.1109/ISSCC.2007.373495.

[61] Y. Hu et al. "A 2.87μW 1kHz-BW 94.0dB-SNDR 2-0 MASH ADC using FIA with Dynamic-Body-Biasing Assisted CLS Technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731544.

[62] Sheng-Jui Huang and Yung-Yu Lin. "A 1.2V 2MHz BW 0.084mm² CT ΔΣ ADC with -97.7dBc THD and 80dB DR Using Low-Latency DEM". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2009. DOI: 10.1109/ISSCC.2009.4977363.

[63] Y-C. Huang and T-C. Lee. "A 10b 100MS/s 4.5mW Pipelined ADC with a Time Sharing Technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2010. DOI: 10.1109/ISSCC.2010.5433927.

[64] D.J. Huber, R.J. Chandler, and A.A. Abidi. "A 10b 160MS/s 84mW 1V Subranging ADC in 90nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2007. DOI: 10.1109/ISSCC.2007.373490.

[65] T. Jang et al. "A 0.61fJ/conv-step 270kS/s SAR ADC with Charge-Average-Loop-Preset Technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2018. DOI: 10.1109/ISSCC.2018.8310276.

[66] T. Jang et al. "A 118dB DR Delta-Sigma Modulator for Audio Applications". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2018.

[67] Young-Deuk Jeon et al. "A 4.7mW 0.32mm² 10b 30MS/s Pipelined ADC Without a Front-End S/H in 90nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2007. DOI: 10.1109/ISSCC.2007.373491.

[68] Kyeongwon Jeong et al. "A 3.47 NEF 175.2dB FOMS Direct Digitization Front-End Featuring Delta Amplification for Enhanced Dynamic Range and Energy Efficiency in Bio-Signal Acquisition". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904745.

[69] H. Jiang et al. "A 0.059-pJ/conv-step Sigma-Delta ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2018.

[70] David A. Johns and Ken Martin. *Analog Integrated Circuit Design*. 2nd. John Wiley & Sons, 2012.

[71] Joseph Ingino Jr. and Bruce Wooley. "A continuously-calibrated 10Msample/s 12b 3.3V ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1998. DOI: 10.1109/ISSCC.1998.672409.

[72] T. Kang et al. "A Multimode 157μW 4-Channel 80dBA-SNDR Speech-Recognition Frontend With Self-DOA Correction Adaptive Beamformer". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731571.

[73] G. Kim et al. "A 0.3V Biofuel-Cell-Powered Glucose/Lactate Biosensing System Integrating a 142nW ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2018. DOI: 10.1109/ISSCC.2018.8310240.

[74] Geunha Kim et al. "A 1V-Supply 1.85VPP-Input-Range 1kHz-BW 181.9dB-FOMDR 179.4dB-FOMSNDR 2nd-Order Noise-Shaping SARADC with Enhanced Input Impedance in 0.18μm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067844.

[75] Hwi-Cheol Kim, Deog-Kyoon Jeong, and Wonchan Kim. "A 30mW 8b 200MS/s pipelined CMOS ADC using a switched-opamp technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2005. DOI: 10.1109/ISSCC.2005.1493980.

[76] Jinseok Koh, Yunyoung Choi, and G. Gomez. "A 66dB DR 1.2V 1.2mW single-amplifier double-sampling 2nd-order $\Delta\Sigma$ ADC for WCDMA in 90nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2005. DOI: 10.1109/ISSCC.2005.1493923.

[77] Sandeep Santhosh Kumar et al. "A 750mW 24GS/s 12-bit Time Interleaved ADC for Direct RF Sampling in Modern Wireless Systems". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067793.

[78] S.-U. Kwak, B.-S. Song, and K. Bacrania. "A 15 b 5 MSample/s low-spurious CMOS ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1997. DOI: 10.1109/ISSCC.1997.585309.

[79] C. Y. Lee and U-K. Moon. "A 0.0375mm2 203.5μW 108.8dB DR DT Single-Loop DSM Audio ADC Using a Single- Ended Ring-Amplifier-Based Integrator in 180nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731606.

[80] Jaewon Lee et al. "A 353mW 112Gb/s Discrete Multitone Wireline Receiver Datapath with Time-Based ADC in 5nm FinFET". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904707.

[81] Jongmi Lee et al. "A 6th-Order Quadrature CTDSM using Double-OTA and Quadrature NSSAR with 171.3dB FoMs in 14nm". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454568.

[82] Sangheon Lee et al. "A 1.2V High-Voltage-Tolerant Bootstrapped Analog Sampler in 12-bit SAR ADC Using 3nm GAA's 0.7V Thin-Gate-Oxide Transistor". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454351.

[83] Seung-Chul Lee et al. "A 10b 205MS/s 1.0mm² 90nm CMOS Pipeline ADC for Flat Panel Display Applications". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2007. DOI: 10.1109/ISSCC.2007.373492.

[84] Sewon Lee, Hyein Kang, and Minjae Lee. "A 2.72fJ/conv 13b 2MS/s SAR ADC Using Dynamic Capacitive Comparator with Wide Input Common Mode". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454566.

[85] Manxin Li et al. "A Rail-to-Rail 12MS/s 91.3dB SNDR 94.1dB DR Two-Step SAR ADC with Integrated Input Buffer Using Predictive Level-Shifting". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067703.

[86] Y. Lim, S. Salehi, et al. "Asynchronous Level-Crossing Sampling ADC for Bio-Signals". In: *IEEE Transactions on Biomedical Circuits and Systems* 7.3 (2013).

[87] Yong Lim et al. "A 2.08mW 64.4dB SNDR 400MS/s 12b Pipelined-SAR ADC using Mismatch and PVT Variation Tolerant Dynamically Biased Ring Amplifier in 8nm". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454422.

[88] Chin-Yu Lin, Yen-Hsin Wei, and Tai-Cheng Lee. "A 10b 2.6GS/s Time-Interleaved SAR ADC with Background Timing-Skew Calibration". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2016. DOI: 10.1109/ISSCC.2016.7418110.

[89] Ying-Zu Lin et al. "A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC with Passive Signal-Residue Summation in 14nm FinFET". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2019. DOI: 10.1109/ISSCC.2019.8662299.

[90] C-C. Liu et al. "A 10b 100MS/s 1.13mW SAR ADC with Binary-Scaled Error Compensation". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2010. DOI: 10.1109/ISSCC.2010.5433970.

[91] Chun-Cheng Liu. "A 0.35mW 12b 100MS/s SAR-Assisted Digital Slope ADC in 28nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2016. DOI: 10.1109/ISSCC.2016.7418107.

[92] J. Liu, M. Hassanpourghadi, and M. S-W. Chen. "A 10GS/s 8b 25fJ/c-s 2850um2 Two-Step Time-domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731625.

[93] Q. Liu et al. "A 5GS/s 360MHz-BW 68dB-DR Continuous-Time 1-1-1 Filtering MASH ΔΣ ADC in 40nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731789.

[94] W. Liu, P. Huang, and Y. Chiu. "A 12b 22.5/45MS/s 3.0mW 0.059mm² CMOS SAR ADC Achieving Over 90dB SFDR". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2010. DOI: 10.1109/ISSCC.2010.5433830.

[95] Zijian Liu et al. "A 10b 3GS/s Time-Domain ADC with Mutually Exclusive Metastability Correction and Wide Common-Mode Input". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904818.

[96] Yaohui Luan et al. "A 12.2μW 99.6dB-SNDR 184.8dB-FOMS DT Zoom PPD ΔΣM with Gain-Embedded Bootstrapped Sampler". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904732.

[97] C. Lukas et al. "A 20-GS/s 6-bit Interleaved ADC with 1.2-V Supply". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2014. DOI: 10.1109/ISSCC.2014.6757512.

[98] Ewout Martens et al. "A 42GS/s 7b 16nm Massively Time-Interleaved Slope-ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454361.

[99] MathWorks. *Measuring Offset and Gain Errors in ADC*. Accessed: Jan. 12, 2026. 2024. URL: https://www.mathworks.com/help/msblks/ug/offset-error-and-gain-error.html.

[100] F. Michel and M. Steyaert. "A 250mv 7.5μw 61dB SndR cMoS Sc ΔΣ Modulator using a near-Threshold-voltage-Biased cMoS inverter Technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2011. DOI: 10.1109/ISSCC.2011.5746404.

[101] G. Mitteregger et al. "A 14b 20mW 640MHz CMOS CT ΔΣ ADC with 20MHz Signal Bandwidth and 12b ENOB". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006. DOI: 10.1109/ISSCC.2006.1696042.

[102] Monolithic Power Systems. *MPScholar*. https://www.monolithicpower.com/en/learning/mpscholar/analog-to-digital-converters/adc-errors-and-compensation/sources-of-errors-in-adcs. Accessed: Jan. 9, 2026.

[103] R. Muller et al. "A 3nW Signal-Acquisition IC Integrating an Amplifier and a 1.5fJ/conv-step ADC". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2015.

[104] Vaibhav Nijhawan et al. "Design of Current Mode Low Power Flash ADC Structure for High Speed Circuits". In: *2022 9th International Conference on Computing for Sustainable Global Development (INDIACom)*. 2022 9th International Conference on Computing for Sustainable Global Development (INDIACom). Mar. 2022, pp. 255–260. DOI: 10.23919/INDIACom54597.2022.9763285. URL: https://ieeexplore.ieee.org/document/9763285/ (visited on 11/11/2025).

[105] A.K. Ong and B.A. Wooley. "A two-path bandpass ΣΔ modulator for digital IF extraction at 20 MHz". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1997. DOI: 10.1109/ISSCC.1997.585337.

[106] Kieren Pae and Ifana Mahbub. "A Low-Power Asynchronous Level Crossing ADC Designed in 180 nm CMOS Process for Electrophysiological Signal Recording Applications". In: *2022 IEEE 15th Dallas Circuits and Systems Conference (DCAS)*. 2022, pp. 1–4. DOI: 10.1109/DCAS53974.2022.9845498.

[107] Divya Panchal et al. "DESIGN OF 2-BIT FLASH ADC BASED ON CC-II". In: 2.1 ().

[108] Sharvil Patil et al. "A 700MHz-BW –164dBFS/Hz-Small-Signal-NSD 703mW Continuous-Time Pipelined ADC with On-Chip Digital Reconstruction Achieving <-85dBFS HD3 using Digital Cancellation of DAC Errors". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454477.

[109] R. J. van de Plassche. "Integrated Analog-to-Digital and Digital-to-Analog Converters". In: (1994).

[110] Hendrik van der Ploeg and Robert Remmers. "A 3.3V 10b 25Msample/s two-step ADC in 0.35µm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1999. DOI: 10.1109/ISSCC.1999.759267.

[111] C. Pochet and D. Hall. "A 4.4μW 2.5kHz-BW 92.1dB-SNDR 3rd-Order VCO-Based ADC with Pseudo Virtual Ground Feedforward Linearization". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731549.

[112] Liang Qi et al. "A 76.6dB-SNDR 50MHz-BW 29.2mW Noise-Coupling-Assisted CT Sturdy MASH ΔΣ Modulator with 1.5b/4b Quantizers in 28nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2019. DOI: 10.1109/ISSCC.2019.8662529.

[113] Sourja Ray and Bang-Sup Song. "A 13b Linear 40MS/s Pipelined ADC with Self-Configured Capacitor Matching". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006. DOI: 10.1109/ISSCC.2006.1696125.

[114] Behzad Razavi. *Microelectronics*. Prentice Hall, 1998.

[115] R. Schreier and G. C. Temes. "Understanding Delta-Sigma Data Converters". In: (2005).

[116] P. Schvan et al. "A 22GS/s 5b adc in 0.13/spl mu/m SiGe BiCMOS". In: *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*. IEEE, 2006, 2340â€"2349. DOI: 10.1109/isscc.2006.1696297. URL: http://dx.doi.org/10.1109/ISSCC.2006.1696297.

[117] P. Schvan et al. "A 22GS/s 5b ADC in 130nm SiGe BiCMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006. DOI: 10.1109/ISSCC.2006.1696297.

[118] P. Schvan et al. "A 24GS/s 6b ADC in 90nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2008. DOI: 10.1109/ISSCC.2008.4523298.

[119] Y. Segal et al. "A 1.41pJ/b 224Gb/s PAM-4 SerDes Receiver with 31dB Loss Compensation". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731794.

[120] D. Senderowicz et al. "Low-voltage double-sampled ΣΔ converters". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1997. DOI: 10.1109/ISSCC.1997.585336.

[121] C. E. Shannon. *Communication in the Presence of Noise*. Vol. 37. 1. 1949, pp. 10–21.

[122] Jyoti Sharma et al. "Design of 3-bit Current Mode Flash ADC". In: *2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*. 2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT). May 2018, pp. 652–657. DOI: 10.1109/RTEICT42901.2018.9012379. URL: https://ieeexplore.ieee.org/document/9012379/ (visited on 11/11/2025).

[123] Junhua Shen et al. "A 12GS/s 9b 16× Time-Interleaved SAR ADC in 16nm FinFET". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904660.

[124] Y. Shimizu et al. "A Split-Load Interpolation-Amplifier-Array 300MS/s 8b Subranging Adc in 90nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2008. DOI: 10.1109/ISSCC.2008.4523302.

[125] Yasuhide Shimizu et al. "A 30mW 12b 40MS/s Subranging ADC with a High-Gain Offset-Canceling Positive-Feedback Amplifier in 90nm Digital CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006. DOI: 10.1109/ISSCC.2006.1696120.

[126] P.G.R. Silva et al. "An 118dB DR CT IF-to-Baseband ΣΔ Modulator for AM/FM/IBOC Radio Receivers". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006. DOI: 10.1109/ISSCC.2006.1696044.

[127] Anand Subramanian et al. "A 118.5dBA DR 3.3mW Audio ADC with a Class-B Resistor DAC, Non-Overlap DEM and Continuous-Time Quantizer". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454526.

[128] A. Tabatabaei et al. "A dual channel ΣΔ ADC with 40MHz aggregate signal bandwidth". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2003. DOI: 10.1109/ISSCC.2003.1234210.

[129] Y. Tamba and K. Yamakido. "A CMOS 6 b 500 MSample/s ADC for a hard disk drive read channel". In: *1999 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC. First Edition (Cat. No.99CH36278)*. ISSCC-99. IEEE, 324â€"325. DOI: 10.1109/isscc.1999.759272. URL: http://dx.doi.org/10.1109/ISSCC.1999.759272.

[130] Yuko Tamba and Kazuo Yamakido. "A CMOS 6b 500MSample/s ADC for a hard disk drive read channel". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 1999. DOI: 10.1109/ISSCC.1999.759272.

[131] Yunsong Tao et al. "A 4.8GS/s 7-ENoB Time-Interleaved SAR ADC with Dither-Based Background Timing-Skew Calibration and Bit-Distribution-Based Background Ping-Pong Comparator Offset Calibration". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454299.

[132] Yunsong Tao et al. "An 8b 10GS/s 2-Channel Time-Interleaved Pipelined ADC with Concurrent Residue Transfer and Quantization, and Automatic Buffer Power Gating". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904751.

[133] E. Van Veldhoven et al. "A Sub-pJ Energy-Efficient ADC for IoT". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2021.

[134] Bram Veraverbeke and Filip Tavernier. "A Cryo-CMOS 800MS/s 7b CI-SAR with only 4fF Input Capacitance and 64dB SFDR". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904533.

[135] Naveen Verma and Anantha Chandrakasan. "A 25μW 100kS/s 12b ADC for Wireless Micro-Sensor Applications". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2006. DOI: 10.1109/ISSCC.2006.1696122.

[136] K. Vleugels, S. Rabii, and B.A. Wooley. "A 2.5 V broadband multi-bit ΣΔ modulator with 95 dB dynamic range". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2001. DOI: 10.1109/ISSCC.2001.912541.

[137] Patrick Vogelmann, Michael Haas, and Maurits Ortmanns. "A 1.1mW 200kS/s Incremental ΔΣ ADC with a DR of 91.5dB Using Integrator Slicing for Dynamic Power Reduction". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2018. DOI: 10.1109/ISSCC.2018.8310271.

[138] M. Waltari et al. "A self-calibrated pipeline ADC with 200MHz IF-sampling frontend". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2002. DOI: 10.1109/ISSCC.2002.993058.

[139] Chi-Yun (Stanley) Wang et al. "An 80MHz-BW 31.9fJ/conv-step Filtering ΔΣ ADC with a Built-In DAC-Segmentation/ELDCompensation 6b 960MS/s SAR-Quantizer in 28nm LP for 802.11ax Applications". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2019. DOI: 10.1109/ISSCC.2019.8662416.

[140] Yi-Hu Wang and Soon-Jyh Chang. "A 7b 4.5GS/s 4× Interleaved SAR ADC with Fully On-Chip Background Timing Skew Calibration". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067573.

[141] J-C. Wang and T-H. Kuo. "A 0.82mW 14b 130MS/s Pipelined-SAR ADC with a Distributed Averaging Correlated Level Shifting (DACLS) Ringamp and Bypass-Window Backend". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731546.

[142] Jia-Ching Wang and Tai-Haur Kuo. "A 3-mW 2.7-GS/s 8b Subranging ADC with Multiple-Reference-Embedded Comparators". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067498.

[143] R. Wang et al. "A 3.3 mW 12 MS/s 10b pipelined ADC in 90 nm digital CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2005. DOI: 10.1109/ISSCC.2005.1493977.

[144] T. Wang et al. "An 84dB-SNDR Low-OSR 4th-Order Noise-Shaping SAR with an FIA-Assisted EF-CRFF Structure and Noise-Mitigated Push-Pull Buffer-in-Loop Technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731771.

[145] H. Wei et al. "A 0.024mm² 8b 400MS/s SaR adc with 2b/cycle and Resistive dac in 65nm cMoS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2011. DOI: 10.1109/ISSCC.2011.5746276.

[146] Amy Whitcombe et al. "A 76mW 40GS/s 7b Time-Interleaved Hybrid Voltage/Time-Domain ADC with Common-Mode Input Tracking". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454355.

[147] Jianxiong Xu et al. "Event-Based Spatially Zooming Neural Interface IC with 10nW/Input Reconfigurable-Inverter Fabric and Input-Adaptive Quantization". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904733.

[148] S. Yan and E. Sanchez-Sinencio. "A continuous-time ΣΔ modulator with 88dB dynamic range and 1.1MHz signal bandwidth". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2003. DOI: 10.1109/ISSCC.2003.1234208.

[149] J. Yao, J. Liu, and H. Lee. "Bulk Voltage Trimming Offset Calibration for High-Speed Flash ADCs". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 57.2 (2010), pp. 110–114. DOI: 10.1109/TCSII.2010.2040317.

[150] L. Yao. "Bulk-Driven Switched-Opamp Integrator for Low-Voltage Low-Power Data Converters". In: *IEEE Journal of Solid-State Circuits* 46.10 (2011).

[151] L. Yao, M. Steyaert, and W. Sansen. "A 1 V 88 dB 20 kHz ΣΔ modulator in 90 nm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2004. DOI: 10.1109/ISSCC.2004.1332603.

[152] F. M. Yaul and A. P. Chandrakasan. "A 10b 0.6nW leakage SAR ADC with data-dependent energy savings using LSB-first successive approximation". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2014. DOI: 10.1109/ISSCC.2014.6757398.

[153] Siyuan Ye et al. "A 2mW 70.7dB SNDR 200MS/s Pipelined-SAR ADC with Continuous-Time SAR-Assisted Detect-and-Skip and Open-then-Close Correlated Level Shifting". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. DOI: 10.1109/ISSCC49657.2024.10454412.

[154] Siyuan Ye et al. "A Rail-to-Rail 3rd-Order Noise-Shaping SAR ADC Achieving 105.4dB SFDR with Integrated Input Buffer Using Continuous-Time Correlated Level Shifting". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904773.

[155] Serdar Abdullah Yonar et al. "An 8b 1.0-to-1.25GS/s 0.7-to-0.8V Single-Stage Time-Based Gated-Ring-Oscillator ADC with 2X- Interpolating Sense-Amplifier-Latches". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067745.

[156] Kentaro Yoshioka et al. "A 0.7V 12b 160MS/s 12.8fJ/conv-step Pipelined-SAR ADC in 28nm CMOS with Digital Amplifier Technique". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2017. DOI: 10.1109/ISSCC.2017.7870469.

[157] M. Yoshioka et al. "A 0.8V 10b 80MS/s 6.5mW Pipelined ADC with Regulated Overdrive Voltage Biasing". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2007. DOI: 10.1109/ISSCC.2007.373489.

[158] M. Yoshioka et al. "A 10 b 125 MS/s 40 mW pipelined ADC in 0.18 μm CMOS". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2005. DOI: 10.1109/ISSCC.2005.1493979.

[159] M. Yoshioka et al. "A 10b 50MS/s 820μW SAR ADC with On-Chip Digital Calibration". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2010. DOI: 10.1109/ISSCC.2010.5433965.

[160] Jiang Yu and F. Maloberti. "A low-power multi-bit $\Delta\Sigma$ modulator in 90nm digital CMOS without DEM". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2005. DOI: 10.1109/ISSCC.2005.1493922.

[161] M. Zhan et al. "A 0.004mm2 200MS/s Pipelined SAR ADC with kT/C Noise Cancellation and Robust Ring-Amp". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731599.

[162] Mingtao Zhan, Lu Jie, and Nan Sun. "A 10mW 10-ENoB 1GS/s Ring-Amp-Based Pipelined TI-SAR ADC with Split MDAC and Switched Reference Decoupling Capacitor". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067475.

[163] Hongshuai Zhang et al. "A 25MHz-BW 77.2dB-SNDR 2nd-Order Gain Error Shaping and NS Pipelined SAR ADC Based on Quantization-Prediction-Unrolled Scheme". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067438.

[164] Minglei Zhang et al. "A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2019. DOI: 10.1109/ISSCC.2019.8662350.

[165] Yanbo Zhang et al. "A Single-channel 70dB-SNDR 100MHz-BW 4th-Order Noise-Shaping Pipeline SAR ADC with Residue Amplifier Error Shaping". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067687.

[166] Yannan Zhang et al. "A 72GS/s 9b Time-Interleaved Pipeline-SAR ADC Achieving 55.3/49.3dB SFDR at 20GHz/Nyquist Inputs in 16nm FinFET". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904672.

[167] H. Zhao and F. F. Dai. "A 0.97mW 260MS/s 12b Pipelined-SAR ADC with Ring-TDC-Based Fine Quantizer for PVT Robust Automatic Cross-Domain Scale Alignment". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2022. DOI: 10.1109/ISSCC42614.2022.9731702.

[168] Han Zhao et al. "A Fully Dynamic Noise-Shaping SAR ADC Achieving 120dB SNDR and 189dB FoMS in 1kHz BW". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904778.

[169] Hongzhi Zhao et al. "A 2×-Interleaved 9b 2.8GS/s 5b/cycle SAR ADC with Linearized Configurable V2T Buffer Achieving >50dB SNDR at 3GHz Input". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2023. DOI: 10.1109/ISSCC42615.2023.10067627.

[170] Junlin Zhong et al. "A PVT-Robust 2× Interleaved 2.2GS/s ADC with Gated-CCRO-Based Quantizer Shared Across Channels and Steps Achieving >4.5GHz ERBW". In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2025. DOI: 10.1109/ISSCC49661.2025.10904585.