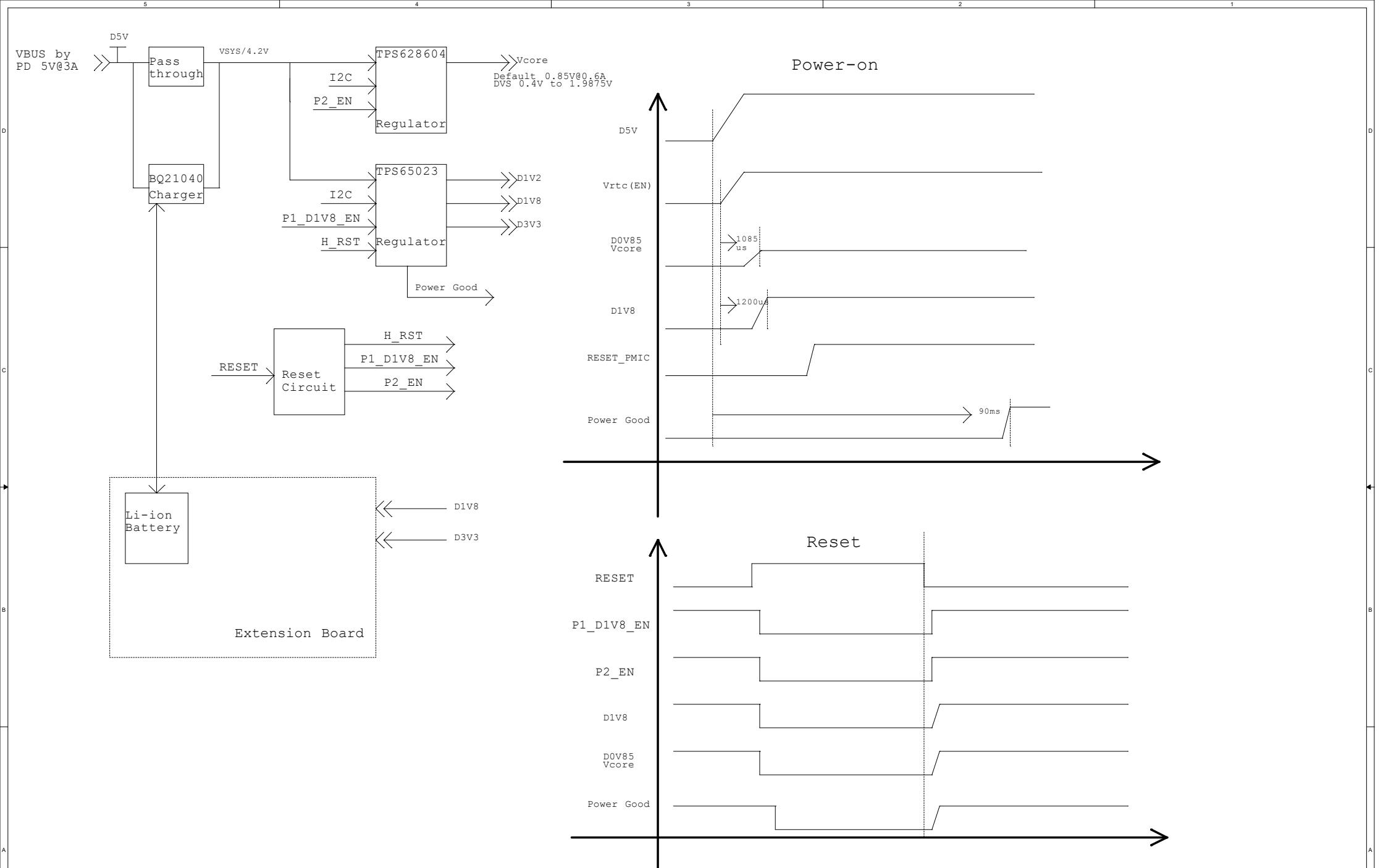


Version	Description
0.1	<p>1. Initial</p> <p>2. Fixed IO:a.AON_I2C0_PMIC b.JTAG c.UART0_ISP d.OSPI_nor_flash</p> <p>3. Flex IO & conetc to extension board:a.AON_I2C1 b.AON_PWM c.AON_ADC d.AON_SPI1 e.SPI_LCD f.SPI0 g.GPIO for RTC & AON h.PMIC_CTRL</p> <p>4. Extension board pin count:IO x 21. Gnd x 11. P: 8</p>
0.2	1. Fix typo
0.3	<p>1. CON1 add 40 more pin</p> <p>2. Change U13 footprint</p>
0.4	<p>1. U11 & U12 Change footprint from TSSOP to UQFN</p> <p>2. PCB dimension change to 31mm x 51mm.</p>
0.5	<p>1. Change U2 footprint from SOIC-8 to USON8</p> <p>2. PCB dimension change to 31mm x 61mm.</p>
0.6	<p>1. U7 change to CON1</p> <p>2. Modify SOT23 footprint</p> <p>3. CON1 add pin5 & 6</p> <p>4. Add 90ohm impedance, 4-5.5-4</p>
0.7	<p>1. U7 change to CON2</p> <p>2. Modify SOT23 footprint</p>
0.8	<p>1. Add pull up R on Flash reset pin</p> <p>2. Add C55 on RESET#_FT</p> <p>3. R72 connect to D1V8_IO</p> <p>4. R34 connect to Vrtc</p> <p>5. Remove Q1 & Q2, add U14 & U15</p>
0.9	<p>1. Change Y2 ground from GND_USB to DGND</p> <p>2. Add silkscreen</p>
1.0	Release
1.1	<p>1. D1V8 at U13/pin 5 issue.==> D1V8 change to Vrtc.</p> <p>2. The voltage at Vbat is over 4.6V when disconneted li-ion battery ==>add divide R84/R85 to reduce voltage to UP201</p> <p>3. The 1V8 from TPS65023 can not drop to 0V when disable this power rail ==> only drop to 0.5V and seems chip internally issue.</p> <p>4. Add CB22.</p> <p>5. Add power sw IC for nor-flash power rail.</p> <p>6. Change 32.768K crystal from DIP to SMD.</p>
1.2	<p>1. Change the power for EN_DVS pull up from Vrtc to Vsyst</p> <p>2. Change the power for U16 EN pull up from D1V8 to Vrtc</p>

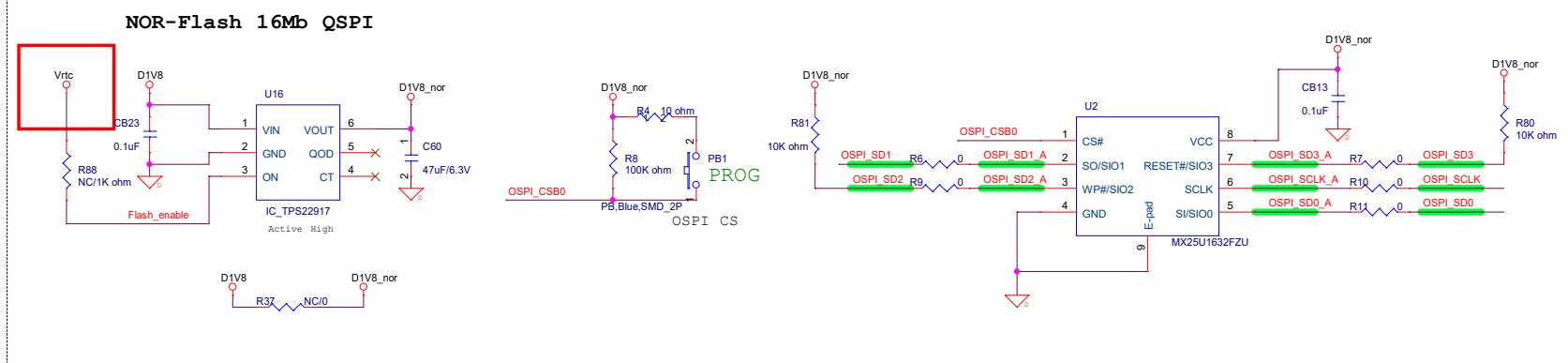
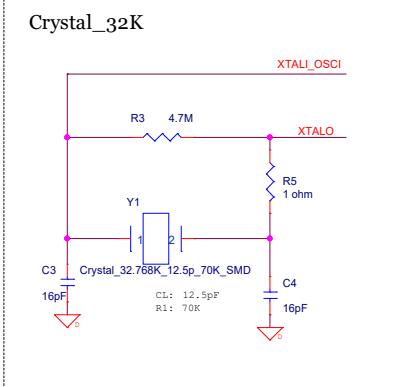
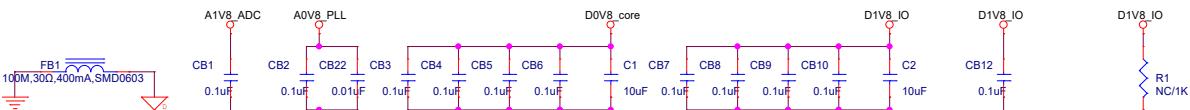
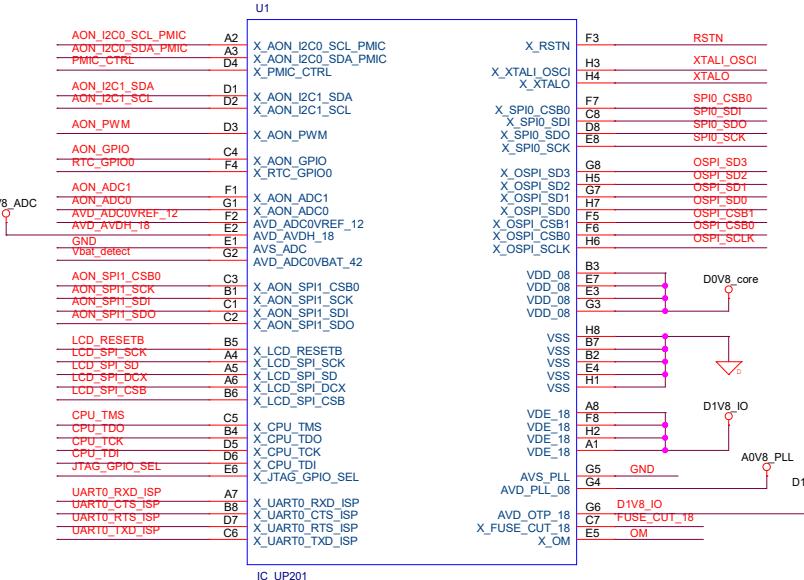
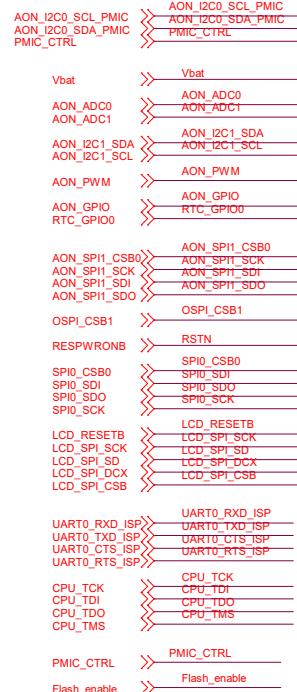
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Size: Document Number: Department: Designer: Rev:
Custom_Placement System Cliff Yeh 1.2
Date: Thursday, March 13, 2025 Sheet: 1 of 6

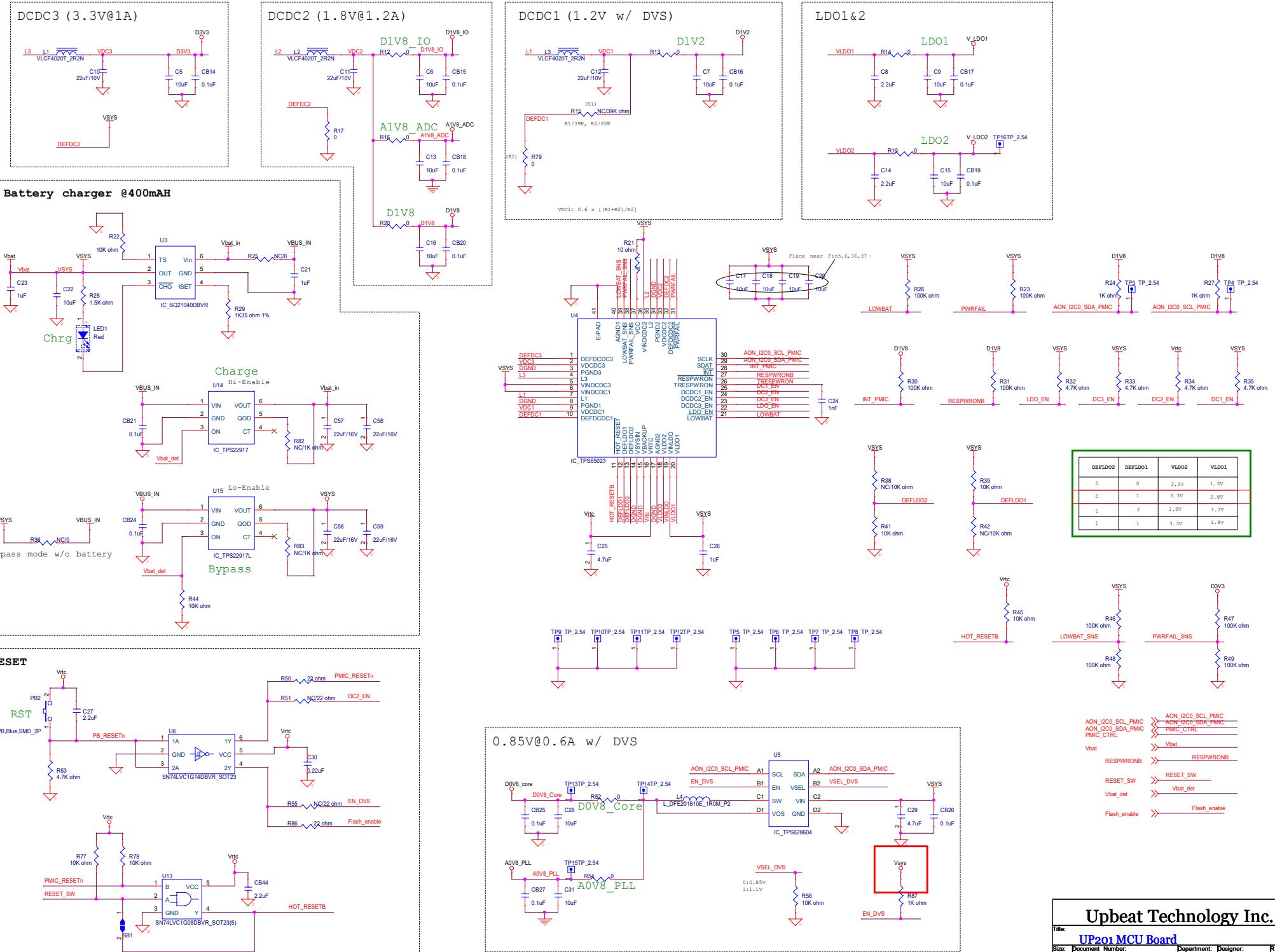


Upbeat Technology Inc.

UP201 MCU Board

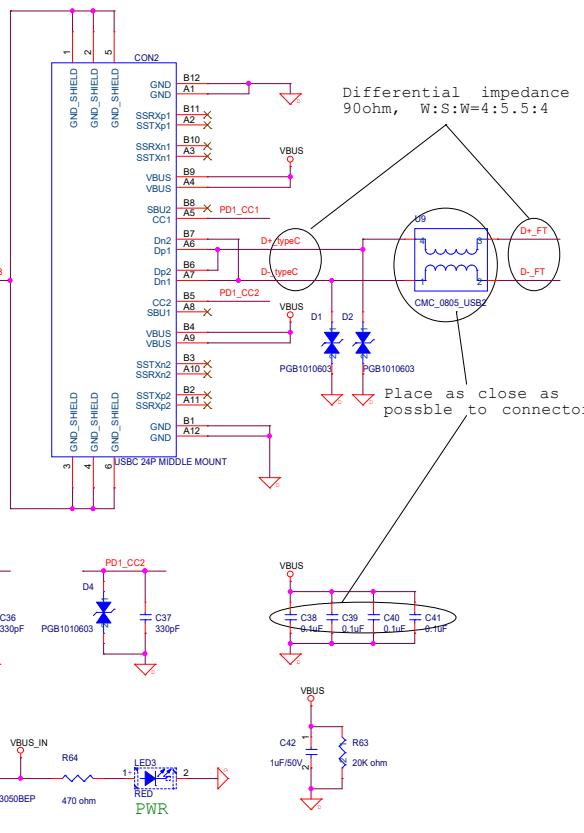
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Date:	Thursday, March 13, 2025	Sheet:	2	of 6



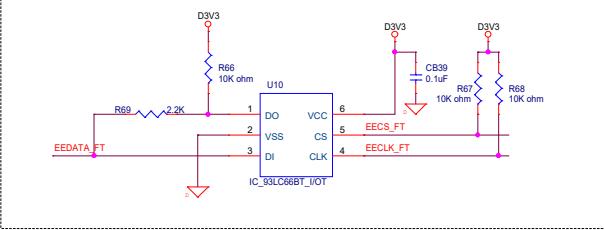


Type-C connector

5V@3A



EEPROM for FTDI



```

    graph LR
      USART0_RXD_ISP[USART0_RXD_ISP] --> TXD_ISP[UART0_TXD_ISP]
      USART0_TXD_ISP[USART0_TXD_ISP] --> RXD_ISP[UART0_RXD_ISP]
      USART0_CTS_ISP[USART0_CTS_ISP] --> CTS_ISP[UART0_CTS_ISP]
      USART0_RTS_ISP[USART0_RTS_ISP] --> RTS_ISP[UART0_RTS_ISP]
  
```

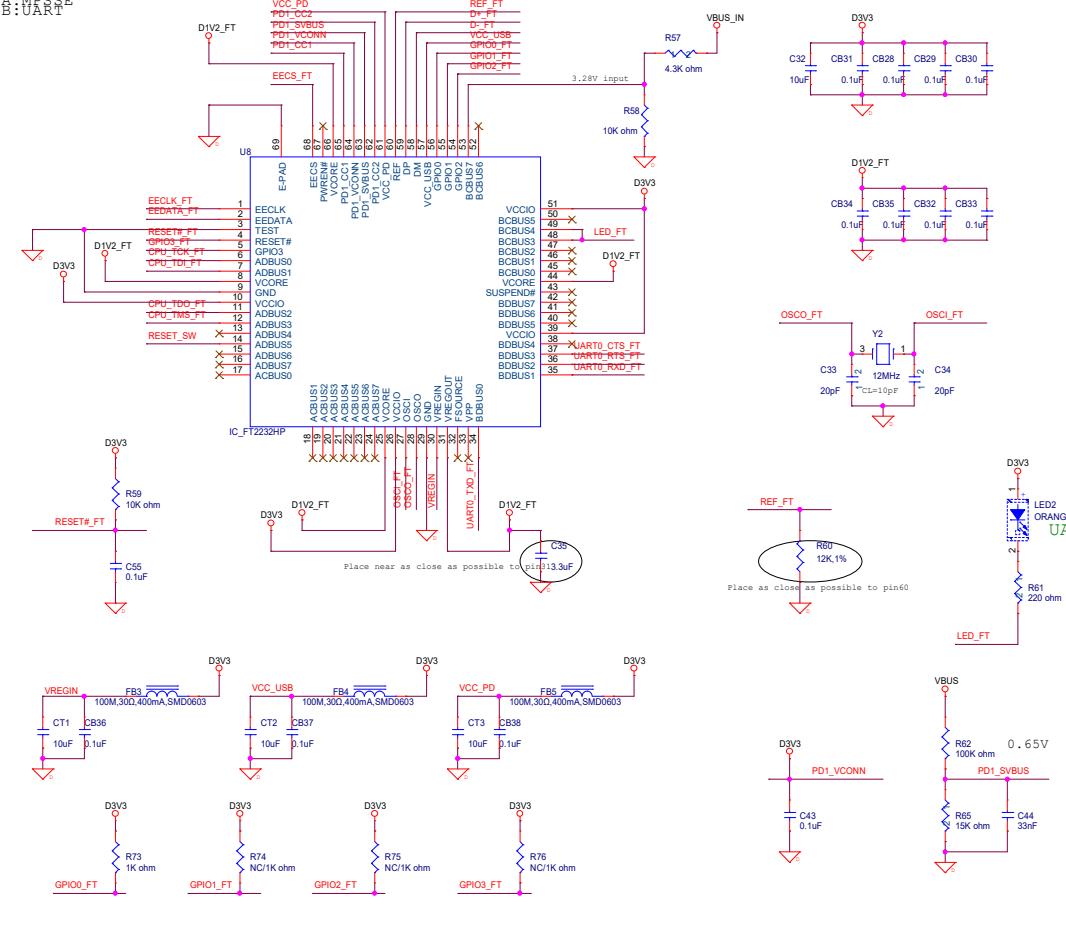
```

    graph LR
      CPU_TCK --- JTAG_TCK
      CPU_TDI --- JTAG_TDI
      CPU_TDO --- JTAG_TDO
      CPU_TMS --- JTAG_TMS
  
```

CPU_TMS ➤ -
RESET_SW

FTD

A: MPSSE



Level shift

