SEMESTER II

Course Code	Course name	L	T	P	C
	Computer Organization and Architecture	3	0	0	3
Total Units to be Covered: 6	**Total Contact Hours: 45**				
Prerequisite(s):	Basic Knowledge of computer systems.	**Syllabus version: 1.0**			

Course Objectives

To equip students with the necessary knowledge and skills to comprehend, analyze, and design digital computer systems, ensuring they can effectively develop and optimize software applications and systems.

Course Outcomes

On completion of this course, the students will be able to

CO1: Analyze the components and organization of digital computers.

CO2: Apply knowledge of instruction codes, instruction formats, and addressing modes to analyze and design computer instructions in different CPU architectures.

CO3: Examine the design and organization of control units in digital computers to comprehend their role in executing instructions and managing system operations.

CO4: Analyze the organization and performance implications of memory units and input –output systems in digital computer systems.

CO5: Assess the benefits and challenges of pipelining in computer architecture on system performance and throughput.

CO-PO Mapping

Program Outcomes / Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3

CO 1	1		2		1	1	1					3	2		
CO 2	1	1	2		1	1	1					3	2		
CO 3	1	1	2		1	1	1					3	2		
CO 4	1		2		1	1	1					3	2		
CO 5	1	1	2		1	1	1					3	2		
Average	1	0.6	2		1	1	1					3	2		

1 – Weakly Mapped (Low) **2 – Moderately Mapped (Medium)**

3 – Strongly Mapped (High) **"_" means there is no correlation**

Syllabus

Unit I: Digital Computers **8 Lecture Hours**

Introduction; Block Diagram for Digital Computers: CPU (Registers, ALU, Clock, Control unit), Memory, I/O subsystems, Common Bus System (External and Internal Bus: Address Bus, Data Bus and Control Bus); Computer Organization; Computer Architecture; Introduction to Vonn Neumann and Harvard Architecture, Data representation: Number System, r complement and r-1 complement arithmetic, Unsigned and Signed number representation, Big Endian and Little Endian, Signed Arithmetic- Addition, Subtraction, Multiplication (Booth Algorithm), Division, Fixed and Floating point representation. Register Transfer Language (RTL) and Micro operations (Arithmetic, Logical and Shift micro operations), Arithmetic Logic and Shift unit (ALU).

Unit II: Basic Computer Organization and Design **7 Lecture Hours**

Instruction Codes; Instruction Format (Three-Address Instructions, Two-Address Instructions, One-Address Instructions, Zero-Address Instruction); Computer Instructions, Registers (General Purpose and Special Purpose Registers); General Register Organization, Stack organization, Types of Instructions (Memory Reference, Register Reference and Input Output Instructions); Addressing Modes and its types; Instruction cycle, Interrupt cycle;

Case Study: Some common CPU architectures (Intel IA-32 Architecture, ARM),

Unit III: Control Unit Organization **6 Lecture Hours**

Hardwired Control Unit and Timing Signals, Microprogrammed control unit: control memory, Address sequencing, Microprogram Example, Designing of microprogrammed control unit. Comparison of hardwired and microprogrammed control units, RISC and CISC Processors;

Case Study: Designing a hypothetical processor with minimum number of instructions so that it can perform basic arithmetical and logical operations.

Unit IV: Memory Organization **8 Lecture Hours**

Memory hierarchy; Different types of memory: Primary (RAM-Static and Dynamic, ROM-EPROM,EEPROM, Cache-Level 1, Level 2 and Level 3) and Secondary/Auxiliary Memory (Magnetic Disk), Introduction to emerging in-situ memory technologies- ReRAM, PCM, STTRAM; Main Memory: RAM and ROM Chips, Memory Address Map, Memory Connection to CPU; Associative Memory. Cache Memory: Principle of Locality, Cache mapping techniques; Performance considerations: Hit Rate and Miss Penalty, cache coherence, cache read and write policy, caches on the Processor Chip.

Unit V: Input Output Organization **8 Lecture Hours**

Peripheral Devices; I/O interface; I/O bus and interface modules; I/O Bus vs Memory Bus, Interrupts and Types of Interrupts. Modes of data transfer: Programmed, Interrupt-initiated, Direct Memory Access (DMA), Priority Interrupt, Input Output processor.

Unit VI: Pipelining **8 Lecture Hours**

Multiprogramming, Multiprocessing, Single instruction single data stream (SISD); Single instruction multiple data stream (SIMD); Multiple instruction single data stream (MISD); Multiple instruction multiple data stream (MIMD), Multiprocessors: Shared memory and distributed memory, Parallel processing: Pipeline processing, Vector processing, Array processors. Pipelining: Arithmetic Pipeline, Instruction Pipeline: Example: Four-Segment Instruction Pipeline. Pipelining Conflicts: Resource conflicts, Data dependency and Branch difficulties, Pipeline Conflicts Handling techniques: Throughput and Speed; RISC pipeline;

Case study: Pipelining in CISC Processors, Pipelining in ColdFire Processors, and Pipelining in Intel Processors, Designing pipeline architecture for 2, 3, 4 stage pipeline.

Total lecture Hours 45

Textbooks

1. M. M. Mano, "Computer System Architecture", Revised 3rd Edition, Pearson Education, 2017.

2. Carl Hamacher, Zvonko Vranesic , Safwat Zaky, and Naraig Manjikian, "Computer Organization and Embedded Systems", 6th Edition, McGraw Hill, Standard Edition, 2023.

3. David A. Patterson, and John L. Hennessy, "Computer Organization and Design MIPS Edition: The Hardware/Software Interface", 5th Edition, The Morgan Kaufmann Series in Computer Architecture and Design, Morgan Kaufmann, 2020.

Reference Books

1. John P. Hayes, "Computer Architecture and Organization", 3rd Edition, McGraw-Hill Education, 2017.

2. William Stallings, "Computer Organization and Architecture: Designing for Performance", 11th Edition, Pearson, 2022.

Modes of Evaluation: Quiz/Assignment/ presentation/ extempore/ Written Examination

Examination Scheme

Components	IA	MID SEM	End Sem	Total
Weightage (%)	50	20	30	100

Detailed breakup of Internal Assessment

Internal Assessment Component	Weightage in calculation of Internal Assessment (100 marks)
Quiz 1	15%
Quiz 2	15%
Class Test 1	15%
Class Test 2	15%
Assignment 1/Project	20%
Assignment 2/Project	20%