**PAPER TITLE**

**1AUTHOR’S NAME(<First name> <Second name>), 2CO-AUTHOR’S NAME(<First name> <Second name>)**

1Author’sDesignation, College name/University name, College address

2Co-Author’sDesignation, College name/University name, College address

Email: 1Author’s email id, 2Co-Author’s email id.

**Abstract:** This paper presents a modified design of an Area-Efficient Low power Carry Select Adder (CSLA) Circuit. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position, the speed of addition is limited by the time required to transmit a carry through the adder. Carry select adder processors and systems. Has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries.

***Keywords:***Area-efficient, Low power, CSLA, Binary to excess one converter, Multiplexer.

1. **INTRODUCTION**

Conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because logic circuit sharing sacrifices the length of the parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder to excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure, the basic idea of the proposed work is by using n-bit binary to excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure.

1. **LITERATURE REVIEW**
   1. Second Level Heading (Head 2)

To excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure, and the area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block.

Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

Table 2.1: Delay and Area Evaluation of the Basic Blocks of CSLA

Basic Blocks Delay Area

XOR 3 5

2:1 MUX 3 4

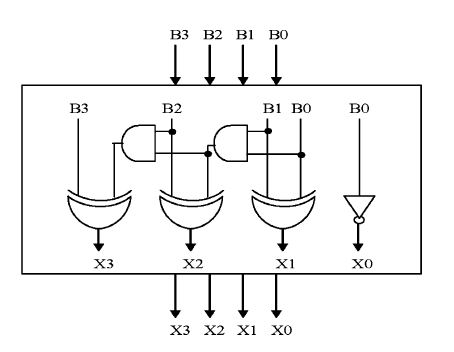
Half Adder 3 6

Full Adder 6 13

1. **METHODOLOGY**

Conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because logic circuit sharing sacrifices the length of the parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-bit BEC are shown in Figure.2 and Table .2, respectively.



**Figure 3.1: 4-Bit BEC**

The Boolean expressions of the 4-bit BEC are

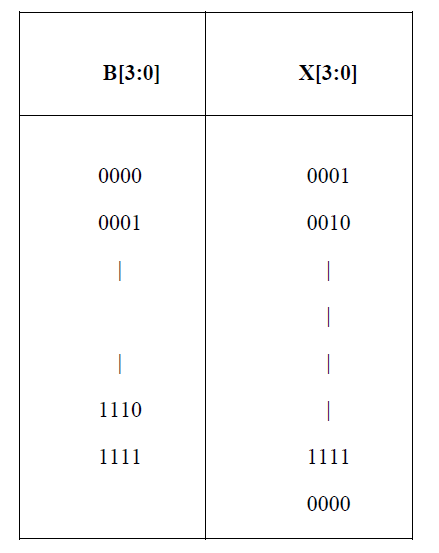
X0 = ~B0 (1)

X1 = B0^B1 (2)

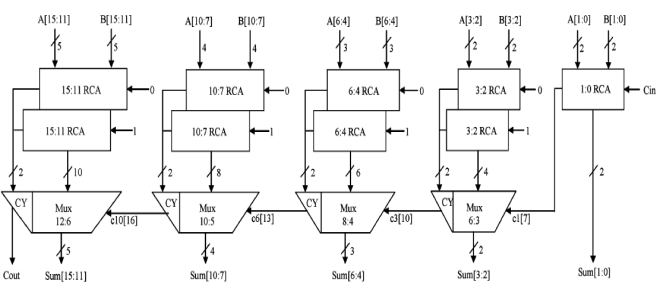
X2 = B2^ (B0 & B1) (3)

X3 = B3^ (B0 & B1 & B2) (4)

**Table 3.2: Function table of the 4-bit BEC**



1. **RESULTS AND DISCUSSION**



**Figure 4.1: Regular CSLA circuit**

The structure of the 16-b regular SQRT CS conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because logic circuit sharing sacrifices the length of the parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder

Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in Table 3.

Table 4.1: Regular SQRT CSLA are evaluated and listed

Group Delay Area

2 11 57

3 13 87

4 16 117

5 19 147

1. **CONCLUSION**

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with Cin=1 to optimize the area and power is shown in Fig. 4. We again split the structure into five groups. The steps leading to the conventional carry select adder perform better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder) are depending on s3and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.

For the remaining group’s the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC’s. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table 4.

Table 5.1: Modified SQRT CSLA are evaluated and listed

Group Delay Area

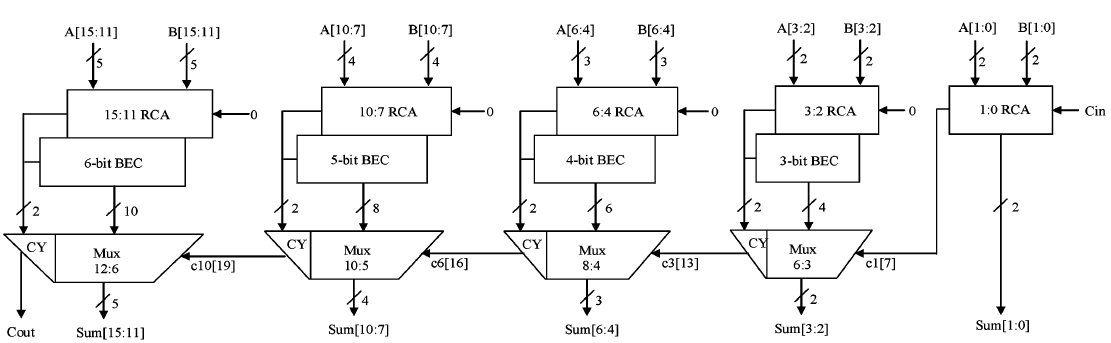
2 13 43

3 16 61

4 19 84

5 22 107

Comparing Tables 3and 4, it is clear that the proposed modified CSLA saves 113 gate areas than the regular CSLA, with only 11 increases in gate delays.



**Figure 5.1: CSLA circuit using BEC Converter**

**AUTHORS’ CONTRIBUTIONS**

The title "AUTHORS’ CONTRIBUTIONS" should be in all caps.

**ACKNOWLEDGMENTS**

The title "ACKNOWLEDGMENTS" should be in all caps and should be placed above the references. The references should be consistent within the article and follow the same style. List all the references with full details.

**REFERENCES**

[1] O. J. Bedrij, “Carry-select adder,” *IRE Trans. Electron. Comput,* pp. 340–344, 1962.

[2] B. Ramkumar, H.M. Kittur, and P. M. Kannan, “ASIC implementation of modified faster carry save adder,” *Eur. J. Sci. Res.*, vol. 42, no. 1, pp.53–58, 2010.

[3] T. Y. Ceiang and M. J. Hsiao, “Carry-select adder using single ripple carry adder,” *Electron. Lett.*, vol. 34, no. 22, pp. 2101–2103, Oct. 1998.

[4] J. M. Rabaey*, Digtal Integrated Circuits— A Design Perspective* Upper Saddle River, NJ: Prentice-Hall, 2001

[5] J. M. Rabaey*, Digtal Integrated Circuits— A Design Perspective* Upper Saddle River, NJ: Prentice-Hall, 2001.

[6] Y. He, C. H. Chang, and J. Gu, “An area efficient 64-bit square root carry-select adder for lowpower applications,” in *Proc. IEEE Int. Symp. Circuits Syst.*, 2005, vol. 4, pp. 4082–4085.

[7] Cadence, “Encounter user guide,” Version 6.2.4, March 2008

[8] E.M. Clarke, E.A. Emerson, Design and synthesis of synchronization skeletons using branching time temporal logic, in: D. Kozen (Eds.), Workshop on Logics of Programs, Lecture Notes in Computer Science, vol. 131, Springer, Berlin, Heidelberg, 1981, pp. 52–71. DOI: <https://doi.org/10.1007/BFb0025774>

[9] J.P. Queille, J. Sifakis, Specification and verification of concurrent systems in CESAR, in: M. Dezani-Ciancaglini and U. Montanari (Eds.), Proceedings of the 5th International Symposium on Programming, Lecture Notes in Computer Science, vol. 137, Springer, Berlin, Heidelberg, 1982, pp. 337–351. DOI: https://doi.org/10.1007/3-540-11494-7\_22

★★★