6 Register mapping

The table below provides a list of the 8-bit registers embedded in the device and the related addresses.

Table 15. Register address map

Name	Type	Register address (hex)	Default (hex)
Reserved		00-0E	Do not modify
WHO_AM_I	R	0F	BC
AV_CONF	R/W	10	1B
Reserved		11-1C	Do not modify
CTRL_REG1	R/W	20	0
CTRL_REG2	R/W	21	0
CTRL_REG3	R/W	22	0
Reserved		23-26	Do not modify
STATUS_REG	R	27	0
HUMIDITY_OUT_L	R	28	Output
HUMIDITY_OUT_H	R	29	Output
TEMP_OUT_L	R	2A	Output
TEMP_OUT_H	R	2B	Output
Reserved		2C-2F	Do not modify
CALIB_0..F	R/W	30-3F	Do not modify

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the CALIB_0..F registers that are loaded at power-on from device internal non-volatile memory should never be modified.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve humidity and temperature data. The register address, made up of 7 bits, is used to identify and to read/write the data, through the serial interfaces.

7.1 WHO_AM_I (0Fh)

Device identification

7	6	5	4	3	2	1	0
1	0	1	1	1	1	0	0

This read-only register contains the device identifier, set to BCh

7.2 AV_CONF (10h)

Humidity and temperature resolution mode

7	6	5	4	3	2	1	0
Reserved		AVGT2	AVGT1	AVGT0	AVGH2	AVGH1	AVGH0

To configure humidity/temperature average.

[7:6]	Reserved
[5:3]	AVGT2-0: To select the numbers of averaged temperature samples (2 - 256), see *Table 16*.
[2:0]	AVGH2-0: To select the numbers of averaged humidity samples (4 - 512), see *Table 16*.

Table 16. Humidity and temperature average configuration

AVGx2:0	Nr. internal average		Noise (RMS)		I_{DD} 1 Hz
	Temperature (AVGT)	Humidity (AVGH)	Temp (°C)	rH %	µA
000	2	4	0.08	0.4	0.80
001	4	8	0.05	0.3	1.05
010	8	16	0.04	0.2	1.40
011(1)	16	32	0.03	0.15	2.10
100	32	64	0.02	0.1	3.43
101	64	128	0.015	0.07	6.15
110	128	256	0.01	0.05	11.60
111	256	512	0.007	0.03	22.50

1. Default configuration

7.3 CTRL_REG1 (20h)

Control register 1

7	6	5	4	3	2	1	0
PD	Reserved				BDU	ODR1	ODR0

[7]	PD: power-down control (0: power-down mode; 1: active mode)
[6:3]	Reserved
[2]	BDU: block data update (0: continuous update; 1: output registers not updated until MSB and LSB reading)
[1:0]	ODR1, ODR0: output data rate selection (see table 17)

The **PD** bit is used to turn on the device. The device is in power-down mode when PD = ‘0’ (default value after boot). The device is active when PD is set to ‘1’.

The **BDU** bit is used to inhibit the output register update between the reading of the upper and lower register parts. In default mode (BDU = ‘0’), the lower and upper register parts are updated continuously. If it is not certain whether the read will be faster than output data rate, it is recommended to set the BDU bit to ‘1’. In this way, after the reading of the lower (upper) register part, the content of that output register is not updated until the upper (lower) part is read also.

This feature prevents the reading of LSB and MSB related to different samples.

The ODR1 and ODR0 bits permit changes to the output data rates of humidity and temperature samples.The default value corresponds to a “one-shot” configuration for both humidity and temperature output. ODR1 and ODR0 can be configured as described in *Table 17*.

Table 17. Output data rate configuration

ODR1	ODR0	Humidity (Hz)	Temperature (Hz)
0	0	One-shot	
0	1	1 Hz	1 Hz
1	0	7 Hz	7 Hz
1	1	12.5 Hz	12.5 Hz

7.4 CTRL_REG2 (21h)

Control register 2

7	6	5	4	3	2	1	0
BOOT	Reserved					Heater	ONE_SHOT

[7]	BOOT: Reboot memory content (0: normal mode; 1: reboot memory content)
[6:2]	Reserved
[1]	Heater (0: heater disable; 1: heater enable)
[0]	One-shot enable (0: waiting for start of conversion; 1: start for a new dataset)

The **BOOT** bit is used to refresh the content of the internal registers stored in the Flash memory block. At device power-up, the content of the Flash memory block is transferred to the internal registers related to trimming functions to permit good behavior of the device itself. If, for any reason, the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to '1' the content of the internal Flash is copied inside the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and are different for every device. They permit good behavior of the device and normally they should not be changed. At the end of the boot process, the BOOT bit is set again to '0'.

The **ONE_SHOT** bit is used to start a new conversion. In this situation a single acquisition of temperature and humidity is started when the ONE_SHOT bit is set to '1'. At the end of conversion the new data are available in the output registers, the STATUS_REG[0] and STATUS_REG[1] bits are set to '1' and the ONE_SHOT bit comes back to '0' by hardware.

The **Heater** bit is used to control an internal heating element, that can effectively be used to speed up the sensor recovery time in case of condensation. The heater can be operated only by an external controller, which means that it has to be switched on/off directly by FW. Humidity and temperature output should not be read during the heating cycle; valid data can be read out once the heater has been turned off, after the completion of the heating cycle. Typical power consumption related to V_{DD} is described in *Table 18*.

Table 18. Typical power consumption with heater ON

V_{DD} [V]	I [mA]
3.3	33
2.5	22
1.8	12

7.5 CTRL_REG3 (22h)

Control register 3

7	6	5	4	3	2	1	0
DRDY_H_L	PP_OD	Reserved			DRDY	Reserved	

Control register for data ready output signal

[7]	DRDY_H_L: Data Ready output signal active high, low (0: active high - default;1: active low)
[6]	PP_OD: Push-pull / Open Drain selection on pin 3 (DRDY) (0: push-pull - default; 1: open drain)
[5:3]	Reserved
[2]	DRDY_EN: Data Ready enable (0: Data Ready disabled - default;1: Data Ready signal available on pin 3)
[1:0]	Reserved

The **DRDY_EN** bit enables the DRDY signal on pin 3. Normally inactive, the DRDY output signal becomes active on new data available: logical OR of the bits STATUS_REG[1] and STATUS_REG[0] for humidity and temperature, respectively. The DRDY signal returns inactive after both HUMIDITY_OUT_H and TEMP_OUT_H registers are read.

7.6 STATUS_REG (27h)

Status register

7	6	5	4	3	2	1	0
Reserved						H_DA	T_DA

Status register; the content of this register is updated every one-shot reading, and after completion of every ODR cycle, regardless of the BDU value in CTRL_REG1.

[7:2]	Reserved
[1]	H_DA: Humidity data available. (0: new data for humidity is not yet available; 1: new data for humidity is available)
[0]	T_DA: Temperature data available. (0: new data for temperature is not yet available; 1: new data for temperature is available) H_DA is set to 1 whenever a new humidity sample is available. H_DA is cleared anytime HUMIDITY_OUT_H (29h) register is read. T_DA is set to 1 whenever a new temperature sample is available. T_DA is cleared anytime TEMP_OUT_H (2Bh) register is read.

7.7 HUMIDITY_OUT_L (28h)

Relative humidity data (LSB)

7	6	5	4	3	2	1	0
HOUT7	HOUT6	HOUT5	HOUT4	HOUT3	HOUT2	HOUT1	HOUT0

Humidity data (see HUMIDITY_OUT_H)

[7:0]	HOUT7 - HOUT0: Humidity data LSB

7.8 HUMIDITY_OUT_H (29h)

Relative humidity data (MSB)

15	14	13	12	11	10	9	8
HOUT15	HOUT14	HOUT13	HOUT12	HOUT11	HOUT10	HOUT9	HOUT8

Humidity data are expressed as HUMIDITY_OUT_H & HUMIDITY_OUT_L in 2's complement. Values exceeding the operating humidity range (see *Table 3*) must be clipped by SW.

[7:0]	HOUT15 - HOUT8: Humidity data MSB

7.9 TEMP_OUT_L (2Ah)

Temperature data (LSB)

7	6	5	4	3	2	1	0
TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

[7:0]	TOUT7 - TOUT0: Temperature data LSB (see TEMPERATURE_OUT_H)

7.10 TEMP_OUT_H (2Bh)

Temperature data (MSB)

15	14	13	12	11	10	9	8
TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

[15:8]	TOUT15 - TOUT8: Temperature data MSB.

Temperature data are expressed as TEMP_OUT_H & TEMP_OUT_L as 2's complement numbers.
The relative humidity and temperature values must be computed by linear interpolation of current registers with calibration registers, according to *Table 19* and scaling as described in *Section 8*.