About Organisation

Name of Company:	NVIDIA Graphics Pvt. Ltd.
Date of Establishment:	1993-04-05
Number of Employees:	29000
Social Media Page Link:	https://www.linkedin.com/company/nvidia/
Website:	https://www.nvidia.com/en-in/
Type of Organization:	MNC (Foreign Origin)
Location of Head office:	Santa Clara, US
Nature of Business:	Core Engineering & Technology

Internship Profile

Job Title: Hardware Engineering Intern

Job Description:

HARDWARE INTERN JD – NVIDIA

Do you have a passion for computing using new age technologies?

Do you want to work on leading-edge problems alongside some of the best & brightest in the world?

Do you like working in a dynamic working environment that involves creative problem solving and thinking on your feet?

We, at NVIDIA, are in the lookout for the brightest young technologists of our generation to do their life's best work at NVIDIA.

We are hiring for our summer internship program across multiple positions in our HW group, and the following is a brief about the teams.

GPU ARCHITECTURE TEAM
GPU architecture team is engaged in the development of industry leading high performance and power efficient GPUs.
Specific areas include architecture modelling, analysis, and performance verification. The team works on GPUs across all application domains such as gaming for PC and mobile devices, professional graphics and visualization and high-performance computation.
Skills you will use/develop:
• C++ modelling, test development

• RTL design, debug
• ASIC design & verification tools, methodologies
• Computer architecture, Graphics, GPU micro-architecture, parallel computing
• Performance evaluation, analysis and debug
• Perl/Python scripting
Areas you will be working on: Computer Architecture, Memory Systems Architecture, Compiler Architecture / Performance Modelling

GPU ASIC DESIGN / VERIFICATION TEAM
Today NVIDIA's GPUs simulate human intelligence, running deep learning algorithms and acting as the brain of super computers, robots, and self-driving cars that can perceive and understand the world. We are seeking a passionate, innovative, and highly motivated senior verification engineer to join us in the development of the next generation of PCI Express controllers used in NVIDIA's GPUs and SOCs.
In this position, you will be responsible for verification of the ASIC design, architecture and microarchitecture using advanced verification methodologies. You are expected to understand the design and implementation, define the verification scope, develop the verification infrastructure and verify the correctness of the design. You will be working with architects, designers, pre and post silicon verification teams to accomplish your tasks.
What you'll be doing:
• Develop test plans, tests and verification infrastructure for PCIE at IP/sub system/SOC level
• Create verification environment using UVM methodology
• Create reusable bus functional models, monitors, checkers and scoreboards
• Drive functional coverage driven verification closure
• Work with architects, designers and post silicon teams

Ways to stand out from the crowd:
• Good knowledge of PCIE protocol Gen 3 and above
• Good debugging and problem-solving skills
• Good communication skills
• Ability/ desire to work as a team player

TEGRA SOC DESIGN & VERIFICATION
As a Hardware Engineer at NVIDIA, you will design and implement the industry's leading Graphics, Video and Mobile Communications Processors. Specific areas include 2D and 3D graphics, mpeg, video, audio, network protocols, high-speed IO interfaces and bus protocols, and memory subsystem design. You will be responsible for Architecture and microarchitecture design of the ASICs, RTL design and synthesis, Logic and Timing verification using leading edge CAD tools and Semiconductor process technologies.
Areas you will be working on:
• ASIC, RTL, Design and Verification of Processors
• Low Power verification
• Power Estimation and Modelling
• PCIe Design verification
• Functional / Formal verification

CPU VERIFICATION TEAM
As a design and verification/validation engineer in the

ARM CPU team, you will be working on the next generation of 64bit ARM CPUs and SOCs. As part of this assignment, you will get a chance to learn about computer architecture at a very granular level, System Verilog, Design Verification, SOC Verification, Verification methodologies and C/C++ programming. You also will get an opportunity to get familiar with industry standard tools in verification and validation.
During the course of the internship, you will contribute to building test benches, developing architectural simulators, modifying random instruction generators and creating stimulus for verification and validation of different units of the CPU and SOC.

Areas you will be working on:
• Computer Architecture
• Digital Design and Programming in C/C++/Perl
• ARM, CPU Design and Verification/ Validation

VLSI TEAM
VLSI team works in the areas of RTL Design, Verification, Design for Test, CAD tools, Synthesis, Timing, Place & Route, Circuit Design, Silicon Bring-up and Characterization. Responsible for state-of-the-art methodologies, tools, flows and project execution on all Nvidia GPU, CPU, Auto, and Switch chips. As an intern you will be working on one or more such areas.
Skills you will use/develop:
• RTL Design, VCS, SV, UVM, Formal
• Verilog, C/C++, Python, TCL, Perl
• Logic Scan Test, Memory Test, High-speed IO Test, In-System Test
• Synthesis, Timing Closure (Primetime)
• Physical Design, Innovus, ICC2, Physical extraction, Place and Route, Floorplan
• SRAM, Analog, Digital circuit design, Hspice, EMIR, Silicon Correlation (ATPG, data
visualization & analysis)
• Layout (Cadence Virtuoso)
• Silicon characterization for ageing, DPPM, Signal Integrity, Power Integrity, and familiarity with PC/SOC sub-system Architecture

Minimum No. of Hires:	-
Expected No. of Hires:	4
Location(s)/Place of Posting/Online:	Bangalore, Hyderabad
Skillset:	Please refer the JD
Minimum CGPA:	8
Students with backlog eligible:	No

Selection Process

Resume Shortlist:	Yes

Mode of Selection:	Virtual
Resume shortlisting before test?:	No
Test:	Yes
Mode of Test:	Online
Test duration (minutes):	60
Aptitude/Psycometric:	Yes
Technical:	Yes
Group Discussion:	No
Personal Interview:	No
Technical Round:	Yes
HR Round:	No
Medical Test:	No

Eligible Academic Programs

Diversity Recruiting:	No
Eligible Years:	Graduating in 2026 (Pre-Final Year Students) - B.Tech / Dual / Master's
Eligible Departments:	B.Tech in Computer Science & Engineering, B.Tech in Electrical Engineering, B.Tech in Electrical Engineering (Power and Automation), B.Tech and M.Tech in Computer Science & Engineering

Stipend Details

Stipend (per month) (In INR Per Month):	75,000 INR Per Month
Accommodation:	Yes
Provision of PPO based on performance?	Yes
Tentative CTC for PPO select:	Total Compensation + Annualized Equity: B.Tech - INR 2,899,758, Dual Degree - INR 3,290,063 INR Per Annum

Others

Medical Requirements:	NA

Other Requirements:	NA