How to prevent *"context switch"* and *"out-of-order execution"* issues?

To prevent the about issues, we can add `lock` prefix.

For example:

```
x

lock cmpxchgl %ecx, (lock_addr)
```

The `LOCK` prefix ensures that the CPU has exclusive ownership of the appropriate cache line for the duration of the operation, and provides certain additional ordering guarantees.

This may be achieved by asserting a bus lock, but the CPU will avoid this where possible.

If the bus is locked then it is only for the duration of the locked instruction.

Reference:

- what-does-the-lock-instruction-mean-in-x86-assembly
- LOCK — Assert LOCK# Signal Prefix