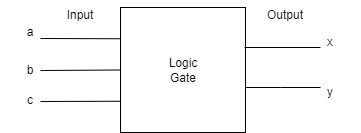
Experiment # 2

Submitted To:

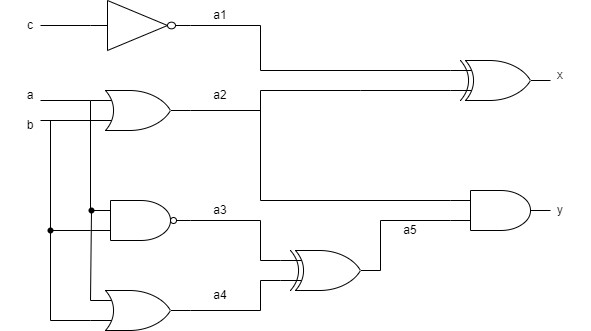
Submitted By:

Digital System

Number of Inputs and outputs:



Circuit Diagram:

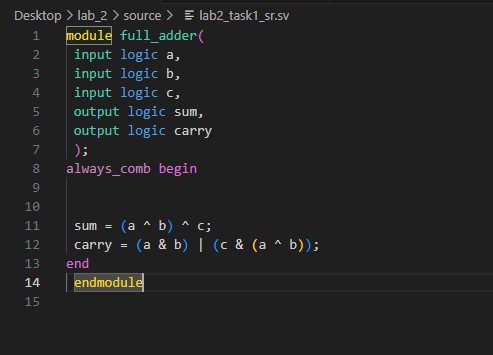


Truth Table:

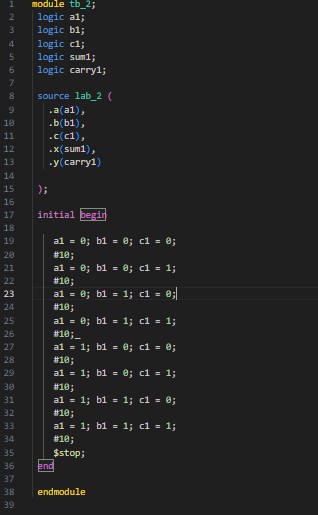
|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| a | b | c | a1 | a2 | a3 | a4 | a5 | x | Y |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

Code Errors

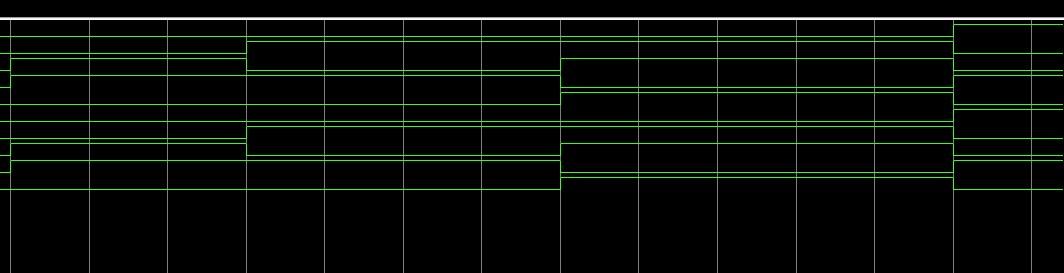
Listing 4

* Remove extra comma from line 6.
* Add a library of “always\_comb” so take program inputs in logoc sense.
* Add “end” before endmodule to end the program.
* Add “&” sign after c in line 10 which refers and gate.
* 

Listing 5

* After logic sum1 in line 6 “logic carry1” missing.
* In line 18,20,22,24,26,28,30 correct all a,b,c to a1,b2,c3.
* Give a function DUT in line 7.
* Give a increase of regular interval in time.
* Before endmodule , write “end” to end the task.
* 

Task 1 Simulation



Task 2 Simulation

