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BUCK CONVERTERS AND LINEAR REGULATORS

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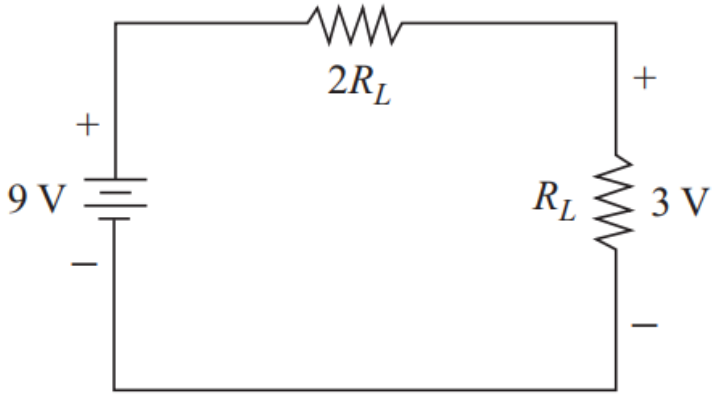
Contents

BASIC CONCEPTS

It all starts with the will of having different voltage levels.

Let's say we would like to get 3 volts output voltage from a 9 volts battery. The first idea is to use the voltage divider.



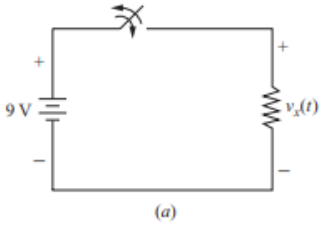
$$V_{out} = \frac{V_{in} * R_L}{2R_L + R_L} = \frac{9\,V}{3} = 3\,V$$

We get the result we would like to have but some problems occur:

1. If the load resistor changes, the output voltage changes except we change the 2RL resistance accordingly.
2. The energy is dissipated as the heat. So, this circuit has low efficiency.

A solution to the first problem could be to use a transistor to be controlled so that the voltage across it is 6 volts.

A solution to the second problem incorporates the usage of switches. Whenever a switch is open, theoretically, and since there is no current across it, the power absorbed is zero. Whenever a switch is closed since it becomes a short circuit, there is no voltage difference across it and the power absorbed by it zero.



(a)

If we close the switch one third of a period, the average value of the output voltage is one third of the input voltage, in this case 3 volts voltage.

The waveform of the output voltage includes AC terms as well as DC terms. An ideal low-pass filter allows the dc component of voltage the pass while removing the AC terms. The final circuit, if everything is ideal, is 100 percent efficient.

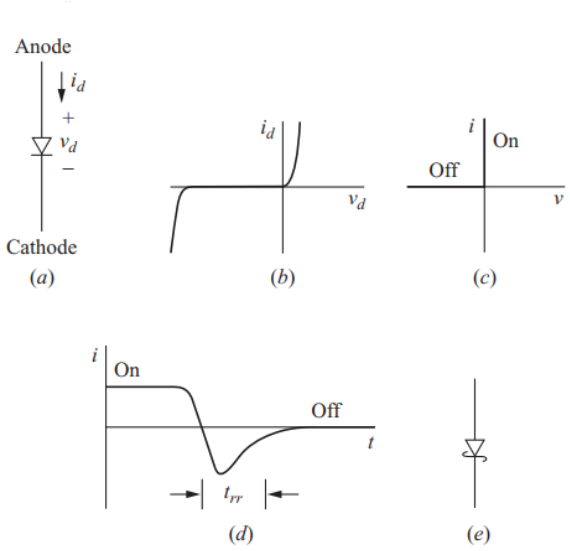
In real world, nothing is ideal and there will be losses, but these simple circuits and definitions are great way to grasp these concepts firmly. Thus, it builds a solid basis block to understand the further concepts.

ELECTRONIC SWITCHES

Diodes

Diodes are simple on and off devices. When a diode turns off, the current in it decreases and momentarily becomes negative before becoming zero. This period is called Reverse Recovery Time.

Schottky diodes are used in low voltage applications and have voltage drop at 0.3V. The reverse voltage is up to 100V. They turn on and off faster than P-N junction diodes.



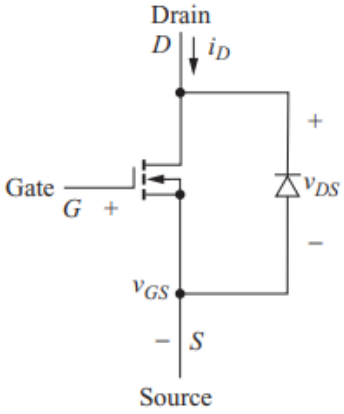
Thyristors

They are used where control of switch turn-on is required. The switching frequencies cannot be as high as other devices such as MOSFETs.

Triac is a thyristor that can conduct current in either direction.

Transistors

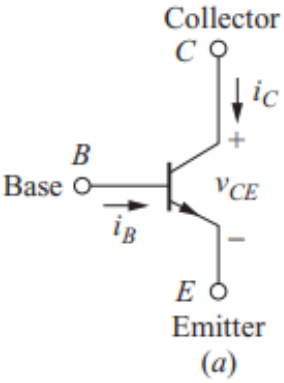
The turn-on and turn-off are controllable. The types are BJTs, MOSFETs, IGBTs.



MOSFET

A sufficiently large gate-to-source voltage (Vgs) will turn the device on, resulting in a small drain-to-source voltage (Vds).

In the on state, the change in Vds is linearly proportional to the change in Id. Therefore, the on MOSFET can be modeled as an on-state resistance called Rds(on).



BJT

The on-state for the transistor is achieved by providing sufficient base current to drive the BJT into saturation.

If a power BJT with hfe = 20 is to carry a collector current of 60A, for example, the base current would need to be more than 3A to put the transistor into saturation.

IGBT

It is an integrated connection of a MOSFET and a BJT. IGBTs replace BJTs in many applications.

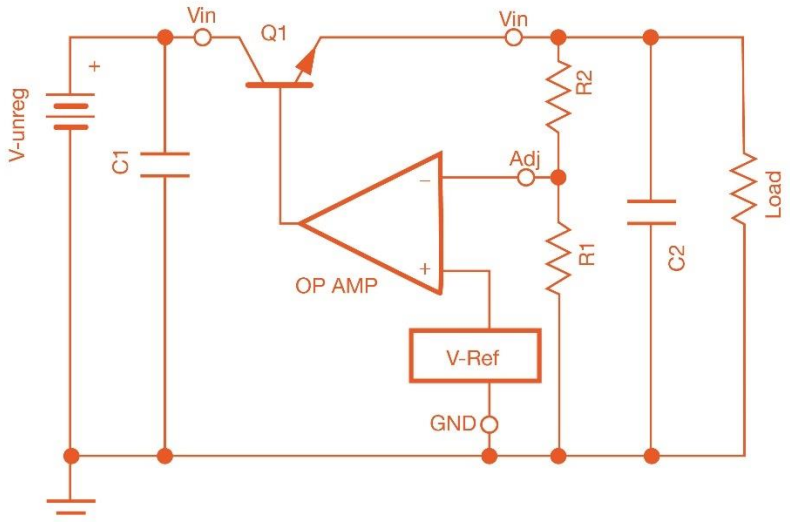
Switch Selection

MOSFET generally has lower switching losses and is preferred over the BJT.

DC-DC CONVERTERS

Linear Regulators

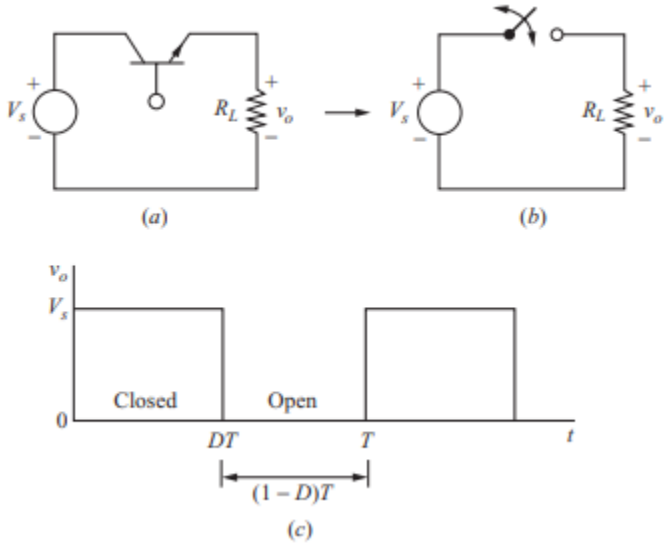
Before diving into converters, let's review the concepts we discussed in the "basic concepts" section.



I explained that to keep a constant voltage output, we can incorporate in our design a transistor and a feedback loop. This is an example of internal operation of a linear regulator image taken from Digikey.

It is inefficient due to the power loss in the transistor. The transistor operates in the linear region, hence the name "Linear Regulators".

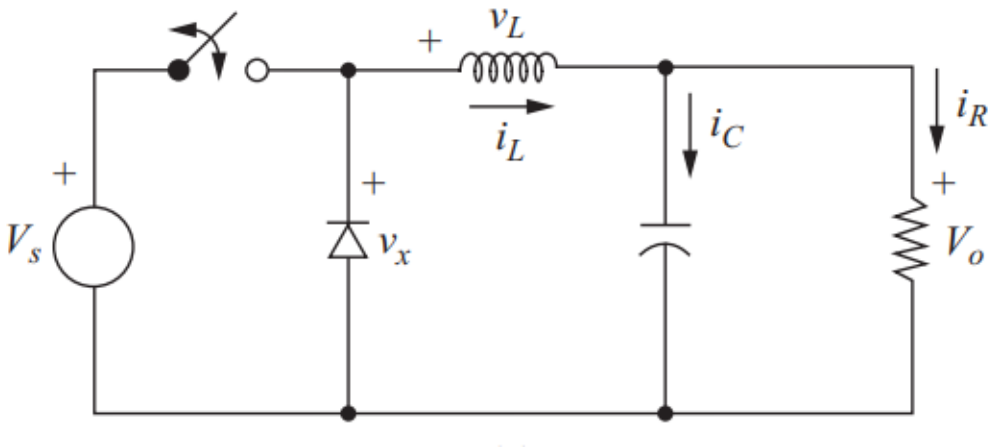
A Basic Switching Regulator



An efficient alternative to the linear regulator is the switching converter. In a switching converter circuit, the transistor operates as an electronic switch by being completely on or completely off (saturation or cutoff for a BJT or the triode and cutoff regions of a MOSFET).

Buck Converter

One way of obtaining a dc output is to insert a low-pass filter after the switch. Figure below shows an LC low-pass filter added to the basic converter. The diode provides a path for the inductor current when the switch is opened and is reverse-biased when the switch is closed. This circuit is called a buck converter or a step-down converter because the output voltage is less than the input. Here is a buck converter topology.



A way of analyzing the operation of the buck converter is to examine inductor voltage and current. This is useful for designing the filter and analyzing circuits.

An inductor current that remains positive throughout the switching period is known as conductor current.

DC-DC converters have the following properties when operating in the steady-state.

1. The inductor current is periodic.

$$i_L(t+T) = i_L(t)$$

2. The average inductor voltage is zero.

$$V_L = \frac{1}{T}\int_t^{t+T} V_L(\lambda)d\lambda = 0$$

3. The average capacitor current is zero.

$$I_C = \frac{1}{T}\int_t^{t+T} i_C(\lambda)d\lambda = 0$$

4. In an ideal structure the power of the output is equal to the power of the source. For a non-ideal structure losses must be added to the power of the output.

$$P_s = P_o \qquad Ideal$$
$$P_s = P_o + losses \qquad Non-ideal$$

Analysis of the Buck Converter

Analysis of the Buck Converter begins by making these assumptions.

1. The circuit is operating in the steady state.
2. The capacitor is very large, the output voltage is held constant at voltage Vo.
3. The switching period is T; the switch is closed for time DT and open for time (1-D)T.
4. The components are real.

The key to the analysis for determining the output Vo is to examine the inductor current and inductor voltage first for the switch closed and then for the switch open.
The net change in inductor current over one period must be zero for steady-state operation.
The average inductor voltage is zero.

Calculations

- Analysis for the Switch Closed

$$(\Delta i_L)_{closed} = \left(\frac{V_s - V_o}{L}\right) DT$$

- Analysis for the Switch Open

$$(\Delta i_L)_{open} = -\left(\frac{V_o}{L}\right)(1-D)T$$

$$(\Delta i_L)_{closed} + (\Delta i_L)_{open} => V_o = V_s D$$

The average inductor current must be the same as the average current in the load resistor, since the average capacitor current must be zero for steady-state operation:

$$I_L = I_R = \frac{V_o}{R}$$
$$I_{max} = I_L + \frac{\Delta i}{2} = V_o \left(\frac{1}{R} + \frac{1-D}{2Lf}\right)$$
$$I_{min} = I_L - \frac{\Delta i}{2} = V_o \left(\frac{1}{R} - \frac{1-D}{2Lf}\right)$$

For the preceding analysis to be valid, continuous current in the inductor must be verified.

$$I_{min} = 0 = V_o \left(\frac{1}{R} - \frac{1-D}{2Lf}\right)$$

$$L_{min} = \frac{(1-D)R}{2f} \qquad for\ continous\ current$$

In the design of buck converter, the peak-to-peak variation in the inductor current is often used as a design criterion.

$$L = \frac{V_s - V_o}{\Delta i_L f} D = \frac{V_o(1-D)}{\Delta i_L f}$$

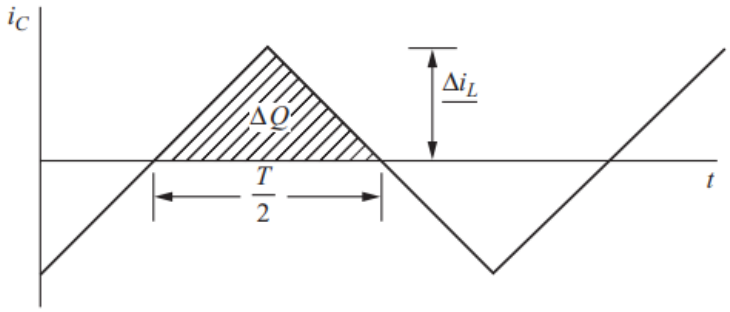
Output Voltage Ripple

In the preceding analysis, the capacitor was assumed to be very large to keep the output voltage constant.

In practice, the output voltage cannot be kept perfectly constant with a finite capacitance.

While the capacitor current is positive, the capacitor is charging.

$$Q = CV_o$$
$$\Delta Q = C\Delta V_o$$
$$\Delta V_o = \frac{\Delta Q}{C}$$



(a)

The change in charge ΔQ is the area of the triangle above the time axis.

$$\Delta Q = \frac{1}{2}\left(\frac{T}{2}\right)\left(\frac{\Delta i_L}{2}\right) = \frac{T\Delta i_L}{8}$$

$$\Delta V_o = \frac{T\Delta i_L}{8C} = \frac{V_o(1-D)}{8LCf^2}$$

ΔV_o is the peak-to-peak ripple voltage at the output. It is also useful to express the ripple as a fraction of the output voltage.

$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8LCf^2}$$

In design, it is useful to rearrange the preceding equation to express required capacitance in terms of specified voltage ripple:

$$C = \frac{1 - D}{8L(\frac{\Delta V_o}{V_o})f^2}$$

If the ripple is not large, the assumption of a constant output voltage is reasonable, and the preceding analysis is essentially valid.

Capacitor Resistance – The effect on Ripple Voltage
A real capacitor can be modeled as a capacitance with an equivalent series resistance (ESR) and an equivalent series inductance (ESL).

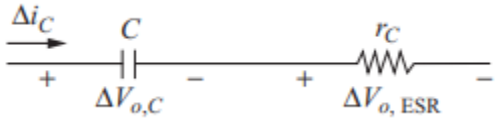
Capacitor ESR is inversely proportional to the capacitance value.

The voltage variation across the capacitor resistance is,

$$\Delta V_{o,ESR} = \Delta i_C r_C = \Delta i_L r_C$$

The ripple voltage due to the ESR can be much larger than the ripple due to the pure capacitance. In that case, the output capacitor is chosen based on the equivalent series resistance rather than capacitance only.

$$\Delta V_{o,C} \approx \Delta V_{o,ESR} = \Delta i_C r_C$$



Design Considerations

- Most buck converters are designed for continuous-current operation.
- As the switching frequency increases, the minimum size of the inductor to produce continuous current and the minimum size of the capacitor to limit output ripple both decrease.
- Increased power loss in the switches means that heat is produced. This decreases the converter's efficiency and may require a large heat sink.
- The inductor value should be larger than L_{min} to ensure continuous-current mode. The main practice is the use 25 percent larger than the L_{min}.
- The ESR of the capacitor should be included because it typically gives a more significant output voltage ripple than the ideal device.
- Typical switching frequencies are above 20kHz to avoid audio noise, and they extend well into the 100s of kilohertz and into the megahertz range.
- The inductor wire must be rated at the rms current, and the core should not saturate for peak inductor current. The capacitor must be selected to limit the output ripple to the design specifications, to withstand peak output voltage, and to carry the required rms current.

LDO AND BUCK PCB DESIGN

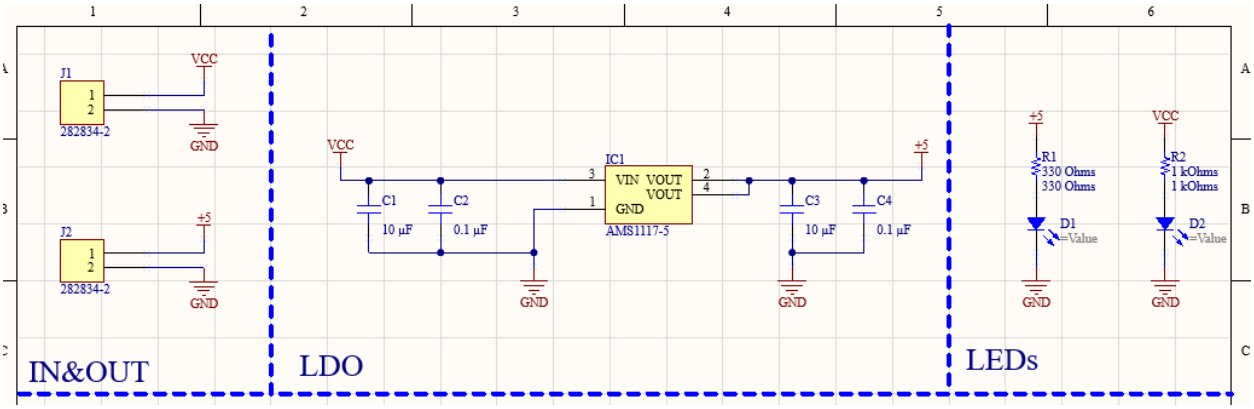
Voltage Regulator

I had several voltage regulators in my mind from LM7805 to AMS1117 and I chose AMS1117 as my final choice since it is a device widely used and a schematic or a PCB design wouldn't change from one regulator to another significantly.

When we examine the datasheet of the device, we see that there are various fixed-output devices available under the name of AMS1117. We are particularly interested in the AMS1117-5.0 low dropout regulator.

We can examine the file further and get the specifications thoroughly but that drawing a schematic of an LDO is rather easy. It only needs decoupling capacitors at the input and the output.

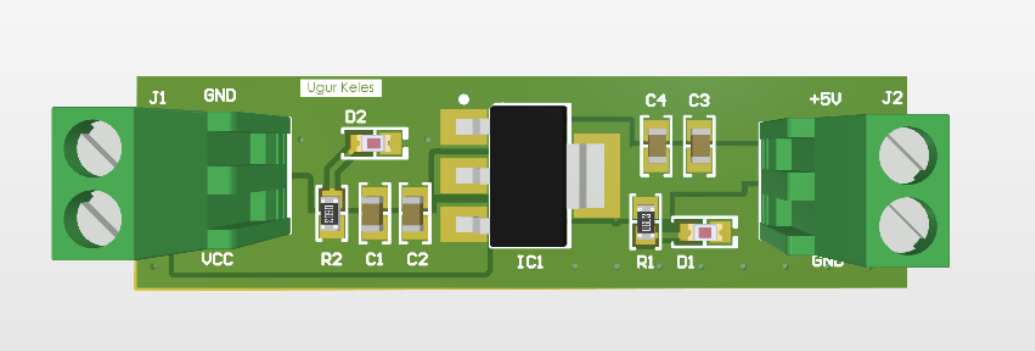
Schematics



Here is the schematics.

In&Out part is for voltage input and voltage output connectors. LEDs are for indicating power. LDO is the part where magic happens. As you can see, all is there to add capacitors. Capacitors are for getting rid of noises and ripples.

PCB of LDO



Here is how the PCB looks.

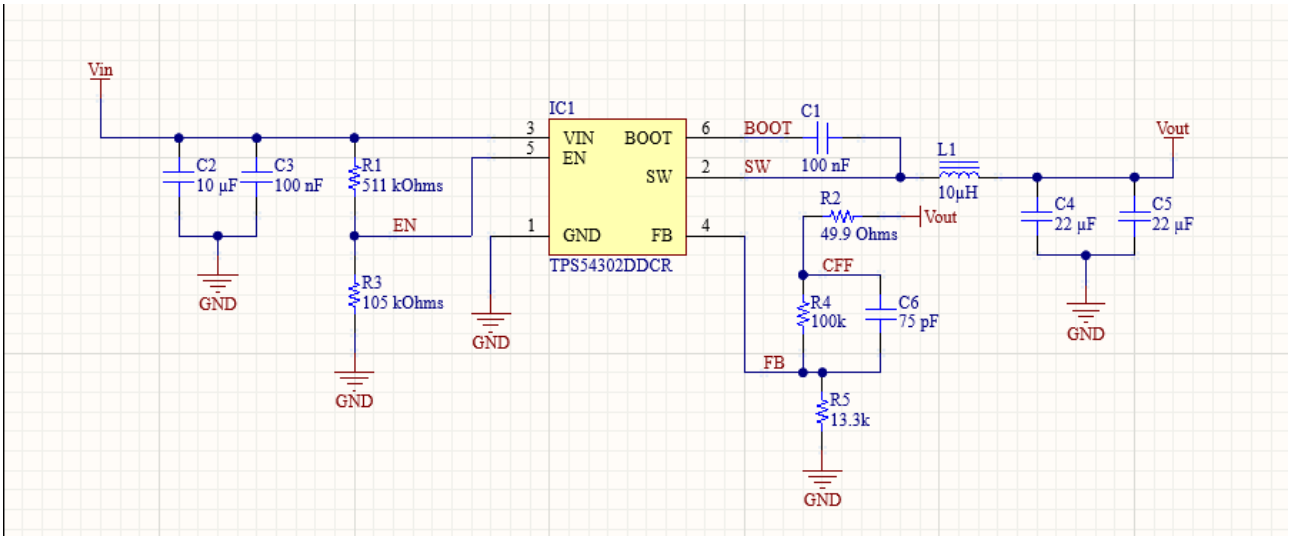
You can’t see the 2D view and thus the traces but if you pay attention to the board, you can make out that I used polygon pours for power traces and GND planes on both side. We talked that LDOs are inefficient due to their capability of dissipating the power as heat. As stated in the datasheet we can decrease total thermal resistance by increasing copper area in application board.

Buck Converter

The first choices I had as a buck converter were MC34063 and LM2596. Then I started to search for a one that I do not know.

I have used JLCPCB parts website, direnc.net and celestial Altium library parts for my research. I chose several components from the Altium library and then I check the availability of the part both in JLCPCB parts and in direnc.net. I chose the cheaper, popular, and available one which is TPS54302.

Schematics



Here is my design and now we will examine it.

First, I have read the datasheet and figured out the general concepts.

Then I started designing using the typical application circuit.

8.2.1 TPS54302 8-V to 28-V Input, 5-V Output Converter

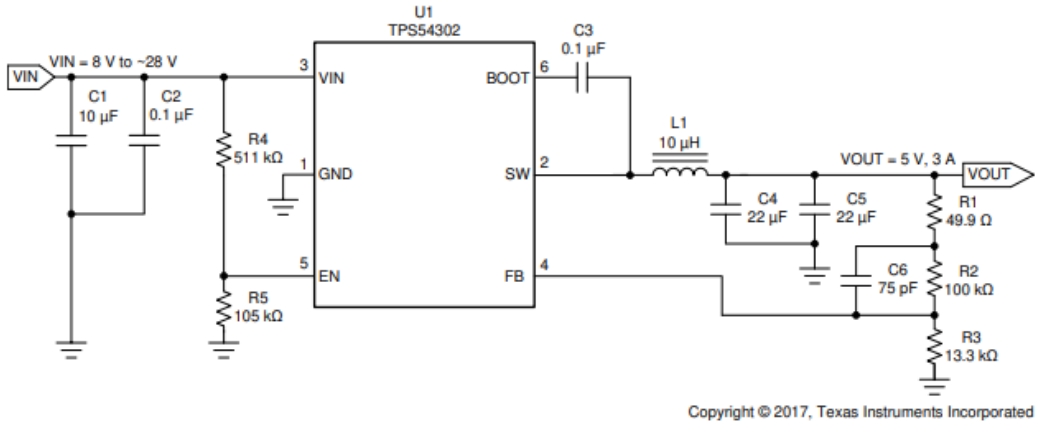


Figure 8-1. 5-V, 3-A Reference Design

Detailed Design Procedure

1. Input Capacitor Selection

The device requires an input decoupling capacitor, and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1-µF capacitor (C2) from the VIN pin to GND is optional to provide additional high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

2. Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to SW pin for proper operation. TI recommends using a ceramic capacitor. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

3. Output Voltage Set Point

Select a value of R2 to be approximately 100 kΩ. Slightly increasing or decreasing the value of R3 can result in closer output voltage matching when using standard value resistors. In this design, R2 = 100 kΩ and R3 = 13.3 kΩ which results in a 5-V output voltage. The 49.9-Ω resistor, R1, is provided as a convenient location to break the control loop for stability testing.

$$R_3 = \frac{R_2 * V_{ref}}{V_{OUT} - V_{ref}} \qquad V_{OUT} = V_{ref} * (\frac{R_2}{R_3} + 1)$$

TI recommends using divider resistors with 1% tolerance or better. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

4. Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) set point can be adjusted using the external-voltage divider network of R4 and R5. The R4 resistor is connected between the VIN and EN pins of the TPS54302 device. The R5 resistor is connected between the EN and GND pins. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the minimum input voltage is 8 V, so the start voltage threshold is set to 6.74 V and the stop voltage threshold is set to 5.83 V.

5. Output Filter Components

Two components must be selected for the output filter: the output inductor (LO) and CO.

- Inductor Selection

  Use the equation to calculate the minimum value of the output inductor (LMIN).

$$L_{MIN} = \frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} * K_{IND} * I_{OUT} * f_{SW}}$$

  where KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

  For this design example, use KIND = 0.35. The minimum inductor value is calculated as 9.78 µH. For this design, a close standard value of 10 µH was selected for LMIN. For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use the equation to calculate the RMS inductor current (IL(RMS)).

$$I_{L(MAX)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} * \left(\frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT}}{V_{IN(MAX)} * L_O * f_{SW} * 0.8}\right)^2}$$

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT})}{1.6 * V_{IN(MAX)} * L_O * f_{SW}}$$

- Output Capacitor Selection

  The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

  Use the equation to calculate the minimum required output capacitance.

$$C_O > \frac{2 * \Delta I_{OUT}}{f_{SW} * \Delta V_{OUT}}$$

Using values in the datasheet results in a minimum capacitance of 30 µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Use the equation to calculate the minimum output capacitance required to meet the output voltage ripple specification. In the datasheet, the maximum output voltage ripple is 30 mV. Under this requirement, the equation yields 10.7 µF.

$$C_O > \frac{1}{8 * f_{SW}} * \frac{I_{ripple}}{V_{OUTripple}}$$

Use the equation to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. The equation indicates the ESR should be less than 29.2 mΩ.

$$R_{ESR} < \frac{V_{OUTripple}}{I_{ripple}}$$

Additional capacitance deratings for aging, temperature, and DC bias should be considered which increases this minimum value. For this example, two 22-uF 25-V, X7R ceramic capacitors are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor datasheets specify the RMS value of the maximum ripple current. Use the equation to calculate the RMS ripple current that the output capacitor must support. For this application, the equation yields 296 mA for each capacitor.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} * (\frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} * L_O * f_{SW} * N_C})$$

- Feedforward Capacitor

Depending on the VOUT, if the output capacitor COUT is dominated by low ESR (ceramic types) capacitors, it could result in low phase margin. To improve the phase, boost an external feedforward capacitor C6 can be added in parallel with R2. The C6 capacitor is chosen such that phase margin is boosted at the crossover frequency.

$$C_6 = \frac{1}{2\pi f_o} * \frac{1}{R_2}$$

The C6 capacitor is not needed when COUT has high ESR, and C6 calculated from the equation should be reduced with medium ESR.

Below you can find the recommended component values.

Table 8-2. Recommended Component Values

V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R2 (kΩ)	R3 (kΩ)	C8 (pF)
1.8	4.7	66	100	49.9	33
2.5	5.6	66	100	31.6	47
3.3	6.8	44	100	22.1	47
5	10	44	100	13.3	75
12	15	44	100	5.23	100

Power Supply Recommendation

The device is designed to operate from an input voltage supply range from 4.5 V to 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

PCB of Buck Converter

Designing a buck converter PCB is something you need to pay attention to very well. It has an inductor, hence electromagnetic effects. So, if you would like to protect signals on your board, you need to design it taking care of guidelines on how to do it.

The datasheet includes a layout practice and guidelines for this purpose.

10.2 Layout Example

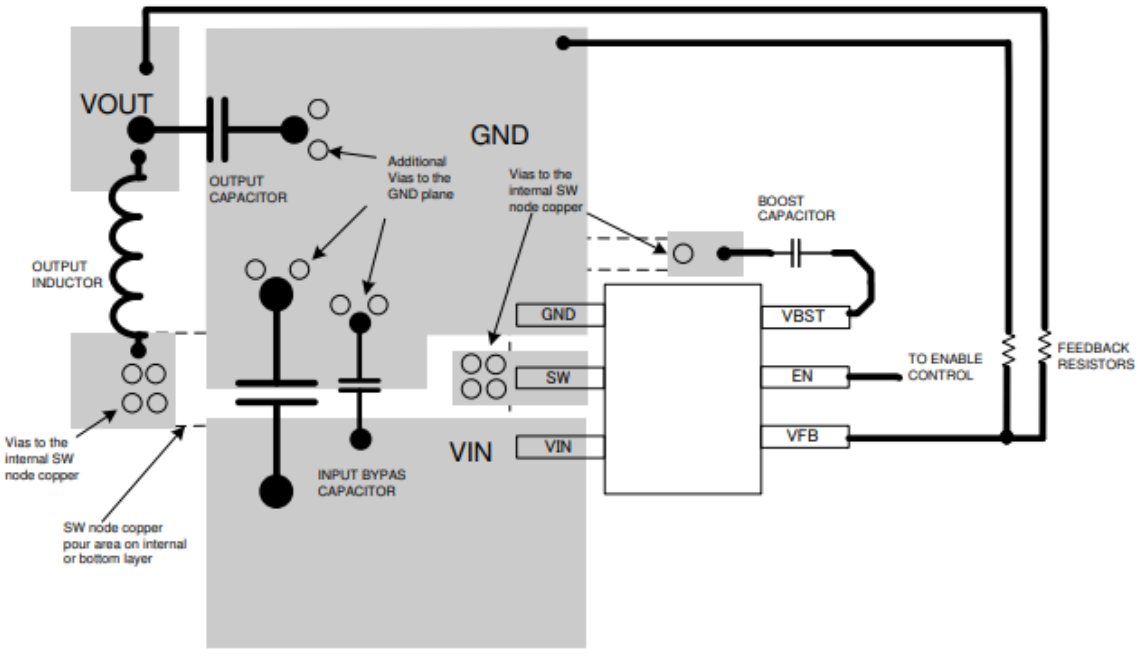


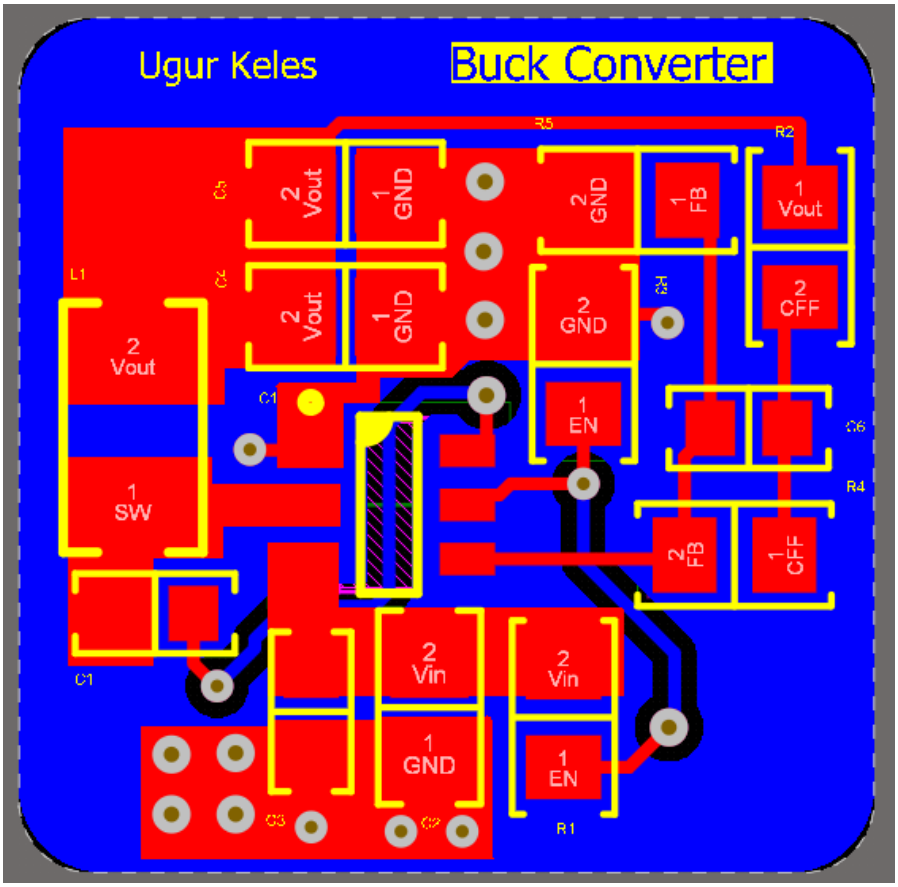
Figure 10-1. Board Layout

Layout Guidelines

Follow these layout guidelines:

• The VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the viewpoint of heat dissipation.
• The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
• Provide sufficient vias for the input capacitor and output capacitor.
• Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
• Do not allow switching current to flow under the device.
• A separate VOUT path should be connected to the upper feedback resistor.
• Make a Kelvin connection to the GND pin for the feedback path.
• The voltage feedback loop should be placed away from the high voltage switching trace, and preferably has ground shield.
• The trace of the VFB node should be as small as possible to avoid noise coupling.
• The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

Here is my design which is different from what it suggests in this guideline.



I used a double layer PCB. I tried to minimize SW node and used polygon pours for VIN and GND planes. I dedicated my double layer as a GND plane. Only two traces routes at the bottom layer. Those are ENABLE and BOOT pins. BOOT pin also goes under the IC. I do not know its

effect but in the datasheet, it is also stated that we do not allow switching current to flow under the device.

Here are some other guides that I preferably followed to design the PCB by myself instead of using the one that is provided in the datasheet. These guides are taken from the YouTube channel Phil's Lab and the YouTube video Switching Power Supply PCB Layout Seminar.

General Layout and Routing Rules

- Keep loops tight.
- Start with critical (high-frequency, high-current) loops first.
- Finish with control circuitry (feedback, enables etc.)
- Keep all high-frequency, high-current components on same side as controller IC.
- Make traces as short and as wide as reasonably possible.
- Keep sensitive lines (feedback) away from areas of high energy (avoid coupling)
- Ground plane directly underneath the switcher.

Here are some of the reasons the recommended layouts from the datasheet cannot be implemented as is:

- Major components are different in size and shape
- Circuit functions omitted or added
- Mechanical restrictions
- Proximity to other circuits and board density
- Additional thermal requirements
- Test requirements
- Fine pitch parts requiring thinner copper weight
- Larger vias required due to board thickness
- Larger vias required due to reliability concerns
- Different number of PCB layers

REFERENCES

- Dr, D. W. H. P. (n.d.). Power Electronics. McGraw-Hill Education.