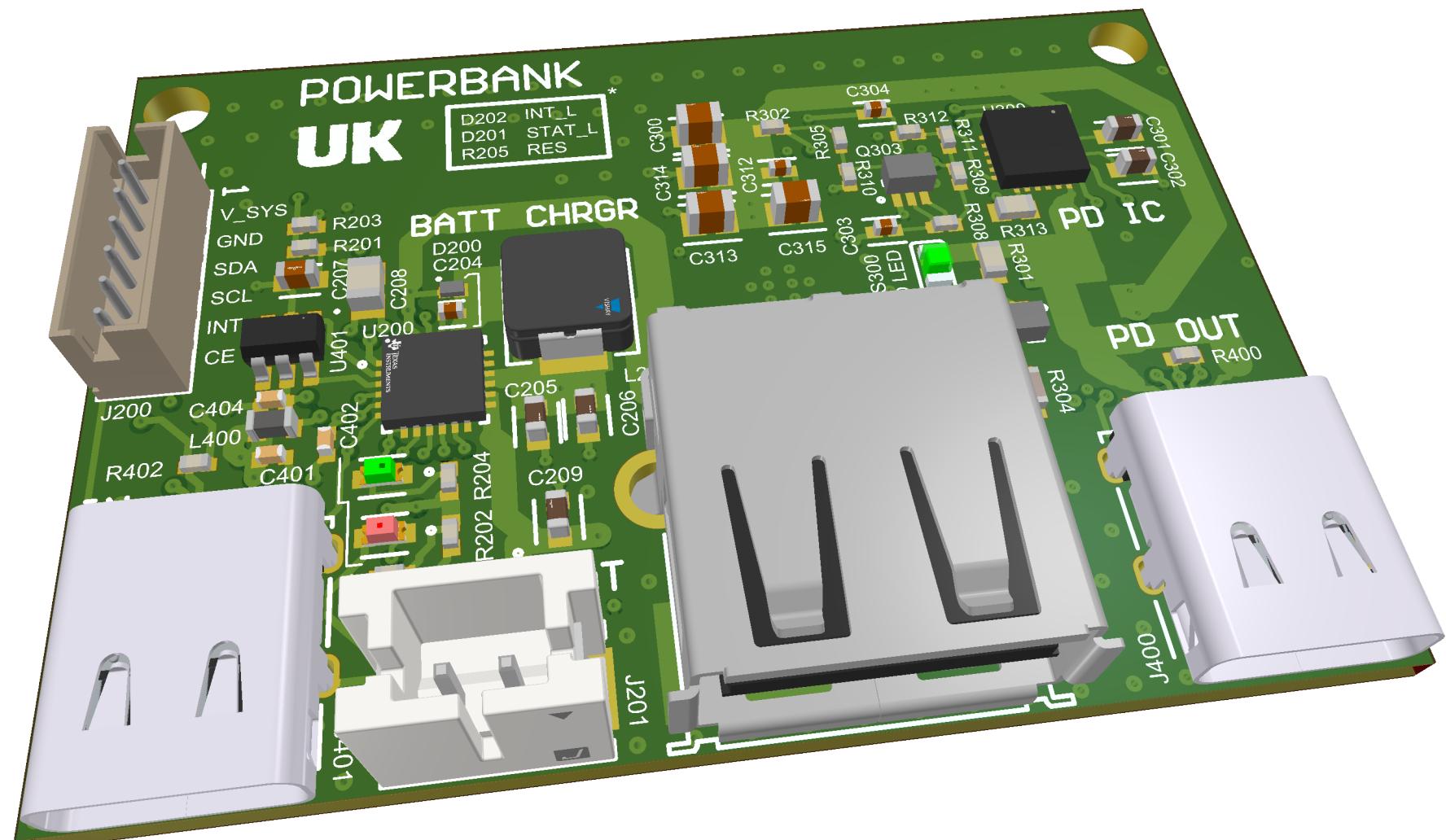


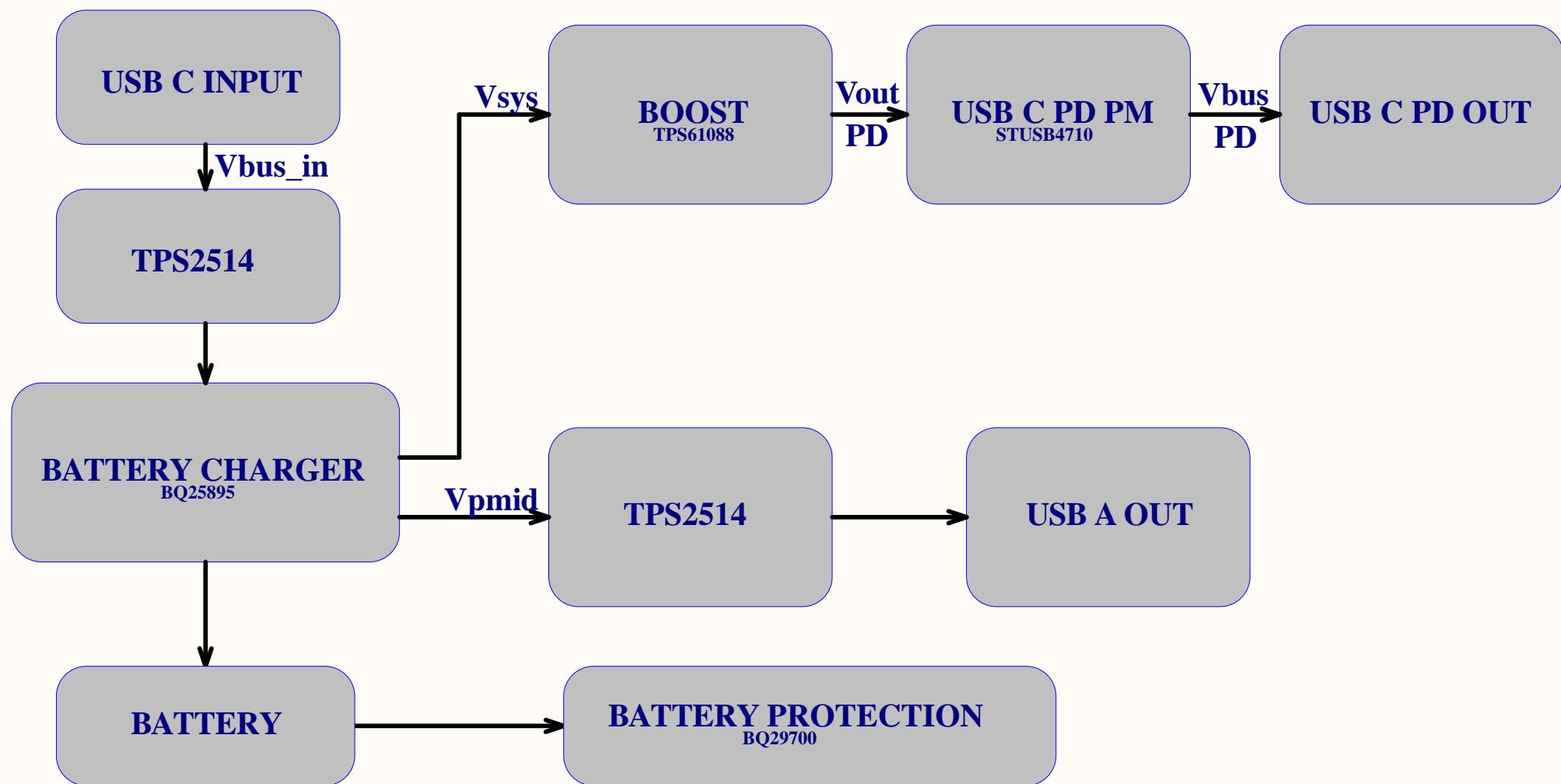
POWERBANK PROJECT

@ugurkeles



Realistic View

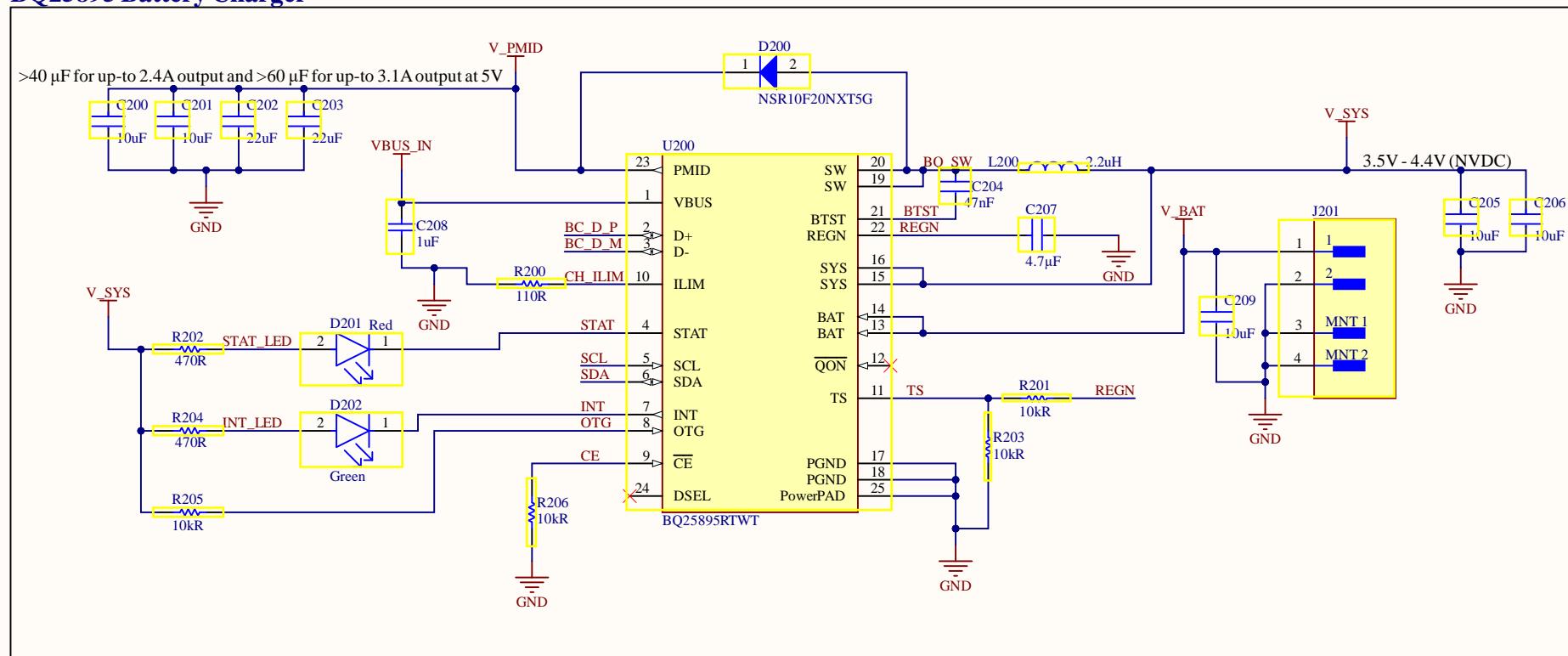
[1] Powerbank Block Diagram



Project Title		Powerbank-PCB.PrjPcb	
Drawn By	Uğur KELEŞ	Sheet Name	PB-Block-Diagram.SchDoc
Date	3/23/2025	Sheet	1 / 4
Sheet Size	A4		

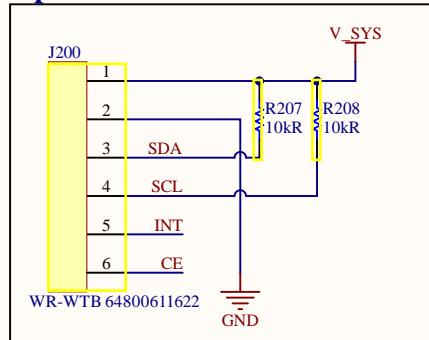
[2] Battery Charger and Protection

BQ25895 Battery Charger

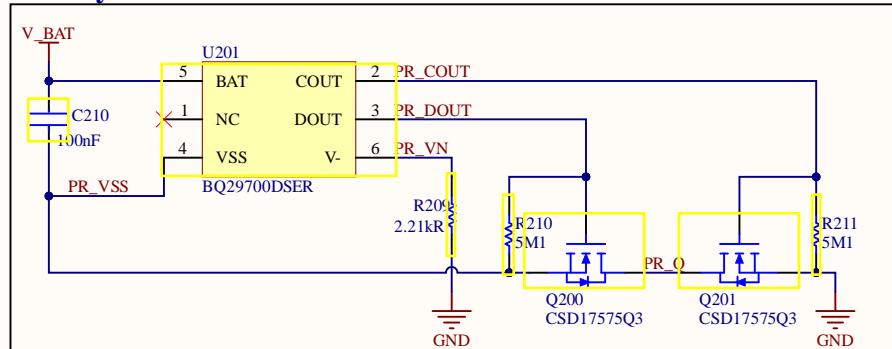


NOTE: INTENDED TO BE USED IN DEFAULT MODE. HOWEVER, NECESSARY CONNECTIONS WILL BE PROVIDED FOR FURTHER MCU IMPLEMENTATION.

Opt. Host Side Conns



Battery Protection



ILIM Pin Res Value Calc

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}}$$

K_{ILIM} VALUES >> TAKE TYP. VALUE = 355
 320 355 390 A x Ω

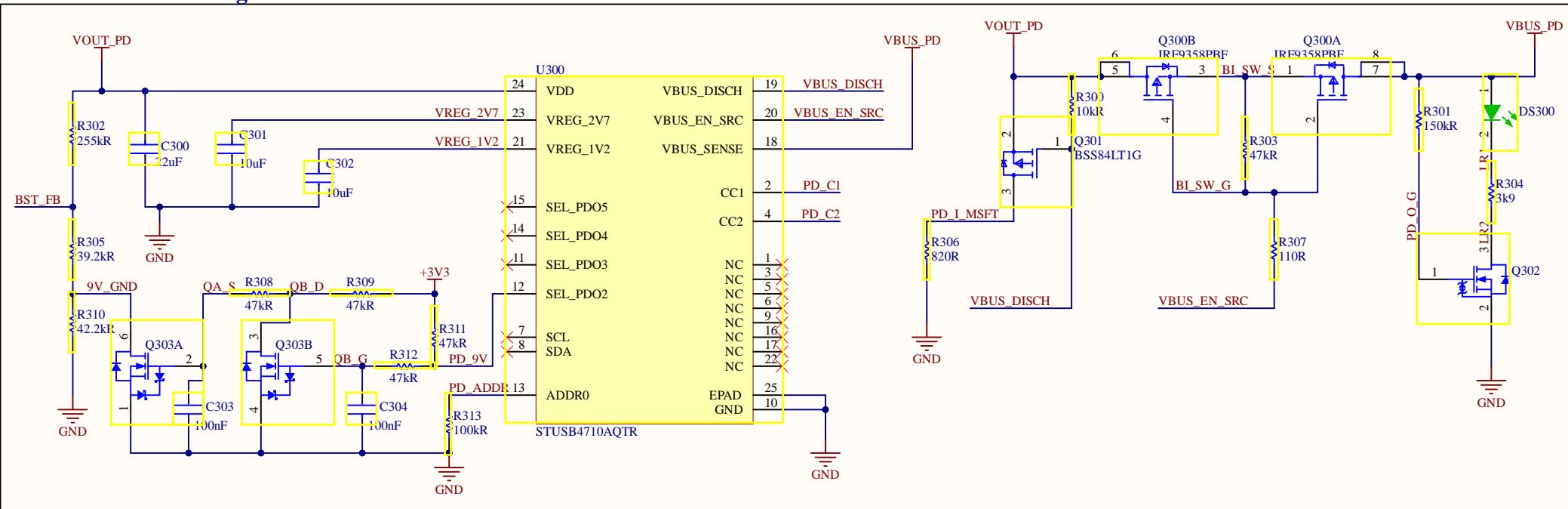
I_{INMAX} is chosen >> 3.25A.
 On doing the math, R_{ILIM} ≈ 110R
 It is the maximum input current limit value.

Project Title Powerbank-PCB.PjPcb

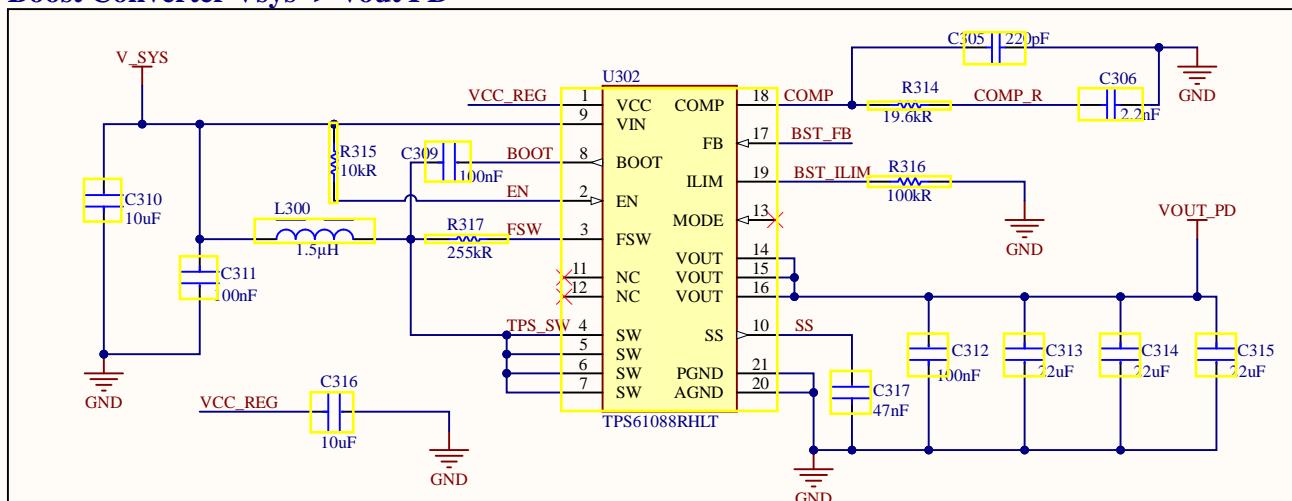
Drawn By	Sheet Name	
Uğur KELEŞ	Battery-Charger.SchDoc	
Date	Sheet	Sheet Size
3/24/2025	2 / 4	A4

[3] PD Management

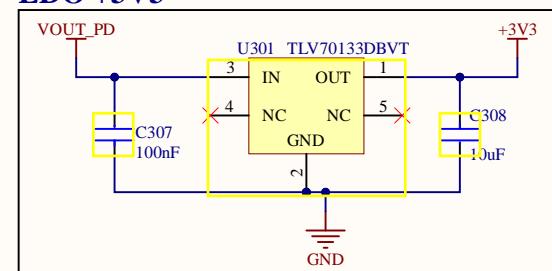
USB PD Source Management



Boost Converter Vsysto -> Vout PD



LDO +3V3



Project Title Powerbank-PCB.PjPcb

Drawn By
Uğur KELEŞ

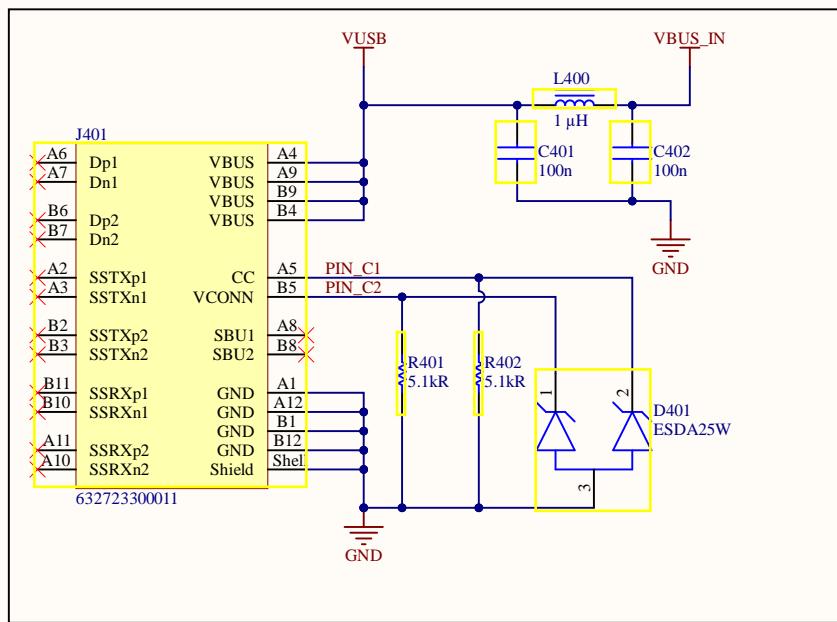
Sheet Name

Power_PD.SchDoc

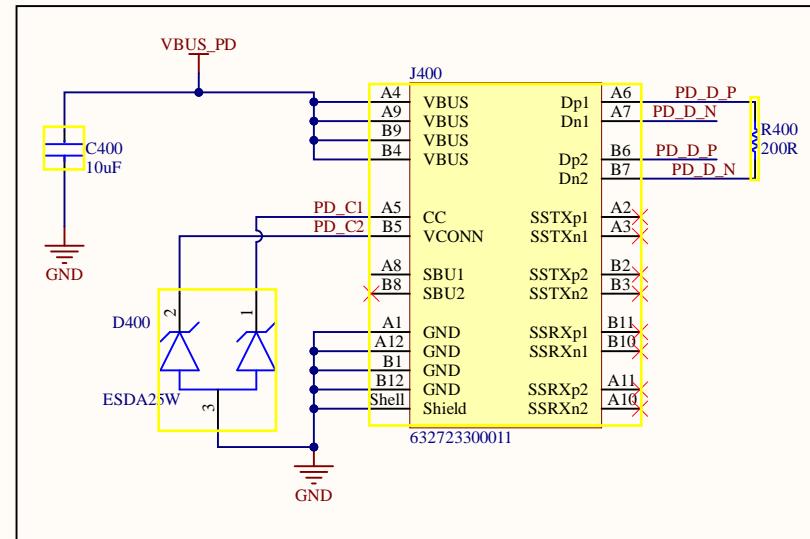
Date 3/24/2025 Sheet 3 / 4 Sheet Size A4

[4] USB Input & Output Connections

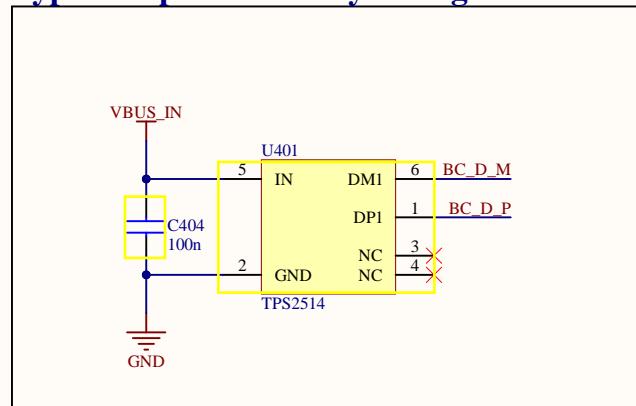
USB C - Input Connector



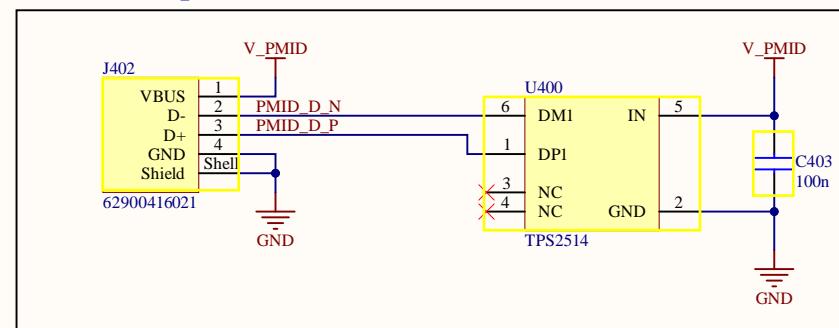
USB C PD - Out



Type C Input to Battery Charger BC1.2



USB A - Output



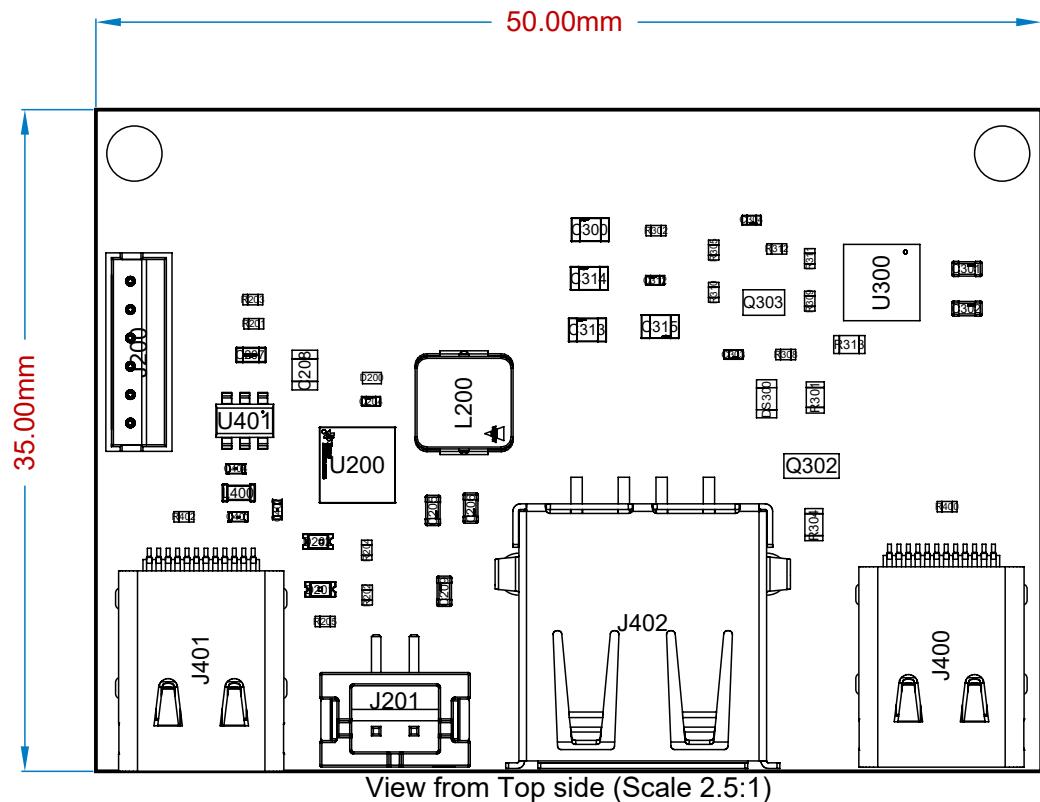
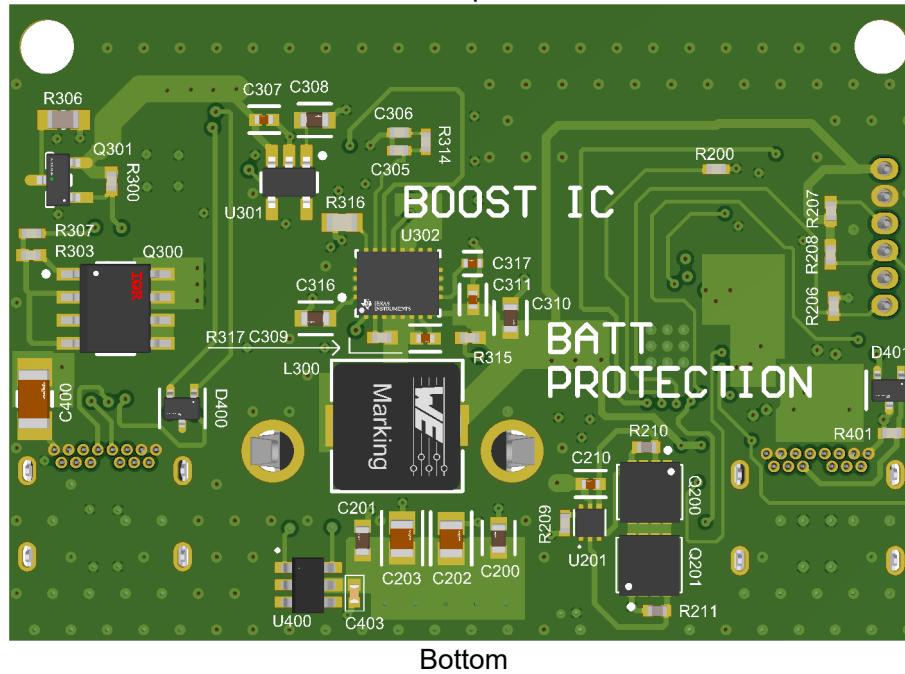
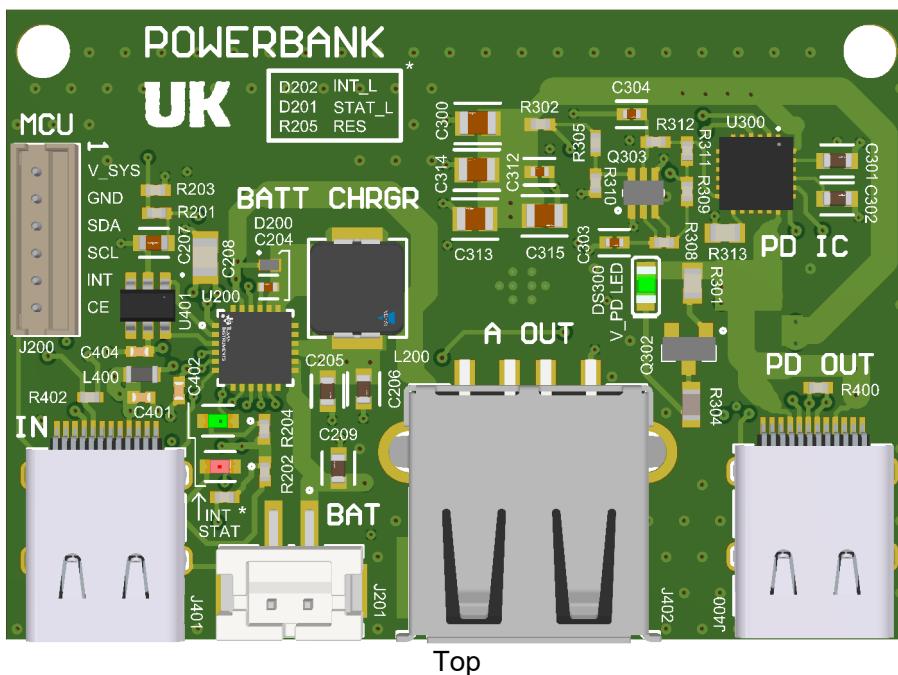
Project Title Powerbank-PCB.PjPcb

Drawn By
Uğur KELEŞ

Sheet Name
USB_CONNS.SchDoc

Date 3/25/2025 Sheet 4 / 4 Sheet Size A4

TOP AND BOTTOM



STACKUP

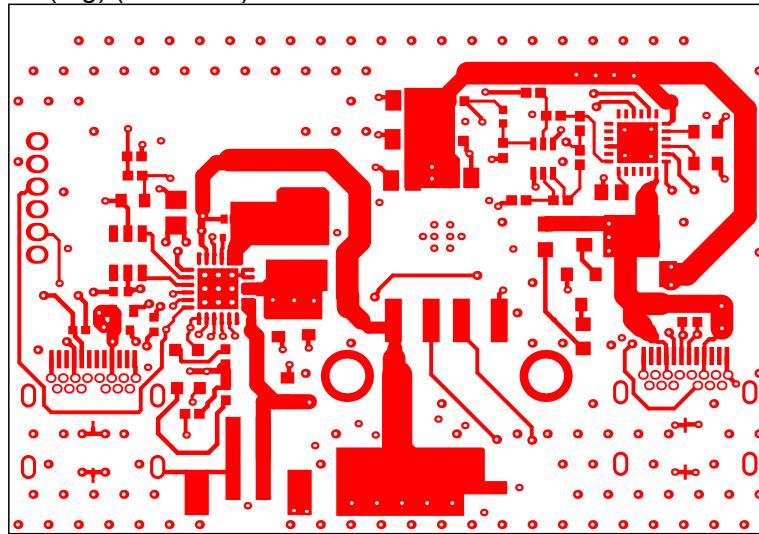
Layer Stack Legend		Material	Layer	Thickness	Dielectric Material	Type	Gerber
			Top Overlay			Legend	GTO
		Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
		Copper	L1 (Sig)	0.04mm		Signal	GTL
		Prepreg		0.10mm	PP-015	Dielectric	
		CF-004	L2 (GND)	0.02mm		Signal	G1
				1.26mm	FR-4	Dielectric	
		CF-004	L3 (GND)	0.02mm		Signal	G2
		Prepreg		0.10mm	PP-015	Dielectric	
		Copper	L4 (Sig)	0.04mm		Signal	GBL
		Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
			Bottom Overlay			Legend	GBO
	Total thickness: 1.58mm						

Notes:

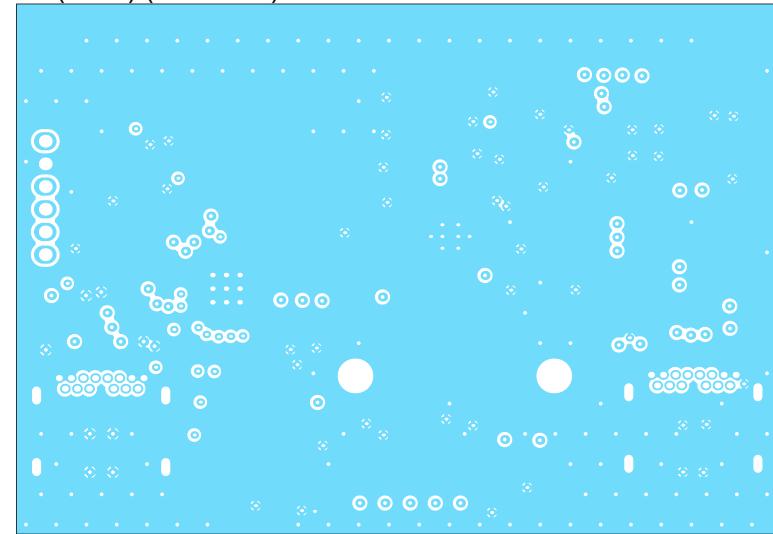
1. The stack-up data was generated using JLCPCB. JLC04161H-3313 was utilized, with calculations based on USB differential parameters, even though differential tracks were not implemented.
2. The stack-up configuration S/P-G-G-S/P is used. Power is routed as tracks rather than utilizing a power plane.

LAYERS

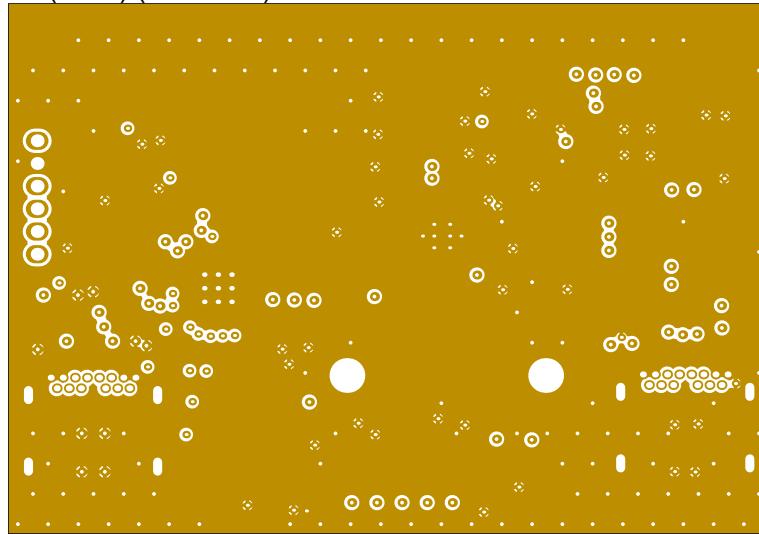
L1 (Sig) (Scale 2:1)



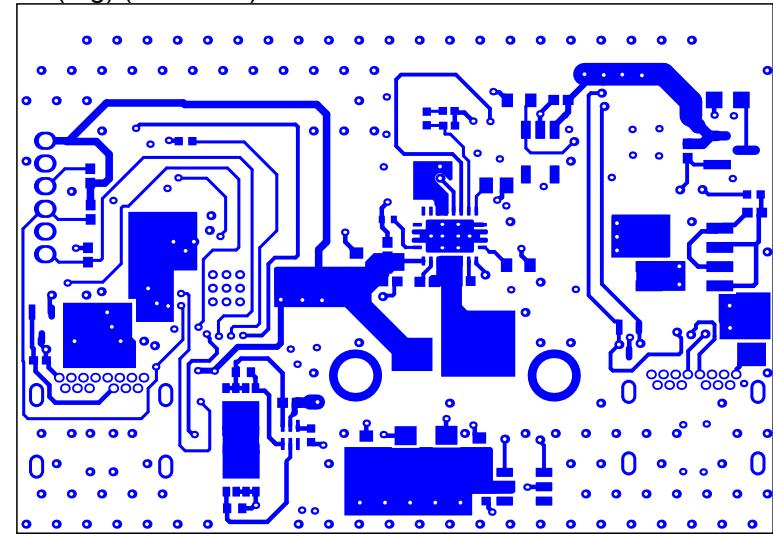
L3 (GND) (Scale 2:1)



L2 (GND) (Scale 2:1)



L4 (Sig) (Scale 2:1)



CONTENTS

- Batteries
- Battery Chargers and Direct vs Path Management
- Topologies
- Battery Protection
- Inductors
- Boost Converter
- USB CHARGING METHODS(USB 2.0, USB 3.1, USBBC 1.2, Special Brands Charging, USB Type-C 1.2, USB PD)
- I2C

- 4-Layer Boards
- Vias
- Traces
- Thermal Management

INTRODUCTION

Similar to the previous projects I've shared, this project focuses on exploring various hardware design concepts. Each concept will be analyzed and clearly explained.

BATTERIES

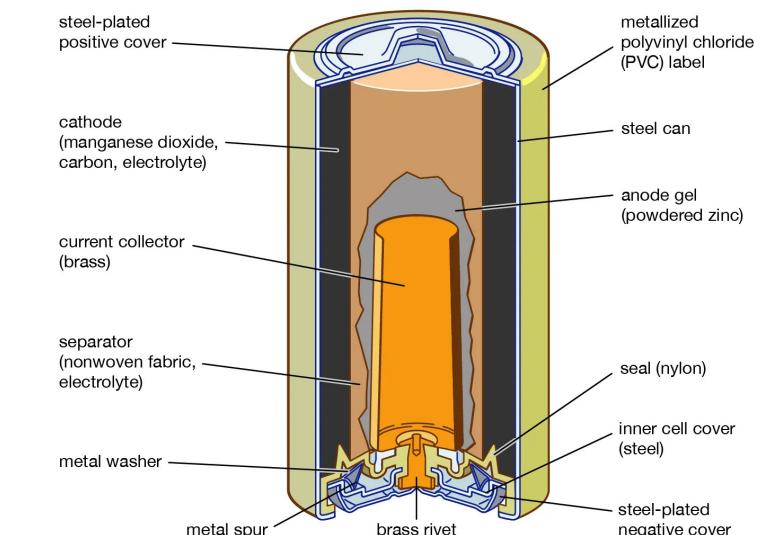
A battery is a device that stores chemical energy and converts it into electrical energy through an electrochemical reaction. It consists of one or more electrochemical cells, where chemical reactions drive the flow of electrons, generating electricity.

Applications of Batteries:

- Provide portable power for devices (e.g., phones, laptops, EVs).
- Act as a backup power source (e.g., UPS, solar storage).
- Enable wireless operation of electronics.

Battery Performance Metrics

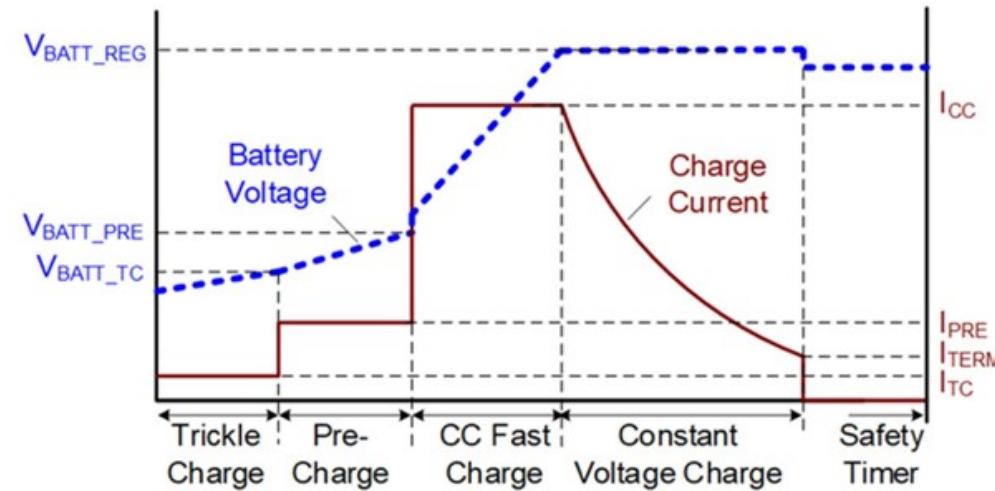
- CAPACITY (Ah, mAh):** Measures how much charge a battery can store.
- ENERGY DENSITY (Wh/kg, Wh/L):** Measures how much energy a battery can store per unit weight or volume.
- C-RATE (Charge & Discharge Rate):** Defines how fast a battery can be charged or discharged relative to its capacity.
- CYCLE LIFE (Number of Charge-Discharge Cycles):** Indicates how many times a battery can be charged and discharged before losing capacity.
- DEPTH OF DISCHARGE (DoD):** The percentage of capacity used before recharging.
- STATE OF CHARGE (SoC):** The percentage of charge remaining in the battery.



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CC-CV Charging Method

- CONSTANT CURRENT (CC):** The initial charging stage where the battery is charged at a constant current until it reaches a predefined voltage.
- CONSTANT VOLTAGE (CV):** After reaching the target voltage, the current gradually decreases while the voltage remains constant.



Battery Types

1. Primary (Non-rechargeable) Batteries

These are single-use batteries and cannot be recharged.

-**ALKALINE BATTERIES:** Common in household devices like remote controls and toys (e.g., AA, AAA).

-**LITHIUM BATTERIES:** Lightweight with high energy density, used in cameras and medical devices.



2. Secondary (Rechargeable) Batteries

These can be recharged multiple times.

-**LITHIUM-ION (LI-ION):** High energy density, long cycle life, used in smartphones, laptops, and electric vehicles.

-**LITHIUM POLYMER (LI-PO):** Slim and lightweight, often found in drones and wearable tech.

BATTERY CHARGERS

A battery charger is an electrical device used to restore energy to a rechargeable battery by supplying it with the appropriate amount of electrical power. It typically converts AC (alternating current) from a wall outlet or DC (direct current) from another power source into the necessary voltage and current to charge the battery.

Selection Criteria

-Battery Type and Configuration

Ensure compatibility with the chemistry (e.g., Li-ion, NiMH) and configuration (e.g., single-cell, multi-cell) of the battery.

-Input Voltage Range

Select a charger that accepts the input voltage available from your power source.

-Charging Current (Maximum)

Choose a device capable of providing the maximum current required to charge the battery efficiently.

-Protection Features

Include integrated circuits for safety. Examined below.

-External Components

Assess the number and type of external components required for the circuit design (e.g., capacitors, resistors).

-Efficiency

Choose a charger with high conversion efficiency to minimize energy loss during charging.

-Package Type

Select a package type suitable for your design, such as compact QFN or TSSOP packages.

-Features and Customization

Look for additional features like: I2C/SPI communication interfaces, status indicators or enable/disable functionality.

-Charging Speed

Slow charging for low power devices or fast charging.

Power Path Management

Power path management enables a charger to supply power to both the battery and the device simultaneously. This ensures uninterrupted operation of the device even when the battery is being charged. It separates the power supply and battery paths, improving efficiency and system reliability.

NVDC (Narrow Voltage Direct Current)

NVDC technology is commonly used in chargers for portable devices. In an NVDC system:

- The charger dynamically adjusts the output voltage to maintain a stable and narrow voltage range.
- This ensures efficient power delivery to the system load and battery, optimizing charging speed and reducing energy loss.
- NVDC also enables seamless switching between battery power and external power without disruption, enhancing user experience.

Popular ICs

-TP4056

Ideal for Li-ion single-cell batteries with integrated protection features.

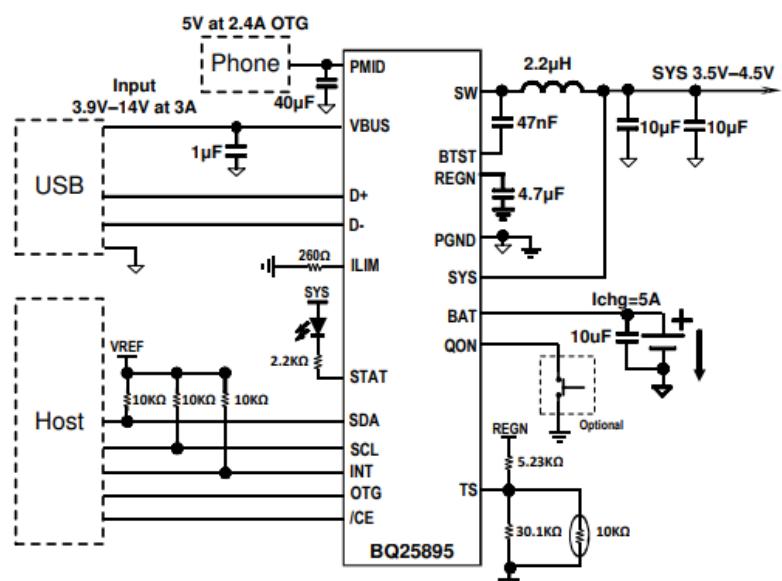
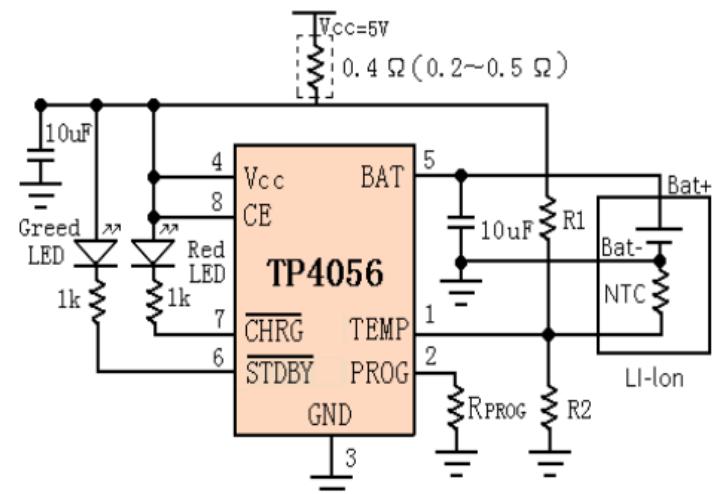
-BQ25895

Supports NVDC, fast charging, and power path management.

-MCP73871

Suitable for Li-ion/polymer batteries with dual power inputs and power path management.

TYPICAL APPLICATIONS



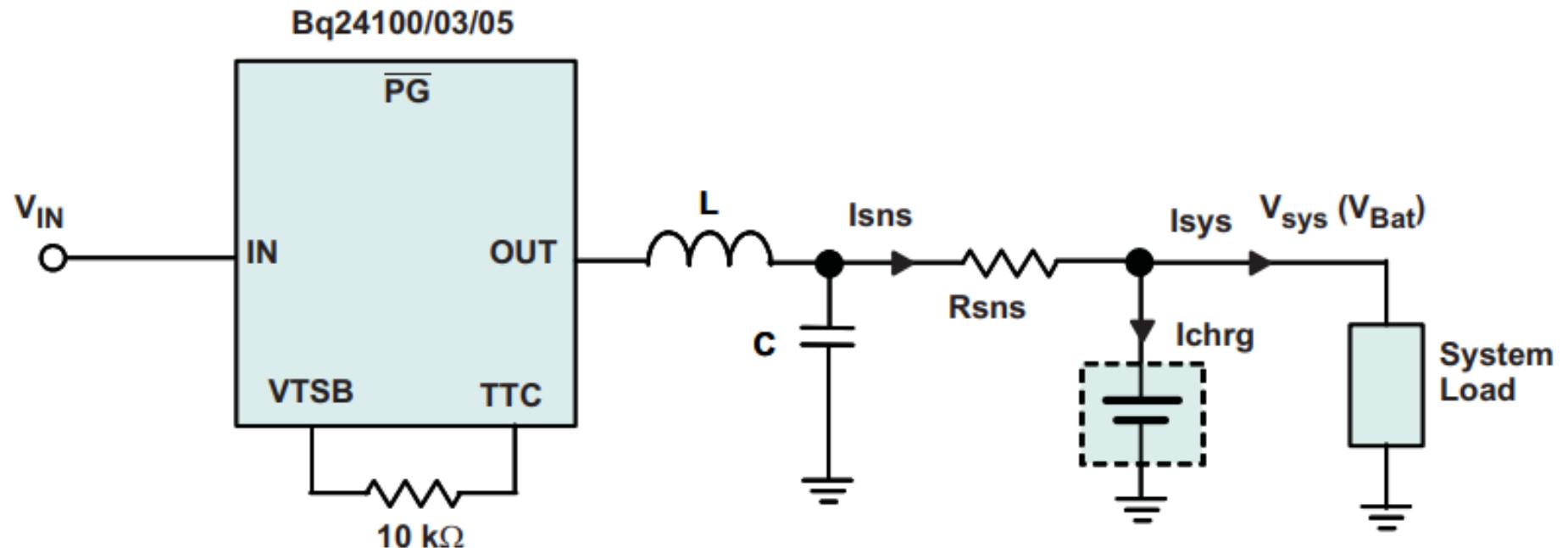
A B C D E

Direct Connection vs Path Management

The source is "Implementations of Battery Charger and Power-Path Management System Using bq2410x/11x/12x (bqSWITCHER™)"

Direct Connection Topology

In a direct connection topology, the charger output and battery are directly connected to the system power bus.

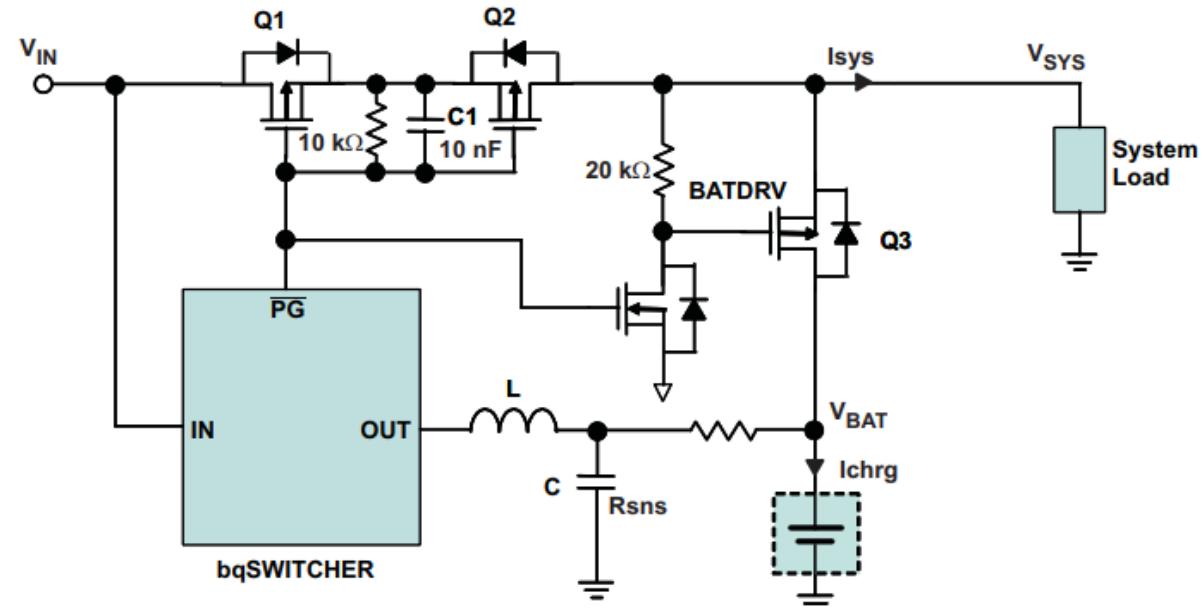


Key Characteristics

- The system load and battery share the same current path.
- The charger regulates the total current, which includes both the system load and the battery charging current.
- If the system load is high, the battery may not charge fully or efficiently.
- Charging termination is based on current thresholds (e.g., TP4056 terminates charging when the current drops to 1/10th of the charging current). If the system load exceeds this threshold, charging may never terminate.
- The battery may experience cycling between charging and discharging due to system load fluctuations, reducing its

Path Management Topology

In a path management topology, the input power is split between the system load and the battery charging path using a switching network.



Key Characteristics

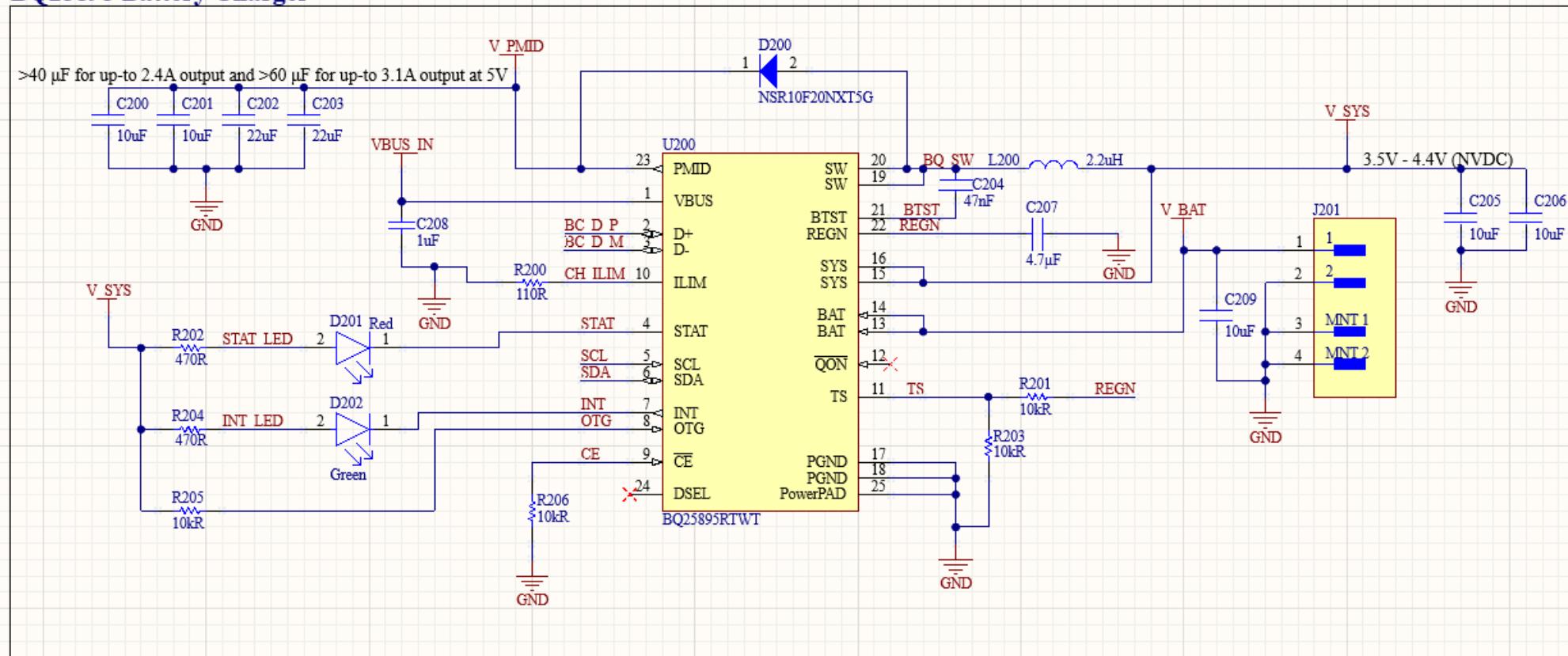
- The system load and battery charging are independent of each other.
- The system load is powered directly by the input source, while the remaining power is used to charge the battery.
- Charging termination is unaffected by the system load, ensuring proper battery management.
- Even if the battery is deeply discharged or faulty, the system can still operate as long as the input power is available.
- Path management improves efficiency and prevents issues like cycling or false charge termination.

Example

- TP4056 uses a direct connection topology, which can lead to issues like indefinite charging if the system load exceeds the termination threshold.
- BQ25895 implement path management, ensuring seamless operation and efficient power distribution.

BATTERY CHARGER IMPLEMENTATION

BQ25895 Battery Charger



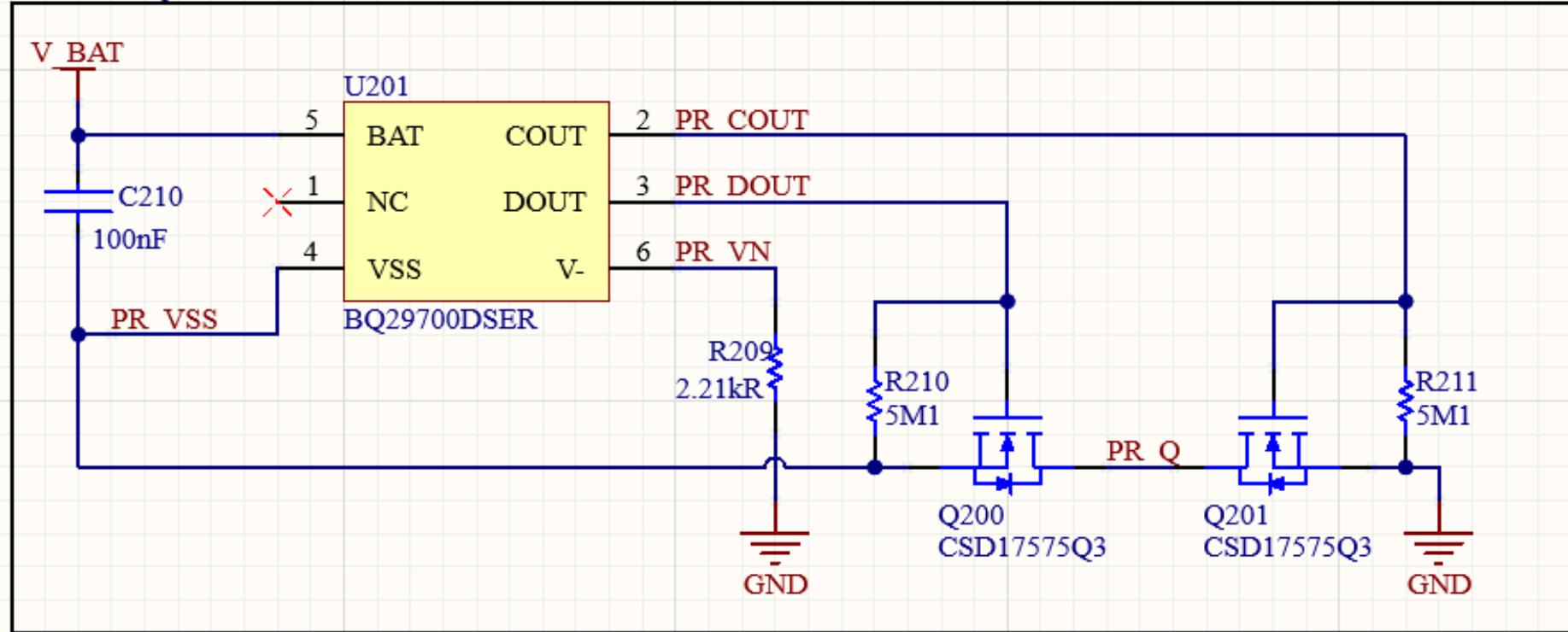
NOTE: INTENDED TO BE USED IN DEFAULT MODE. HOWEVER, NECESSARY CONNECTIONS WILL BE PROVIDED FOR FURTHER MCU IMPLEMENTATION.

Notes:

3. Power is supplied via VBUS_IN, and the input current regulation is determined by both the ILIM pin and input type detection using the data pins.
4. PMID is the boosted voltage generated by the internal boost converter. To activate it, the OTG pin must be pulled high.
5. STAT and INT are designated for status signaling, while SCL and SDA facilitate external host communication. CE serves as the chip enable pin, and TS, although intended as a temperature sensor, is not utilized in this configuration.
6. BAT serves as the battery connection, while SYS represents the system output voltage. SYS is routed to an external boost converter for USB Power Delivery (USB PD), whereas PMID is utilized for USB Type-A charging.

BATTERY PROTECTION IMPLEMENTATION

Battery Protection



BQ29700 Overview

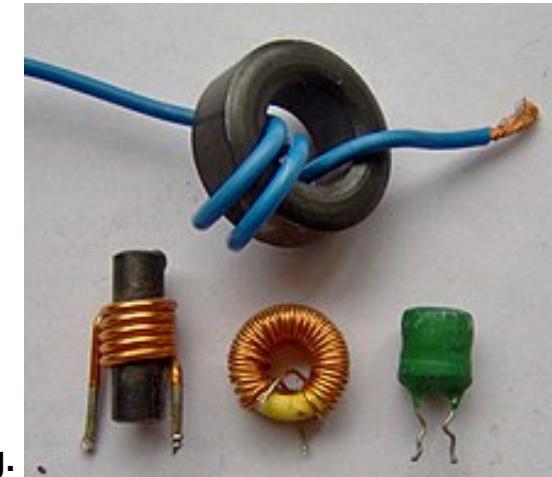
The BQ29700 is a single-cell battery protection IC designed for Li-ion and Li-polymer batteries. It offers comprehensive protection features, including overvoltage protection (OVP) to prevent overcharging, undervoltage protection (UVP) to safeguard against excessive discharge, and overcurrent protection (OCP) for both charging and discharging scenarios. Additionally, it includes short-circuit protection (SCP) to handle load faults and zero-voltage charging capability for depleted batteries. The IC operates with low power consumption in normal mode and features factory-programmed fault thresholds for precise monitoring. Its compact 6-pin DSE package makes it ideal for portable devices like smartphones, tablets, and other handheld electronics.

INDUCTORS

An inductor is a passive electrical component that stores energy in a magnetic field when current flows through it. It resists changes in current according to Faraday's Law of Induction and Lenz's Law. Characterized by its inductance (L), measured in Henries (H), it opposes abrupt current fluctuations and plays a fundamental role in many electronic circuits.

Key Applications

- ENERGY STORAGE:** In power converters (buck, boost) to regulate voltage and current.
- FILTERING:** Smooths out voltage/current ripples in power supplies and suppresses EMI.
- SIGNAL PROCESSING:** Used in RF circuits for impedance matching, frequency tuning, and filtering.
- RESONANCE:** Forms oscillatory LC circuits for radio tuning and frequency selection.

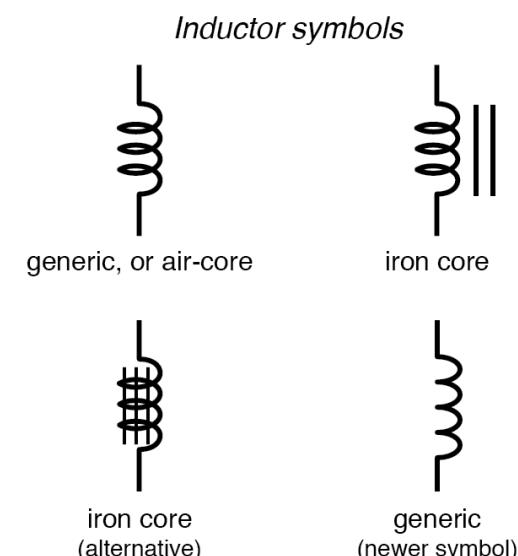


Design Considerations

- INDUCTANCE (L):** Determines energy storage and filtering capability.
- MAXIMUM CURRENT RATING (I_{max}):** Ensure it handles peak current without overheating.
- SATURATION CURRENT (I_{sat}):** Prevents performance issues caused by core saturation.
- DC RESISTANCE (DCR):** Lower values reduce energy loss and heat buildup.
- SELF-RESONANT FREQUENCY (SRF):** The frequency where parasitic effects dominate performance.
- QUALITY FACTOR (Q):** Efficiency measurement in resonant and RF circuits.

Core Materials

- AIR CORE:** No saturation, excellent for RF applications.
- FERRITE CORE:** High inductance and EMI suppression, perfect for power filters.
- IRON POWDER:** Smooth saturation for switching regulators.
- TOROIDAL CORE:** Compact design with low EMI for transformers and power supplies.



BOOST CONVERTERS

A boost converter steps up input voltage to a higher output voltage by storing energy in an inductor during the switch-on phase and releasing it during the switch-off phase. The output voltage is regulated by adjusting the duty cycle, ensuring stable voltage conversion for various applications.

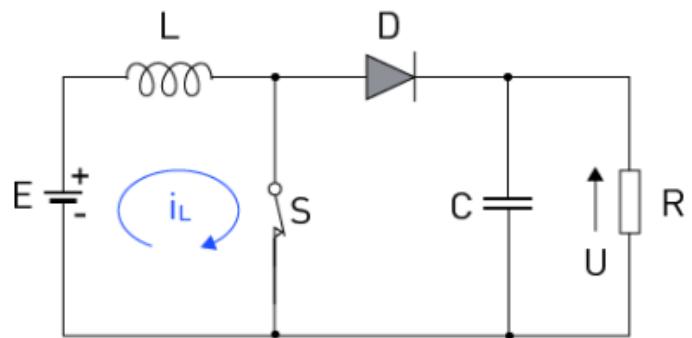


Figure 5: The Boost Converter Circuit Diagram – Interval t_{ON}

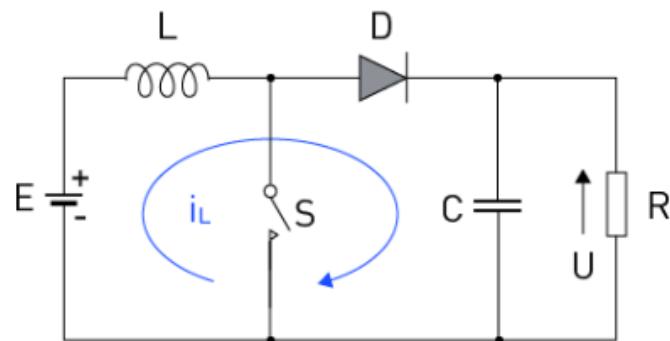


Figure 6: The Boost Converter Circuit Diagram – Interval t_{OFF}

Key Components

- Inductor (L): Stores and releases energy during switching cycles.
- Switch (S): Controls energy flow, typically a MOSFET or IGBT.
- Diode (D): Prevents reverse current flow and directs energy to the output.
- Capacitor (C): Smooths output voltage to ensure stability.

Conduction Modes

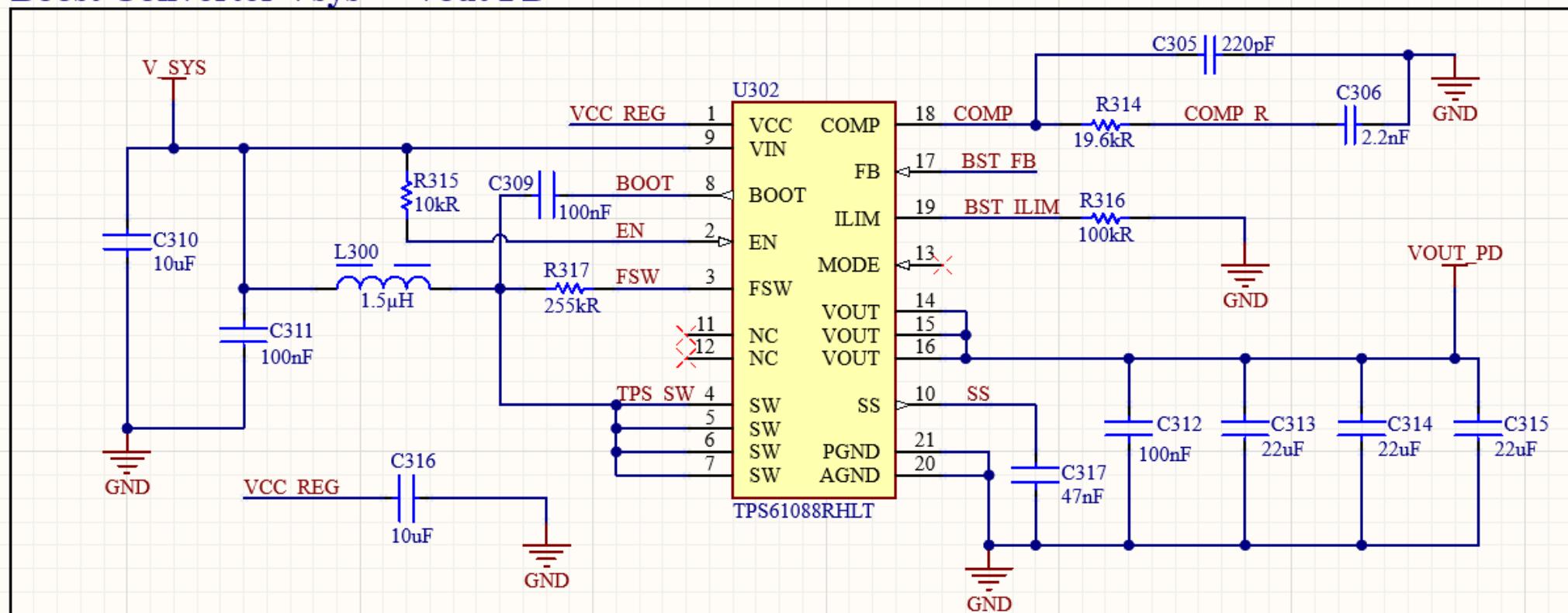
1. Continuous Conduction Mode (CCM): Inductor current never reaches zero, offering lower ripple and higher efficiency but requiring larger inductors.
2. Discontinuous Conduction Mode (DCM): Inductor current drops to zero, allowing compact designs but with higher ripple and lower efficiency.

Notes:

7. The source of this information is Boost Converters (Step-Up Converter) by MPS. For detailed calculations, visiting the website is recommended.

BOOST CONVERTER IMPLEMENTATION

Boost Converter Vsys -> Vout PD



Notes:

8. The SYS voltage is boosted for USB Power Delivery (USB PD). By employing a feedback mechanism with a PD Source controller, the required voltage and current levels are accurately delivered.

USB CHARGING METHODS

Version	Maximum Power	Voltage	Maximum Current
USB 2.0	2.5 W	5 V	500 mA
USB 3.1	4.5 W	5 V	900 mA
USB BC 1.2	7.5 W	5 V	1.5 A
USB Type-C 1.2	15 W	5 V	3 A
USB PD	100 W	5/9/15/20 V	5 A

Evolution of USB power levels. Image: CUI Inc.

Default Modes

In the default USB modes, USB 2.0 supplies 500 mA, while USB 3.1 offers 900 mA. These standards were designed with limited current capabilities, so precautions should be taken to ensure the current is restricted, preventing sink devices from demanding more amperes than intended.

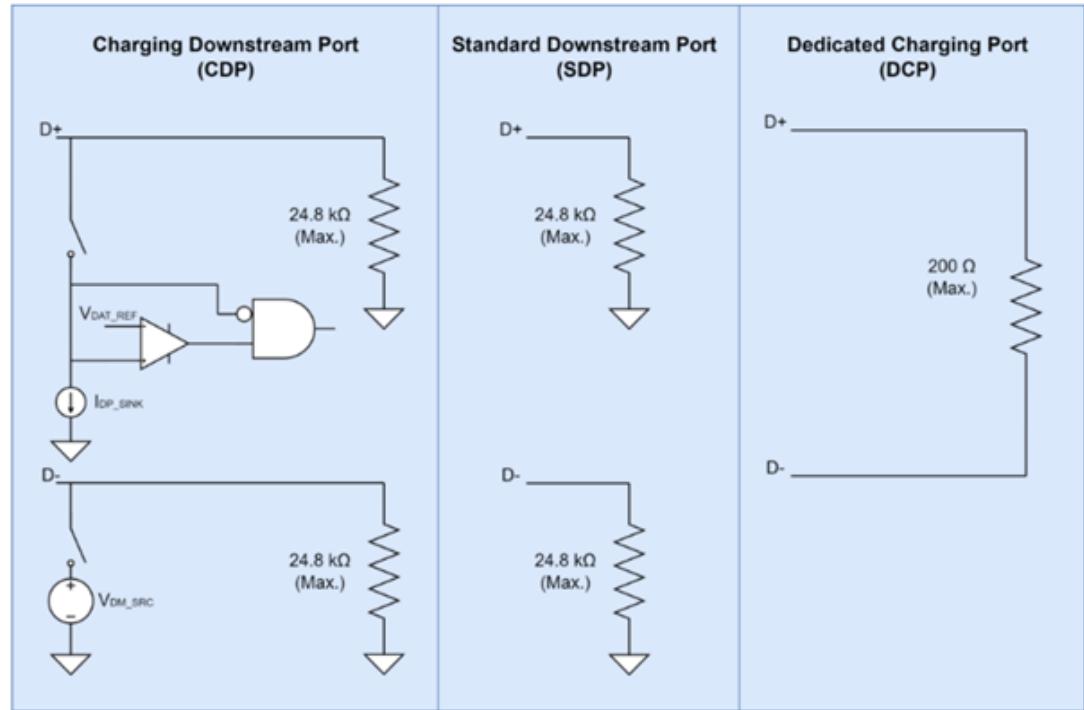
USB BC 1.2

Introduced to meet the increasing power demands of modern devices, USB BC 1.2 expanded on the default modes. It defines three port types for charging:

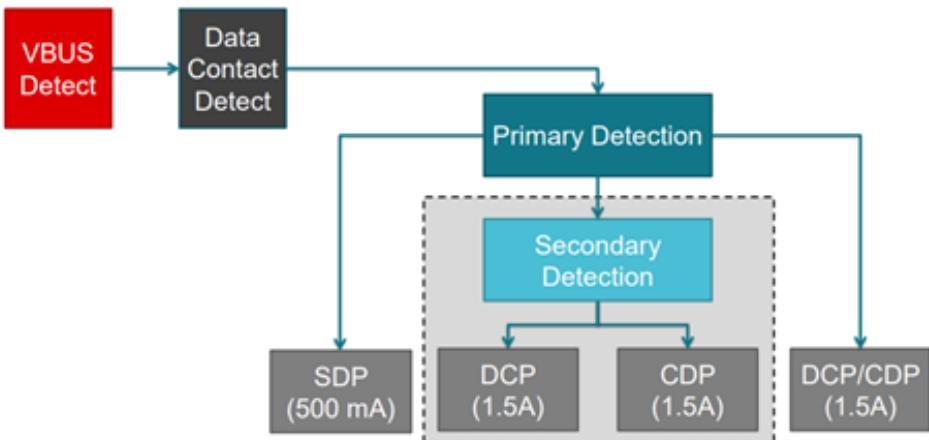
- Standard Downstream Port (SDP): Allows data transfer and supplies 500 mA (USB 2.0) or 900 mA (USB 3.0).
- Charging Downstream Port (CDP): Supports both data transfer and up to 1.5 A of charging current.
- Dedicated Charging Port (DCP): Provides 1.5 A for charging but without data transfer capability.

Notes:

9. Different USB port types, such as SDP, CDP, and DCP, are distinguished by variations in data pin configurations and circuitry, enabling diverse charging and data transfer capabilities.
10. The sources for this information are Understanding USB Battery Charging 1.2 by Emlogic and What is USB Battery Charging 1.2 (USB BC 1.2)? by TI. For detailed insights, consulting these resources is recommended.

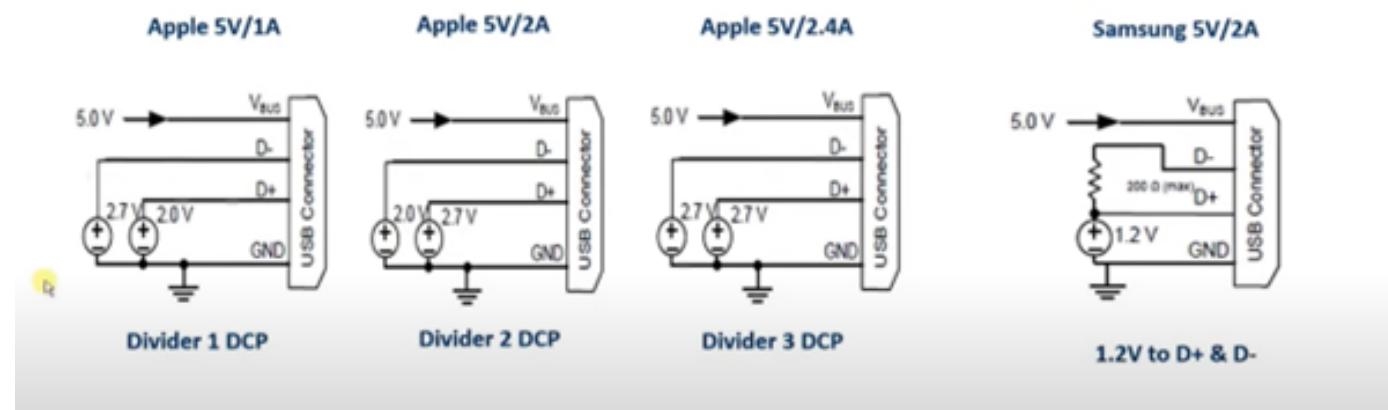


Charger detection by a portable device



Special Brands Charging

It was recognized that increasing power levels were necessary over time, leading to the development of BC1.2. Similarly, various brands have designed proprietary charging circuitries to enable faster charging for their devices. Like BC1.2, these proprietary systems fundamentally rely on modifications to the data pin configurations.



Notes:

11. Other charging standards include proprietary technologies like Sony Fast Charging and Qualcomm Quick Charge versions 2.0 A/B and 3.0, which enable faster charging by leveraging advanced data pin configurations and power delivery methods.
12. To gain deeper insights into charging processes, including USB Power Delivery (USB PD), it is recommended to explore the video [How does mobile phone fast charging work?](#) by Richtek Technology and the resource [USB-IF Power Delivery](#). These provide valuable explanations and technical details about fast charging and USB PD advancements.,

USB Power Delivery

1. USB Type-C Without PD:

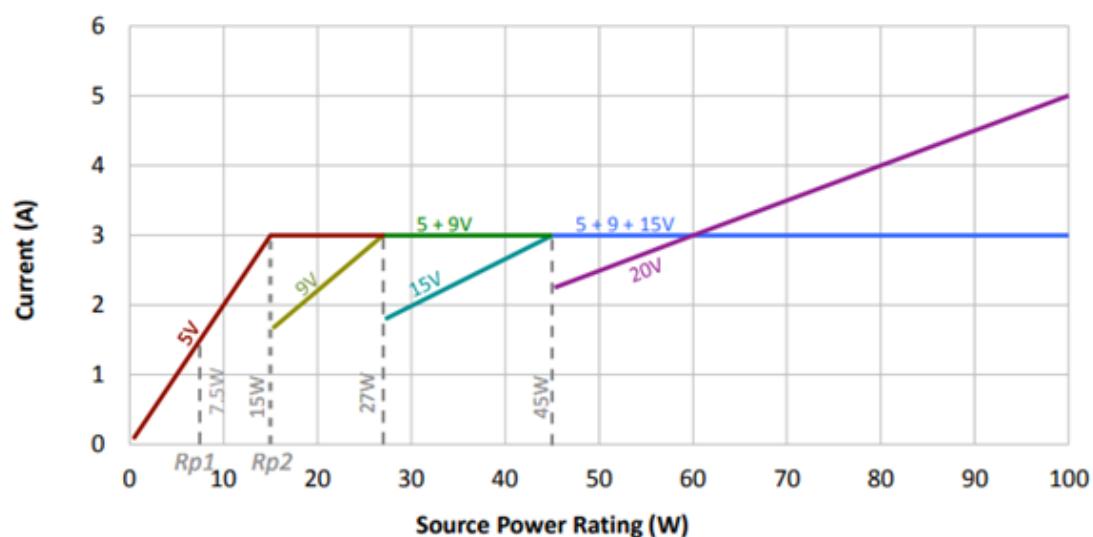
- Supplies up to 15 W.
- Achieves various current and voltage levels by adjusting the downstream-facing port (DFP) resistor.
- Sink devices pull down CC pins via $5.1\text{ k}\Omega$ resistors.

TABLE 6: VALID DFP RP PULL-UP RESISTOR VALUES

DFP Current Capability	Resistor Pull-up to 4.75V - 5.5V	Resistor Pull-up to 3.3V \pm 5%	Current Source to 1.7V - 5.5V
Default USB Power (500mA for USB2.0, 900mA for USB3.0)	$56\text{ k}\Omega \pm 20\%$	$36\text{ k}\Omega \pm 20$	$80\text{ }\mu\text{A} \pm 20\%$
1.5A @ 5V	$22\text{ k}\Omega \pm 5\%$	$12\text{ k}\Omega \pm 5\%$	$180\text{ }\mu\text{A} \pm 8\%$
3.0A @ 5V	$10\text{ k}\Omega \pm 5\%$	$4.7\text{ k}\Omega \pm 5\%$	$330\text{ }\mu\text{A} \pm 8\%$

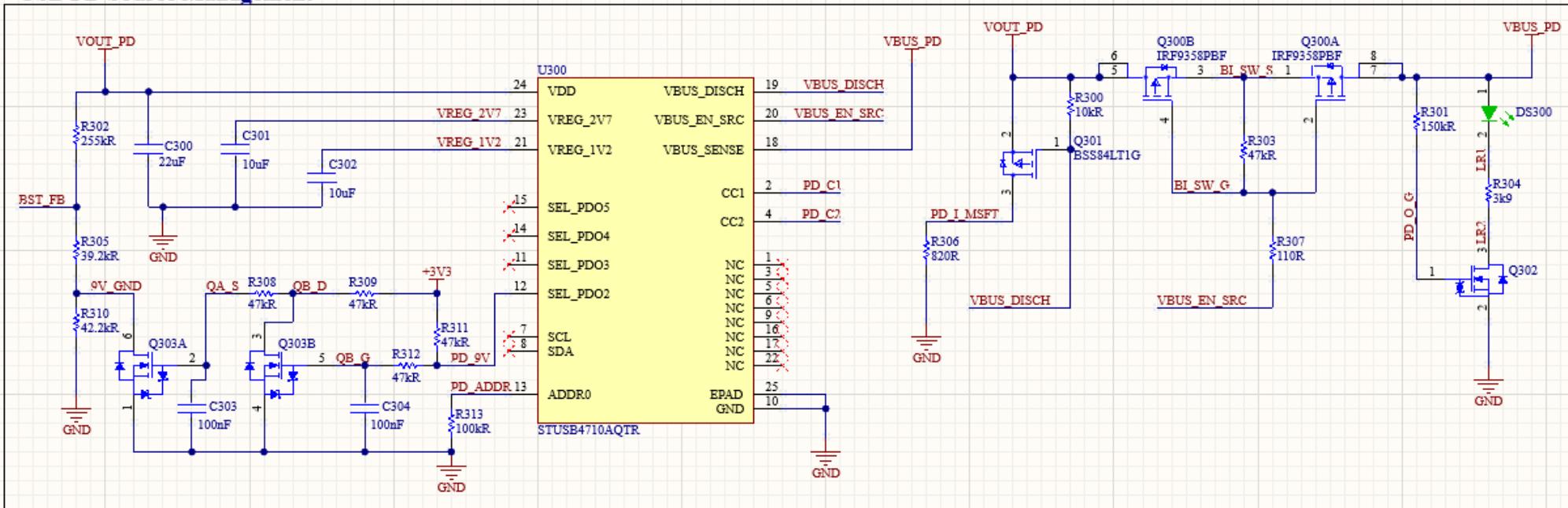
2. USB Type-C With PD:

- Enables power up to 240 W through negotiation.
- Uses PD controllers for voltage/current negotiation via CC pins.
- Allows flexible and efficient power delivery for high-power devices.



USB PD IMPLEMENTATION

USB PD Source Management



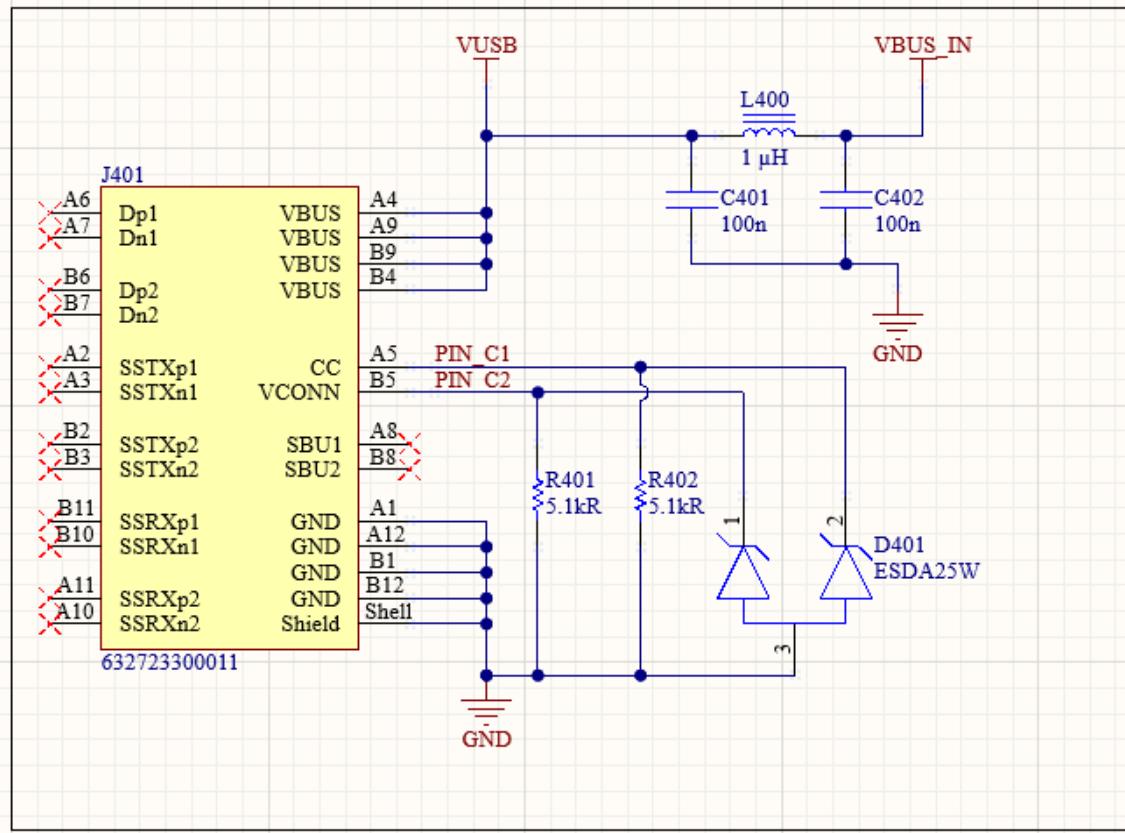
Notes:

13. To achieve higher power levels in USB Power Delivery, specialized ICs are required. In this case, the STUSB4710 source PD controller has been selected for its capabilities.
14. Different voltage and current levels are negotiated through the CC (Configuration Channel) pins of the USB Power Delivery system. Once the desired levels are established, power is delivered through a boost converter, which uses a feedback loop between the boost converter and the PD controller to maintain stability and ensure precise voltage regulation. This setup allows dynamic adjustment of voltage and current, meeting the needs of connected devices efficiently.
15. To enable dynamic power profile selection, a MOSFET-based switching mechanism is employed. When activated, the MOSFET pulls the SEL_PDxx line low, enabling the selection of different power levels. This configuration allows the microcontroller to adjust power settings dynamically based on the specific requirements of connected devices. Additionally, the design ensures protection and isolation, safeguarding the system from interference and maintaining stable operation.
16. Discharge circuitry is implemented to safely dissipate any residual charge stored in the circuit, ensuring stability and preventing voltage spikes. Additionally, back-to-back MOSFETs are utilized for power path control, providing robust isolation and precise switching. This configuration enhances safety by preventing reverse current flow and allows for efficient and stable power delivery within the system.

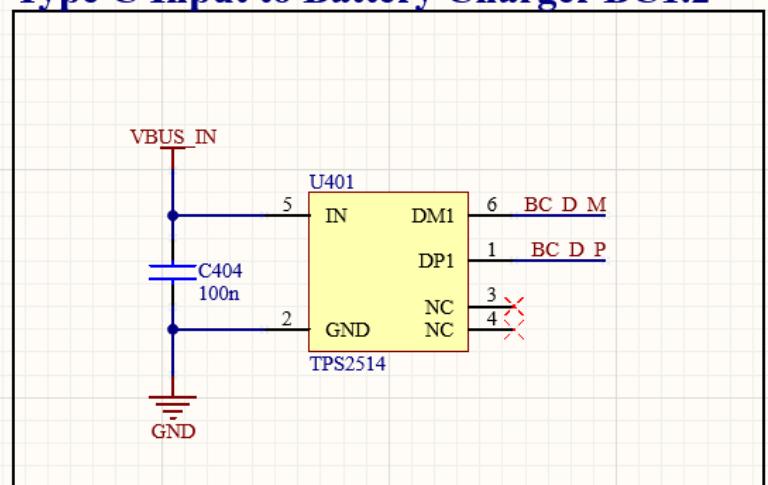
USB CONNECTORS

USB C INPUT

USB C - Input Connector



Type C Input to Battery Charger BC1.2

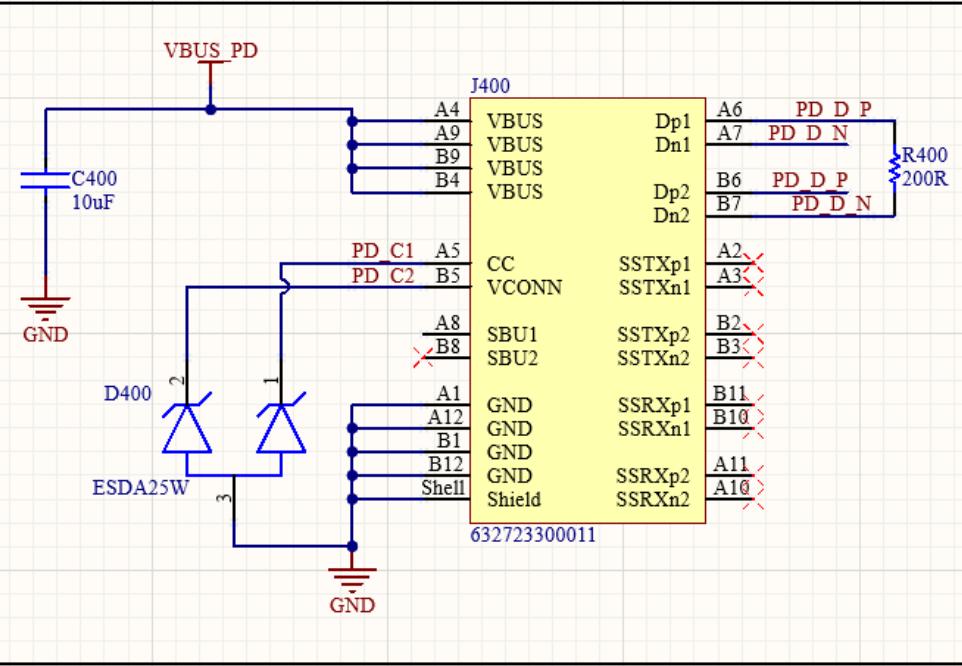


Notes:

17. The input power connector has been chosen as USB-C to support the global transition to this standardized format.
18. The CC lines are pulled low using 5.1K resistors in accordance with the standard, and ESD protection is implemented.
19. The input power is processed through a Pi filter network for effective filtering and noise reduction.
20. The BQ258985 detects the input power type through its data pins. To facilitate negotiation, the TPS2514 is employed.

USB OUTPUT

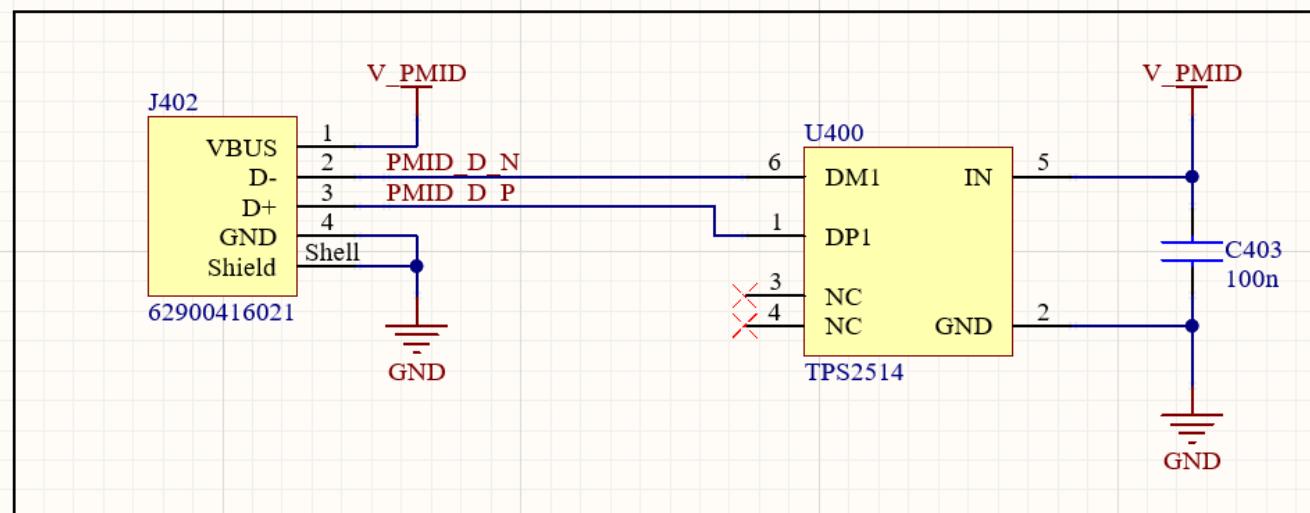
USB C PD - Out



Notes:

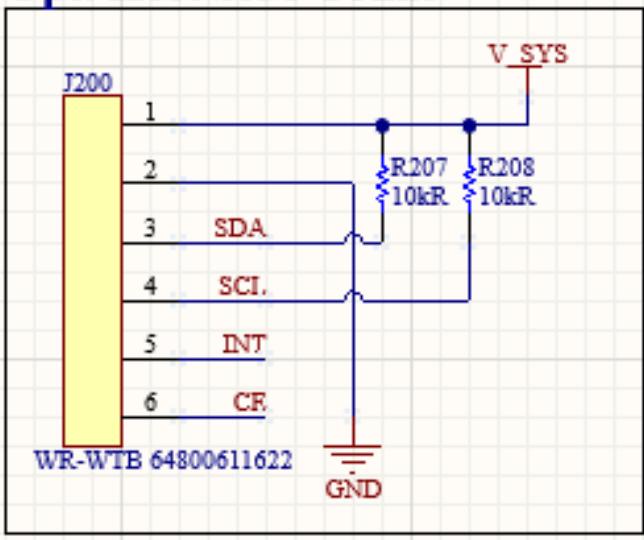
21. The USB-C PD output connector connections are established following the guidelines provided in the USB-C PD Controller documentation. ESD protection is implemented.
22. USB-A charging capability is provided to support legacy devices.
23. V_PMID provides a maximum output of 3A at 5V. The TPS2514 supports negotiation for multiple charging methods, including BC1.2 and proprietary charging protocols for specific brands.

USB A - Output



I2C INTERFACE AND IMPLEMENTATION

Opt. Host Side Conns



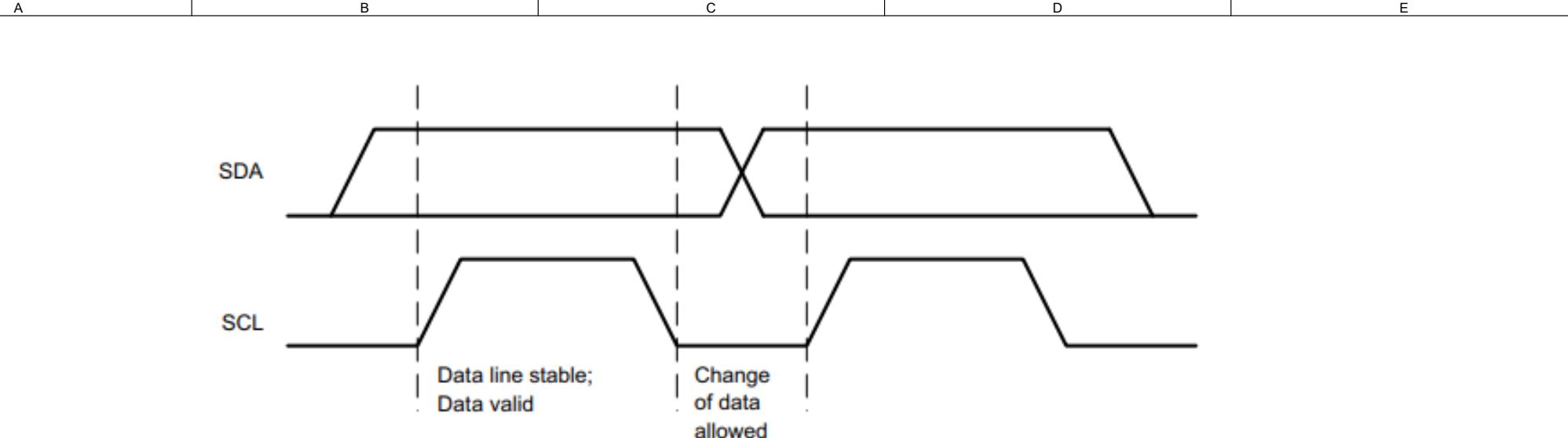
The device functions as a host-controlled charger but can operate in default mode independently of host management. The device is chosen to operate in default mode. However, an optional connector is included to enable host control when necessary.

Serial Interface

The device uses an I2C-compatible interface for flexible programming of charging parameters and real-time device status reporting. The I2C interface is a bi-directional, 2-wire serial protocol that consists of two open-drain lines: SDA (serial data) and SCL (serial clock). Devices on the bus can act as hosts, initiating data transfers and generating clock signals, or as targets, which respond to commands. The device operates as a target, with a fixed address of 6AH, and supports register communication from REG00 to REG14 for control inputs. Standard mode (up to 100 kbytes) and fast mode (up to 400 kbytes) are supported.

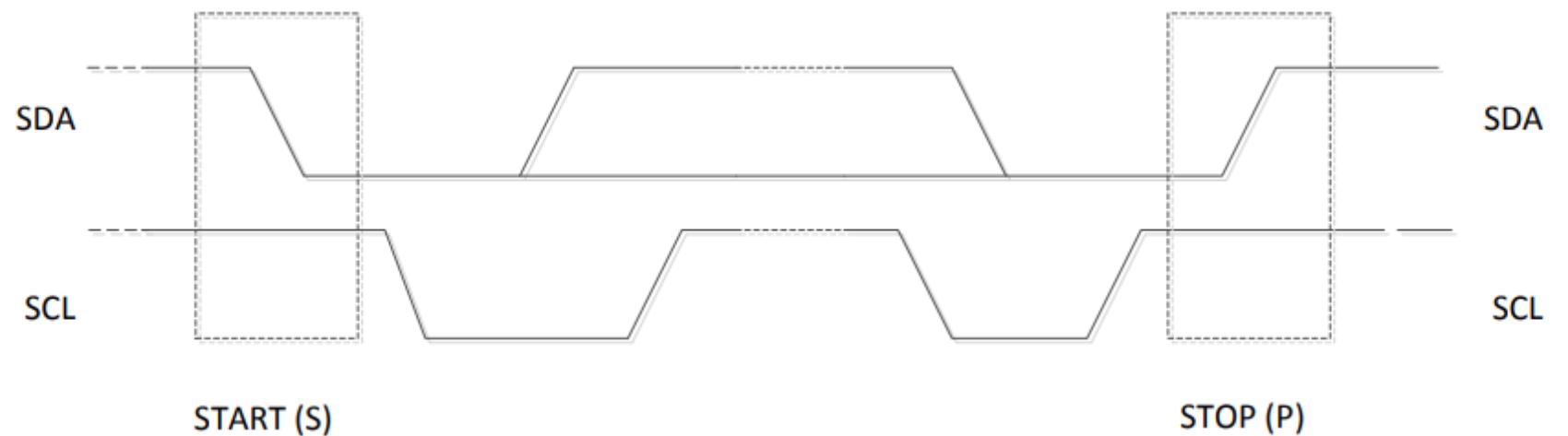
Data Validity

To ensure the integrity of data transfers, the SDA line must remain stable during the HIGH period of the SCL clock signal. Transitions in the data line state (HIGH or LOW) are permitted only when the clock signal on the SCL line is LOW. For every data bit transferred, one clock pulse is generated, which ensures synchronized communication.



START and STOP Conditions

Transactions begin with a **START (S)** condition, which involves a HIGH-to-LOW transition on the SDA line while the SCL line is HIGH. Similarly, a **STOP (P)** condition occurs with a LOW-to-HIGH transition on SDA while SCL is HIGH. The host generates these conditions, controlling when the bus is busy (after START) and when it becomes free (after STOP).



A

B

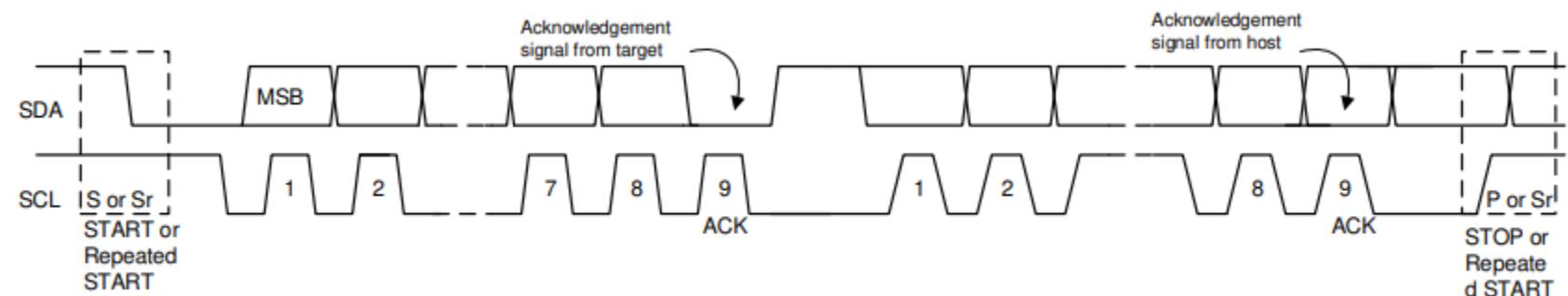
C

D

E

Byte Format

Data bytes on the SDA line are 8 bits long and transmitted MSB (Most Significant Bit) first. Each byte must be followed by an Acknowledge (ACK) bit from the receiver. During communication, the target can perform clock stretching by holding the SCL line LOW, which forces the host into a wait state until the target is ready to proceed.

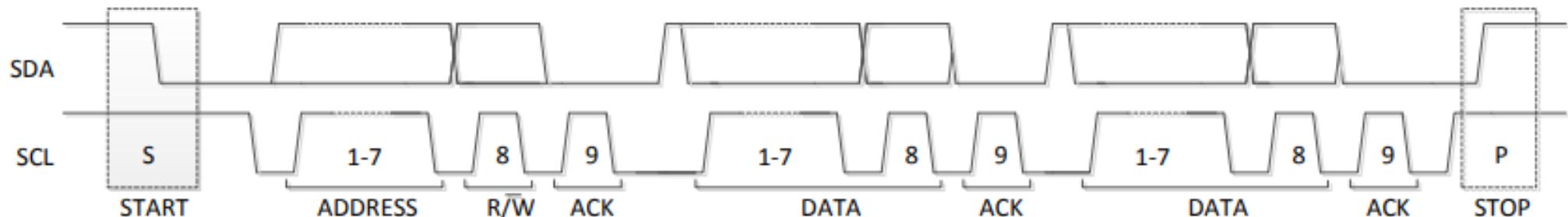


Acknowledge (ACK) and Not Acknowledge (NACK)

After every byte, the receiver sends an ACK signal by pulling the SDA line LOW during the ninth clock pulse. If the receiver cannot process the data or if the register is undefined, it sends a NACK signal by keeping the SDA line HIGH. The host can then issue a STOP to abort the transfer or a repeated START to retry communication.

Target Address and Data Direction Bit

The communication starts with the host sending a 7-bit target address followed by an eighth bit, which specifies the data direction (READ or WRITE). A "0" indicates a WRITE operation, while a "1" indicates a READ request.



A B C D E

Single Read and Write

Single Write: The host sends the target address, a register address, and the data to be written, followed by an ACK from the target.

Single Read: The host sends the target and register address, followed by a repeated START and the target address with a READ request. Data is sent back by the target, ending with a NACK.

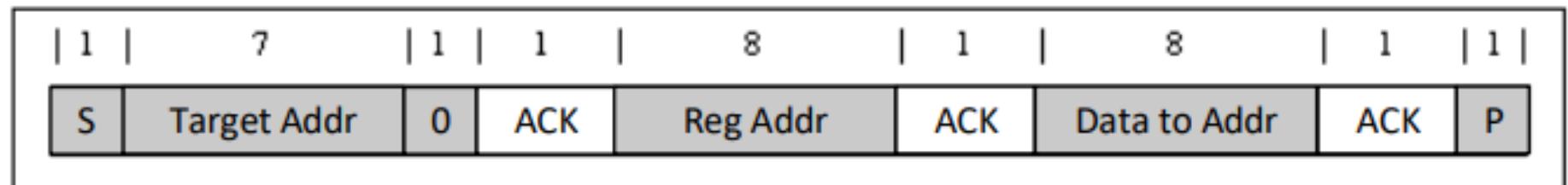


Figure 8-13. Single Write

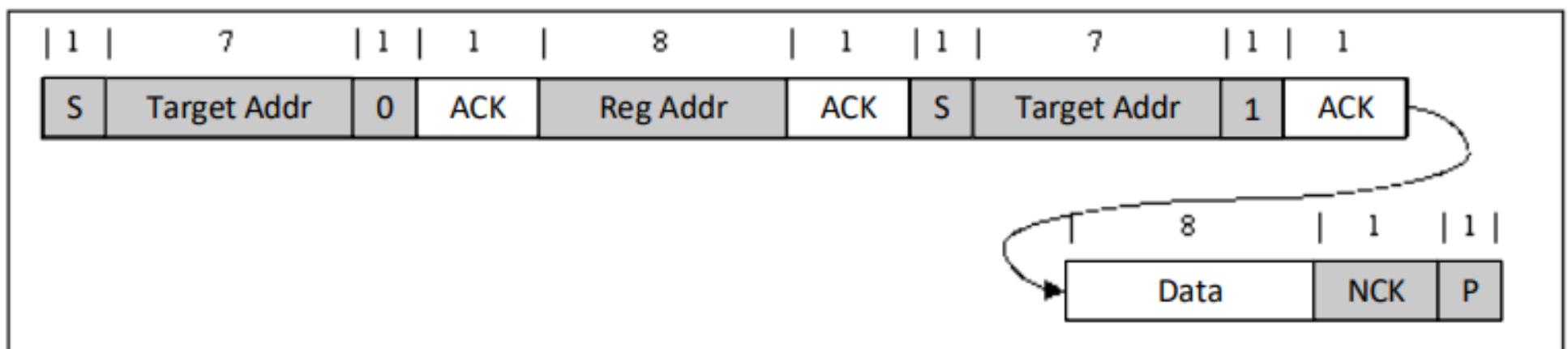


Figure 8-14. Single Read

A B C D E

Multi-Read and Multi-Write

Multi-Write: Multiple bytes can be written to consecutive registers starting from the specified register address.

Multi-Read: Similarly, consecutive registers can be read starting from the specified register address, except for REG0C, which stores fault information and behaves differently.

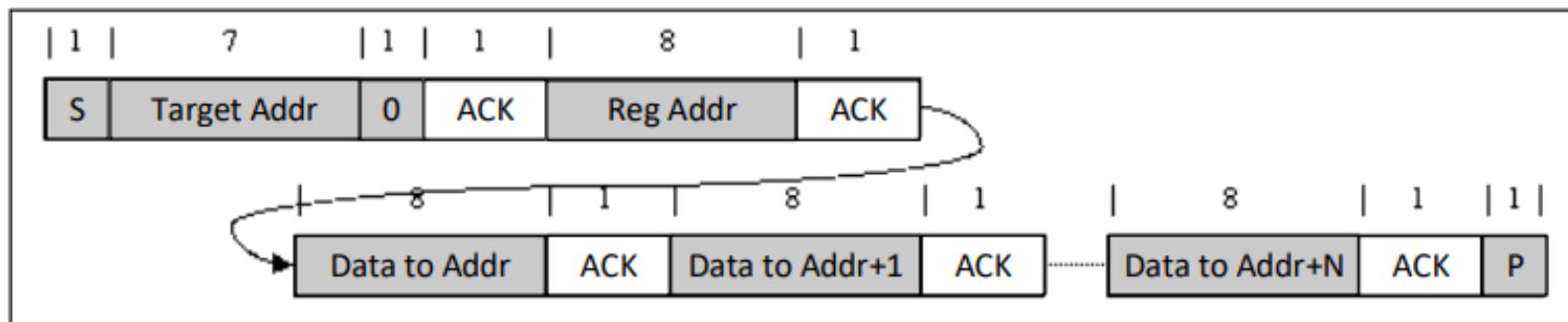


Figure 8-15. Multi-Write

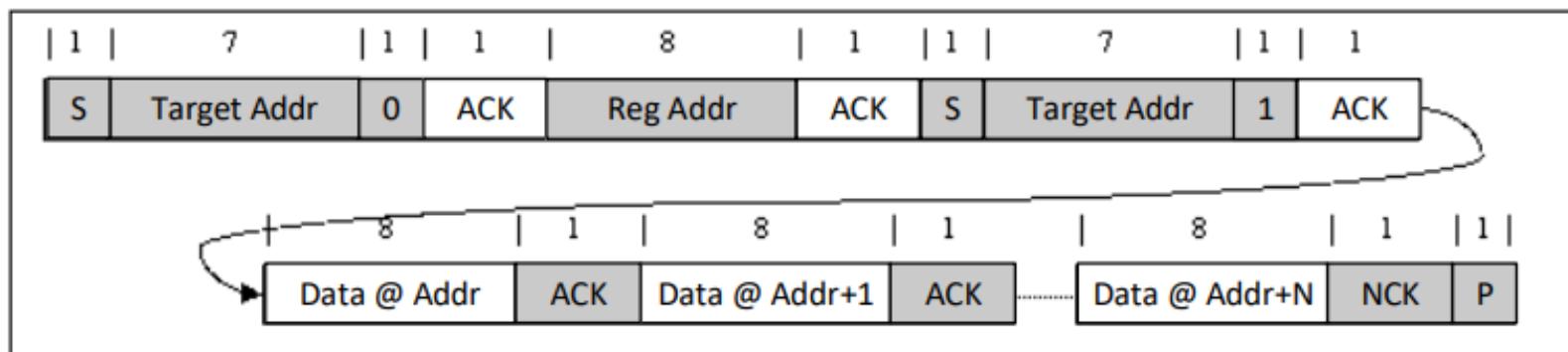


Figure 8-16. Multi-Read

Fault Registers

REG0C stores fault information, retaining the last fault condition until it is read. Fault data resets on the second read unless it represents the actual condition (e.g., NTC_FAULT). REG0C does not support multi-read or multi-write operations.

I2C Bus Pullup Resistor Calculation

The value of the pullup resistor is critical in I2C systems because an incorrect value can lead to signal loss or improper operation. A small resistor (strong pullup) may prevent the IC's I2C pin from pulling the line low, while a large resistor (weak pullup) may cause the line not to rise to a logical high in time.

$$\frac{V_{CC} - 0.4 \text{ V}}{0.003 \text{ A}} < R_P < \frac{t_{rise}}{0.8473 C_b}$$

I2C pull-up resistor value maximum and minimum values:

Note that the number in the denominator above is defined for a 30% to 70% transition time. For a 10%-90% transition time, replace 0.8473 with 2.2. This will further limit the value of the pull-up resistors.

Parameter		Standard Mode (Max)	Fast Mode (Max)	Fast Mode Plus (Max)	Unit
t_r	Rise time of both SDA and SCL signals	1000	300	120	ns
C_b	Capacitive load for each bus line	400	400	550	pF
V_{OL}	Low-level output voltage (at 3 mA current sink, $V_{CC} > 2 \text{ V}$)	0.4	0.4	0.4	V
	Low-level output voltage (at 2 mA current sink, $V_{CC} \leq 2 \text{ V}$)	-	$0.2 \times V_{CC}$	$0.2 \times V_{CC}$	V

Notes:

24. I2C operation guidelines are sourced from the BQ25895 datasheet. For a deeper understanding of I2C functionality, the document Understanding the I2C Bus by Texas Instruments can be reviewed.
25. For pull-up resistor calculations, the document I2C Bus Pullup Resistor Calculation by Texas Instruments can be referenced. The tables and information are sourced from this document.
26. A smaller pullup resistor increases the speed of the I2C bus by shortening the rise time of signals, allowing faster data transfer. However, this comes at the cost of higher power consumption due to increased current draw. On the other hand, a larger resistor minimizes power usage by reducing current, but it results in slower rise times, potentially limiting the communication speed. Designers must strike a balance, selecting a resistor value that meets the system's power and performance requirements effectively.

4-LAYER BOARDS

Introduction to 4-Layer Boards

4-layer PCBs are composed of four copper layers: the top, bottom, and two internal layers (typically power and ground planes). These boards offer enhanced signal integrity, power distribution, and electromagnetic interference (EMI) control, making them suitable for high-performance applications.

Fundamentals and Advantages

- Signal Integrity: Improved return paths and reduced impedance variations.
- Power Distribution: Dedicated power and ground planes stabilize power delivery and reduce noise.
- Compact Design: Supports higher routing density for complex layouts.
- EMI Reduction: Solid ground planes act as shields to minimize emissions.

Differences Between 2-Layer and 4-Layer PCBs

- 2-Layer PCBs: Limited to top and bottom copper layers, shared by signals, power, and ground, leading to constraints.
- 4-Layer PCBs: Add internal layers for dedicated power and ground planes, offering: Better signal integrity, Improved power delivery, Reduced crosstalk and electromagnetic interference.

Layer Stack-Up Configurations

- Optimized Layout: Power and ground planes should be adjacent for plane capacitance and noise filtering.
- Symmetry: Balanced stack-ups reduce warping and ensure signal consistency.
- Copper Distribution: Maintain even copper across layers to avoid manufacturing defects.

Material and Dielectric Considerations

Material Selection:

- FR-4 for standard designs.
- Rogers or Isola for high-speed circuits with low dielectric constant (D_k) and loss tangent (D_f).

Dielectric Properties:

- D_k affects signal propagation and impedance.
- D_f impacts signal loss; lower values are preferable for high-frequency circuits.

A B C D E

Signal Integrity and High-Speed Design

- Return Current Paths: Ensure continuous ground reference to minimize EMI.
- Impedance Control: Match characteristic impedance to prevent reflections.
- Crosstalk Reduction:
 - Increase spacing between traces.
 - Use ground planes and guard traces for isolation.

Power Integrity and Decoupling

- Power and Ground Planes: Provide low-impedance paths and noise suppression.
- Decoupling Capacitors:
 - Place near IC power pins for localized charge delivery.
 - Use a range of values to address noise across frequencies.
- PDN Design: Optimize capacitor placement and minimize voltage drops.

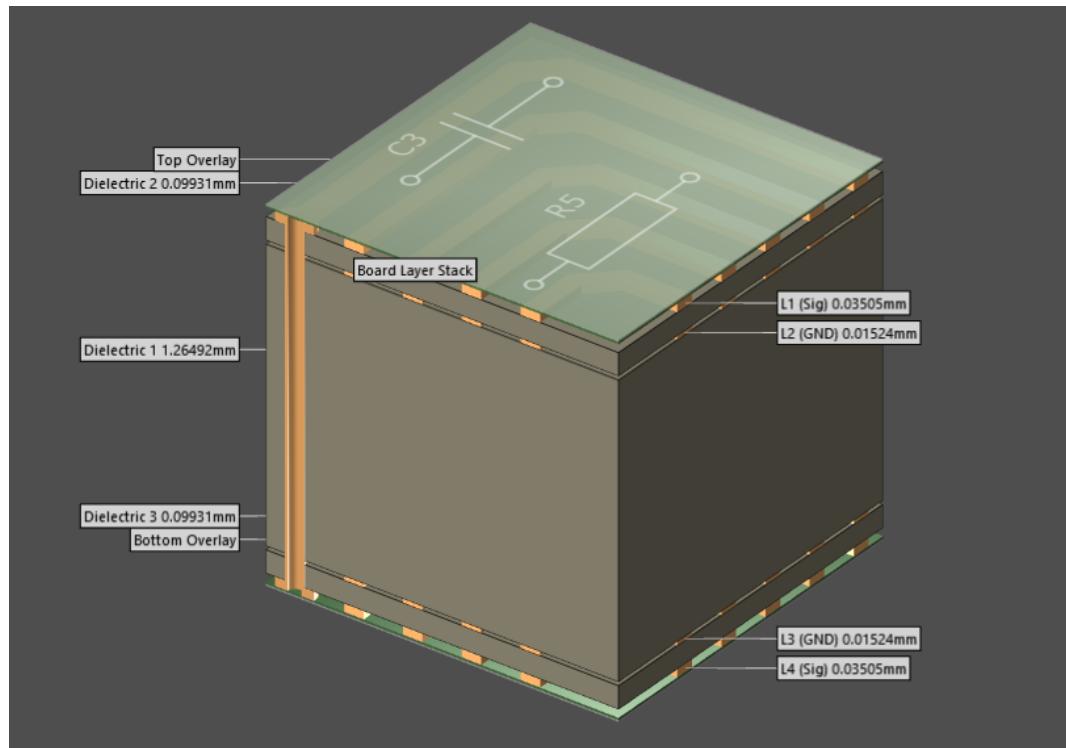
Thermal Management

Sources of Heat:

- Active components like ICs and regulators.
- Resistive losses in high-current traces.

Strategies:

- Thicker copper layers (e.g., 2oz) to distribute heat. (not always recommended as it adds to the cost instead wider tracks or planes could be utilized.)
- Thermal vias and heat sinks for efficient dissipation.
- Proper airflow and component spacing.



VIAS

Introduction to Vias

Vias are conductive pathways that connect different layers of a PCB, enabling electrical and thermal interconnection across the board. Each via consists of:

- A drilled hole (mechanically or laser-drilled).
- Copper plating inside the hole for electrical conductivity.
- Annular rings on connecting layers for reliable connections to traces.

Importance of Vias

Vias are integral to PCB functionality due to their role in:

- Layer Interconnection: Allowing routing across layers, enabling compact designs.
- Signal Integrity: Minimizing impedance mismatches, reflections, and degradation.
- Thermal Management: Dissipating heat from components and spreading it across layers.
- High-Density Interconnect (HDI): Essential for modern electronics like smartphones and high-frequency devices.

Types of Vias

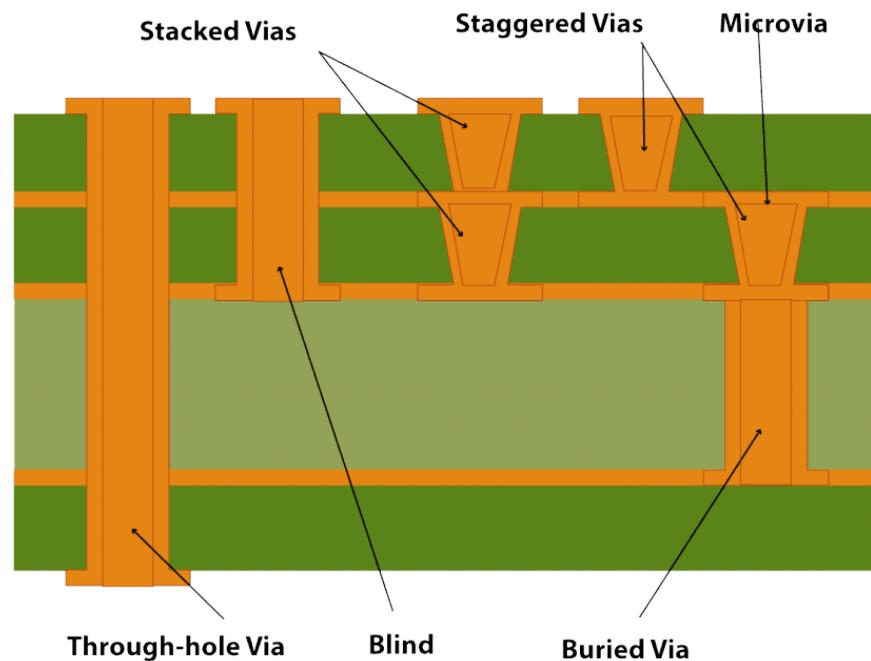
-Through-Hole Vias: Pass through all PCB layers; cost-effective but take up space.

-Blind Vias: Connect outer to internal layers without crossing the entire board; ideal for compact designs.

-Buried Vias: Connect internal layers only; save outer layer space but are costly.

-Microvias: Small laser-drilled vias for HDI designs; offer high-density routing but require specialized manufacturing.

-Via-in-Pad: Vias under component pads for BGAs; save space and improve performance but need careful soldering.



A Specialized Vias

- Stitching Vias:** Provide EMI shielding and ground continuity.
- Transfer Vias:** Transition signals between layers.
- Thermal Vias:** Dissipate heat from high-power components.
- Tented Vias:** Covered with solder mask for protection.

B Electrical Characteristics of Vias

Vias introduce parasitic inductance, capacitance, and resistance, influencing high-frequency signal performance:

- Inductance:** Impacts return path continuity and high-speed signal integrity.
- Capacitance:** Can distort signals through low-pass filtering effects.
- Resistance:** Affects power distribution and heat dissipation.

C Signal Integrity Issues with Vias

1. Via Stubs :An unused portion of a via that acts as a resonant structure at high frequencies.

Effects:

- Causes signal reflections and losses.
- Can generate standing waves, introducing noise.
- Becomes critical for frequencies above 1 GHz.

Solutions:

- Back-drilling: Removes the unused via stub to minimize reflections.
- Laser-Drilled Microvias: Avoid stubs entirely in HDI PCB designs.

2. Return Path Disruptions

Challenges:

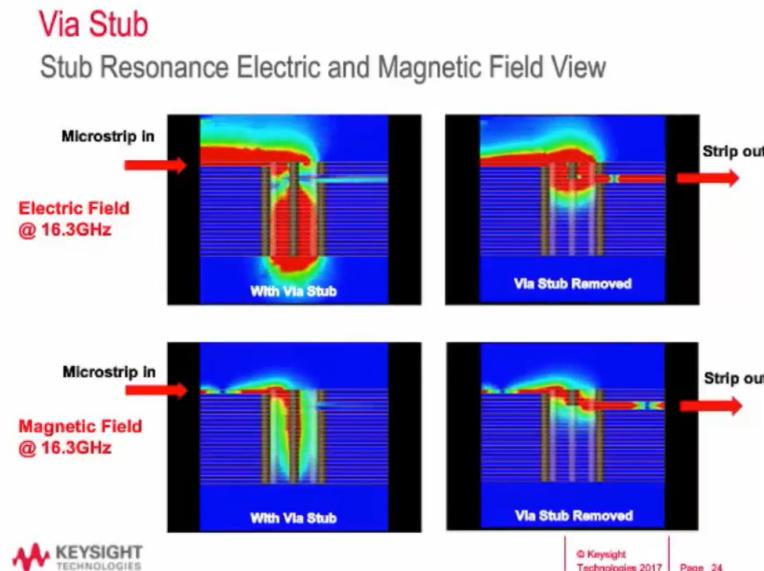
- Vias without nearby ground vias disrupt return paths.
- Such disruptions increase electromagnetic interference (EMI).

Solutions:

- Place ground vias close to signal vias to maintain return path integrity.
- Use stitching capacitors to reduce EMI for high-speed signals.

D Thermal Considerations

1. **Via Diameter:** Larger vias improve heat conduction but may introduce structural challenges.
2. **Copper Plating:** Thicker plating enhances conductivity and heat transfer.
3. **Number of Vias:** Multiple vias distributed across the PCB improve heat dissipation.
4. **Connection to Copper Planes:** Direct links to ground or power planes enhance cooling.



A Aspect Ratio Considerations

The aspect ratio of a via is the ratio of the PCB thickness to the via diameter:

- Lower aspect ratios (e.g., 5:1) are easier to plate and manufacture reliably.
- Higher aspect ratios (above 10:1) increase manufacturing complexity and risk of plating defects.
- Microvias typically have aspect ratios of 1:1 or 2:1 due to their small size.

$$\text{Aspect Ratio} = \frac{\text{PCB Thickness}}{\text{Via Hole Diameter}}$$

B Via Sizing and Annular Ring Diameters

The annular ring surrounds the via hole, ensuring reliable layer connections. Drill sizes are usually measured in mils, with mechanical drilling supporting holes as small as 8 mils. Smaller sizes require laser drilling, which is costlier. Rings must meet IPC-6012 standards for reliability:

- Class 1: Throwaway products that are not intended for long-term usage. These products do not have annular ring requirements for vias.
- Class 2: These electronic products are intended for long-term use and must be reliable. IPC Class 2 requires an annular ring be at least 4 mils thick. In other words, via's pad diameter must be at least the drill diameter + 8 mils.
- Class 3: These products are deployed anywhere human lives would be put in danger should the product fail. IPC Class 3 requires an annular ring be at least 5 mils thick. In other words, via's pad diameter must be at least the drill diameter + 10 mils.

IPC Class	Hole Diameter	Annular Ring	Pad Diameter
Class 2	8 mils (0.2032 mm)	4 mils (0.1016 mm)	16 mils (0.4064 mm)
Class 2	10 mils (0.254 mm)	4 mils (0.1016 mm)	18 mils (0.4572 mm)
Class 2	12 mils (0.305 mm)	4 mils (0.1016 mm)	20 mils (0.508 mm)
Class 3	8 mils (0.2032 mm)	5 mils (0.127 mm)	18 mils (0.4572 mm)
Class 3	10 mils (0.254 mm)	5 mils (0.127 mm)	20 mils (0.508 mm)
Class 3	12 mils (0.305 mm)	5 mils (0.127 mm)	22 mils (0.559 mm)

C Notes:

27. "Via sizing and annular ring diameters" is adapted from Altium Education Resources by Zach Peterson.
28. The current capacity of a via can be calculated using the IPC-2221 standard. Tools like SaturnPCB or similar platforms can assist with these calculations. Typically, a single via can handle approximately 1.5A. For high-current pathways, multiple vias are often used in parallel to distribute the load effectively.
29. This chapter draws from expert resources, including Altium, Zach Peterson, Phil's Lab, Eric Bogatin, Robert Feranec, and Keysight Industries, providing a comprehensive foundation for the insights shared.

TRACES

Introduction to Traces

PCB traces are conductive paths made of copper on a PCB that connect electrical components like resistors, capacitors, ICs, and power sources. They replace traditional wires, acting as the board's electrical "wiring."

Trace Configurations

Microstrip: Trace on the PCB's top layer with a ground plane below.

- Simple, easy to inspect, suitable for RF circuits.

Stripline: Trace embedded between two ground planes.

- Superior shielding, lower EMI, better signal integrity.

Trace Width, Thickness & Spacing

The width of a PCB trace determines:

- Current carrying capacity (wider traces carry more current).
- Resistance (narrower traces have higher resistance, leading to voltage drop).
- Manufacturing limitations (some PCB manufacturers have minimum trace width requirements).

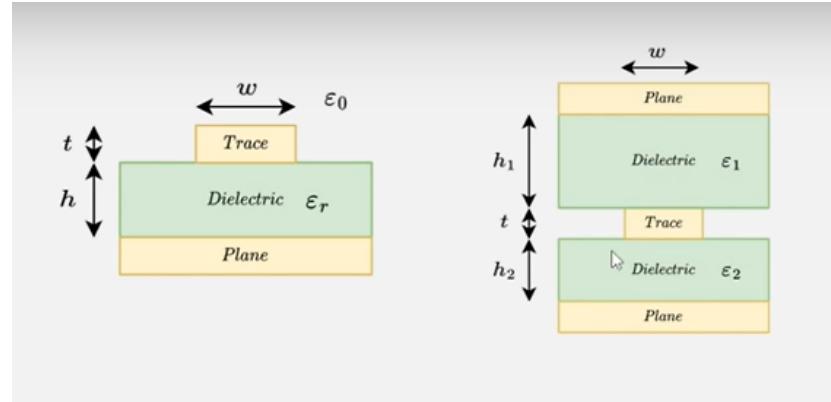
Defined by copper weight, trace thickness affects the trace's cross-sectional area and overall current-carrying capacity

Spacing between traces ensures electrical isolation and reduces the risk of crosstalk and interference: Use the 3W rule->Spacing = 3x the trace width to reduce crosstalk, Maintain clearances defined by the PCB manufacturer to ensure manufacturability.

Electrical Properties

PCB traces are not just simple wires; they have electrical properties that impact circuit performance. The most important characteristics are:

- Resistance (R) – Affects voltage drop and power loss. Wider traces reduce resistance.
- Inductance (L) – Causes signal delay and affects high-speed performance. Use shorter and wider traces with a ground plane beneath them.
- Capacitance (C) – Can create unwanted signal coupling. Increase spacing between critical traces.
- Impedance (Z) – Critical for high-speed designs; must maintain controlled impedance values (e.g., 50Ω for single-ended traces).



A B C D E

High-Speed Trace Design

In modern electronics, many circuits operate at high frequencies (e.g., USB, HDMI, DDR, RF circuits). At these speeds, PCB traces act like transmission lines, meaning that improper design can cause signal reflections, distortion, and interference.

PCB Traces as Transmission Lines

At low frequencies, PCB traces behave like simple wires. However, at high frequencies (>100 MHz), they act as transmission lines, meaning their impedance must be controlled.

Rule of thumb: A PCB trace behaves as a transmission line when its length is greater than 1/10th of the signal wavelength (λ).

Signal Integrity Issues

1. **Signal Reflections:** Caused by impedance mismatches.
 - Causes ringing, overshoot, undershoot in signals.
 - Solution: Use controlled impedance traces.
2. **Crosstalk:** Occurs when traces are too close.
 - Solution: Follow the 3W rule (spacing = $3 \times$ trace width).
3. **Ground Bounce:** Due to shared return paths.
 - Solution: Use a solid ground plane under high-speed traces.

Grounding & Return Paths

Ensures signal integrity in high-speed designs. High-speed signals always follow the path of least inductance, not resistance. Without a proper ground plane, signals take uncontrolled paths, leading to EMI issues.

Best Practices for Grounding

- Use continuous ground planes under high-speed traces.
- Avoid splitting ground planes under signal traces.
- Minimize via transitions to maintain return path continuity.

Thermal Considerations for PCB Traces

PCB traces carrying high currents generate heat due to resistive losses ($P = I^2R$), which can cause voltage drops, material degradation, or failure if unmanaged. Wider traces, thicker copper (e.g., 2 oz/ ft^2), and thermal vias improve heat dissipation. Tools like ANSYS Icepak and Altium Designer optimize trace layout and thermal performance, ensuring reliability in high-power applications.

A

Notes:

- B
- C
- D
- E
30. The current-carrying capability, controlled impedance, and inductance of a PCB trace can be calculated using online tools like SaturnPCB or other reliable resources. As a general guideline, a 10 mil wide trace made from 1 oz copper can handle approximately 1 amp of current under standard conditions.

THERMAL MANAGEMENT

Introduction to Thermal Management

Thermal management refers to techniques and strategies used to dissipate heat generated by electronic components. Effective thermal management ensures reliability, longevity, and optimal performance of PCBs.

Why is Thermal Management Important?

1. Reduced Performance: High temperatures increase resistance and voltage drops.
2. Component Failures: Heat accelerates degradation (e.g., 10°C rise can halve component lifespan).
3. Solder Joint Cracking: Thermal stress weakens connections.
4. PCB Damage: High heat causes warping, delamination, and structural failure.

Heat Transfer Mechanisms

1. Conduction: Heat flows through materials (e.g., copper traces).
 - Copper: $\sim 400 \text{ W/m}\cdot\text{K}$ (highly conductive).
 - FR4: $\sim 0.3 \text{ W/m}\cdot\text{K}$ (poor conductor).
2. Convection: Heat transfers to air or liquid.
 - Enhanced with fans or heatsinks.
3. Radiation: Emission of heat energy.
 - Black surfaces improve heat dissipation.

Heat Sources in PCBs

1. Active Components: ICs, MOSFETs, and voltage regulators dissipate heat due to switching and conduction losses.
2. Passive Components: Resistors and inductors generate heat through power losses.
3. PCB Traces & Planes: Heat from resistance, Copper Losses
4. Environmental Factors: Trapped heat in enclosures or nearby external heat sources.

A B C D E

Thermal Properties of PCB Materials

- 1 1. Thermal Conductivity (k): measures how efficiently a material conducts heat.
 - High k materials conduct heat efficiently and help dissipate it faster.
 - Low k materials trap heat, leading to localized overheating.
- 2 2. Coefficient of Thermal Expansion (CTE): CTE measures how much a material expands when heated.
 - Mismatched CTE values between PCB materials and components (e.g., silicon dies, solder joints) can cause mechanical stress, leading to cracks and failures.
 - High CTE mismatch can cause delamination in multilayer PCBs.
- 3 3. Glass Transition Temperature (T_g): T_g is the temperature at which the PCB material transitions from a rigid to a soft state.
- 4 4. Thermal Resistance (R_{θ}): Thermal resistance represents a material's resistance to heat flow.
 - A lower R_{θ} means better heat dissipation

Key Thermal Design Techniques

- 1 1. Copper Thickness & Planes:
 - Use thicker copper (e.g., 2–4 oz/ft²) for better heat spreading.
 - Power and ground planes act as heat spreaders.
- 2 2. Thermal Vias:
 - Place under components; use filled vias for higher heat transfer.
- 3 3. Dielectric Material Selection:
 - High-k materials reduce thermal resistance.
- 4 4. Heat Sinks & Cooling:
 - Attach heatsinks to power components for effective dissipation.
- 5 5. Active Cooling:
 - Use fans, heat pipes, or liquid cooling for high-power systems.

Notes:

- 1 31. The IPC standards focus on thermal management in PCB design through guidelines like IPC-2221 for effective heat dissipation and IPC-2222 for optimizing multilayer stack-ups to reduce thermal resistance. These ensure reliable heat handling in electronic circuits.
- 2 32. The relevant sources for understanding this topic are Phil's Lab, Altium, and Zach Peterson.