Construction of Electronic Systems

Exercise 11: USB DAQ project: designing the rest of the PCB

Providing the ground polygon pours

Keeping the bottom GND pour unsegmented

By now you probably imagine the beneficial advantages of having a good, *unsegmented* ground polygon pour on the bottom side which can *provide low-impedance return paths for critical signals* and help *catch the electric field* of the problematic fast-changing voltage signals.

In order to help you keep the bottom GND pour as unsegmented as possible, look at the few ideas below.

If possible, try to *arrange the connections into groups that are "traveling" in the same direction* (Figure 1, green parts). When two such groups of signals will meet and crossings will occur, *the smaller group* of signals can change side to the bottom layer, travel under the larger group and then on the other side *return immediately back* to the top layer (orange parts). This will create only small islands on the bottom side where the GND pour will be missing, since the length of the crossings on the bottom side is short and since the signals crossing to the bottom side are joined together (Figure 2).

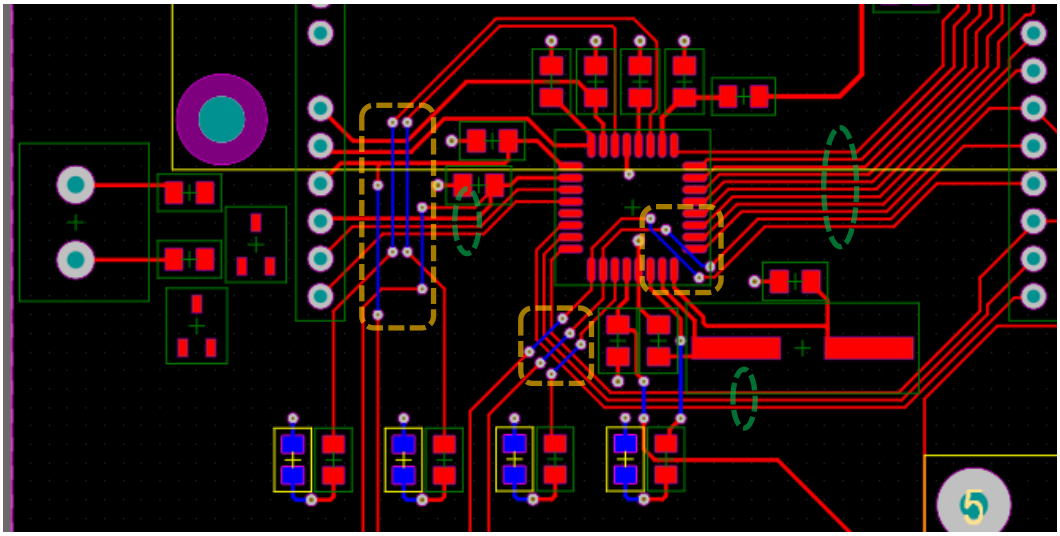


Figure 1 – if possible, join signals into groups that travel in the same general direction. When crossing such groups, change the bottom layer and then immediately return to the top layer.

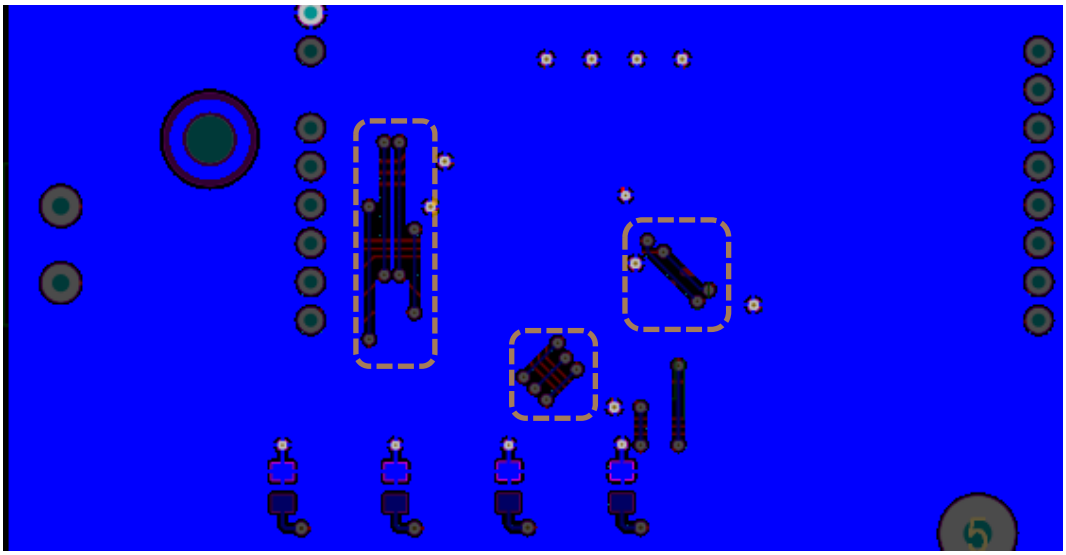


Figure 2 – the idea from the previous figure will result in only small islands where the GND pour will be missing

Also, try to minimize the length of the connections on the bottom side. ***Use the bottom side layer only to cross the obstacle and then immediately return to the top side***. See the idea below.

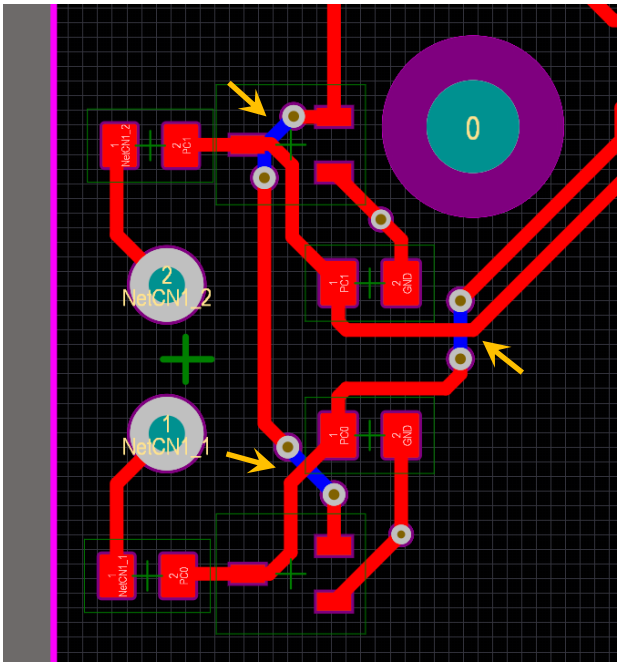


Figure 3 – where this is possible, use the bottom layer just to cross the obstacle and then immediately return to the top side

Using polygon "direct connect" to the GND vias

You can use direct connect between the GND polygon and the GND vias to decrease the inductance of the return current paths.

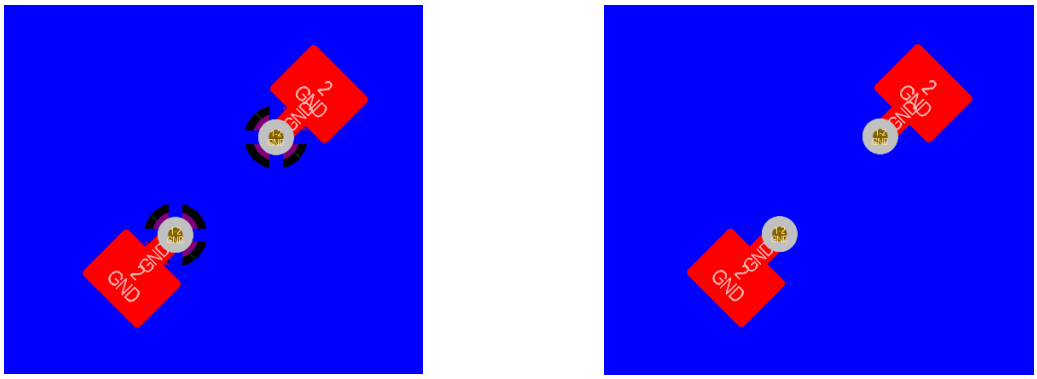


Figure 4 – using the direct connect to connect the GND polygon to the GND via (right figure) will reduce the inductance of the return GND current paths. Remove the thermal relief connection (left figure) using the "polygon connect" design rules.

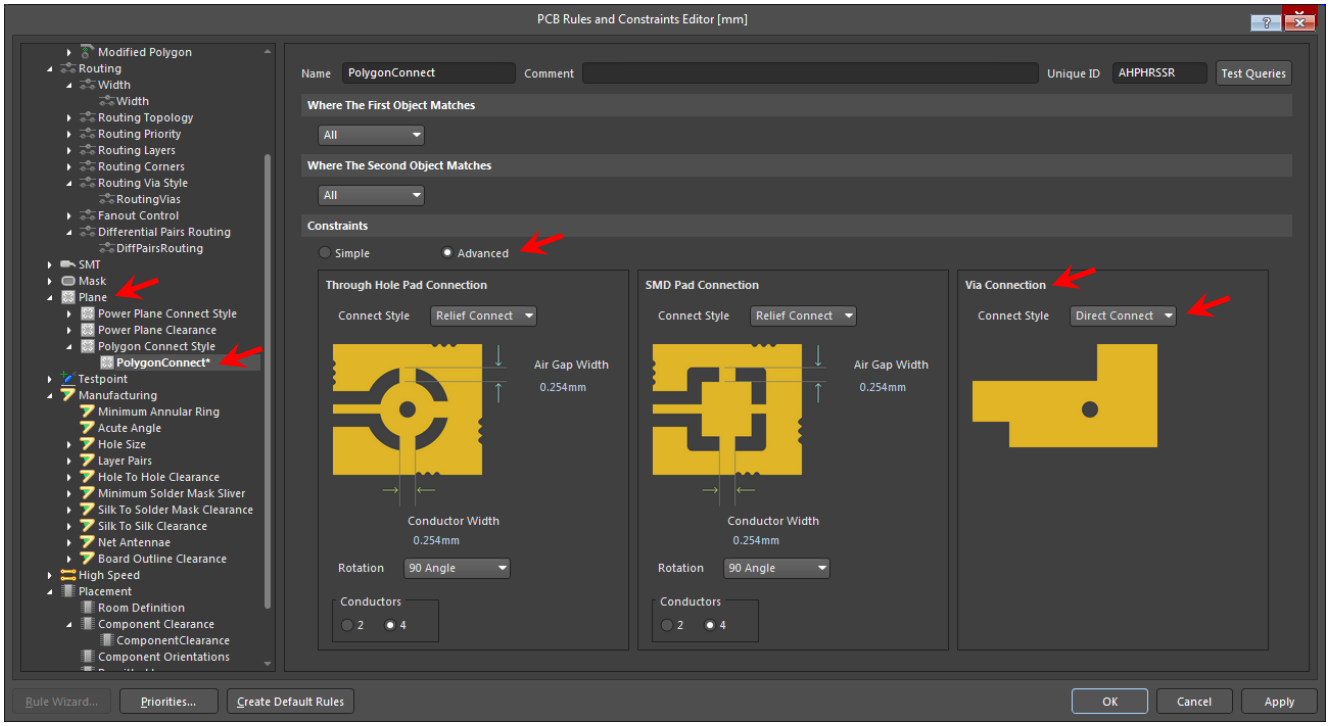


Figure 5 – setting the polygon connect styles. Use direct connect for vias only.

Checking for missing GND vias near the GND pads

When you have *only the bottom GND copper pour present* (and there is still no top side GND pour), the situation is good to check whether any component pads connected to the GND are missing the GND via. See the idea below. If the GND via is missing, you will notice that the airline appears there to the bottom GND pour. Of course, add a missing GND via to ensure short GND return paths. Hint: highlight the GND net by CTRL+[mouse click] on the GND net to make GND copper more visible.

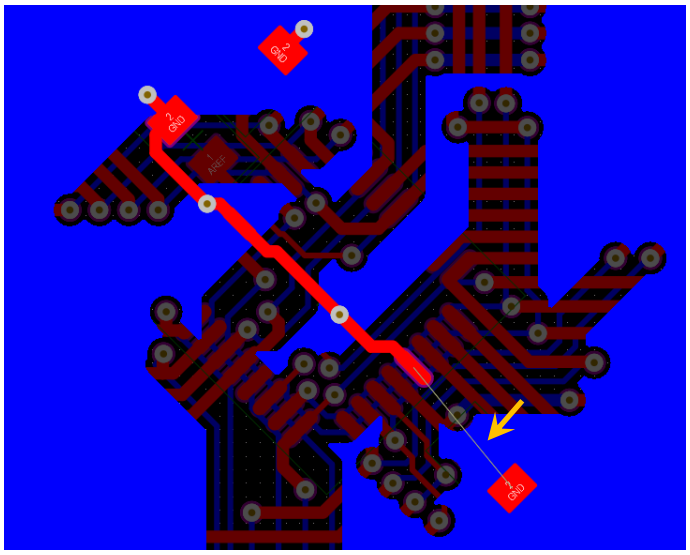


Figure 6 – if the GND pad from the top side is missing a GND via, you will notice this since the airline appears

Remove dead copper

If a part of the polygon is not connected to any other nodes of the circuit, this is called a dead copper or an island.

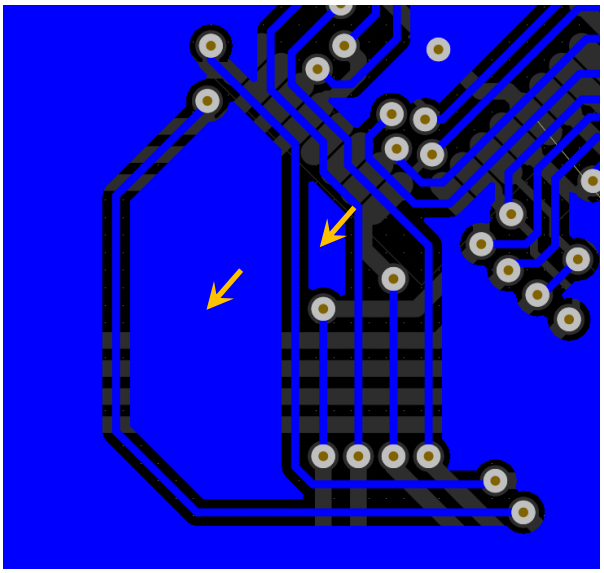


Figure 7 – remove the floating dead copper islands since they can become an antenna for noise

Such a floating island can become a problematic antenna for the electric field, so it is better to remove it. You can do this in the polygon properties (see below).

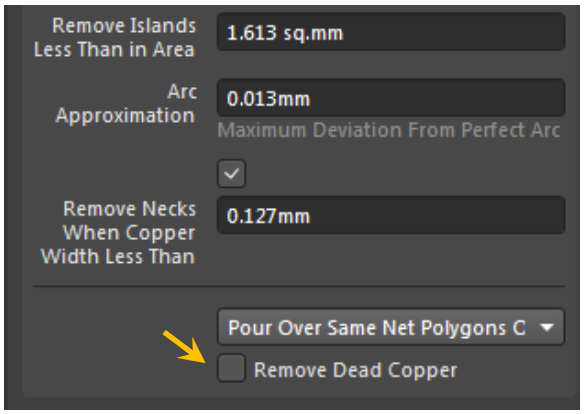


Figure 8 – polygon option that removes the dead copper

Pouring the GND polygon over all GND copper areas

In most cases it is useful to pour copper over all copper areas that are connected to the GND. If you do not do this, you might get a situation similar to that in the Figure 9, where a GND track is not being poured over.

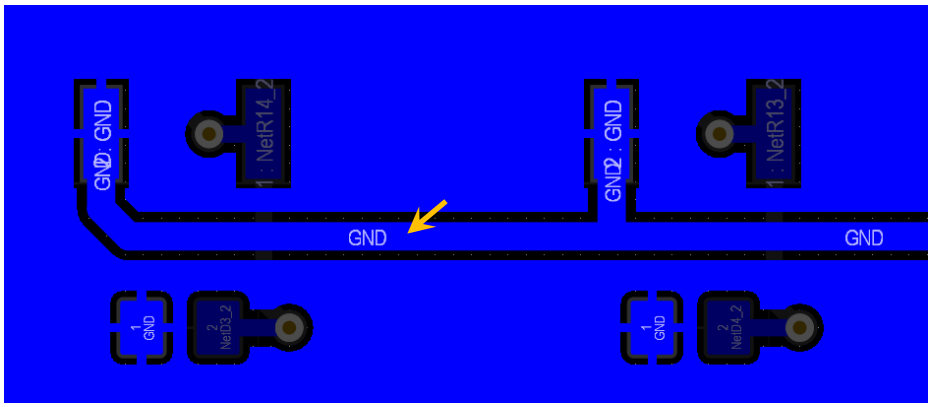


Figure 9 - the GND polygon did not pour over all GND copper areas

In order to avoid this situation, use the polygon option from the figure below.

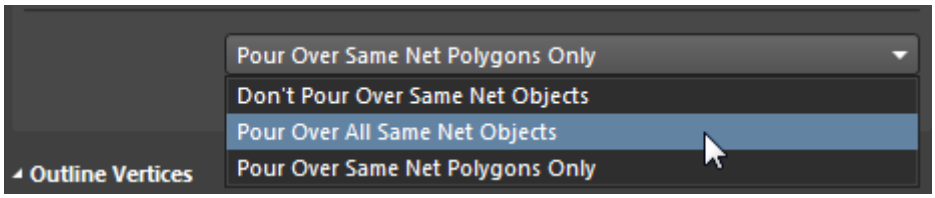


Figure 10 – using the option above will ensure that the polygon pours over all GND copper areas

Adding the GND pour on the top side

One of the fastest way to do this is to simply copy the GND pour from the bottom side, change to the top side layer and then use the "Edit -> Paste Special" tool. See the idea below.

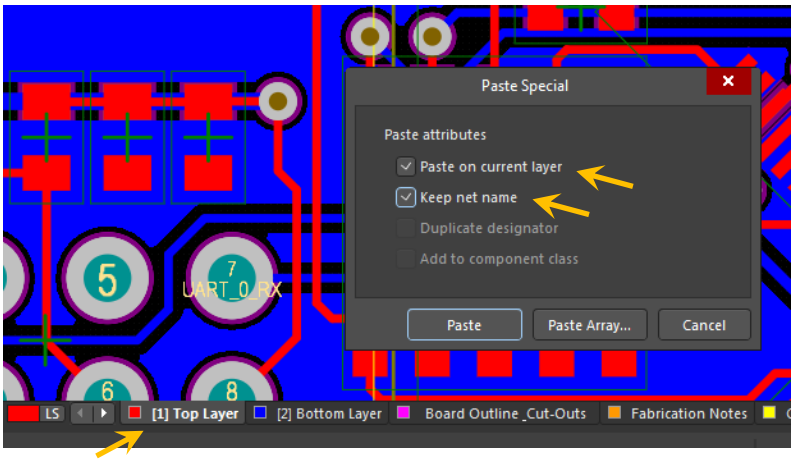
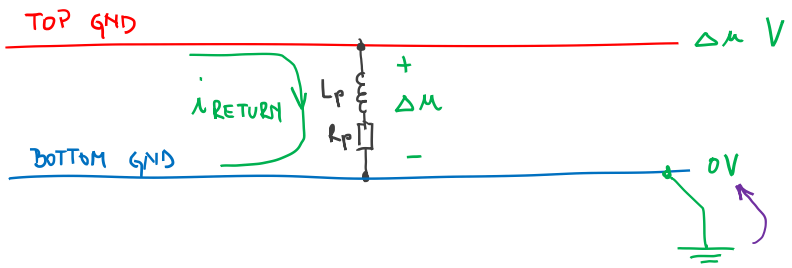


Figure 11 - use the Paste Special tool to copy the GND polygon to the current top layer and keep the net name as well

Ensuring the low-impedance connection between the top GND pour and the bottom GND pour

We must ensure that the top GND pour is connected to the bottom GND pour using the low-impedance connection. If this is not ensured, the potential of the top GND pour will deviate from the bottom GND pour potential, producing the voltage-driven common mode interferences. See the idea below.



In order to ensure the low-impedance connection between the top and bottom GND pours, we use sufficient number of GND vias. See the idea below.

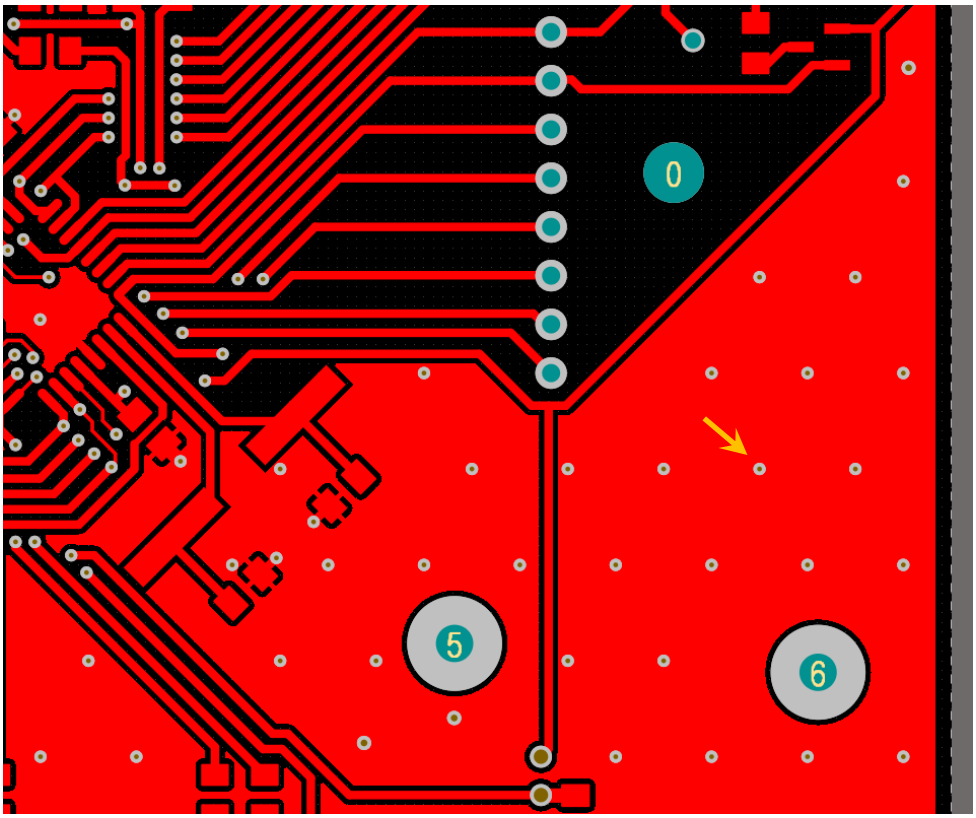


Figure 12 – the sufficient number of GND vias provide the required low-impedance connection between the top GND pour and the bottom GND pour

The rule of thumb: the distance between these GND vias should be less than

$$\lambda_{\min} = \frac{v_{\text{signal}}}{f_{\max}} \quad ; \quad v_{\text{signal}} \approx \frac{c}{\sqrt{\epsilon_r}}$$

where the v_{signal} is the signal velocity on the PCB and $\lambda_{\min}$ is the wavelength of the signal with the highest frequency $f_{\max}$ in the electrical circuit.

Also, by adding the GND vias where the dead copper islands where removed, you can restore the GND pour for this parts of the PCB as well. See the figure below and compare it to the figure above.

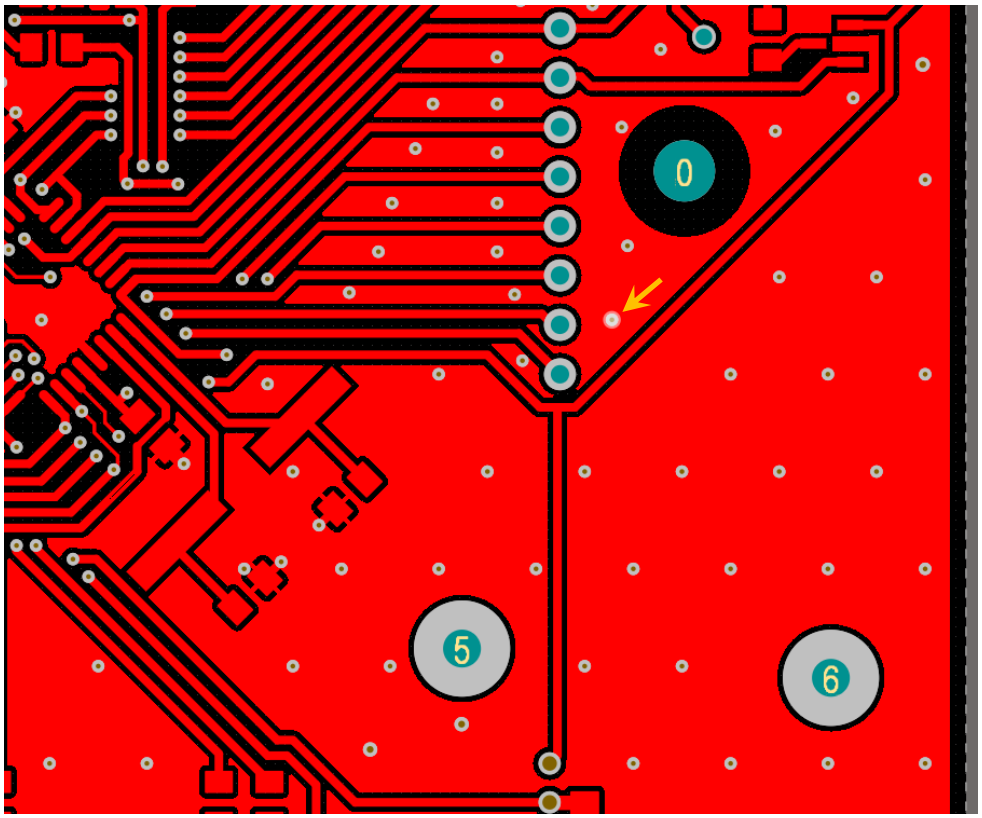


Figure 13 – adding GND vias can restore copper pour where previously only dead copper lied

Separating the GND and AGND copper pours

Your project is using an additional so-called *analog ground* AGND. Therefore, you should use separate copper pours for the analog section of your PCB, using polygons that are connected to the AGND. You will discuss more on this topic with the professor during the actual lab exercise.