2024 Digital IC Design

Homework 3: matrix multiplier

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| NAME | | 陳育政 | | | | | | |
| Student ID | | E24094198 | | | | | | |
| **Simulation Result** | | | | | | | | |
| Functional simulation | Score | | Gate-level simulation | Score | Clock  width | (ns) | Gate-level simulation time | simulation time (ns) |
|  | | | | |  | | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | |  | | | |
| Total memory bit | | | | |  | | | |
| Embedded multiplier 9-bit element | | | | |  | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
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*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (Total cycle used\*clock width)*