Lab Notebook

FPGA Capstone Project

## Academic Integrity

*By signing below you acknowledge the CU Honor Code, "On my honor, as a University of Colorado Boulder student I have neither given nor received unauthorized assistance" applies to this assignment.*

Signed: Uriel Abe Contardi

# Module 1

## Setup

Author: Uriel Abe Contardi

Date: 24/08/2024

Procedure/Description of Test: The module guide was followed and the code was recorded in the development kit.

**Results:**

**DE10\_LITE\_Small**

**Interface gráfica do usuário, Texto, Aplicativo, Email

Descrição gerada automaticamente**

**Interface gráfica do usuário, Texto, Aplicativo, Email

Descrição gerada automaticamente**

**DE10\_LITE\_Default**

Interface gráfica do usuário, Texto, Aplicativo, Email

Descrição gerada automaticamente

Interface gráfica do usuário, Texto, Aplicativo, Email

Descrição gerada automaticamente

**Questions**

1. Record your observations of the board behavior once the FPGA is programmed. Does it behave as you might expect?

Everything works as expected and as written in the guide. The project had timing problems that were ignored by the guide, I believe because it was not the scope of this first module

**Conclusions**

Lessons Learned (What did you learn?):

This first part served its purpose, getting me used to the development kit and the tools available.

## Part 1

Author: Uriel Abe Contardi

Date: 24/08/2024

Procedure/Description of Test: The module guide was followed and the code was recorded in the development kit.

**Results**

No Fmax. The design doesn't use a clock

Interface gráfica do usuário, Texto, Aplicativo, Email

Descrição gerada automaticamente

Interface gráfica do usuário, Texto, Aplicativo, Email

Descrição gerada automaticamente

Diagrama

Descrição gerada automaticamente

**Questions**

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?

Yes, the expected result was achieved. The keys were used to force a value in the 7 segments, if it exceeds the number 9 all the LEDs go out.

1. Explain the reason for the number of flip-flops used in the design.

The design has no registers because the logic implemented has no associated clock or latch

**Conclusions**

Lessons Learned (What did you learn?): It was possible to develop a 7-segment driver in vhdl

## Part 2

Author: Uriel Abe Contardi

Date: 24/08/2024

Procedure/Description of Test: The module guide was followed and the code was recorded in the development kit.

**Results**

No Fmax. The design doesn't use a clock

Interface gráfica do usuário, Texto, Aplicativo, Email

Descrição gerada automaticamente

Interface gráfica do usuário, Texto, Aplicativo

Descrição gerada automaticamente

Diagrama, Esquemático

Descrição gerada automaticamente

**Questions**

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?

Yes, the expected result was achieved. The keys were used to force a value in the 7 segments

1. Does this design use more or less logic than the design in Part 1? Why?

The logic consumption in the first case was higher, this can be explained because we have two 4-bit controllers for each 7-segment display, while in the second case it is as if I had a single 4-bit controller for both displays at once, this saves logic resources

**Conclusions**

Lessons Learned (What did you learn?): It was possible to implement a decimal controller for the 7-segment display

## Part 3

Author: Uriel Abe Contardi

Date: 24/08/2024

Procedure/Description of Test: The module guide was followed and the code was recorded in the development kit.

**Results**

No Fmax. The design doesn't use a clock

Interface gráfica do usuário, Texto, Aplicativo, Email

Descrição gerada automaticamente

**Diagrama

Descrição gerada automaticamente**

**Questions**

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?

Yes, it worked as expected, a simple 4-bit adder

**Conclusions**

Lessons Learned (What did you learn?): Implement a 4-bit adder

## Part 4

Author: Uriel Abe Contardi

Date: 24/08/2024

Procedure/Description of Test: The module guide was followed and the code was recorded in the development kit.

**Results**

Interface gráfica do usuário, Texto, Email

Descrição gerada automaticamente

Diagrama, Esquemático

Descrição gerada automaticamente

**Questions**

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?

Yes, the expected result was achieved

**Conclusions**

Lessons Learned (What did you learn?): It was possible to learn and implement a 4-bit adder and show this mathematical count on the 7-segment display

## Part 5

Author: Uriel Abe Contardi

Date: 24/08/2024

Procedure/Description of Test: The module guide was followed and the code was recorded in the development kit.

**Results**

Interface gráfica do usuário, Texto, Email

Descrição gerada automaticamente

Diagrama, Esquemático

Descrição gerada automaticamente

**Questions**

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?

Yes, the expected result was achieved

1. How does this compare to the number of Logic Cells in Part 4?

By writing the +- operations explicitly, we obtained a smaller number of logical resources used, possibly because the Synthesize tool has greater flexibility for optimization and can optimize more resources

**Conclusions**

Lessons Learned (What did you learn?): It was possible to learn and implement a 4-bit adder and show this mathematical count on the 7-segment display

# Module 2

## PWM

Author:

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

|  |  |
| --- | --- |
| Fmax |  |
| % Logic Utilization |  |
| Total registers |  |
|  |  |

Questions:

1. Did the LED change brightness depending on the setting of the first 3 switches?

Conclusions:

Lessons Learned (What did you learn?):

## ADC

Author:

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

|  |  |
| --- | --- |
| Fmax |  |
| %Logic Utilization |  |
|  |  |
|  |  |

Questions:

1. Does the board behave as you expected?

2. Is this a good voltmeter as is?

3. What could you change in either the board hardware or FPGA logic to make it perform better?

Conclusions:

Lessons Learned (What did you learn?):

# Module 3

## NIOS II Hardware Design

Author:

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

|  |  |
| --- | --- |
| Fmax |  |
| Logic Utilization |  |
|  |  |
|  |  |

Questions:

1. What is the purpose of the Avalon Memory-Mapped Clock-Crossing Bridge?

Conclusions:

Lessons Learned (What did you learn?):

# Module 4

## NIOS II Software Design and System Test

Author:

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

|  |  |
| --- | --- |
| Fmax |  |
| Logic Utilization |  |
|  |  |
|  |  |

Questions:

1. Is the control of the 10 LEDs implemented in hardware or in software?
2. Is the control of the 7-segment LEDs done by hardware or by software?
3. How much memory is required to run your Nios II program? Can you fit it into the onchip RAM if you redesign the onchip RAM block?
4. Your Nios II processor is running at what clock speed? How much faster can it run in your MAX10 design?

Conclusions:

Lessons Learned (What did you learn?):