An FPGA-based All-Digital Transmitter with 9.6-GHz 2nd order Time-Interleaved Delta-Sigma Modulation for 500-MHz bandwidth

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***Abstract*—An FPGA-based all-digital transmitter with 9.6-GHz 2nd order Time-Interleaved ΔΣ-modulation (TI-DSM) is presented. To improve the operation frequency of TI-DSM, bit separation architecture is proposed. This proposed architecture realizes the 1-bit digital transmitter with 500-MHz bandwidth. This is the widest bandwidth modulation among state-of-the-art FPGA-based all-digital transmitters.**

***Index Terms*—5G mobile communication, All-Digital Transmitter, Time-Interleaved Delta-Sigma Modulator (TI-DSM), Field-Programmable Gate Array (FPGA).**

I. Introduction

To cope with the recent demand of rapidly increased data traffic, 5G system requires wider bandwidth than 4G and 4G LTE advanced. It is said that at least 500-MHz bandwidth is required for representative 5G transceivers [1]. Accordingly, the increase of power consumption (especially, ADC (Analog to Digital Converter) and DAC (Digital to Analog Converter)) in transceivers becomes a big problem.

FPGA-based all-digital transmitters ([2] – [5]) are the promising approach to achieve low power consumption. In FPGA-based all-digital transmitters, the greater part of the transmitter is constituted by digital circuits implemented by FPGA. It leads to the reduction of power consumption due to get rid of analog circuits (such as mixers and DAC). In addition, by using 1-bit RF signal as input of PA, the class-D PA, which has the possibility of the highly efficient operation (theoretically 100 %), can be applied.

To enable FPGA-based all-digital transmitters with wide bandwidth, there are two different approaches. The one is increasing the operation frequency of ΔΣ-modulation (DSM). The other is applying the high order DSM. The architectures which enable to increase the operation frequency of DSM have been developed [4], [5]. However, they are restricted to 1st order DSM. On the other hand, the all-digital transmitters with 2nd order DSM have also been developed [2], [3]. Nevertheless, due to the longer critical path, 2nd order DSM has a limit in the operation frequency, sub 1-GHz at present.

This paper presents the novel architecture which can satisfy both increasing the operation frequency of DSM and using high order DSM. To fit in the low core clock rate of FPGA, 2nd order time-interleaved ΔΣ modulator (TI-DSM) is applied. To increase the operation frequency of 2nd order TI-DSM, bit separation architecture is proposed. The architecture is characterized as the separate operation between higher-order bits and lower-order bits. By FPGA implementation of the proposed 2nd order TI-DSM, the all-digital transmitter with 500-MHz bandwidth is realized.

II. Design of FPGA-based All-Digital Transmitter

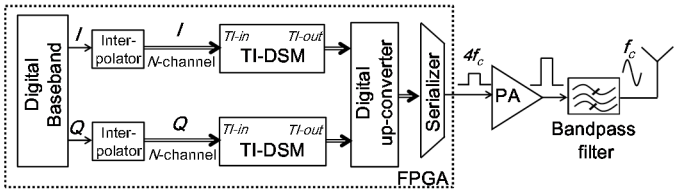

Fig. 1. FPGA-based all-digital transmitter

In an FPGA-based all-digital transmitter, as shown in Fig. 1, Multi-channel (the channel number is set to *N*) time-interleaved input *I* and *Q* signals are separately ΔΣ-modulated and the output signals are digitally up-converted into the multi-channel RF signals. Then, the multi-channel RF signals are serialized into the 1-bit RF signal. Finally, a 1-bit RF signal is fed to the PA and the output signal passes through the band-pass filter to restore the original RF signal.

Fig. 2. Relationship between SNR and OSR in 1st and 2nd order DSM

Fig. 2 shows the theoretical SNR as a function of over sampling ratio (OSR) of 1st and 2nd order DSM. This graph shows that 10-GHz operation of 2nd order DSM realizes 500-MHz bandwidth (OSR: 20) with 43.5-dB of SNR, which is sufficient for higher level modulation such as 256 QAM. Next, to achieve 10-GHz operation frequency of 2nd DSM, bit separation architecture is proposed.

III. Proposed 2nd order TI-DSM with Bit Separation Architecture

Fig. 3 shows the block diagram of 2nd order DSM. The computation time in the critical path, which consists of the two adders and the comparator, is too long to achieve 10-GHz operation. Moreover, 2nd order DSM is too complex to apply the previously-published high-speed operation scheme such as

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pipeline processing with look-ahead block [4] which is available in 1st order DSM.

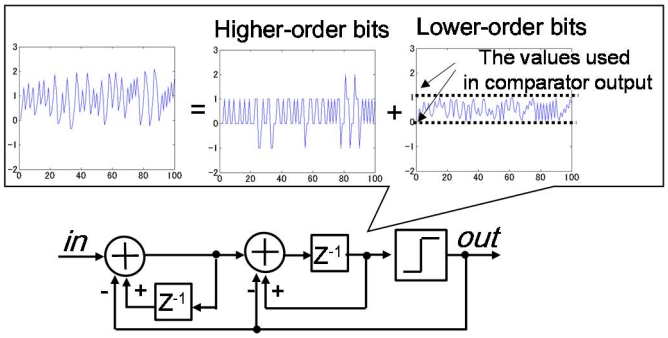

Fig. 3. The block diagram of 2nd order ΔΣ-modulator

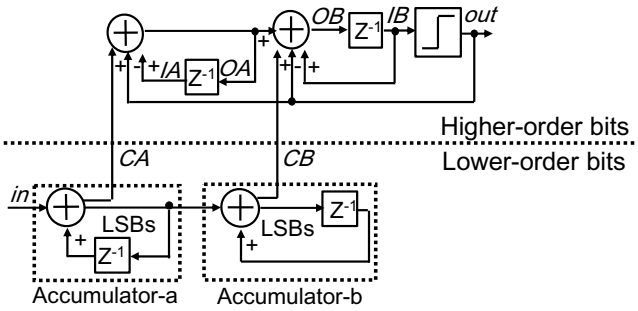

Fig. 4. Proposed 2nd order DSM with bit separation architecture

To achieve 10-GHz operation, 2nd order DSM with bit separation architecture is proposed as shown in Fig. 4. In this architecture, two series-connected accumulators are applied for lower-order bits, whose order is lower than that used in the comparator output. It is noted that the feedback path from the comparator to the internal block, as is seen in the original block in Fig.3, does not exist in lower-order bits calculation. 2nd order DSM operation is achieved by using remaining higher-order bits and the carry bits, *CA* and *CB*, which are fed from the two accumulators. This architecture enables to increase the operation frequency of 2nd order DSM by applying the two different high-speed schemes to higher-order bits and lower-order bits separately, as follows.

A. Pipeline structure in lower-order bits calculation

In lower-order bits calculation, the two accumulators, named as Accumulator-a and Accumulator-b, in Fig 4 are series-connected. They can be easily applied to time-interleave and pipeline structure for high-speed processing [4]. Fig. 5 (a) and (b) show the block diagram of time-interleaved pipeline structure and time-interleaved-accumulator. The sum bits of Full-Adders (FAs) in Accumulator-a are fed to the input of FAs in Accumulator-b. This enables to increase the operation speed as much as that of 1st order DSM with the same time interleave pipeline structure.

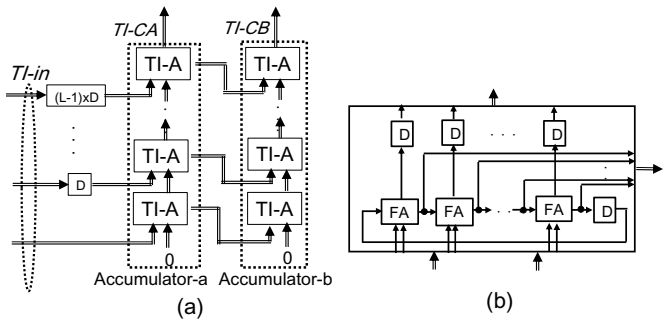

Fig. 5. The block diagram of lower-order bits calculation
(a) time-interleaved pipeline structure
(b) time-interleaved-accumulator

B. Parallel processing structure with the state assignment in higher-order bits calculation

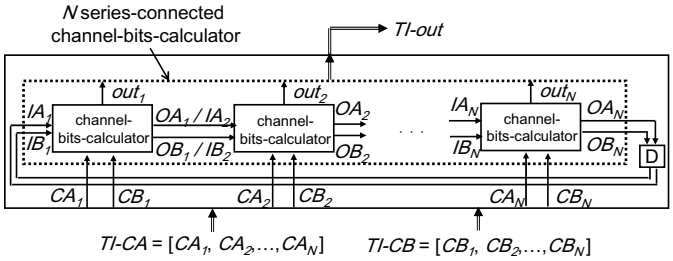

Fig. 6. The block diagram of TI-higher-order bits calculation

For high-speed operation, the block diagram of TI-higher-order bits calculation is shown in Fig 6. The channel number of time interleave is defined as *N*. This block consists of *N* series-connected channel-bits-calculator which is corresponding to the block for higher-order bits in Fig. 4. The *N* series-connected channel-bits-calculator has four inputs (*TI-CA*, *TI-CB*, IA_1, IB_1) and three outputs (OA_N, OB_N, *TI-out*). Output OA_N and OB_N are used as input IA_1 and IB_1 on the next clock cycle.

TABLE I
THE STATE ASSIGNMENT TABLE

State	(OA_N, OB_N)
$st_{1,1}$	(A_1, B_1)
$st_{1,2}$	(A_1, B_2)
:	:
$st_{1, Mb}$	(A_1, B_{Mb})
$st_{2,1}$	(A_2, B_1)
:	:
$st_{Ma, Mb}$	(A_{Ma}, B_{Mb})

To accelerate the TI-higher-order bits calculation, parallel processing with the state assignment is proposed. Here, *TI-out* is conducted from *TI-CA*, *TI-CB* and internal state (OA_N, OB_N,). In this parallel processing, a plural of *TI-outs* are conducted from all possible internal states in advance. For the next clock cycle, the *TI-out*, which was conducted from the same internal state as the current internal state, is selected.

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Table I shows the state assignment table in the N series-connected channel-bits-calculator. Considering that the bit number used in the higher-order bits are much reduced thanks to bit separation architecture, the number of possible internal states (OA_N, OB_N) is quite small. In the Table, the numbers of the possible values for OA_N and OB_N are respectively Ma and Mb, and the possible values of OA_N and OB_N are defined as $A_1, A_2, \ldots, A_{Ma}$ and $B_1, B_2, \ldots, B_{Mb}$, respectively. Then, the numbers of the internal states (OA_N, OB_N), M, are equal to $Ma \times Mb$.

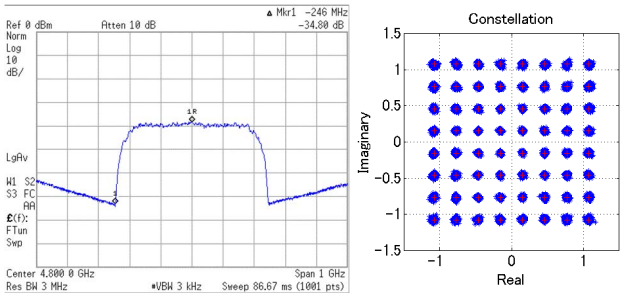
It is noted that the internal states number M is excessive since some internal states do not appear actually in the calculation. By omitting the calculation with such unused internal states, the resource usage can be further reduced.

IV. Measurement

An FPGA-based all-digital transmitter with the proposed DSM was implemented for 4.8-GHz band. The Xilinx VCU108 evaluation kit (with UltraScale XCVU095) was used. The architecture follows Fig. 1 and GTY transceiver (19.2-Gbps) was used as a serializer. Here, the precision number L = 12, the channel number N = 32 on 300-MHz reference clock (equivalently 9.6-GHz DSM for I and Q signals) in FPGA-implementation. The 64-QAM signal with the symbol rate of 400-Msps (2.4-Gbps) and sampling rate of 1.2-GS/s was used. It is noted that in this case, M can be set to 14 by reducing the unused internal states.

The FPGA output signal was directly connected to the spectrum analyzer E4440A (Keysight) and the oscilloscope DSO81204A (Keysight) for spectral and signal analysis.

Fig. 7 (a) shows the measured output spectrum at 4.8-GHz band. The transmitter achieved SNR of 34.8-dB in 488-MHz bandwidth. Fig. 7 (b) shows the constellation calculated from measured time domain signal. EVM was evaluated as 2.7 %. This EVM value means that the transmitter satisfies the requirements of not only 64 QAM but also 256 QAM [6]. These results indicate that the proposed transmitter has enough performance for 500-MHz bandwidth modulation. It is also noted that the measured outband spectrum is sub-standard. Thus, in practical cases, the bandpass filter is required to suppress the outband spectrum.



(a) (b)

Fig. 7. Measured output (a) spectrum at 4.8-GHz band (b) constellation

TABLE II
COMPARISON WITH ΔΣ TRANSMITTER FOR FPGAS

	Band-width	SNR	Sampling Freq	Modulation
[2]	8 MHz	60 dB	0.8 GHz	TI-DSM (2nd)
[3]	19 MHz	37.9 dB	0.9 GHz	TI-DSM (2nd)
[4]	20 MHz	> 40 dB	10.4 GHz	TI-DSM (1st)
[5]	122 MHz	31.4 dB	3.2 GHz	Parallel-DSM (1st)
This work	488 MHz	34.8 dB	9.6 GHz	TI-DSM (2nd)

TABLE III
UTILIZATION IN PROPOSED FPGA-BASED TRANSMITTER

Resource	Utilization	Available	Utilization %
CLB LUTs	9413	537600	1.75
CLB Registers	8865	1075200	0.82
Memory	61	1728	3.53
IO	9	832	1.08
DSPs	0	768	0

TABLE II shows the benchmark of FPGA-based all-digital transmitters. It indicates that the much higher operation frequency (up to 9.6-GHz) of 2nd order TI-DSM leads to over four times wider bandwidth modulation than the previous works.

TABLE III shows the utilization in the proposed FPGA-based digital transmitter. In this transmitter, DSP resource is not needed and the total occupied resource is remarkably small.

V. Conclusion

An FPGA-based wideband all-digital transmitter was demonstrated. For increasing the operation frequency of 2nd order TI-DSM, bit separation architecture was proposed. By implementing the proposed architecture in an FPGA, 9.6-GHz operation of 2nd order TI-DSM has been achieved and realized 500-MHz bandwidth modulation, which is the widest among state-of-the-art FPGA-based all-digital transmitters, in 4.8-GHz band. It will contribute to 5G systems with low power consumption.

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