Agile All-Digital RF Transceiver Implemented in FPGA

R. F. Cordeiro, *Student Member, IEEE*, André Prata, *Student Member, IEEE*, Arnaldo S. R. Oliveira, *Member, IEEE*, José M. N. Vieira, and N. B. De Carvalho, *Fellow, IEEE*

***Abstract*— This paper presents a new all-digital transceiver architecture fully integrated into a single field-programmable gate array chip. Both the radio frequency (RF) receiver and the transmitter were entirely implemented using a digital datapath from the baseband up to the RF stage without the use of conventional analog-to-digital converter, digital-to-analog converter, or analog mixer. The transmitter chain uses delta–sigma modulation and digital upconversion to produce a two-level RF output signal. The receiver uses a high-speed comparator and pulsewidth modulation to convert the RF signal into a single-bit data stream, which is digitally filtered and then downconverted. Both the transmitter and the receiver are agile with flexible carrier frequency, bandwidth, and modulation capabilities. The transceiver error vector magnitude and the signal-to-noise ratio figures of merit were analyzed in a point-to-point transmission to evaluate the transmitter's performance. The results show the feasibility of this approach as a more flexible alternative to common radio architectures.**

***Index Terms*— All-digital transceivers, delta–sigma modulation (DSM), pulsewidth modulation (PWM), software-defined radio (SDR).**

I. Introduction

IN THE last two decades, mobile wireless communications have witnessed a phenomenal growth in terms of users, mobile terminals, and throughput requirements to drive multimedia and video services. This has led to successive generations of mobile cellular standards from the highly successful 2G networks (GSM), going through the 3G (HSPA), and up the current 4G (LTE). During the next decade, this trend will continue, due to the proliferation of personal communication devices and the Internet of Things phenomena. This will spread machine-to-machine communications by embracing billions of constantly connected devices and seeking the integration of different standards to provide ubiquitous high-rate and low-latency experience [1].

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The authors are with the Departamento de Electrónica, Telecomunicações e Informática, Instituto de Telecomunicações, Universidade de Aveiro, 3810-193 Aveiro, Portugal (e-mail: ruifiel@ua.pt; andre.prata@ua.pt; arnaldo.oliveira@ua.pt; jnvieira@ua.pt; nbcarvalho@ua.pt).

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Therefore, 5G must be capable to efficiently answer the new communication challenges and, at the same time, act as an integrator over the previous standards. A number of new ideas and concepts are being suggested and evaluated by the industry and academia for 5G support technologies, such as massive MIMO, exploitation of higher radio frequency (RF) bands, such as millimeter wave range, and centralized radio access networks for highly digital radio access networks [1], [2]. Nonetheless, the increasing use of new wireless standards using different frequencies, diverse coding and modulation schemes, and targeting various applications is already taking place. The need for cooperation between access points and devices in the network using different heterogeneous technologies will be essential to support the required flexibility and spectral efficiency for 5G networks.

Ultimately, 5G and all networks beyond will be extremely dense, flexible, and heterogeneous, which introduces many new challenges for network modeling, analysis, design, and optimization. The core network will also have to reach unprecedented levels of flexibility. Spectrum regulation will need to be rethought, and energy and cost efficiencies will become even more critical [2]. Furthermore, there will be an increasing trend to digitalization motivated by the flexibility and high performance allowed by the cognitive radio and software-defined radio (SDR) approaches, where mixed-signal and all digital systems will have a rising importance in the design of radio and telecommunication systems. The all-digital transceivers will be the focus of this paper due to their improved flexibility permitted by the completely digital signal processing up to the RF stage.

In this paper, a new all-digital RF transceiver architecture, fully integrated into a single field-programmable gate array (FPGA) chip, will be presented and evaluated. The entire signal processing from the baseband up to the RF stage for the transmitter, and the opposite for the receiver, is completely performed in the digital domain. In this sense, the proposed system does not use conventional analog-to-digital (ADC) and digital-to-analog converters neither any kind of analog mixing device, enabling the creation of a much more compact and integrated radio. To the best of our knowledge, this is the first time a fully integrated all-digital RF transceiver architecture is presented.

This paper is organized as follows. In Section II, the state of the art of SDR transceiver architectures is presented. Section III presents the proposed transmitter and receiver architectures and their hardware implementation. To validate

the proposed system, the measurement results of error vector magnitude (EVM) and signal-to-noise ratio (SNR) will be presented and discussed in Section IV. Finally, some conclusions are drawn in Section V.

II. State of the Art

SDR transceiver architectures will be fundamental in the future radio communication systems in order to endow the physical layer with high flexibility, spectral, and energy efficiency [3]. Therefore, this section addresses the state of the art on SDR transceivers focusing on all-digital platforms, due to the enormous advantages that such architectures can provide.

A. Transmitters

All-digital transmitter architectures typically use pulsed-modulation approaches to allow the full digitalization of the radio system, which poses an important step toward the complete software description of RF signals proposed in SDR.

Recent advances involving pulsed-RF transmitters include the development of novel all-digital transmitter architectures, where the radio datapath is digital from the baseband up to the RF stage. These transmitters perform a conversion from an m-bit digital representation to a two-level signal, usually done by means of the delta–sigma modulation (DSM) or pulsewidth modulation (PWM) schemes. The state-of-the-art pulsed transmitters can use amplitude and phase modulation of the RF carrier using PWM [4]–[7], bandpass DSM [8], [9], or low-pass DSM with digital upconversion (DUC) [10]–[14]. To improve signal quality, many works have focused into the increase of the signal oversampling ratio (OSR). Most of pulsed-RF transmitters achieve higher OSR by optimizing the digital design for a higher frequency [15]. However, digital switching logic has frequency limits that bound the achievable OSR to a maximum value depending on the used technology. An alternative approach for higher OSR is to use parallelized processing followed by dedicated high-speed logic, such as a multiplexer or a serializer [16]–[18]. This eases the design of higher bandwidth transmitters working at reduced logic frequencies and the competitive integration with lower cost technologies.

The functionality and the flexibility of the transmitter are also of great importance, since the purpose of a digitally controlled transmitter is to easily adapt the radio to its environment and user needs. Carrier frequency flexibility means that a single digital chip can be a wideband radio with multiple channels and standards. In this paper, we present a transmitter capable of covering signal bands from 400 MHz to 2.4 GHz.

B. Receivers

Traditional RF receivers are commonly based on homodyne or heterodyne architectures, usually performing analog down-conversion up to the baseband or up to an IF stage, where the signal is sampled by an I/Q (ADC) or by an IF ADC. These architectures present a high dependence on analog components imposing problems, such as limited bandwidth, due to the analog components frequency response. Alternatively, the IF ADC can be replaced by an RF ADC, allowing sampling the spectrum directly at the RF stage and, therefore, performing the entire signal processing in the digital domain, as it was envisioned as the ideal SDR receiver [3] (Fig. 1). These architectures present high flexibility and high bandwidth and allow taking profit of the high efficient and accurate digital signal processing techniques, avoiding the analog impairments and mismatches [19].

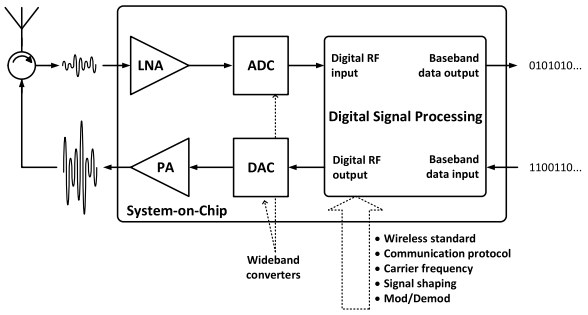


Fig. 1. Ideal SDR transceiver architecture.

Modern SDR receiver performance and flexibility is susceptible to the ADC's bandwidth as well as its linearity. Current commercial RF ADCs have reached a few gigahertz of sampling frequency and analog input bandwidth. However, they are expensive and have a significant energy consumption, which may reduce the overall systems efficiency.

Recently, new possibilities to build RF ADCs based on pulsed-modulation converters were proposed, such as, DSM [20], pulse frequency modulation (PFM) [21], [22], or PWM [23], [24]. All these types of ADCs are single-bit ADCs, i.e., all deal with a digital pulsed representation of the analog signal. The DSM ADCs are often used in audio applications, due to their high resolution that they provide [19]. Several research works presented RF DSM ADCs, such as [20] where a high resolution ADC was built, however with low analog input bandwidth. A PFM ADC is based on a voltage-controlled oscillator (VCO) to create a PFM representation of the input analog signal [21]. These types of ADCs present high undesirable nonlinear behavior related to the VCO that may be improved using techniques as the ones presented in [22]. A PWM ADC is made of a single comparator, whose inputs are the analog signal and a given reference wave (usually a triangular wave), generating a PWM representation of the analog signal [25]. They are commonly used in low-frequency applications [25]; nevertheless, they are also being applied in the RF world, as presented in [23] and [24]. In [23], high-speed comparators to generate the PWM representation are used, and in [24], a single FPGA-chip is used to build the ADC and the remaining receiver, presenting a flexible and promising architecture. However, none of these works present an exact way to obtain the best reference waveform to optimize the receiver figures of merit. In this paper, we present an algorithm that optimizes the frequency of a reference triangular wave in order improve the receiver performance.

III. Proposed Architecture

This section presents and explains the proposed architecture for the all-digital transceiver. For the sake of clarity,

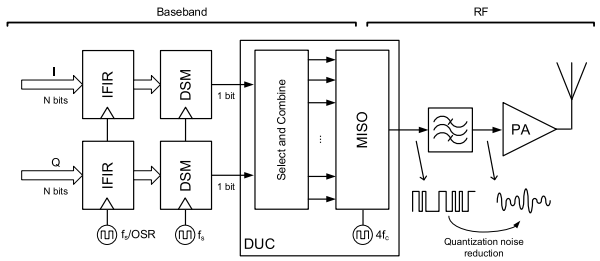


Fig. 2. DSM-based ADT architecture. Baseband delta–sigma clock frequency is f_s, while the DUC works at a four times the carrier frequency f_c.

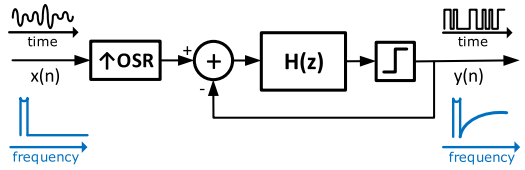


Fig. 3. DSM loop with loop filter $H(z)$.

the transmitter and receiver architectures will be presented separately, but implemented and tested together.

A. Proposed Transmitter Architecture

This section presents and explains the proposed architecture for the all-digital transmitter. The digital transmitter architecture used is shown in Fig. 2. The baseband complex signal is divided into two components, the in-phase (I) and quadrature (Q) signals. It should be noted that for the purpose of this paper, no particular protocol or standard is considered, i.e., the digital baseband processing can be performed as in conventional transmitter architectures, for any particular standard use.

The proposed architecture uses DSM with a two-level output. The delta–sigma modulator, as shown in Fig. 3, is a signal shaping stage of the modulator, which converts the I and Q signals with N bits resolution, into single-bit representation signals, at the tradeoff a higher resolution in time. The signal is initially upsampled to improve the OSR using a digital interpolation filter. The filter inside the delta–sigma loop shapes the quantization noise inserted by the 1-b quantizer at the output by feeding back the error signal. The output of the modulator is a binary signal with added out-of-band quantization noise.

The DSM loop filter will define the transmitted signal resolution and consequent signal quality in terms of SNR. Higher order DSM allows higher noise rejection for the signals band at the same OSR. However, the higher in-band noise rejection increases the noise in the adjacent bands. In [26], an extensive study was made on the influence of the DSM's order on the signal to quantization noise ratio (SQNR). An approximation of the SQNR value given by (1) and equivalent signal resolution in number of bits is shown in Fig. 4 for a first-, second-, and third-order DSMs. In the presented equation, OSR is the oversampling ratio and L is the DSM order. Higher DSM orders require lower values of OSR to achieve the same performance when compared with lower DSM orders, and

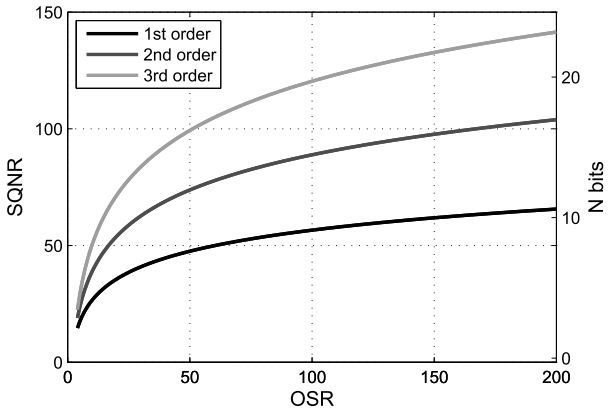


Fig. 4. SQNR and effective number of bits for two-level DSM with different orders of modulation.

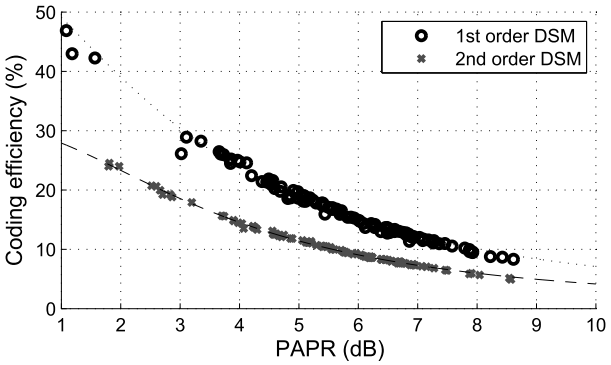


Fig. 5. CE variation with input signal for the first- and second-order DSM. The measured PAPR and CE values are from random phase and amplitude multisine signals.

therefore, lower sampling frequencies could be used. Hence, it should be desirable to use a higher order modulator to improve the transmitter SNR

$$\mathrm{SQNR_{dB}} = 3.01 \times \log_2(\mathrm{OSR}) \times (2L+1) - 9.36L - 2.76. \tag{1}$$

In RF applications, this becomes a problem, since additional out-of-band noise reduces the transmitter efficiency. The relationship between in-band power and total transmitted power is the modulator coding efficiency (CE). It can be defined as the signal channels power P_s over the total transmitted power P_t [27], as it is shown in

$$\mathrm{CE} = \frac{P_s}{P_t}. \tag{2}$$

The CE of DSM varies subject to the nature of the input signal, particularly its peak-to-average power ratio (PAPR), and is typically lower than 30%. However, higher orders of modulation will decrease even further the CE of the transmitter. Fig. 5 shows a representative graph of CE measurements for an all-digital transmitter with both the first-order and the second-order modulators for different PAPR signals. It is perceptible that for common wireless communication standards with PAPR varying from 3 dB up to 12 dB, the CE is considerably low, especially for higher order modulators.

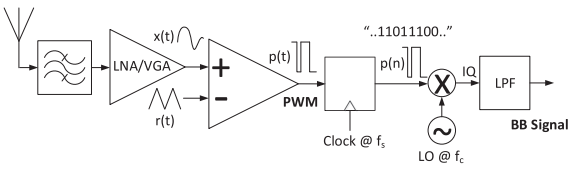


Fig. 6. PWM-based all-digital receiver architecture.

Since higher order DSM limits the transmitters CE, increasing the modulators order is not a satisfactory solution to improve the signal SNR. A possible alternative is to increase the OSR of the modulator by increasing its operation speed. However, a key limitation in digital DSM is the typically low bandwidth of the signal modulator due to frequency restrictions for the digital logic clock because of the loop-filter propagation delays. To overcome this, it was used a time-interleaved DSM to improve the maximum modulator sampling frequency. This parallel DSM architecture used was initially presented in [18] to improve the modulator OSR by allowing the processing of multiple parallel delta–sigma samples in a single clock period.

The DSM used is a first-order modulator, because it has a higher CE for the transmitted signal. In addition, a simpler loop filter can be implemented with fewer logic elements. Less logic gates allow for a smaller logic delay path and, therefore, a higher sampling rate and signal bandwidth.

The DUC is achieved by time interleaving the delta–sigma modulated two-level samples (I and Q) in time with their inverted versions. The resulting wave, w in (3), is equivalent to the multiplication of I and Q baseband components with two square waves with a 90° phase shift between them. To do this, a parallel to series block with a switching frequency four times superior to the desired carrier frequency f_c can be used

$$w = [I; Q; \overline{I}; \overline{Q}]. \tag{3}$$

The resulting output signal has the baseband complex signal upconverted to f_c with added quantization noise in the sidebands added by the DSM. This noise can be filtered and the RF signal recovered.

B. Proposed Receiver Architecture

In this section, the receiver architecture will be presented and explained, considering a PWM-based topology, which was chosen mainly due to the high analog input bandwidth and flexibility that such topology can provide.

The generic block diagram architecture for the proposed receiver is shown in Fig. 6, where the signal $x(t)$ represents the RF signal, centered at f_c with bandwidth BW, received at the antenna after filtering and low noise variable gain amplification (LNA/VGA). The $x(t)$ signal is one of the inputs of a comparator, while the other is a reference signal $[r(t)]$, of frequency f_r, which is usually a triangular wave. At the output of this comparator, there is a continuous time PWM signal $p(t)$ that contains the information of the $x(t)$ signal. The $p(t)$ signal is a natural sampling PWM representation of $x(t)$ [28], which implies that no quantization noise is added into the signal's band. Following the comparator, there is a single-bit register responsible to sample and discretize the continuous time PWM signal $p(t)$, at a sampling rate of f_s, with ($f_s \geq 2f_c$ and $f_s \gg$ BW). Thereafter, the signal is available for further processing regarding digital downconversion and filtering in order to recover the baseband signals information.

The analog-to-digital conversion stage, which is the key element of this receiver, as any other converter can be separated in two processes; sampling and quantization, which are related to discretization in both time and amplitude, respectively. The proposed way to implement the conversion (PWM) is similar to the stochastic ergodic converter presented in [29], which was a popular idea in the 1960s to build low-cost and low-frequency ADCs. However, at the time, due to the lack of enabling technology, the idea was abandoned and sigma–delta converters were preferred [29]. This converter is mainly based on adding a dithering wave to an analog signal and then feeding it to a single-bit quantizer. The theoretical demonstration of this converter can be developed based on the statistical quantization theory, which shows that if the dithering signal presents uniform distribution, the input signal will be equally quantized, i.e., the mean of the input signal will be contained in the output quantized signal, allowing its recovering. A common selection for the dithering wave is a triangular or sawtooth wave, since both present uniform amplitude distributions [29], [30]. This dithering wave can be directly transposed for the PWM RF ADC, playing the same role as the reference signal $r(t)$, which should also present uniform amplitude distribution.

In addition to the reference signal amplitude distribution, two other important characteristics are the reference frequency and the sampling frequency of the sampler after the comparator, which define the maximum bandwidth of the signal to acquire. The latter two variables will also impose the converters resolution, since the ratio between the effective sampling frequency (f_s) and the reference signal frequency (f_r) indicates the number of PWM levels and, therefore, the number of bits of the converter (4) and its SNR (5), as follows:

$$N_{\text{bits}} = \log_2(N_{\text{levels}}) = \log_2 \frac{f_s}{f_r} \tag{4}$$

$$\text{SNR} = 6.02N_{\text{bits}} + 1.76. \tag{5}$$

The previous relationships indicate that the higher the ratio between the sampling frequency and the reference signal, the higher will be the converter effective resolution. Therefore, we may consider that the limit for f_s will be imposed by the maximum frequency allowed by a given technological process or by a set of requirements, such as resolution or power consumptions of a certain application. Nonetheless and without loss of generality, in order to simplify the digital architecture and to provide the maximum resolution, f_s should be fixed to the maximum achievable value and maintaining the previous assumptions $f_s > 2f_c$ and $f_s \gg$ BW. Thereafter, considering an analog signal occupying a given bandwidth (BW), it is important to select the minimum reference signal frequency to provide the higher resolution, while a selection of a minimum

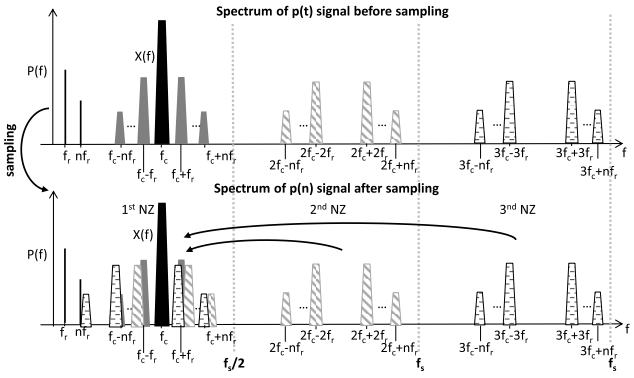


Fig. 7. Conceptual representation of the PWM signal spectrum, in the first three NZs, before and after sampling.

reference frequency, f_r, of 2 BW for a sawtooth waveform or of BW for a triangular waveform allows achieving the same resolution, and it creates a different harmonic content in the PWM spectrum. The sawtooth wave puts the first distortion band closer to the interest band, making the triangular wave a preferable way to acquire the signal and to provide a relaxation of the filtering requirements in the digital downconvert (DDC) chain.

At the register's input, ideally, there is a perfect square wave with varying duty cycle of infinitesimal resolution, which presents an infinite power spectrum, as shown in spectrum before sampling in Fig. 7. Then, the single-bit register running at f_s samples the continuous time $p(t)$ waveform, generating a discrete-time $p(n)$ PWM waveform. As already mentioned, the relation $f_s > 2f_c$ imposes the signal of interest $x(t)$ to be in the first Nyquist zone (NZ). However, the sampling process causes a frequency overlap at the first NZ due to the aliasing of PWM harmonics coming from higher NZs, as shown in Fig. 7 after sampling. This aliasing is unavoidable, since an antialiasing filter cannot be included between the comparator and the register, in order to maintain a two-level signal. The use of a binary signal allows to simplify the sampling hardware to a single-bit register. Therefore, an analysis of the $p(t)$ PWM spectrum signal should be considered, in order to understand how this overlapping can be avoided in the signal's band.

The PWM modulation process (6), which is the comparison between the RF signal, $x(t)$, and the reference signal, $r(t)$, can be described by the sign function (7)

$$p(t) = \text{sign}(x(t) - r(t)) \tag{6}$$

$$\text{sign}(x(t)) = \begin{cases} -1, & \text{if } x(t) < 0 \\ +1, & \text{if } x(t) > 0. \end{cases} \tag{7}$$

In [31], a general mathematical model to approximate (6) is presented in (8), and is valid for every $x(t)$ signals

$$p(t) = x(t) + \frac{2}{\pi} \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \frac{1}{n} e^{jn\omega_r t} \sin\left(\frac{n\pi}{2}(1 + x(t))\right) \tag{8}$$

where ω_r is the angular reference signal frequency and $x(t)$ is the RF signal that can be described as $x(t) = x_{BB}(t) \sin\,¡(\omega_c t)$, where $x_{BB}(t)$ is the baseband signal's envelope modulated by a carrier centered at ω_c. Then, replacing $x(t)$ by the previous description and applying some well-known trigonometric identities (8) can be simplified into

$$p(t) = x(t) + \sum_{n=1}^{+\infty} \frac{4}{n\pi} \cos(n\omega_r t) \times \sin\left(\frac{n\pi}{2} x_{BB}(t) \sin(\omega_c t) + \frac{n\pi}{2}\right). \tag{9}$$

Consequently, applying the sum-to-product trigonometric identity, (9) becomes

$$p(t) = x(t) + \sum_{n=1}^{+\infty} \frac{4}{n\pi} \cos(n\omega_r t) \sin\left[A(t)_{n\,\text{even}} + A(t)_{n\,\text{odd}}\right] \tag{10}$$

where $A(t)_{n\,\text{even}}$ and $A(t)_{n\,\text{odd}}$ are, respectively, given by

$$A(t)_{n\,\text{even}} = \cos\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{2} x_{BB}(t) \sin(\omega_c t)\right) \tag{11}$$

$$A(t)_{n\,\text{odd}} = \sin\left(\frac{n\pi}{2}\right) \cos\left(\frac{n\pi}{2} x_{BB}(t) \sin(\omega_c t)\right). \tag{12}$$

To know the spectrum of the PWM signal $p(t)$, a Fourier transform must be applied on (10). However, the Fourier transform of all the elements is not trivial, since it implies to calculate the transform of a function in the format $\sin(\beta \sin(\theta))$ and $\cos(\beta \sin(\theta))$. It can be further simplified using the Jacobi–Anger expansion, which uses the first-order kind Bessel function [32]

$$\sin(\beta \sin(\theta)) = 2 \sum_{k=1}^{+\infty} J_{2k-1}(\beta) \sin((2k-1)\theta) \tag{13}$$

$$\cos(\beta \sin(\theta)) = J_0(\beta) + 2 \sum_{k=1}^{+\infty} J_{2k}(\beta) \cos(2k\theta) \tag{14}$$

where $J_k, k \geq 0$ represents the first-order kind Bessel function. Therefore, by applying (13) and (14) on (11) and (12) a new approximation for $A(t)_{n\,\text{even}}$ and $A(t)_{n\,\text{odd}}$ can be achieved in the form of (15) and (16)

$$A(t)_{n\,\text{even}} = \cos\left(\frac{n\pi}{2}\right) 2 \sum_{k=1}^{\infty} J_{2k-1}\left(\frac{n\pi}{2} x_{BB}(t)\right) \times \sin((2k-1)\omega_c t) \tag{15}$$

$$A(t)_{n\,\text{odd}} = \sin\left(\frac{n\pi}{2}\right) \left[J_0\left(\frac{n\pi}{2} x_{BB}(t)\right) + 2 \sum_{k=1}^{\infty} J_{2k} \times \left(\frac{n\pi}{2} x_{BB}(t)\right) \cos(2k\omega_c t) \right]. \tag{16}$$

Considering now (10) with the new expressions for $A(t)_{n\,\text{even}}$ and $A(t)_{n\,\text{odd}}$ it is possible to reach an approximation of the central frequency bins, where the PWM distortion will fall. In fact it is not relevant to solve the entire Fourier transform of (10), since the idea is just to choose a reference frequency $r(t)$ to avoid the distortion overlap in the first NZ and, consequently, optimize the receiver SNR.

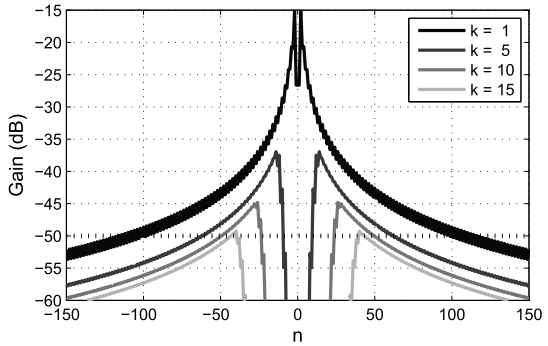


Fig. 8. Magnitude of the amplitude response of $P^*(f)$.

Thus, (17) and (18) present the center frequencies of the PWM distortion bands

$$P^*_{n\,\text{even}}(f) = \sum_{n=1}^{\infty} \frac{2}{n\pi}\delta(f - nf_r) * \left[\sum_{k=1}^{\infty} |J_{2k-1}(B(t))|_{\max}\delta(f - (2k-1)f_c)\right]$$

$$P^*_{n\,\text{odd}}(f) = \sum_{n=1}^{\infty} \frac{2}{n\pi}\delta(f - nf_r) \quad (17)$$

$$* \left[|J_0(B(t))|_{\max} + \sum_{k=1}^{\infty} |J_{2k}(B(t))|_{\max}\delta(f - 2kf_c)\right] \quad (18)$$

where $P^*_n(f)$ are the central bins of the positive part of the $p(t)$ spectrum, $\delta(f)$ is the Dirac delta function, $|J_k\ (B(t))|_{\max}$ with, $B(t) = (n\pi/2)x_{BB}(t)$, is the maximum absolute value of the amplitude response for a given distortion bin.

At this point, it is important to note that (17) and (18) give the information of the central frequencies of each PWM harmonic, as shown in spectrum before sampling in Fig. 7. Thus, considering a certain level of required or imposed SNR, it should be guaranteed that the PWM harmonics do not fall over the interest band in the first NZ. Therefore, the folding frequency bins placement in the first NZ should be calculated using (19)

$$f_{\text{fold}} = \left| f_c - \left\lfloor \frac{f_c}{f_s} \right\rceil f_s \right| \quad (19)$$

where f_{fold} is the folding frequency in the first NZ, f_c is the carrier frequency, f_s is the sampling frequency, $\lfloor \ldots \rceil$ is the rounding operation toward nearest integer, and $|\ldots|$ is the absolute value. In addition, the amplitude response of $|J_k\ (B(t))|_{\max}$ must be analyzed, up to an n and k value that guarantee the calculation of all distortion bands above the SNR limit.

The maximum k and n values from (17) and (18) can be extrapolated from an imposed limit of the amplitude response of $P^*_n(f)$. In Fig. 8, a limit of -50 dB is considered for the amplitude gain which immediately imposes a maximum value of 15 for the maximum carrier frequency harmonic k. Then,

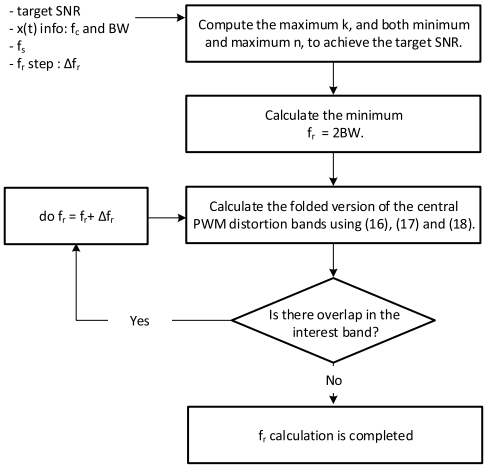


Fig. 9. Flowchart diagram of the proposed algorithm to find the best reference frequency to improve the SNR.

after obtaining n, k that will be considered, for the calculation of the folding spectrum version using (19), this information must be used in an algorithm to obtain the best reference frequency (Fig. 9).

The proposed algorithm starts with a set of inputs, which are the target SNR, the carrier frequency, f_c and the bandwidth, BW, of the signal $x(t)$, the sampling frequency, f_s, and a step for the reference frequency (Δf_r). It should be noted that BW here considered is the channel bandwidth instead of the signal bandwidth in order to allow for a small frequency margin for filtering, usually a small percentage of the signal bandwidth, for example, 30% is considered reasonable.

Regarding the algorithm, it starts by computing k and both minimum and maximum n to guarantee the target SNR, as previously described. Then, it calculates the minimum reference frequency, which is given by 2BW. Following, there is the calculation of the folded version of the spectrum and the verification of the presence of any overlap that may jeopardize the SNR. If there are no overlaps, the reference frequency calculation finishes, otherwise a new reference frequency is tested, given by the previous frequency plus a given step (Δf_r). This step should be small enough to allow a small loss of resolution and should have an irrational relation to f_s in order to avoid successive occurrences of overlaps from various NZs. Therefore, this step was fixed to be a submultiple of π. An alternative should also be to vary f_s, however that would increase the complexity of the DDC chain due to the need of irrational decimation filters. This procedure will allow to obtain a f_r that will generate a sampled signal, which obeys to the target SNR limit.

In order to exemplify the proposed algorithm, Fig. 10 presents the simulation results of the proposed receiver considering an ideal comparator. The simulation was performed considering a carrier frequency of 1650 MHz and a 16-QAM signal with 5 MHz of symbol rate. The minimum reference is 14 MHz and the optimized reference after computing the proposed algorithm is 30.9 MHz. As it is possible to verify in Fig. 10, the signal's spectrum using the minimum reference frequency presents a degraded SNR when compared with the spectrum with the best reference. In fact, after computing the

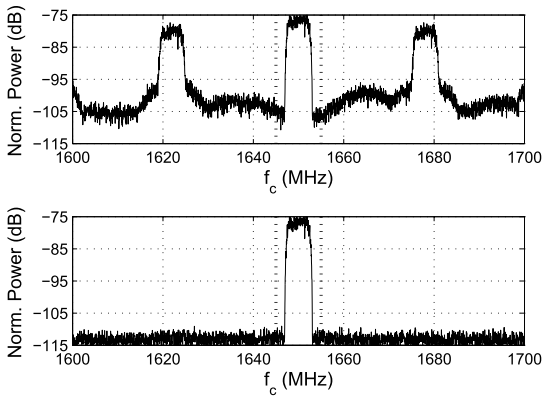


Fig. 10. Receiver simulation results with and without best reference calculation, top and bottom plot, respectively.

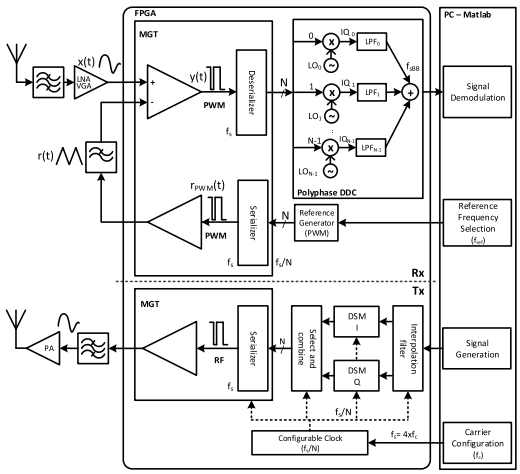


Fig. 11. Block diagram representation of the proposed FPGA-based all-digital transceiver architecture.

EVM of both situations, it was verified an SNR improvement of 9 dB, which validates the proposed technique.

Finally, during laboratorial measurements new spectral bins, different from the ones predicted by (17) and (18) were detected. In fact, these new distortion bins are associated with a dc offset error α at the input of the comparator, which can be modeled by (8) considering that $x(t)$ is now given by $x(t)+\alpha$. Therefore, applying the mathematical steps presented previously, a new expressions for $P_n^*(f)$ considering the mismatch Î±, can be reached (20) and (21), as shown at the bottom of this page.

C. FPGA Implementation

A proof of concept prototype was developed using the proposed transmitter and receiver architectures presented in the previous sections. The hardware design was implemented in a KC705 board from Xilinx with a Kintex-7 XC7K325T FPGA. An FPGA design allows for a completely integrated approach of both the all-digital transmitter and receiver due to the high logic capacity of modern FPGAs. Also, their inherent reconfigurability allows for a fast adjustment of the radio hardware to different purpose scenarios, which strongly falls within the concept of SDR. The FPGA-based transceiver architecture, shown in Fig. 11, can be separated into its two main functional blocks, the transmitter (ADT) and the receiver (ADR). The implemented system has an Ethernet connection to a local PC running a MATLAB routine responsible for the baseband signal generation and demodulation, transceiver carrier control, and reference signal frequency calculation. The transmitter interpolation filter defines the datapath sampling rate. Higher sampling frequencies will improve the signal OSR in the DSM and, therefore, the transmitted signal quality. However, the sampling rate must be adjusted depending on the carrier frequency. For carriers between 400 MHz and 1 GHz, the sampling frequency is equal to f_c, and the RF waveform is the following parallel word w_{low} on (22). The use of repeated samples in (22) reduces the carrier frequency to half while maintaining the transceiver clock within the FPGA PLL frequency lock range. This allows to use this ADTx architecture for carrier frequencies between 400 MHz and 2.4 GHz

$$w_{\text{low}} = [I_0;\, I_0;\, Q_0;\, Q_0;\, \overline{I_1};\, \overline{I_1};\, \overline{Q_1};\, \overline{Q_1};\, I_2;\, I_2;\, Q_2;\, Q_2;\, \overline{I_3};\, \overline{I_3};\, \overline{Q_3};\, \overline{Q_3}] \quad (22)$$

The input IQ signal is upsampled to an equivalent sampling frequency of $f_s = f_c$ using a polyphase interpolation filter with four parallel paths. This enforces a digital hardware clock frequency of $f_c/4$ (between 100 and 250 MHz depending on f_c) for the interpolation filter, DSM and select and combine logic. For carriers above 1 GHz and up to 2.4 GHz, the sampling frequency is half of f_c and the RF waveform is given

$$P^*_{n\,\text{even}}(f) = \sum_{n=1}^{\infty} \frac{n\pi}{2}\delta(f-nf_r) * \left[\left|\sin\left(\frac{n\pi}{2}\alpha\right)\right| \left|J_0(B(t))\right|_{\max} + \left|\cos\left(\frac{n\pi}{2}\alpha\right)\right| \sum_{k=1}^{\infty} \left|J_{2k-1}(B(t))\right|_{\max} \delta(f-(2k-1)f_c) + \left|\sin\left(\frac{n\pi}{2}\alpha\right)\right| \sum_{k=1}^{\infty} \left|J_{2k}(B(t))\right|_{\max} \delta(f-(2k)f_c) \right] \quad (20)$$

$$P^*_{n\,\text{odd}}(f) = \sum_{n=1}^{\infty} \frac{n\pi}{2}\delta(f-nf_r) * \left[\left|\cos\left(\frac{n\pi}{2}\alpha\right)\right| \left|J_0(B(t))\right|_{\max} + \left|\cos\left(\frac{n\pi}{2}\alpha\right)\right| \sum_{k=1}^{\infty} \left|J_{2k}(B(t))\right|_{\max} \delta(f-2kf_c) - \left|\sin\left(\frac{n\pi}{2}\alpha\right)\right| \sum_{k=1}^{\infty} \left|J_{2k-1}(B(t))\right|_{\max} \delta(f-(2k-1)f_c) \right] \quad (21)$$

by the word w_{high} as in

$$w_{\text{high}} = [I_0;\, Q_0;\, \overline{I_0};\, \overline{Q_0};\, I_1;\, Q_1;\, \overline{I_1};\, \overline{Q_1};\, I_2;\, Q_2;\, \overline{I_2};\, \overline{Q_2};\, I_3;\, Q_3;\, \overline{I_3};\, \overline{Q_3}] \quad (23)$$

In this case, the equivalent sampling rate varies between 500 and 1200 MHz (four parallel paths), and the logic clock will be between 150 and 300 MHz depending on f_c. The DSM stage is built with two parallel modulators, one for each of I and Q datapath, with polyphase implementation of a first-order modulator with four parallel paths. The DSM hardware runs with the same clock as the interpolation filter, being able to process up to 1200 Ms/s. The output will be a parallel word of 4 b for each modulator correspondent to four consecutive time samples. The upconversion to the carrier frequency is done by combining the DSM outputs accordingly to a specific order, as stated in (20) or (21) subject to the carrier frequency. The word w is then serialized accordingly to the specified order. The serialization of the word is using an integrated high-speed transceiver capable of data rates up to 10 Gb/s. The transceiver's clock frequency will be either $4f_c$ or $8f_c$ depending on whether the word at the input is w_{low} or w_{high}. At the output of the serializer, the two-level signal will be centered in f_c surround by quantization noise from the DSM in the sidebands. To remove the quantization noise, an output filter at the target frequency band can be used.

Similar to the RF output signal, the proposed transceiver also uses a binary output to produce the reference waveform for the receiver. In this case, a baseband PWM is used to generate a triangular wave at the specified reference frequency, varying between 4 and 30 MHz. The signal is filtered with a low-pass filter to recover the required waveform by removing the PWM quantization noise. The reference signal is compared with the input RF signal using the FPGA high-speed differential input buffers as a comparator. This comparator is followed by a register working at 10 GHz of sampling frequency, generating a digital bitstream that will be deserialized by a factor of N, as shown in Fig. 11. Therefore, the sampled PWM waveform arrives at the remaining FPGA logic at f_s/N, with $N = 64$. Then, the RF data have to be downconverted to baseband, filtered, and decimated. The downconversion and the filtering are performed using a polyphase digital direct synthesizer and a polyphase filter, in this case with $N = 64$ parallel branches. After the DDC, the signal is transferred to the local PC via an Ethernet connection, where the baseband data are demodulated and analyzed for its EVM.

IV. Measurement Results

The transceiver performance was measured in terms of signal quality for both the transmitted and received signals. The figure of merit used to evaluate the signal quality is the EVM using two different signals 16-QAM and 64-QAM, with 2 and 5 MHz of symbol rate, both generated using a root raised cosine filter with a roll-off of 0.22, which implies a channel bandwidth of 2.44 and 6.1 MHz. The following sections show the performance results for the isolated transmitter (Figs. 12 and 13), isolated receiver (Fig. 14), and transceiver point-to-point configuration.

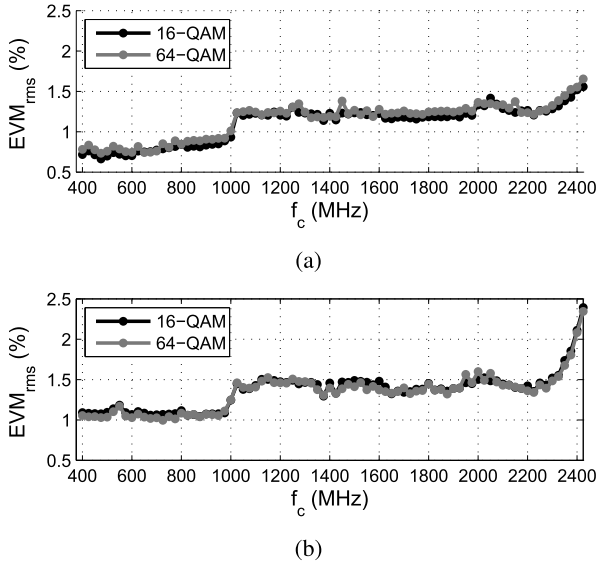


Fig. 12. Transmitter EVM using 16-QAM and 64-QAM signals. (a) 2-MHz bandwidth signal. (b) 5-MHz bandwidth signal.

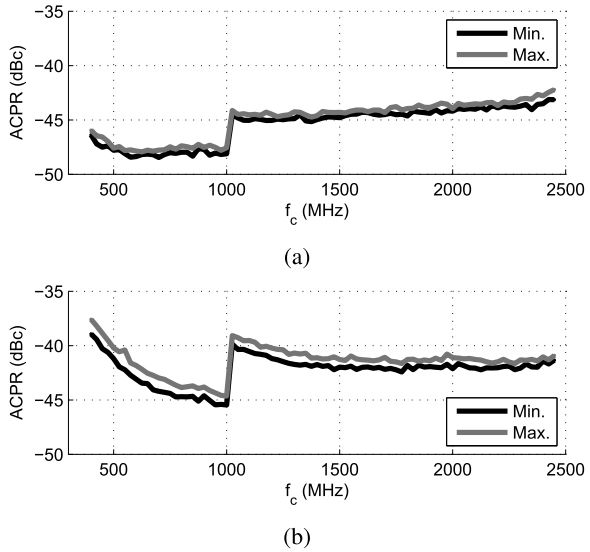
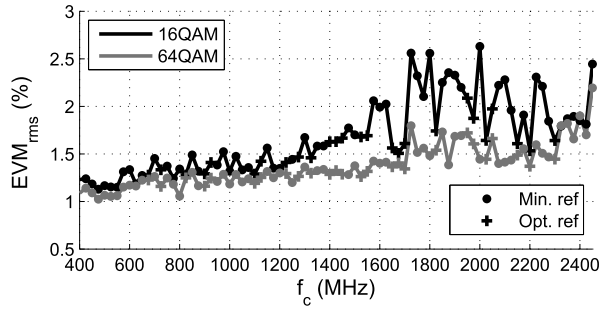


Fig. 13. Transmitter ACPR measurement. (a) 2-MHz bandwidth channels. (b) 5-MHz bandwidth channels.

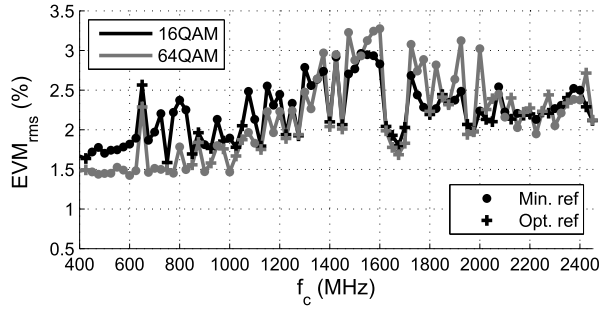
A. Transmitter

The transmitter performance was measured in terms of SNR performing a sweep over the carrier frequencies between 400 MHz and 2.425 GHz with a step of 25 MHz. The measurement setup was assembled, as shown in Fig. 15. In Fig. 12(a) and (b), the EVM results are shown for a 2- and 5-MHz symbol rate. The results show that for the tested modulations and symbol rates, the EVM along the measured carrier frequencies is always inferior to 2.5%.

The adjacent channel power ratio (ACPR) was measured for both the 2- and 5-MHz channels along the tested carrier frequencies. The measured ACPR values are shown in Fig. 13, and the maximum and minimum values correspond to the best and worst ACPR scenarios considering the tested modulation of 16-QAM and 64-QAM. Both the lower and upper channels were measured for every frequency and the worst case was considered as the ACPR value for that carrier frequency.



(a)



(b)

Fig. 14. Receiver EVM measurement. (a) 2-MHz symbol rate signal. (b) 5-MHz symbol rate signal.

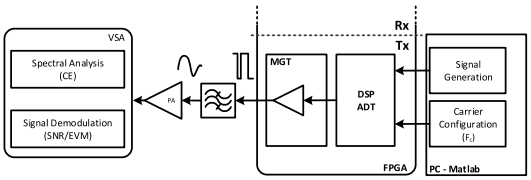


Fig. 15. Block diagram of the transmitter measurement setup.

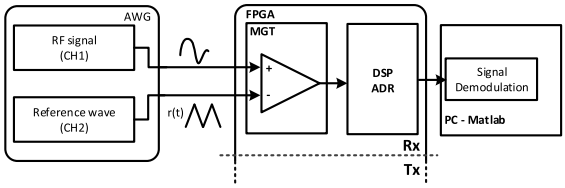


Fig. 16. Block diagram of the receiver measurement setup.

The CE for the transmitted signal of 16-QAM and 64-QAM was also measured and was found to vary between 15% and 22% depending on the PAPR of the signal. The EVM variation around 1 GHz occurs due to the change from w_{low} to w_{high}, which presents worst jitter behavior. The EVM change around 2.4 GHz, however, appears because the DSM reaches its maximum clock operation and starts to present errors. Nonetheless, these results demonstrate the viability for this transmitter to be used over the measured frequencies.

B. Receiver

The receiver performance was measured performing a sweep over the carrier frequency from 400 up to 2400 MHz with a step of 25 MHz considering the setup shown in the block diagram of Fig. 16. A two channel arbitrary waveform generator (AWG7000A from Tektronix) is directly connected to the receiver and is responsible to generate both the reference and RF signals. For each carrier frequency, the reference signal frequency was previously optimized, considering the algorithm described in Section III.

The EVM sweep results for 2- and 5-MHz symbol rate signals are shown in Fig. 14(a) and (b). In both these sweeps, it is possible to see the points that were measured using the minimum reference and optimized reference. The use of the optimized reference allows for the EVM to maintain relatively constant value for the swept carrier frequencies, despite of the PWM folded harmonics. Regarding the 2-MHz signal, it was possible to reach an EVM below 2.7% for the entire bandwidth.

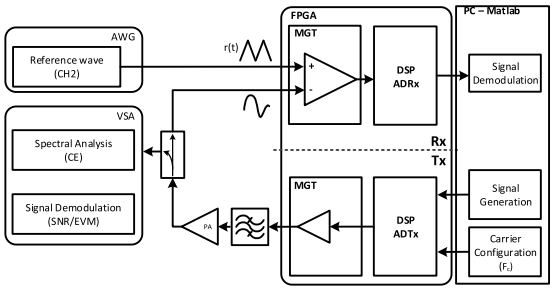


Fig. 17. Block diagram of the transceiver loop-back measurement setup.

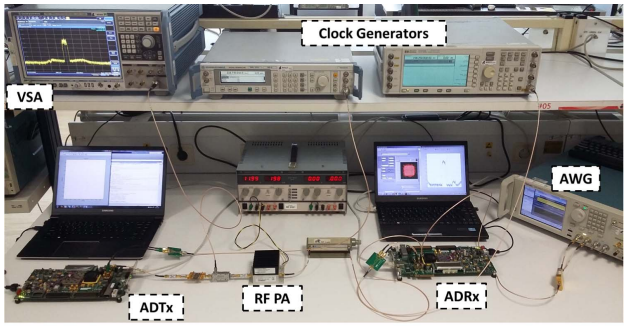


Fig. 18. Measurement setup photograph.

C. Full System Transceiver

The implemented all-digital transceiver was tested in a Tx/Rx point-to-point configuration for some frequency bands of interest and feasible with the proposed architecture. For this measurement, the transmitted signal is filtered by a bandpass filter, and is sent directly to the receiver that acquires the signal. Then, after the DDC, the signal quality is analyzed in terms of EVM. Simultaneously, the signal is also analyzed and demodulated in a VSA, in order to have a reference EVM measurement for the transmission. The measurement setup is shown in Fig. 17. Fig. 18 presents a photograph of measurement setup. In addition, Fig. 19 shows the spectrum of the transmitted and the received signals at 1850 MHz. In the latter, it is possible to observe the PWM distortion around the carrier frequency.

The test signals are 64-QAM with a 2- and 5-MHz sampling rate varying the carrier frequency over the selected bands with

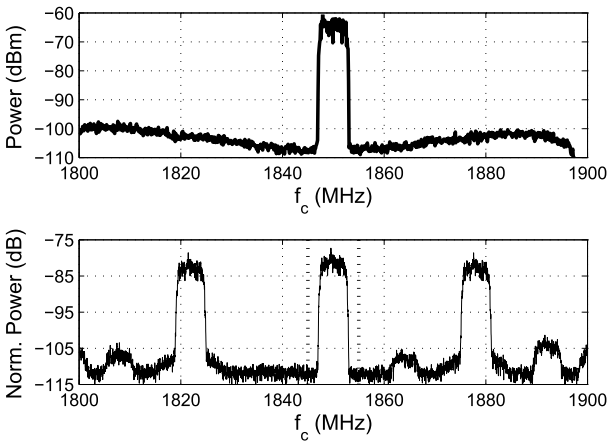


Fig. 19. Top: spectral capture of the transmitted signal with a VSA. Bottom: RF received signal at the all-digital receiver.

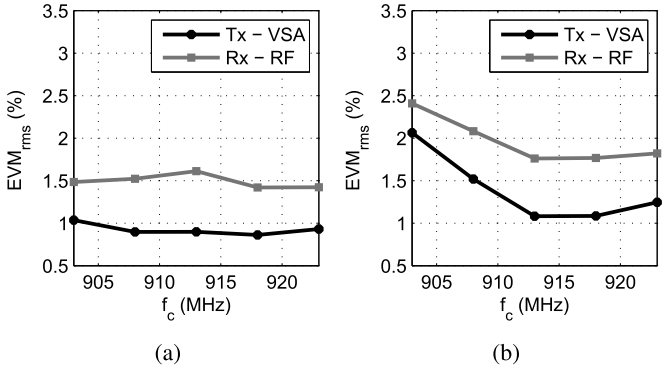


Fig. 20. Measurement over the 900-MHz ISM band. (a) Using a 2-MHz 64-QAM signal. (b) Using a 5-MHz 64-QAM.

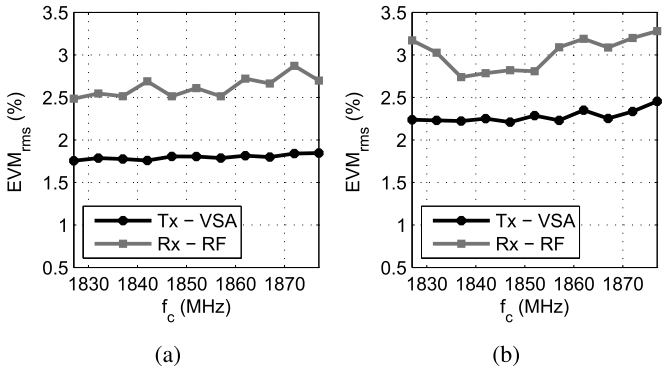


Fig. 21. Measurement over the 1800-MHz LTE band. (a) Using a 2-MHz 64-QAM signal. (b) Using a 5-MHz 64-QAM.

a step of 5 MHz. Fig. 20 shows a sweep over f_c in the 900-MHz ISM band starting on 903 and up to 923 MHz. Fig. 21 shows a sweep over f_c in the 1800-MHz LTE band starting on 1827 and up to 1881 MHz. The presented measurements show the feasibility of the proposed transceiver architecture for some of common frequency bands.

Finally, an overall comparison between the proposed architecture and other similar state-of-the-art transceivers must be considered. However, since this is the first time, such an architecture is presented, and this comparison can only be done to the transmitter and receiver independently with the respective state-of-the-art architectures.

The proposed transmitter uses polyphase architecture as presented in [18], which is in line with the state-of-the-art figures of merit in terms of bandwidth, SNR, and CE. However, the transmitter architecture was designed to allow for fast carrier frequency flexibility, and in fact, this is the first time that such a large set of carrier frequencies were tested showing the feasibility and functionality of this transmitter for those frequencies.

On the receiver side, the same carrier frequencies were also tested presenting reasonable results. When comparing this system with [23], focusing on the 5-MHz signals, there were improvements in terms of SNR/EVM. Despite the fact that in [23], the PWM sampling is two times superior to 10 GHz used in this paper, the proposed technique allowed to obtain an EVM lower than 3.5%, whereas in [23], the presented EVM is about 6%. Moreover, when comparing this paper with [24], an improvement was also obtained. Both the previous improvements are due to the new technique for selecting the reference frequency.

In order to consider a receiver evaluation in terms of sensitivity and dynamic range, the LNA/VGA should be mandatorily included, which is out of the scope of this paper. However, it is possible to get an estimation of the instantaneous dynamic range transposing the EVM values into SNR by applying the formulation presented in [33]. Therefore, considering that the best and the worse obtained EVM values are, respectively, 1% and 3.5%, by applying the previous formulation it is possible to get an SNR of 40 and 30 dB. Hence, this leads to an indicative value of the receiver instantaneous dynamic range.

V. Conclusion

In this paper, it was presented for the first time a fully integrated single FPGA-based all-digital RF transceiver, which marks a breakthrough in digital RF system design. The entire signal processing from the baseband up to the RF stage for the transmitter, and the opposite for the receiver, is completely performed in the digital domain. The transmitter chain of the radio is implemented recurring to DSM modulation and the receiver based on PWM modulation, which was optimized with a nonlinear analysis of its behavior.

The proposed system presents high flexibility in a bandwidth of almost 2.5 GHz while maintaining reasonable EVM results for 2- and 5-MHz symbol rate signals. The obtained results make this system highly suitable for the future radio transceivers, specifically focusing on the integration of previous standards that operated in sub-2.5-GHz bands. An FPGA was used as an implementation proof of concept, due to its faster verification and deployment capability. Nevertheless, an application specific integrated circuit could be built following the proposed architecture. However, due to the FPGA's reconfigurability capabilities, it adds an increase degree of flexibility required by SDR applications.

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R. F. Cordeiro (S'12) received the M.S. degree in electronic engineering from the University of Aveiro, Aveiro, Potugal, where he is currently pursuing the Ph.D. degree in electrical engineering under the Doctoral Program.

He was with the Telecommunications Institute, Aveiro, where he performed researching activities under the subjects of reconfigurable embedded systems, digital signal processing, wireless communications, and software defined radio. He is currently with Bosch Car Multimedia, Hildesheim, Germany, where he performs hardware development activities in the area of automotive wireless communications.

André Prata (S'13) was born in Santa Comba Do, Portugal, in 1990. He received the M.Sc. degree in electronics and telecommunications engineering from the Universidade de Aveiro, Aveiro, Portugal, in 2013, where he is currently pursuing the Ph.D. degree in electrical engineering.

His current research interests include software defined radio, mixed-signal systems, and digital signal processing.

Mr. Prata was a recipient of the 2013 IEEE Microwave Theory and Techniques Society International Microwave Symposium Undergraduate Software Defined Radio and Digital Signal Processing Student Design Competition.

Arnaldo S. R. Oliveira (M'10) received the B.Sc. and M.Sc. degrees in electronics and telecommunications from the University of Aveiro, Aveiro, Portugal, and the Ph.D. degree in electrical engineering from the University of Aveiro, in 2007.

Since 2001, he has been teaching computer architecture, digital systems design, programming languages, and embedded systems with the University of Aveiro, where he is currently an Assistant Professor. He is also a Researcher with the Telecommunications Institute, Aveiro. He participates in several national and European funded research projects. He has authored or co-authored over 80 journal and international conference papers. His current research interests include reconfigurable digital systems, software-defined radio, and next-generation radio access networks.

José M. N. Vieira received the B.Sc. degree in electrical engineering and M.Sc. degree in systems and automation from the University of Coimbra, Coimbra, Portugal, in 1988 and 1993, respectively, and the Ph.D. degree in electrical engineering from the University of Aveiro, Aveiro, Portugal, in 2000.

Since 2000, he has been an Assistant Professor with the University of Aveiro. In 2004, he founded the AES Portuguese Section, where he was the President from 2005 to 2011. His current research interests include digital audio signal processing, ultrasonic location, software-defined radio, and all-digital radio front-ends.

Dr. Vieira was the recipient of the Plug Award from APRITEL with the Bioinspired Cochlear Radio in 2010.

N. B. De Carvalho (S'97–M'00–SM'05–F'15) was born in Luanda, Angola, in 1972. He received the Diploma and Ph.D. degrees in electronics and telecommunications engineering from the University of Aveiro, Aveiro, Portugal, in 1995 and 2000, respectively.

He is currently a Full Professor and a Senior Research Scientist with the Institute of Telecommunications, University of Aveiro. He co-authored *Intermodulation in Microwave and Wireless Circuits* (Artech House, 2003), *Microwave and Wireless Measurement Techniques* (Cambridge Univ. Press, 2013), and *White Space Communication Technologies* (Cambridge Univ. Press, 2014). He co-invented four patents. His current research interests include software-defined radio front-ends, wireless power transmission, nonlinear distortion analysis in microwave/wireless circuits and systems, measurement of nonlinear phenomena, design of dedicated radios, and systems for newly emerging wireless technologies.

Dr. De Carvalho was a recipient of the 1995 University of Aveiro and the Portuguese Engineering Association Prize for the Best 1995 Student at the University of Aveiro, the 1998 Student Paper Competition (Third Place) of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS), and the 2000 IEE Measurement Prize. He has been a Reviewer and an author of over 200 papers in magazines and conferences. He is an Associate Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, *IEEE Microwave Magazine*, and the *Cambridge Wireless Power Transfer Journal*. He is the Co-Chair of the IEEE MTT-20 Technical Committee and the Past-Chair of the IEEE Portuguese Section and MTT-11. He also belongs to the Technical Commitees, MTT-11, MTT-20, and MTT-26. He is also the Chair of the URSI-Portugal Metrology Group.