

Gowin FPGA Offline Programmer **User Guide**

UG291-1.1E,07/15/2019

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Revision History

Date	Version	Description	
01/03/2018	1.0E	Initial version.	
		Description of vcc1and vcc2 voltage	
07/15/2019	1.1E	configuration added;	
		Selection of verification added.	

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1About This Guide 1.1Purpose

1 About This Guide

1.1 Purpose

This guide includes two parts:

- 1. How to use FPGA offline programmer;
- 2. Description of Programmer functions.

1.2 Supported Products

The programmer in the guide applies to the following products: GW1N-1, GW1N-2/2B, GW1N-4/4B, GW1NR-4/4B, GW1NR-9, and GW1NR-9.

Note!

The corresponding data stream files are respectively named as GW1N1.fs, GW1N2.fs, GW1N4.fs, and GW1N9.fs.

1.3 Related Documents

The latest user guides are available on our Website. Refer to the related documents at www.gowinsemi.com:

- 1. UG107, GW1N-1 Pinout
- 2. <u>UG105</u>, GW1N-2&2B&4&4B Pinout
- 3. UG114, GW1N-6&9 Pinout
- 4. DS117, GW1NR series FPGA Products Data Sheet
- 5. UG116, GW1NR-4&4B Pinout
- 6. <u>UG801</u>, GW1NR-9 Pinout

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1.4 Terminology and Abbreviation

The terminology and abbreviations used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Terminology and Abbreviation	Meaning	
DFU	Device Firmware Upgrade	
FPGA	Field Programmable Gate Array	
JTAG	Joint Test Action Group	
ID	Identification	

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com
E-mail:support@gowinsemi.com

+Tel: +86 755 8262 0391

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2FPGA Offline Programmer Instructions

2.1 Overview

Offline programmer is a device that offline programs GW1N(R) chips. It has the features of data confidentiality, portability, multi-path programming, etc. It is suitable for rapidly large-volume production at the factory and is convenient for maintenance personnel to carry out. The offline programmer can simultaneously program four FPGA devices, and automatically detect device access and program in a single interface, which greatly increases the mass production rate.

The offline programmer encrypts and saves the data using an AES-128 advanced encryption algorithm, and the key is saved after several times of encrypting. AES is a set of internationally recognized, commonly used and secure encryption standards that ensure securely delivering data.

2.2 Offline Programmer Instructions

The offline programmer can be configured and managed using the offline programmer software, such as data stream file management, upper burner count management, and writer firmware upgrade. The software supports Windows 7 and above operating systems. After configuration, the offline programmer can be connected to the FPGA to program.

2.2.1 Software Download and Driver Installation

The relevant software and driver package can be downloaded at Gowin website or contact the sales for help. Install the driver and the path is https://www.gowinsemi.com/en/support/devkits_detail/7/. After installation, use USB cable to connect the programmer and computer, and USB Serial Port(COMxx) appears on the port, that is, the driver is installed successfully, as shown in Figure 2-1.

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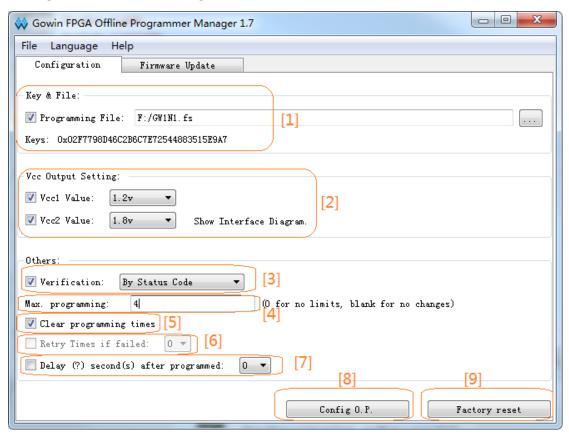
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Figure 2-1 Driver Installed Information

2.2.2 Configuration Interface

OPmanager.exe is the associated software in the "bin" directory. Open OPmanager.exe, and the configuration options are shown in Figure 2-2. Figure 2-2 Software Configuration Interface



- 1. Programming File: The selected one is GW1N1.fs. Open the management tool and generate the key randomly, encrypt the data stream files and store them in the programmer.
- 2. Vcc1 voltage is set as1.2v, Vcc2 is set as 3.3v. The supported voltages are: 1.0v, 1.2v, 1.5v, 1.8v, 2.0v, 2.5v, 3.3v.
- 3. Verification: Options are the status code, read-back, or no verification.

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Note!

- Status code: Determine whether the programming is successful or not according to the status code read from the FPGA after finishing programming data stream files.
- Read-back: Determine whether the programming is successful or not according to the consistency of writing and reading after finishing programming data stream files.
- No verification, that is, only prompts the completion of programming.
- 4. The max. programming times: If it sets 100, "programming times: Error" will pop up on the LCD of the offline programmer if the programming times are greater than 100.
- 5. Clear programming times: Check to clear programming times.
- 6. Retry times if failed: Retry x times automatically if failed, and error will be reported if x times failed.

Note!

1.5 version does not support the setting for the time being.

- 7. Delay after programmed: Delay x seconds after programmed, indicating the result of programming.
- 8. Configure to programmer: Configure the checked information items to programmer.
- 9. You can clear the configured data stream file, secret key, programming times, and the upper limit value of programming times via resetting factory data.

2.2.3 Configure to Programmer

The associated software is required to configure the programmer. Open the OPManaer.exe software to configure it, as shown in Figure 2-3. The configuration steps are as follows:

- 1. Select the data stream file (.FS).
- 2. Select 1.2v as Vcc1.
- 3. Verification selection: No verification.
- 4. Set the max. programming times or leave it blank.
- 5. Click the "Configure to Programmer" button.
- 6. Restart the programmer after configuration.

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_ 0 X File Language Help Configuration Firmware Update Key & File: ▼ Programming File: F:/GW1N1.fs Keys: 0x02F7798D46C2B6C7E72544883515E9A7 Vcc Output Setting: Vcc1 Value: 1.2v • ▼ Vcc2 Value: 1.8v • Show Interface Diagram. Others: Verification: By Status Code Max. programming: (O for no limits, blank for no changes) ✓ Clear programming times ☐ Retry Times if failed: 0 ▼ Delay (?) second(s) after programmed: Config O.P. Factory reset

Figure 2-3 Software Configuration Interface

2.2.4 Program four FPGA devices Simultaneously



Figure 2-4 Programmer Exterior

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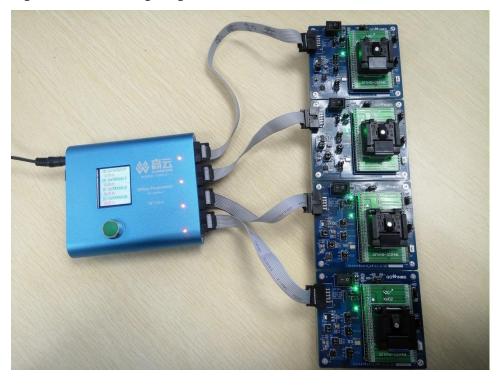


Figure 2-5 Connecting Programmer to SocketBoard

The quad JTAG programming interfaces share the TCK, TDI, and TMS signal lines. After the programmer sends commands, the four FPGA respond and can be programmed simultaneously. Operation steps of programing four FPGA devices simultaneously are as follows:

1. Programmer is powered on and start;

Note!

Support USB power supply or 5V power supply.

- 2. Connect four FPGAs to the programmer;
- Press the green Program key, the screen displays detecting the device and the corresponding ID CODE is displayed after the device is detected. The corresponding indicator turns green after the programming is done successful.

Note!

In this mode, n (<=4) FPGAs can be programmed if they are connected. The programming interfaces of 1.2.3.4 can be selected optionally.

2.2.5 Program One FPGA Automatically

In the automatic programming mode, the programmer can automatically detect the new FPGA. It will program automatically if a new FPAG is connected. Currently, automatically programming only supports one FPGA, and only interface 1 of the programmer supports detecting and programming automatically. Operation steps of programing one FPGA automatically are as follows:

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1. Programmer is powered on and start; "AUTO-PRO-MODE" will be displayed after pressing the program key for 5 seconds, and then the programmer enters the auto programming mode;

Note!

Support USB power supply or 5V power supply.

- 2. Connect one FPGA to interface 1;
- 3. The screen displays detecting the device and the corresponding ID CODE is displayed after the device is detected. The corresponding indicator turns green after the programming is done successful.
- 4. Disconnect the FPGA from the interface1, and then connect it to the interface 1 again. The programmer will automatically program the stream file to the FPGA device, and you do not need to press the green programming key.

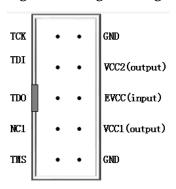
Note!

The automatic detection is used to detect whether there is a device connecting the programmer; if a device is connected, it will be programmed automatically. If not, the programmer will continue detecting and waiting for the new device.

2.3 Diagram and Description of Programmer Interface Connection

2.3.1 Programmer Interface Connection Diagram

Figure 2-6 Programming Interface Connection Diagram



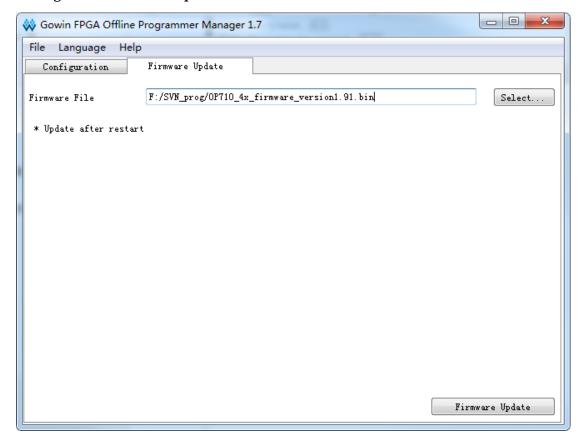
Note!

- 3.3V is the voltage outputting to the FPGA device.
- EVCC is the input voltage, which is the VCCIO voltage of the FPGA chip.
- Vcc1/2 is configurable output voltage.

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2.4 Instructions of FPGA Offline Programmer Firmware Update

Figure 2-7 Firmware Update



Connect the programmer to the PC using a USB cable, select the firmware (PROG.bin) to be updated, and click the programming update button to wait for restarting the programmer. When the prompt box appears, restart the offline programmer to complete the update. The obtaining address of the latest firmware:

https://www.gowinsemi.com/en/support/devkits_detail/7/

2.5 Notes

- 1. When multiple devices are programed simultaneously, only the same series of devices are supported. For example, all the GW1N-1 devices or all the GW1N-4 devices.
- 2. The data stream file is configured in the offline programmer. Select the FPGA to be programmed according to the screen prompt: "currently support: GW1N(R)-x", to avoid other damage to the FPGA.
- 3. When configuring the offline programmer or programing the update file, you need to manually cancel it when the progress bar is stuck at a certain progress, and then restart the programmer.

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2.6 Main features are as follows:

Power Supply

Working voltage: DC5V±10%

Power: 0.75 WOutput voltage: 3.3v

Memory

Internal memory: 8MByte

Reference time of programming

Table 2-1 Programming Time

Chip Type Supported	Programming Time (ms)
GW1N-1	5312
GW1N-2	5312
GW1N(R)-4	5312
GW1N(R)-9	6278
GW1NZ	4600
GW1NS-2	4500

Note!

- In JTAG mode, the data can be programed into the internal flash of the FPGA.
- Programming time is the total time of erasing the internal flash and successfully program the stream file into the FPGA internal flash. Program one FPGA and program four FPGAs requires the same time.

2.7 Specification and Parameter

Working environment: 0-60 ℃

Frame Size: 120 mm * 106 mm * 26 mm

Screen: distinguishability (128*160) size (32mm*38mm)

Net weight: 350g.

2.8 Error code and Troubleshooting

After programming or if programming is successful, it will prompt: Programmed successfully and displayed STA:0x1f020 or STA:0x3f020. If the device is abnormal, an error code will be reported, and the the error code corresponding to the fault information are as follows.

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Table 2-2 Error Code Corresponding to the Fault Information

Error Code	Fault Inforamtion	Troubleshooting
E01	POR error	
E02	GoWin VLD error	
E03	Device error	Detects whether the access
E04	No access device	Check whether the device is
E05	Data stream file	Reconfigure the data stream file
E06	Programming failure	Re - programming, retry 3 times

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