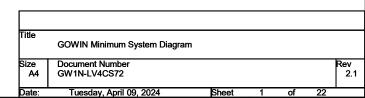
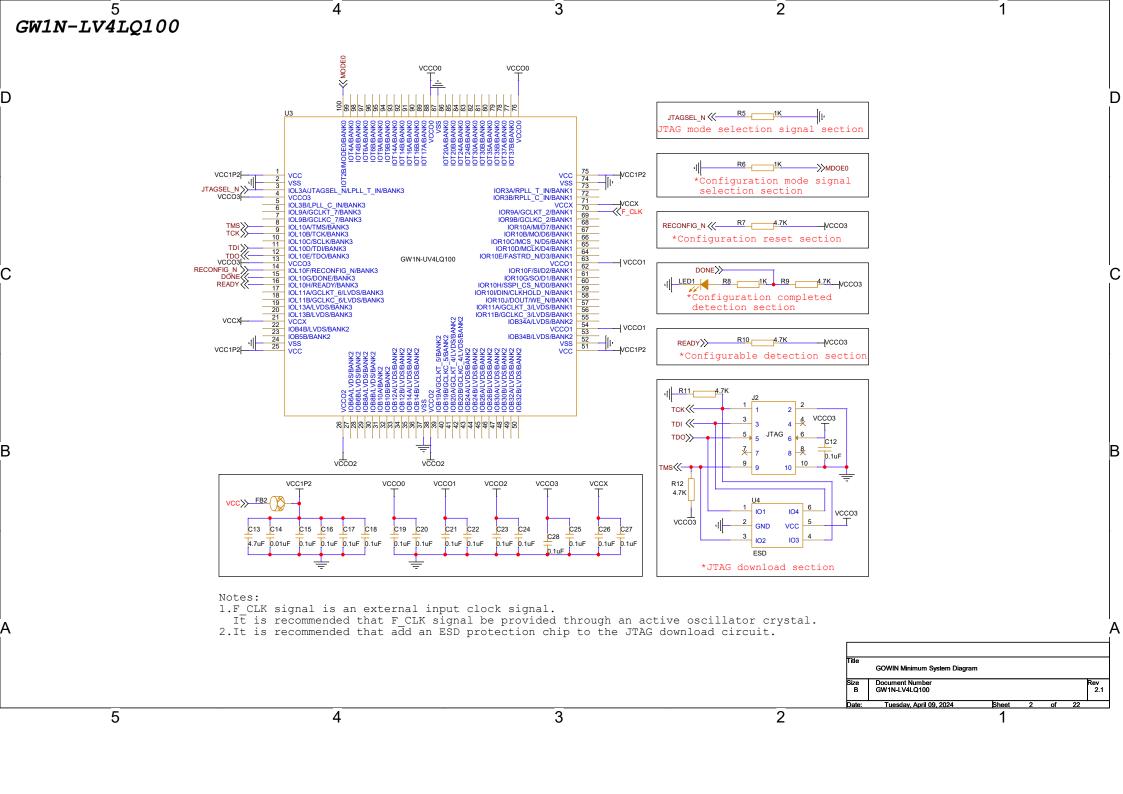
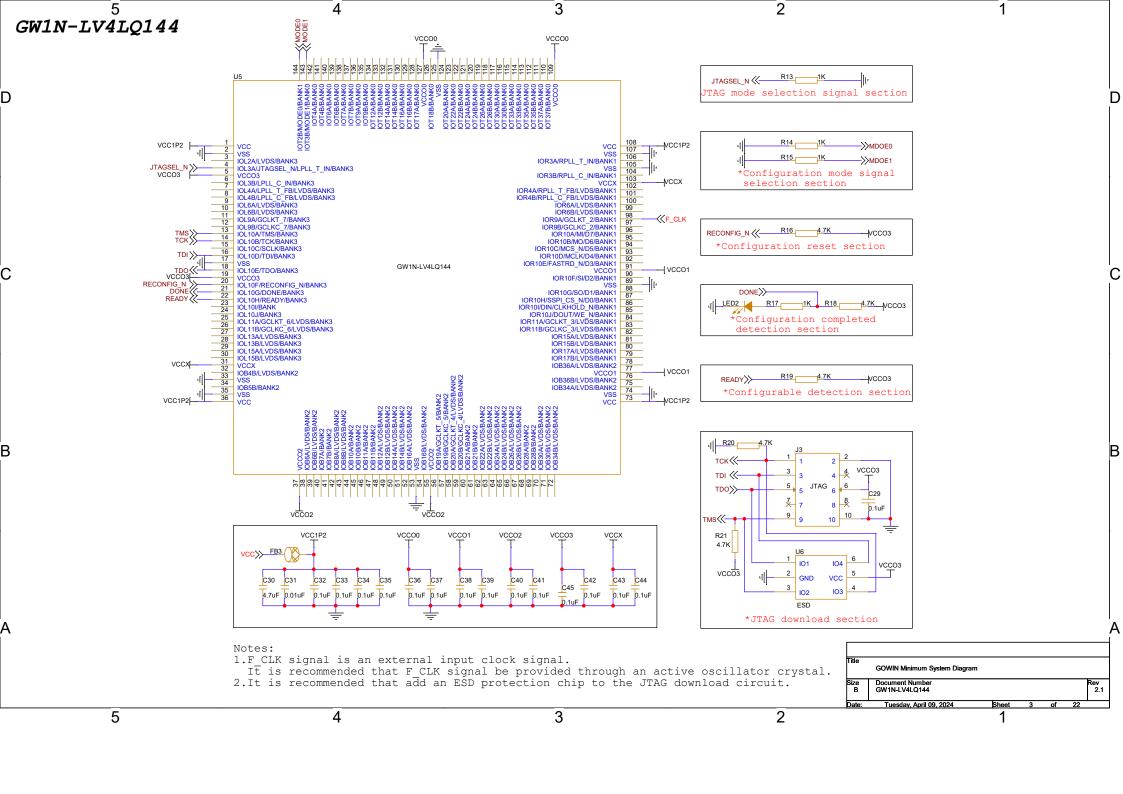
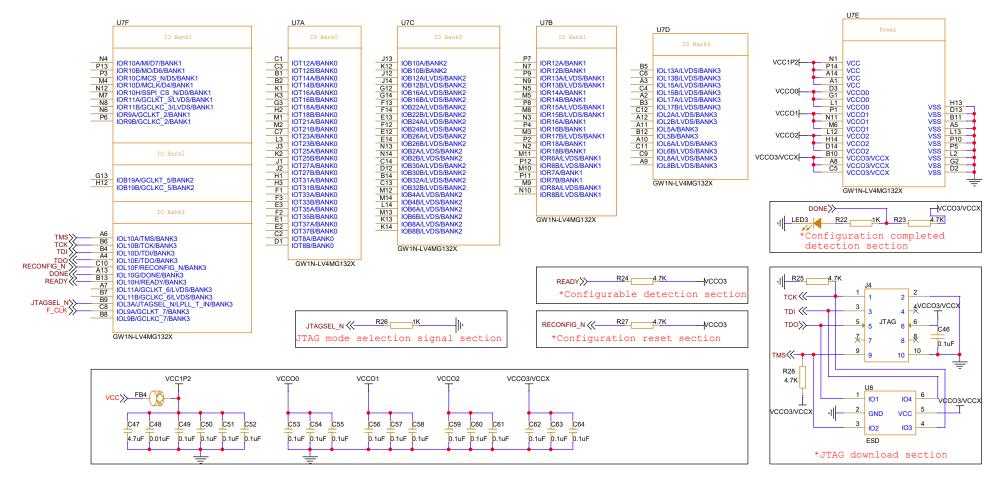


- 1.F CLK signal is an external input clock signal.
 - It is recommended that F CLK signal be provided through an active oscillator crystal.
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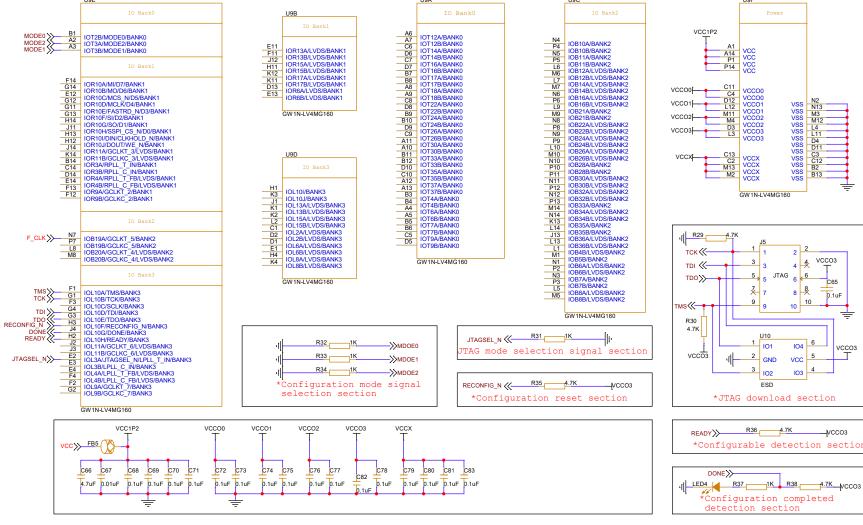
Title **GOWIN Minimum System Diagram** Document Number GW1N-LV4MG132X Rev 2.1 Tuesday, April 09, 2024

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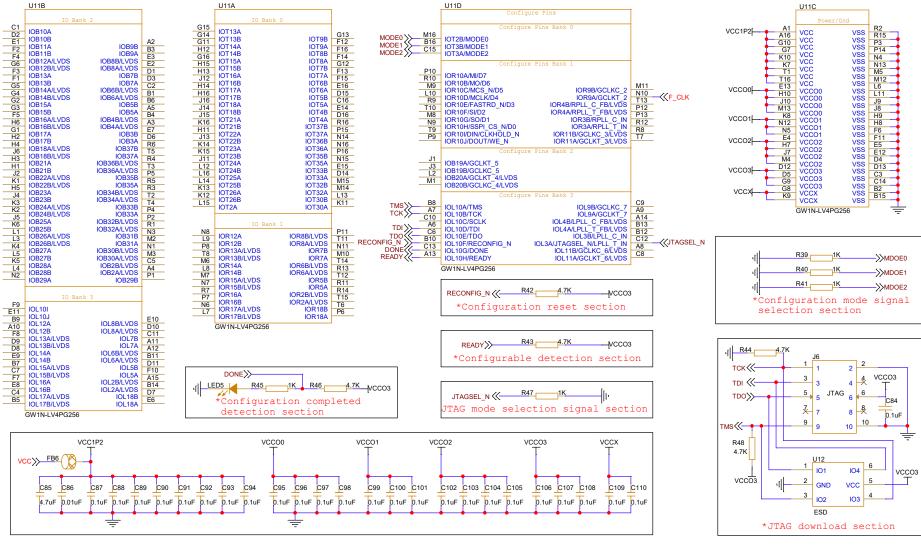
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5 3 GW1N-LV4MG160



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GOWIN Minimum System Diagram Document Number GW1N-LV4MG160 ize A3 Rev 2.1



5

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Title
GOWIN Minimum System Diagram

Size Document Number Rev 2.1

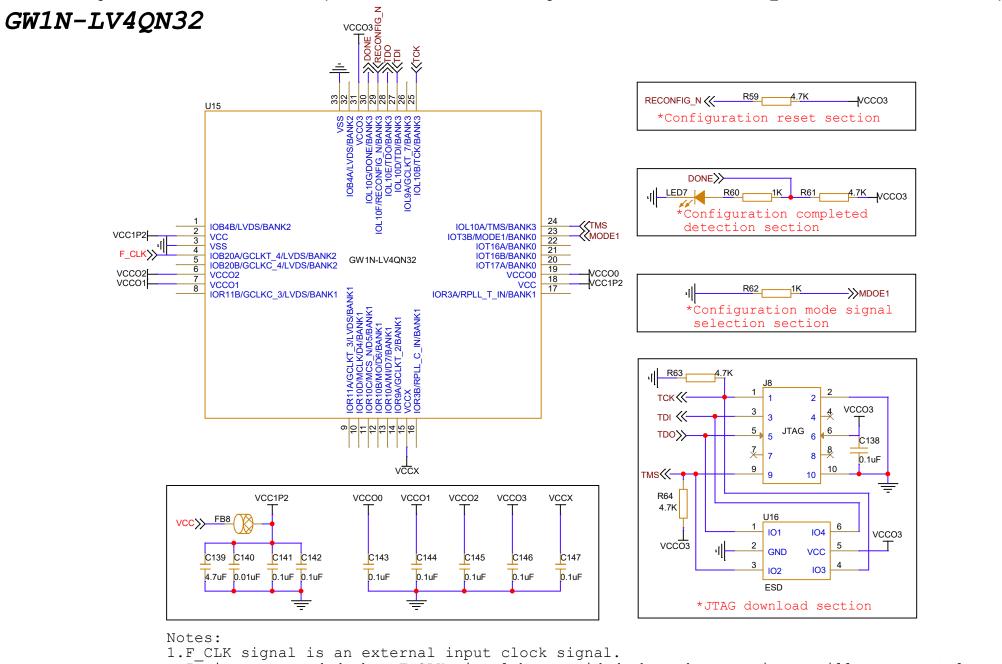
Date: Tuesday, April 09, 2024 Sheet 6 of 22

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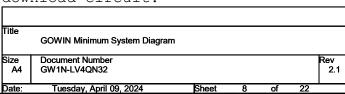
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1



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GW1N-LV4QN48 VCC1P2 RECONFIG N <<--VCCO0/3 U17 *Configuration reset section DONE VCCO0/3 *Configuration completed -VCCX VCCO0/VCCO3 **VCCX** VSS IOR3A/RPLL T IN/BANK1 detection section JTAGSEL N IOL3A/JTAGSEL_N/LPLL_T_IN/BANK3 IOR10A/MI/D7/BANK1

IOR10B/MO/D6/BANK1

IOR17A/LVDS/BANK1

IOR17B/LVDS/BANK1

VCCO1/VCCO2

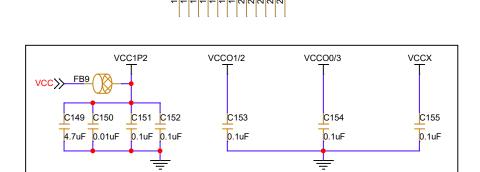
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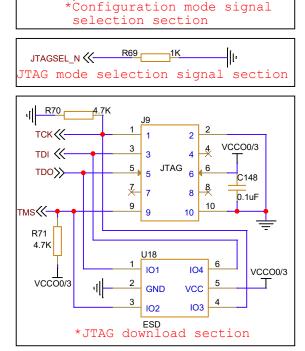
IOR10C/MCS N/D5/BANK1

IOR11A/GCLKT 3/LVDS/BANK1

IOR11B/GCLKC_3/LVDS/BANK1

IOR10D/MCLK/D4/BANK1





->>MDOE1

Notes:

TMS

TCK

TDI

DONE

VCC1P2

TDO RECONFIG N IOL10A/TMS/BANK3

IOL10B/TCK//BANK3

IOL10D/TDI/BANK3

IOL10E/TDO/BANK3

IOL10G/DONE/BANK3

IOL10F/RECONFIG_N/BANK3

IOL11A/GCLKT 6/LVDS/BANK3

IOL11B/GCLKC 6/LVDS/BANK3

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 $\langle\!\langle F_CLK \rangle$

VCCO1/2

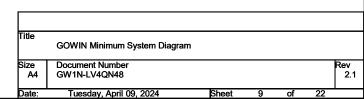
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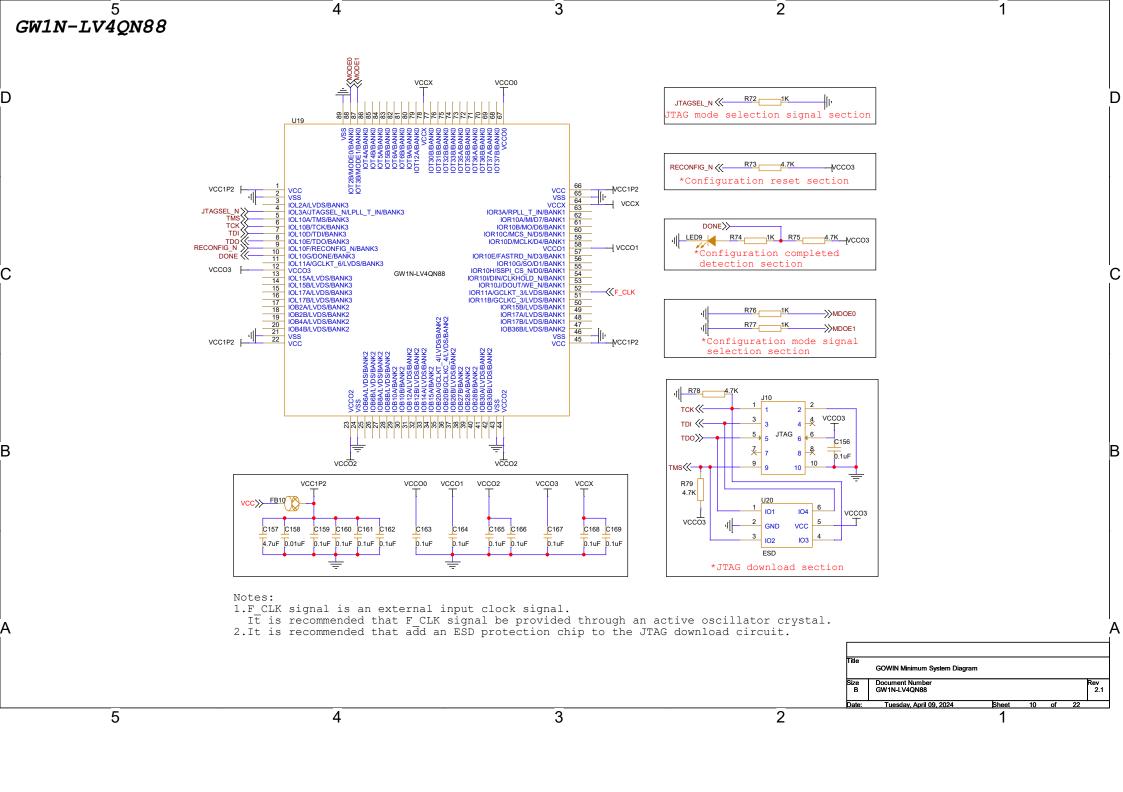
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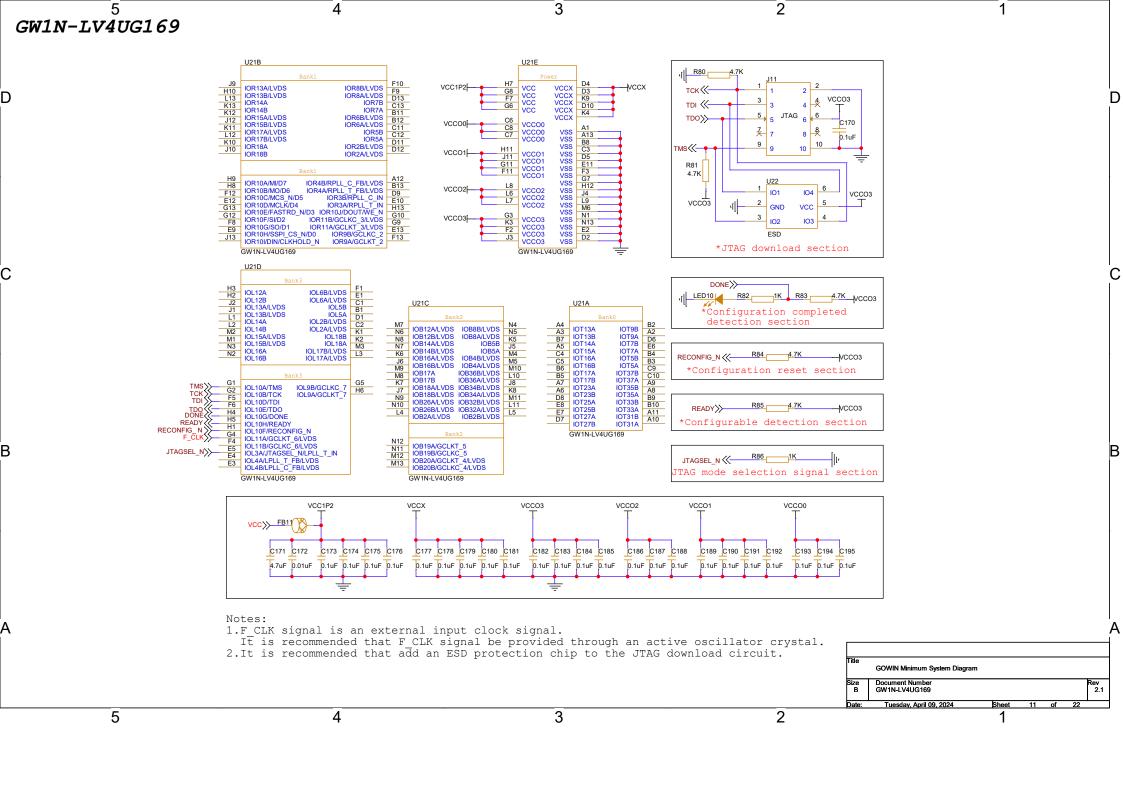
26 25

VSS

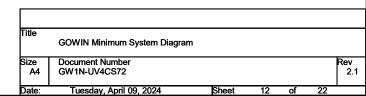
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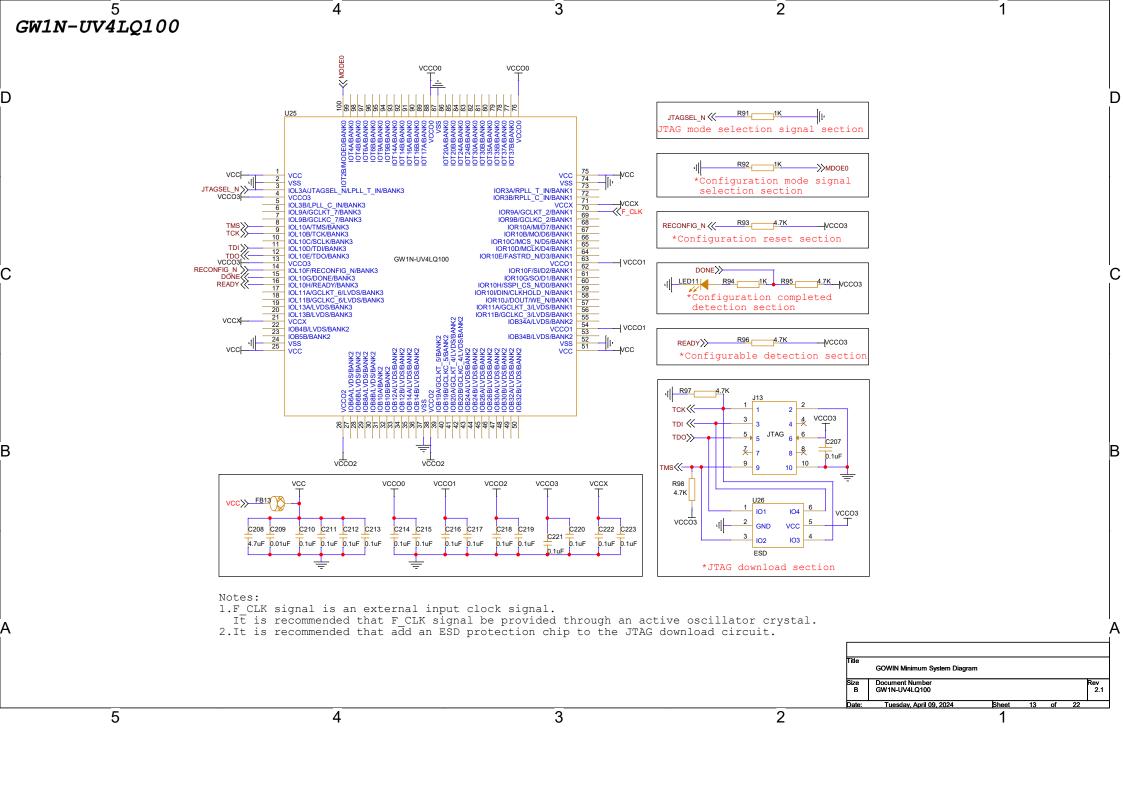


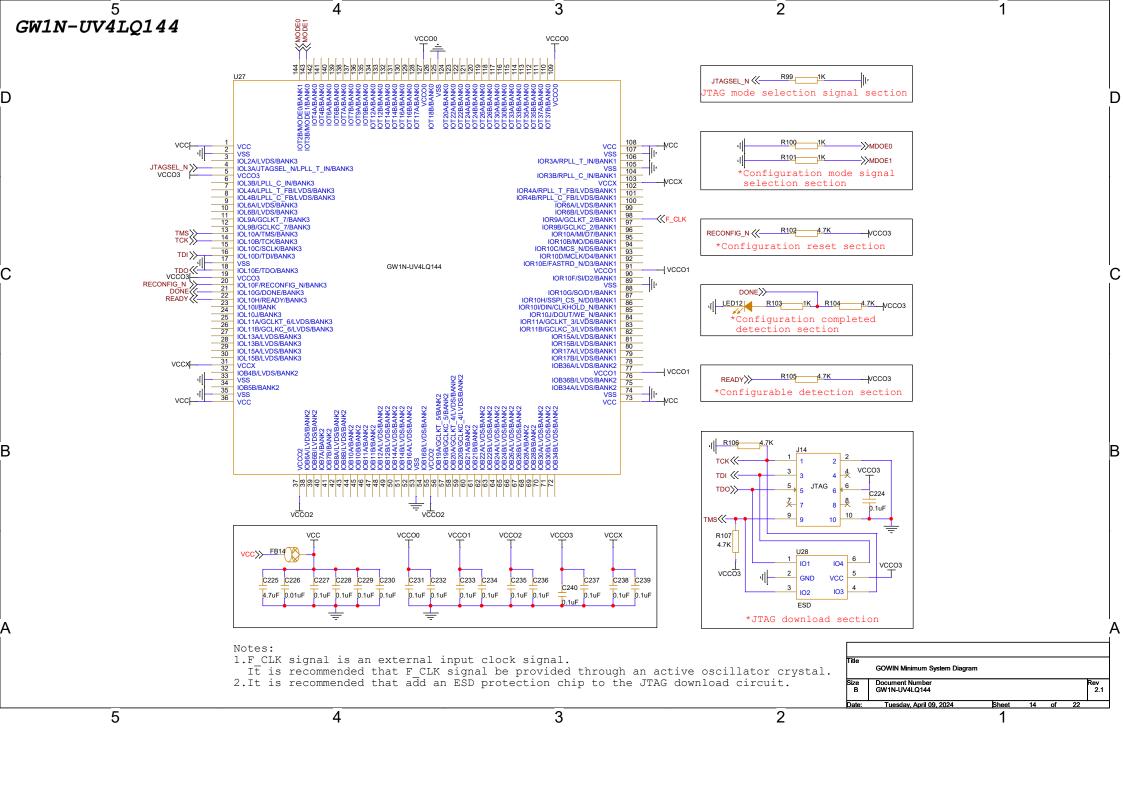


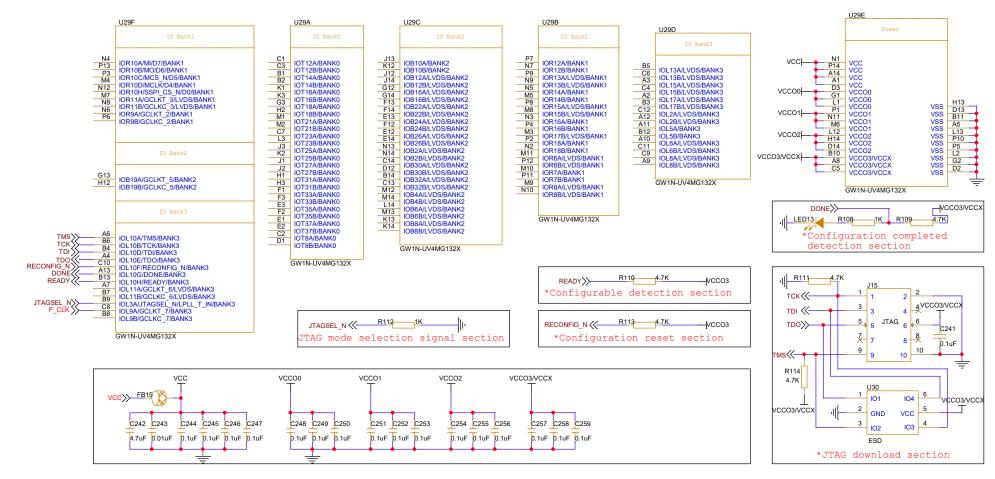


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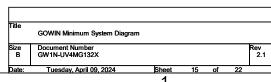






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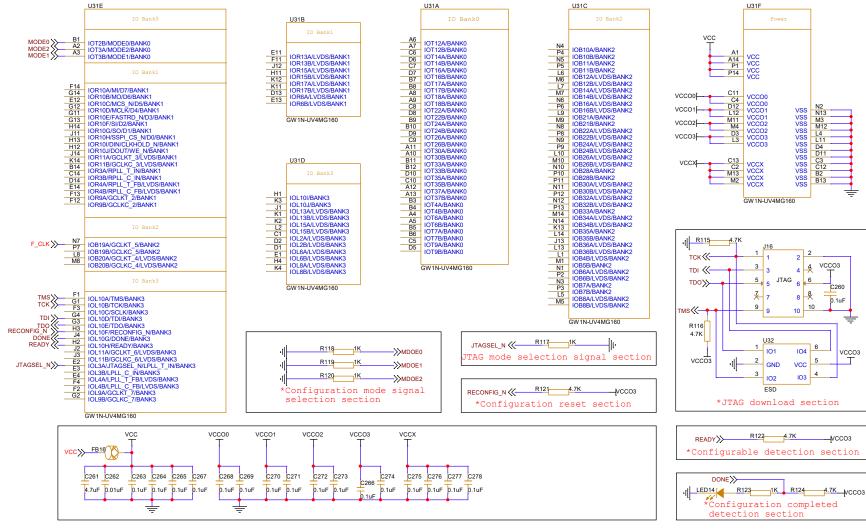


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5 3 GW1N-UV4MG160



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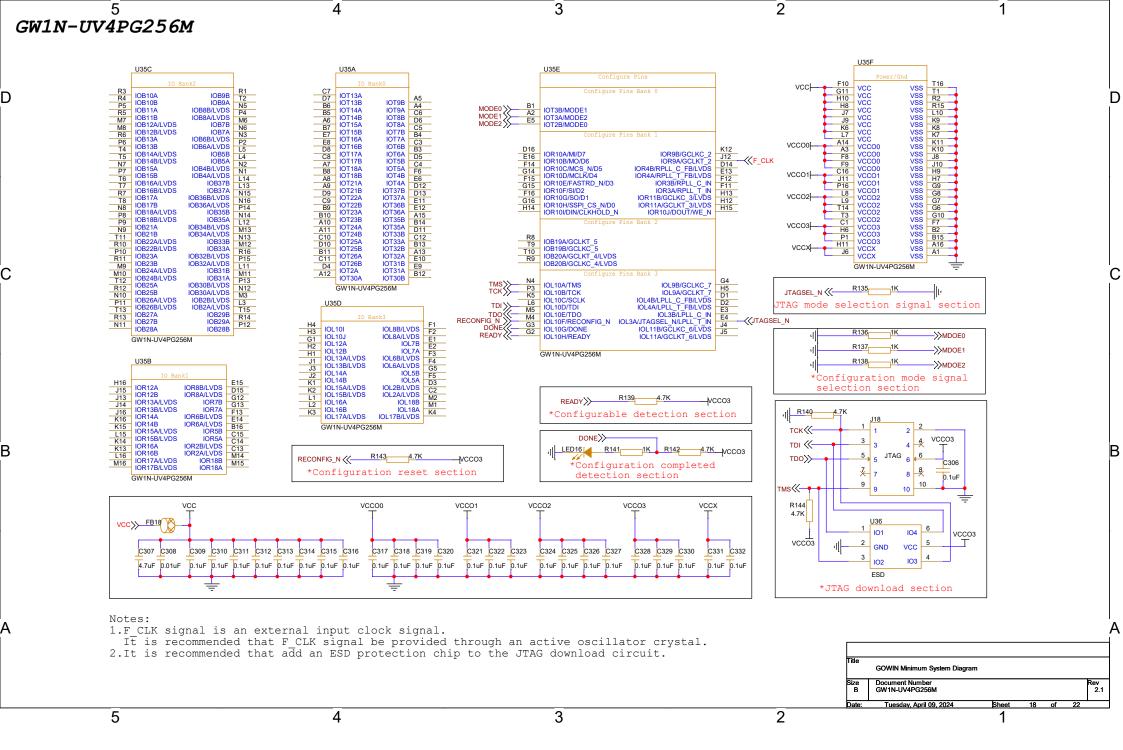
GOWIN Minimum System Diagram ize A3 Rev 2.1 GW1N-UV4MG160

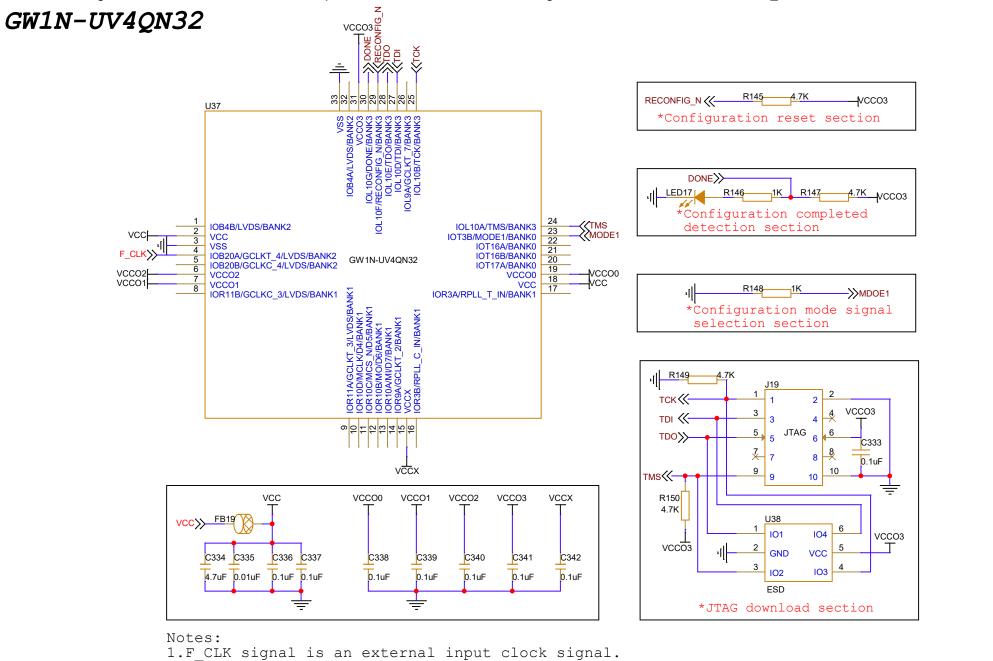
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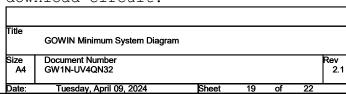
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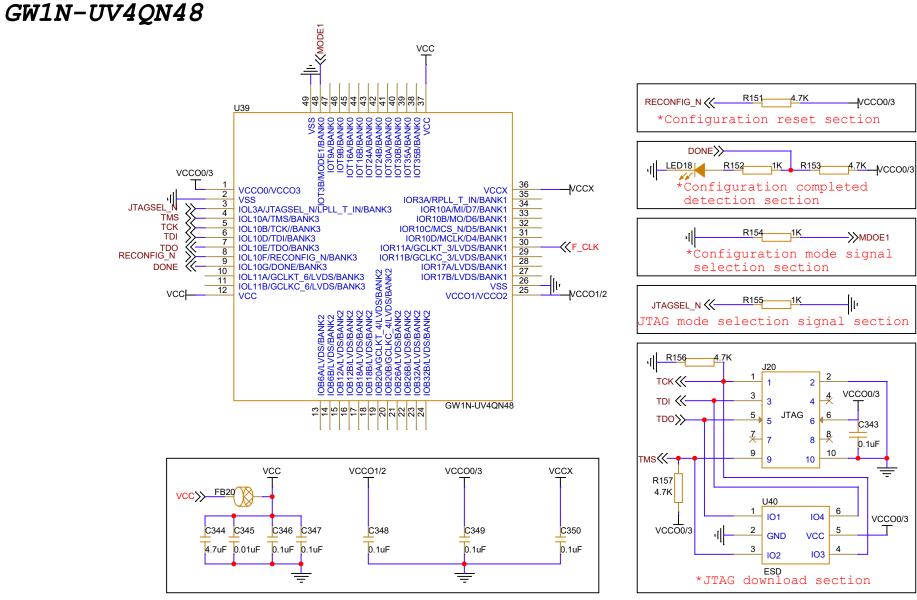
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