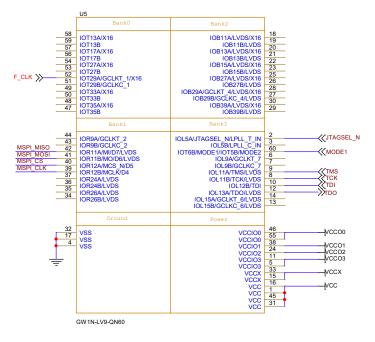
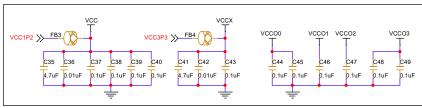
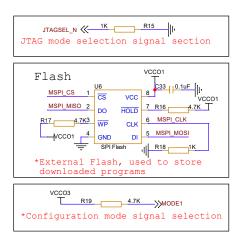
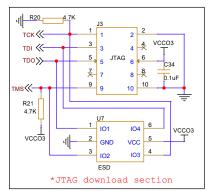


## GW1N-LV9QN60



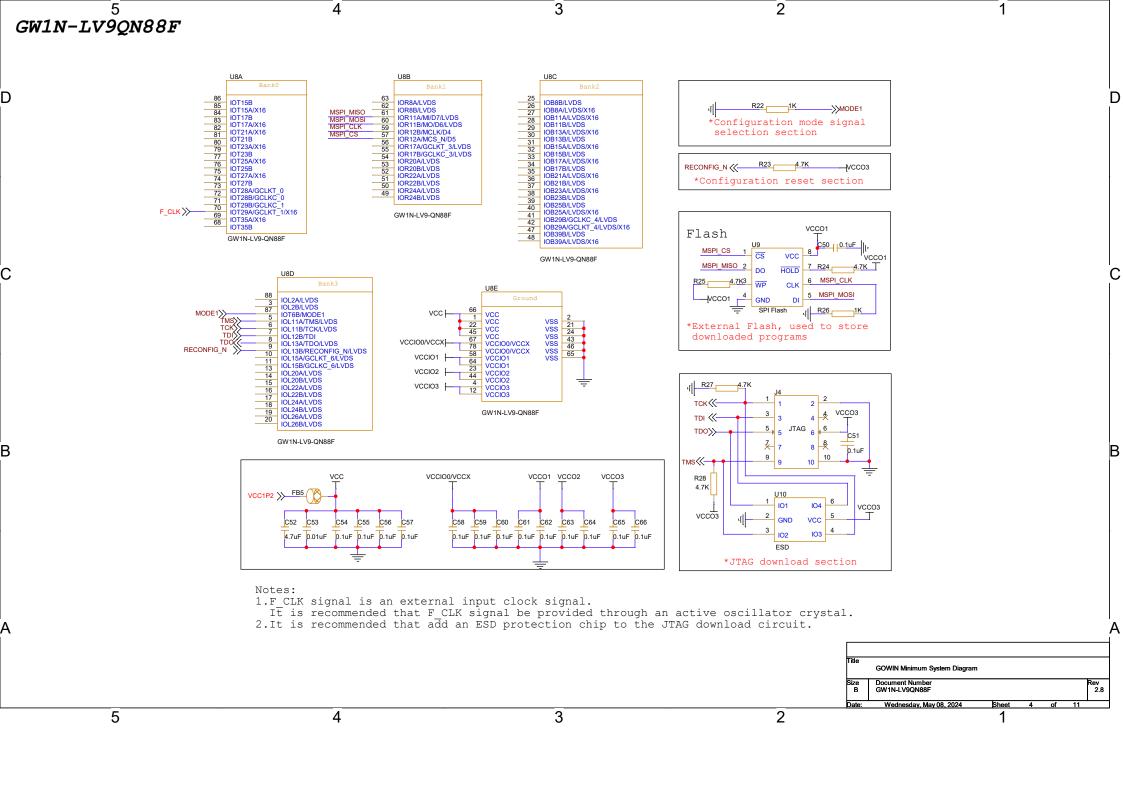


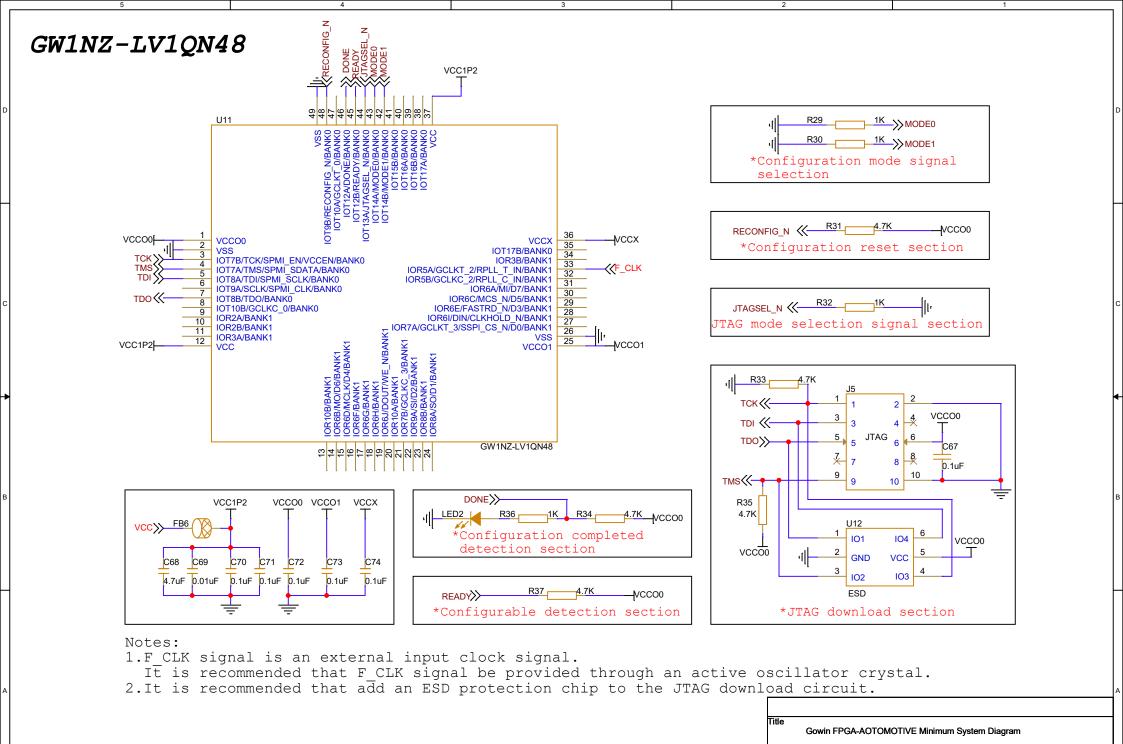




#### NT - - - - -

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.





Document Number

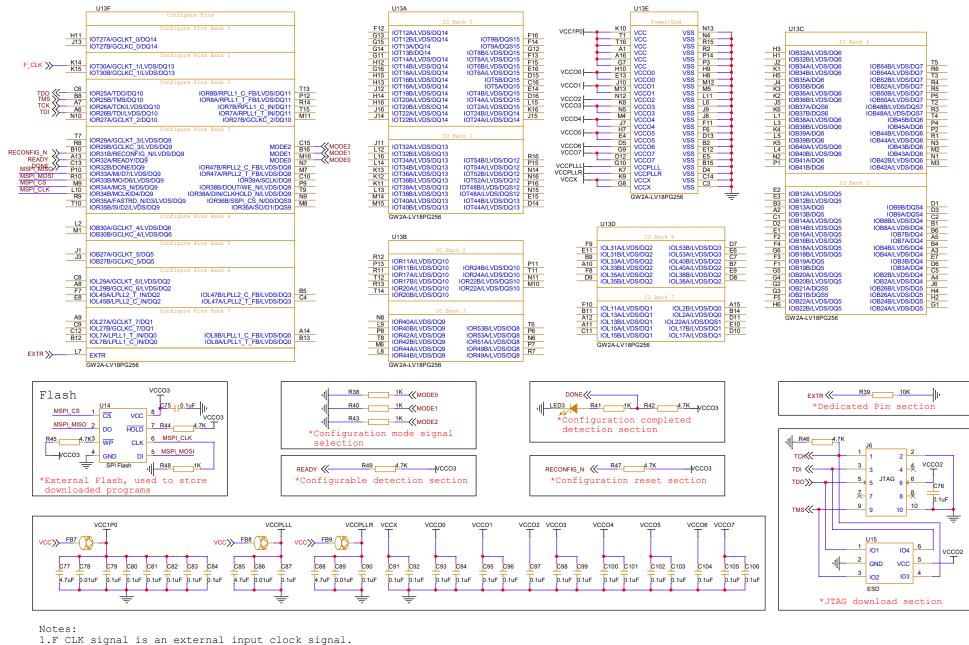
GW1NZ-LV1QN48

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2.8

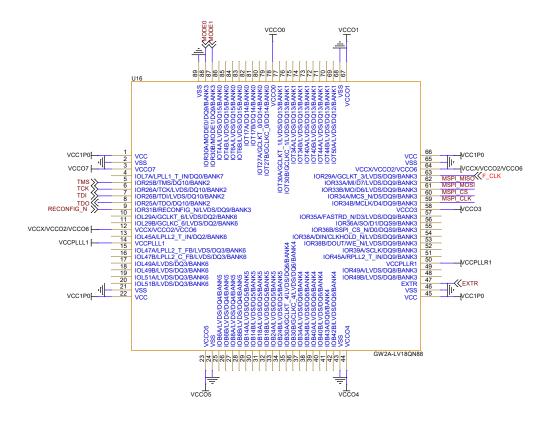
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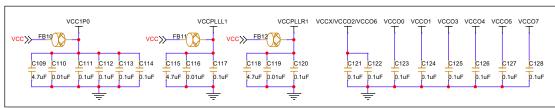


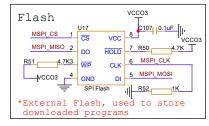
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2. External Flash memory is used to store downloaded programs.
  - For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

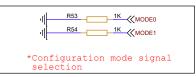
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Size	Document Number					Rev
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# GW2A-LV18QN88

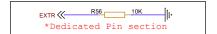


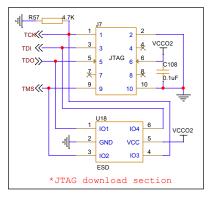












### Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs.
- - For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.

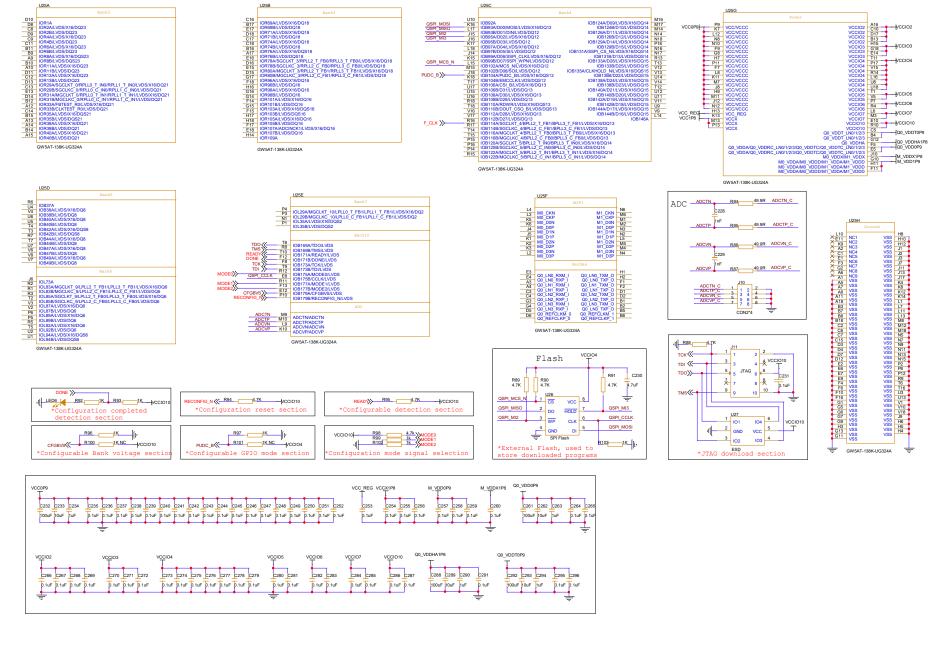
Gowin FPGA-AOTOMOTIVE Minimum System Diagram Document Number GW2A-LV18QN88F Wednesday, May 08, 2024

#### GW5A-LV25PG256 U19E READY (CISPTINGS N TS) READY IORSALVDS IORSBLIVDS IORSBLIVDS IOR7ALVDSIDQ2 IOR7ALVDSIDQ2 IOR7BLIVDSIDQ2 IORRBLIVDSIDQ2 IORSBLIVDSIDQ2 IOB65A/LVDS IOT29A/PUDC\_B/LVDS IOT29B/LVDS IOT31A/LVDS IOT31B/LVDS PUDC\_B >>-B15 B16 F12 G11 D14 IOB65B/DOUT/LVDS IOB69A/LVDS/DQ5 IOB69A/LVDS/DQ5 IOB69B/LVDS/DQ5 IOB71A/LVDS/DQ5 IOB71B/LVDS/DQ5 IOB73A/LVDS/DQ5 IOB73B/LVDS/DQ5 IOT31B/LVDS IOT33A/LVDS IOT33B/LVDS IOT35A/LVDS IOT35B/LVDS IOT37A/LVDS T12 T14 T13 R14 T15 R15 R16 P15 P16 L14 L16 M15 M16 N14 N16 D16 F13 F14 C15 C16 E15 E16 F15 F16 G14 G16 H15 H16 G12 H11 H13 H14 J11 J11 J13 K14 | IGBT-SELVOS/DOS | IGBT-SELVO OREAM, VISIONS IN VISION OF THE VISION OF TH QSPI\_MI2 QSPI\_MI3 GW5A-LV25-PG256 GW5A-LV25-PG256 GW5A-I V25-PG256 GW5A-LV25-PG256 GW54-J V25-PG256 U19I VCC0P9 -VCCI00 IOT1A/GCLKT\_15/LPLL0\_T\_IN0/LVDS IOT1B/GCLKC\_15/LPLL0\_C\_IN0/LVDS VCCIO1 A1 A16 VSS B11 VSS B7 VSS D13 VSS D4 VSS G5 VSS G8 VSS H7 VSS VSS VSS VSS IOL3A/GCLKT 14/LPLL0 T IN2/LPLL0 T FB0/LVDS/DQ7 IOL3B/GCLKC 14/LPLL0 C IN2/LPLL0 C FB0/LVDS/DQ7 IOL5A/GCLKT 13/LPLL0 T IN1/LPLL0 T FB1/LVDS/DQ7 IOL5B/GCLKC 13/LPLL0 C N1/LPLL0 C FB1/LVDS/DQ7 IOT1B/GCLKC\_15/LPLLI IOT3A/GCLKT\_16/LVDS RECONFIG\_N >>-IOB1A/RECONFIG N IOT3B/GCLKC 16/LVDS VCCI02 T1 R6 R10 P3 N13 M8 L2 L15 K9 L5 K5 K6 G6 G5 F4 F3 E2 E1 F6 F5 E4 E3 D3 D1 C1 IOL5B/GCLKC\_13/LPLL0 IOL7A/LVDS/DQ7 IOL7B/LVDS/DQ7 IOL9A/LVDS/DQS7/DQ7 IOL9B/LVDS/DQS7/DQ7 IOL12A/LVDS/DQ7 N15 VCCIO3 M\_VDD1P2 J7 M0\_VDD\_12 IOB4B/D09/SCL/LPLL1\_C\_FB0/LVDS IOB8A/D05/SO/SSI1/LVDS IOB8B/D06/LVDS (DBBBDDBLVDS (DBIQADDJSSP) - (NILVDS (DBIQADDJSSP) - (NILVDS (DBIQADDLG) - (DBIDDJSSP) - (WPNSSIZLPLLI T. INTILVDS (DBIZAGCLIC - 10BRDDVNB - BIPLLI \_C. INTILVDS (DBIZAGCLIC - 10BRD) - (DBIZAGCLIC - 10BRD) -GW5A-LV25-PG256 R8 N10 VCCIO4 R4 VCCIO5 N7 VCCIO6 K2 VCCIO6 K4 G4 VCCIO7 M VDD0P9 -M0 VDDA/M0 VDDD U19J VCCIO6 VCCIO6 VCCIO6 ÷ GW5A-LV25-PG256 IOL18A/LVDS/DQ6 IOL18B/LVDS/DQ6 IOB26B/GCLKC 9B/LVDS VCCIO7 H12 VQPS1P8 GW5A-LV25-PG256 VQPS GW5A-LV25-PG256 GW5A-I V25-PG256 A3 IOT27B/LVDS R58 4.7K GW5A-LV25-PG256 тск <<-VCCIO4 Flash 4 VCCIO10/VCCX R59 1K TDI ≪ PUDC\_B R60 1K NC VCICOO JTAG TDO >> \*Configurable GPIO mode section R62 4.7K R64 8 8 READY N R61 4.7K n tuE 4.7K \*Configurable detection section TMS << QSPI MCS N VCC 8 RECONFIG\_N ( R65 4.7K VCCIOS cs QSPI MISO 2 DO \*Configuration reset section QSPI MI3 HOLD 7 DONE >> U21 QSPI\_MI2 QSPI\_CCLK 104 6 3 WP CLK 6 LED4 R66 1K R67 1K VCCIO4 101 VCC 5 4 GND QSPI\_MOSI DI GND \*Configuration completed 103 4 SPI Flash R68 4.7k MODE IO2 detection section \*External Flash, used to store downloaded programs \*JTAG download section \*Configuration mode signal selection VCC0P9 VQPS1P8 VCCIO10/VCCX VCICO6 VCIC00 VCICO1 VCICO2 VCICO3 VCICO5 VCICO7 C131 C132 C133 C134 C135 C136 C137 C157 C158 C159 C167 C168 C138 C141 C142 C143 C144 C145 C146 C147 C148 C149 C150 C151 C152 C153 C154 C155 C156 C160 C161 C162 C163 C164 C165 C166 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF D.1uF D.1uF D.1uF D.1uF D.1uF D.1uF D.1uF D.1uF 0.1uF 0.1uF 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal. 2. External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora $\,V\,$ 25K FPGA Products Programming and Configuration Guide . 3.It is recommended that add an ESD protection chip to the JTAG download circuit. 4.VCC core voltage requires a large current, so it is recommended to supply power separately. 5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora $\,V\,$ 25K FPGA Products Programming and Configuration Guide. Rev 2.8

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#### GW5A-LV25UG324F 1122K A1 A18 B7 C16 C3 D10 D5 E15 G12 G17 G2 G5 U22I PUDC\_B >>-IOT29A/PUDG B/I VDS IOT61A/GCLKT 2/TPLL T IN0/LVDS/DQS0/DQ0 IOR5A/I VDS IOB65A/LVDS E14 D14 C15 D15 D16 A15 A16 B16 A17 G14 E15 E16 E18 D18 IOT29B/LVDS IOT37A/LVDS IOT61B/GCLKC\_2/TPLL\_C\_IN0/LVDS/DQS0/DQC IOT63A/GCLKT\_3/RPLL0\_T\_IN0/LVDS/DQ0 IOR5B/LVDS IOR7A/LVDS/DQ: IOB65B/DOUT/LVDS | IOTESINGCLKC\_27FBL\_C\_NOLVDSROOSD | IOTESINGCLKC\_3RRLD\_T\_ROLVDSROOD | IOT IOB67A/LVDS N1 P2 P1 L2 L1 T2 T1 U2 M0 CKP IOT39A/LVDS IOT39B/LVDS IOT41A/LVDS IOR7B/LVDS/DQ2 IOR9A/LVDS/DQ2 IOR9B/LVDS/DQ2 IOB67B/LVDS IOT41B/LVDS IOT43A/LVDS IOT43B/LVDS IOB71A/LVDS/DQ IOB71B/LVDS/DQ5 IOB73A/LVDS/DQ5 MIT. | GBF3ALVOSIDOS | MIE. | GBF3ALVOSIDOS | MIE. | GBF3ABLVOSIDOS | MIE. | GBF3ABLVOSIDOS | MIE. | GBF3ABCLKC BBLVDSIDOSSDDS | MIE. | GBF3ABCLKC BBLVDSIDOSSDDS | MIE. | GBF3ABCLKC BBLVDSIDOSSDDS | MIE. | GBF3ABLVOSIDOS | MIE. | GBF3ABCLKC | H10 H8 J11 J15 J4 J9 U1 GW5AT-I V25UG324I K10 K8 L9 M17 M2 M6 N13 R1 R14 R18 R4 R9 T16 U12 U6 V1 H15 G16 F17 G18 F18 H17 H18 K12 K13 L12 L13 F\_CLK >>-### U22E Bank 4 ### | U22E Ban U22J VCCIO10 J18 VCCIO10 E17 VCCIO10 GW5AT-LV25HG324F GW5AT-I V25UG324F VCCIO7 G4 VCCIO7 VCCIO7 VCCIO7 F2 VCCIO7 VCCIO7 J5 GW5AT-LV25UG324F U22F U22G V18 B13 VCCIO6 VCCIO6 VCCIO6 VCCIO6 J3 ÷ GW5AT-LV25UG324 VCCIO5 VCCIO5 VCCIO5 R6 VCCIO5 VCCIO4 VCCIO4 VCCIO4 VCCIO4 VCCIO3 VCCIO3 VCCIO3 VCCIO3 VCCI00 | B10 | VCCI00 VCCIO2 VCCIO2 VCCIO2 VCCIO2 H16 | IOL218/LVDS/DQS6 | IOL238/LVDS/DQ6 | IOL258/LVDS/DQ6 | IOL258/LVDS/DQ6 | IOL258/LVDS/DQ6 | IOL278/LVDS/DQ6 | IOL278/LVDS/DQ6 | IOL298/LVDS | IOL298/LVDS | IOL318/LVDS | IOL318/LVDS VCCIO1 B12 VCCIO1 VCCIO1 VCCIO1 VCCIO1 VCCIO1 IOB56A/LVDS IOB56B/LVDS N11 R15 L11\_\_\_\_\_VQPS1P8 IOB58A/D00/DIN/MISO/MI1/LVDS QSPI\_MOSI QSPI\_CCLK VCC\_REG VCC\_REG \_\_L6 GW5AT-I V25LIG324F GW5AT-LV25UG324 GW5AT-I V25HG324I GW5AT-LV25UG324I GWSATJI V25I IG324E R71 4.7K R72 1K RECONFIG N (CR73 4.7K VCCIO5 тск <<-VCCIO4 R74 1K NC VCCIO0 4 VCCIO10 Flash PUDC B <<-\*Configuration reset section TDI << \*Configurable detection section JTAG 6 6 TDO>> C169 C170 7 7 8 8 R75 4.7K 0.1uF 4.7uF 10 10 READY >> R78 4.7K VCCIO4 тмs <<-U23 ÷ QSPI\_MCS\_N Configurable detection section QSPI\_MISO OSPL MI3 HOLD U24 R79 4.7K VCCIO4 QSPI\_MI2 3 WP QSPI CCLK MODEO << 101 VCCIO10 2 GND QSPI MOSI R80 1K VCCIO4 R81\_\_\_1K VCC MODE1 <<-103 4 SPI Flash DONE >> R82 1K LED5 102 Configuration mode signal selection Configuration completed detection section \*External Flash, used to \*JTAG download section store downloaded programs M VDD1P2 M VDDA0P9 C172 C173 C174 C175 C178 C179 C180 C181 C182 C183 C184 C185 C186 C187 C188 C189 C190 C191 C192 C193 C194 C195 C196 C171 C176 0.1uF 10uF 1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF ÷ vector VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIOS vector VCCIO10 C197 C198 C199 C200 C201 C202 C203 C204 C205 C206 C207 C208 C209 C210 C211 C212 C213 C214 C215 C216 C217 C218 C219 C220 C221 C222 C223 C224 C225 C226 C227 0.1uF ÷ 1.F CLK signal is an external input clock signal. It is recommended that F\_CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora $\,V\,$ 25K FPGA Products Programming and Configuration Guide . 3.It is recommended that add an ESD protection chip to the JTAG download circuit. 4.VCC core voltage requires a large current, so it is recommended to supply power separately. 5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Rev 2.8 Arora V 25K FPGA Products Programming and Configuration Guide. Wednesday, May 08, 2024

### GW5AT-LV138UG324A



#### Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.

 GW5AT-LV15MG132 Bank IOB3A/D02/MI2/LVDS IOB3B/D01/DIN/MISO/MI1/LVDS IOB5A/CCLK/LVDS P5 M0\_CKP P7 M0\_CKN M0\_D0P M0\_D0N M0\_D1N M0\_D1N M0\_D1N M0\_D1N M0\_D1N M0\_D2N M0\_D2N M0\_D3N M0\_D3N M0\_D3N IOB5B/MCS\_N/LVDS IOB7A/D03/MI3/LVDS U28D IOB7B/D00/MOSI/MI0/LVDS B3 C3 B6 C6 B8 C8 B12 C12 Q0\_LN0\_RXP\_I Q0\_LN0\_RXM\_I Q0\_LN1\_RXP\_I Q0\_LN1\_RXM\_I Q0\_LN2\_RXP\_I Q0\_LN2\_RXM\_I Q0\_LN3\_RXP\_I Q0\_LN3\_RXM\_I Bank 3 IOL29ADONELVDS
IOL29BRECONFIG NILVDS
IOL31AGCLRT SMODELIA/DS
IOL31AGCLRT SMODELIA/DS
IOL31AGCLRT SMODELIA/DS
IOL31AGCLRT ARIPLIT THE TERRICSO BROUT/SCLLVDS
IOL33AGCLRT ARIPLIT THE TERRICSO BROUT/SCLLVDS
IOL35AGDUNIS/SOLL FIĞ N >> F\_CLK >>-C1 M1\_D08
D1 M1\_D08
F1 M1\_D0C
G1 M1\_D1A
F2 M1\_D1C
M1\_D1C
M1\_D1C
M1\_D1C
M1\_D1C
M1\_D1C
M1\_D2A
M1\_D2C A8 Q0\_REFCLKP\_0 Q0\_REFCLKM\_0 Q0\_REFCLKP\_1 B10 IOL35B/D05/SSPI\_CS\_N/LVDS GW5AT-LV15-MG132 PE 10022AGGIKT / YUUNL. 1907 BERGEN B GW5AT-LV15-MG132 GW5AT-LV15-MG132 R104 VCCIO2 Flash TCK << 4 VCCIO4 Q0\_VDDT0P9 B4 Q0\_VDDT\_LN0/1/2/3 Q0\_VDDT0P9 C7
Q0\_VDDHA1P8 C7
Q0\_VDDHA
Q0\_VDDHA VCCIO1 K12 VCCIO1 TDI << JTAG 6 6 VSS VSS VSS VSS VSS VSS VSS VSS VSS R105 4.7K R106 4.7K TDO>> 4.7uF C298 Z 7 8 8 VCCIO2 M1\_VDDA0P9 E2 M1\_VDDA\_LN0/M1\_VDDA\_LN1/M1\_VDDA\_LN2 U29 VCCIO3 M4 VCCIO3 QSPI\_MCS\_N ÷ M\_VDDX C2 M0\_VDDX/M1\_VDDX VCCIO4 F3 VCCIO4 QSPI\_MISO 2 DO QSPI MI3 HOLD M0\_VDDA0P9 | M5 M0\_VDDA VCCX VCCX VCCX VCCX 3 WP QSPI\_MI2 QSPI\_CCLK -Vccx QSPI\_MOSI 1 101 DI VCCIO4 GW5ATJ V15JMG132 VQPS L12 VQPS1P8 SPI Flash VCC 5 2 GND VCC\_REG F12 \_\_\_VCC\_REG IO3 4 \*External Flash, used to 3 IO2 DPHY\_VDD12 M7 DPHY\_VDD1P2 store downloaded programs \*JTAG download section GW5AT-LV15-MG132 READY >> R109 4.7K VCCIO2  $\star$ Configurable detection section RECONFIG\_N ( R110 4.7K VCCIO3 Q0\_VDDT0P9 M1 VDDA0P9 M VDDX M0 VDDA0P9 VQPS1P8 VCC REG DPHY VDD1P2 \*Configuration reset section C318 C302 C304 C305 C306 C307 C308 C309 C310 C311 C312 C313 C315 C316 C317 C319 C320 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 1uF 0.1uF 100uF 10uF 1uF 0.1uF 100uF 10uF 1uF 0.1uF 0.1uF 0.1uF 0.1uF 100uF 10uF MODE0 ( R111 4.7K VCCIO3 MODE1 ( R112 1K VCCIO2 VCCIO3 VCCIO4 VCC0P9 VCCX \*Configuration mode signal selection C321 C322 C323 C324 C325 C326 C327 C328 C329 C330 C331 C332 C333 C337 C338 C339 C340 0.1uF R113 1K VCCIO3 R114 1K LED7 // \*Configuration completed detection section Notes: 1.F CLK signal is an external input clock signal. It is recommended that F\_CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. 3.It is recommended that add an ESD protection chip to the JTAG download circuit. 4.VCC core voltage requires a large current, so it is recommended to supply power separately. 5. The MODE pin is the GowinCONFIG configuration mode selection signal.

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