GW5AT-LV15MG132 Bank 2 IOB3A/D02/MI2/LVDS IOB3B/D01/DIN/MISO/MI1/LVDS IOB5A/CCLK/LVDS P5 M0_CKP P7 M0_CKN M0_D0P M0_D0N M0_D1N M0_D1N M0_D1N M0_D1N M0_D1N M0_D2N M0_D2N M0_D3N M0_D3N M0_D3N IOB5B/MCS_N/LVDS IOB7A/D03/MI3/LVDS U6D IOB7B/D00/MOSI/MI0/LVDS B3 C3 B6 C6 B8 C8 B12 C12 Q0_LN0_RXP_I Q0_LN0_RXM_I Q0_LN1_RXP_I Q0_LN1_RXM_I Q0_LN2_RXP_I Q0_LN2_RXM_I Q0_LN3_RXP_I Q0_LN3_RXM_I Bank 3 IOL29ADONELVDS
IOL29BRECONFIG NILVDS
IOL31AGCLRT SMODELIA/DS
IOL31AGCLRT SMODELIA/DS
IOL31AGCLRT SMODELIA/DS
IOL31AGCLRT AIPLL T MILPLL T FB0CSO B/DOUT/SCLL/DS
IOL38AGCLRT AIPLL T MILPLL T FB0CSO B/DOUT/SCLL/DS
IOL38AGCLRT SOIL VDS
IOL38ADON/SISOIL/DS FIĞ N >> F_CLK >>-C1 M1_D08
D1 M1_D08
F1 M1_D0C
G1 M1_D1A
F2 M1_D1C
M1_D1C
M1_D1C
M1_D1C
M1_D1C
M1_D2A
M1_D2C A8 Q0_REFCLKP_0 Q0_REFCLKM_0 Q0_REFCLKP_1 Q0_REFCLKM_1 IOL35B/D05/SSPI_CS_N/LVDS GW5AT-LV15-MG132 PE 10022AGGIKT / YUUNL. 1907 BERGEN B GW5AT-LV15-MG132 GW5AT-LV15-MG132 R12__ VCCIO2 Flash TCK << 4 VCCIO4 Q0_VDDT0P9 B4 Q0_VDDT_LN0/1/2/3 Q0_VDDT0P9 C7
Q0_VDDHA1P8 C7
Q0_VDDHA
Q0_VDDHA VCCIO1 K12 VCCIO1 TDI ≪ JTAG 6 6 VSS VSS VSS VSS VSS VSS VSS VSS VSS TDO>> 4.7uF Z 7 8 8 VCCIO2 M1_VDDA0P9 E2 M1_VDDA_LN0/M1_VDDA_LN1/M1_VDDA_LN2 VCCIO3 M4 VCCIO3 QSPI_MCS_N ÷ M_VDDX C2 M0_VDDX/M1_VDDX VCCIO4 F3 VCCIO4 2 DO QSPI_MISO QSPI MI3 HOLD M0_VDDA0P9 | M5 M0_VDDA VCCX VCCX VCCX VCCX 3 WP QSPI_MI2 QSPI_CCLK -Vccx QSPI_MOSI 1 101 DI VCCIO4 GW5ATJ V15JMG132 VQPS L12 VQPS1P8 SPI Flash VCC 5 2 GND VCC_REG F12 ___VCC_REG IO3 4 *External Flash, used to 3 IO2 DPHY_VDD12 M7 ____DPHY_VDD1P2 store downloaded programs *JTAG download section GW5AT-LV15-MG132 READY >> R17 4.7K VCCIO2 \star Configurable detection section RECONFIG_N (R18 4.7K VCCIO3 Q0_VDDT0P9 M1 VDDA0P9 M VDDX M0 VDDA0P9 VQPS1P8 VCC REG DPHY VDD1P2 *Configuration reset section C53 C46 C47 C48 C52 C44 C45 C54 C55 C56 C58 C59 C60 C61 C62 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 100uF 10uF 1uF 1uF 0.1uF 100uF 10uF 1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 100uF 10uF R19 4.7K VCCIO3 MODE0 << MODE1 (R20 1K VCCIO2 VCCIO4 VCC0P9 VCCX *Configuration mode signal selection C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C79 C80 C81 C82 C83 0.1uF R21 VCCIO3 R22 1K LED2 /// *Configuration completed detection section Notes: 1.F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. 3.It is recommended that add an ESD protection chip to the JTAG download circuit. 4.VCC core voltage requires a large current, so it is recommended to supply power separately. 5. The MODE pin is the GowinCONFIG configuration mode selection signal.

3

5