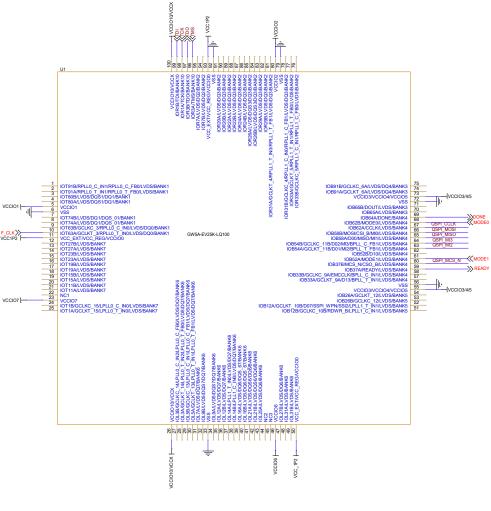
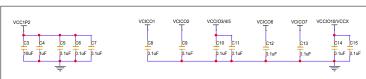
GW5A-EV25LQ100





- Notes:

 1.F CLK signal is an external input clock signal.

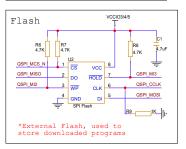
 1.F CLK signal be provided through an active oscillator crystal.

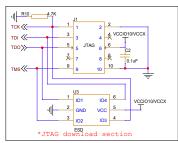
 2.External Flash memory is used to store downloaded programs.

 For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714,
- Arora $\,$ V 25K FFGA Products Programming and Configuration Guide . 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

VCCION/4/5 T R2
READY > R3 4.7K VCC103/4/5 *Configurable detection section

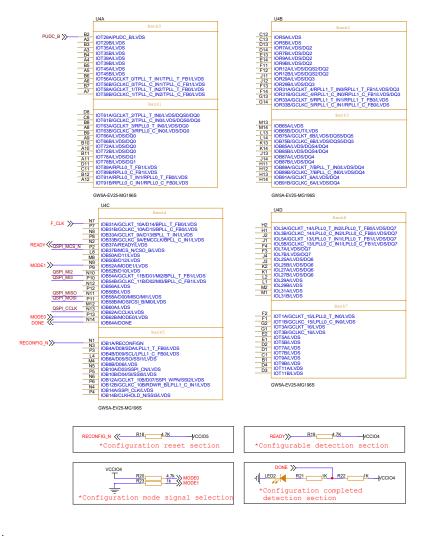


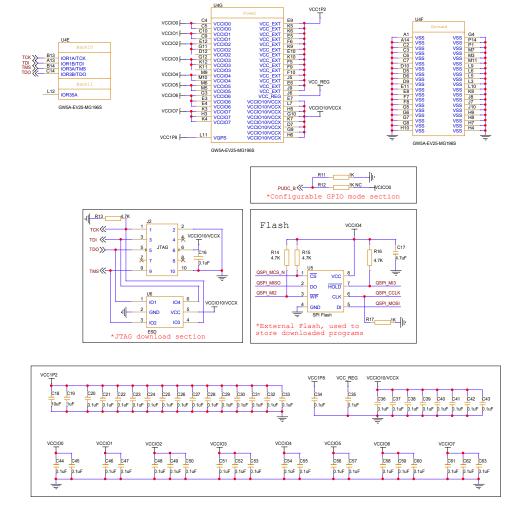




Rev 2.3

GW5A-EV25MG196S





1.F CLK signal is an external input clock signal.

It Is recommended that F CLK signal be provided through an active oscillator crystal.

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora $\,V\,$ 25K FPGA Products Programming and Configuration Guide .

3.It is recommended that add an ESD protection chip to the JTAG download circuit.

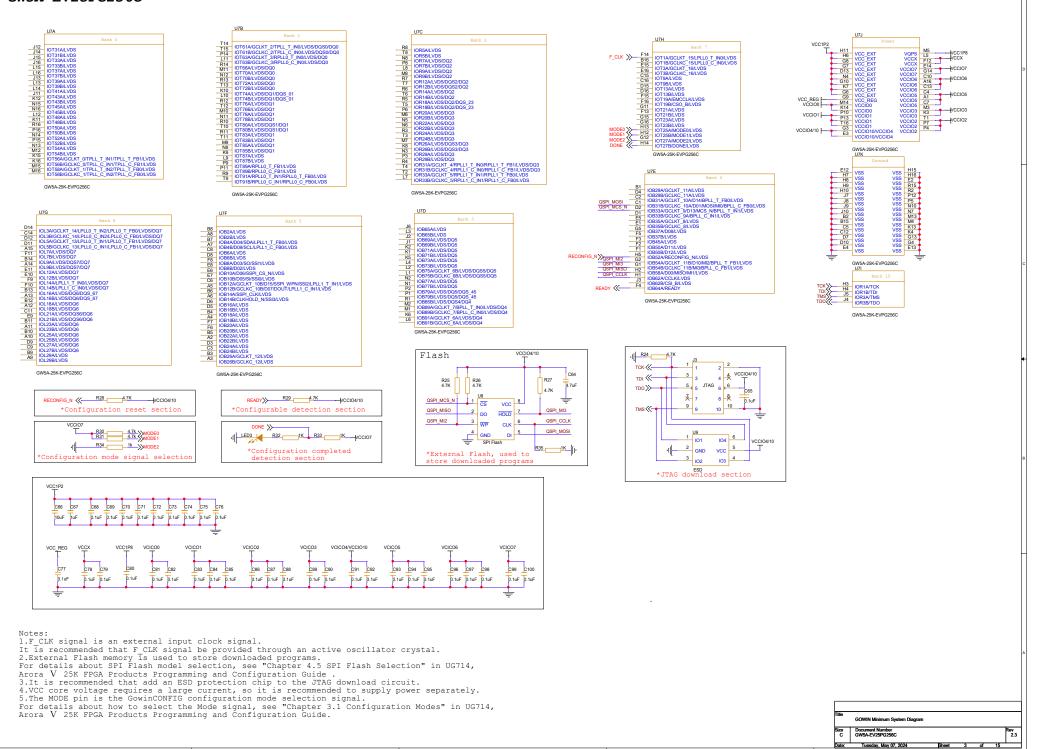
4.VCC core voltage requires a large current, so it is recommended to supply power separately.

5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

> GOWIN Minimum System Diagram Document Number GW5A-EV25MG196S 2.3 Tuesday, May 07, 2024

GW5A-EV25PG256C



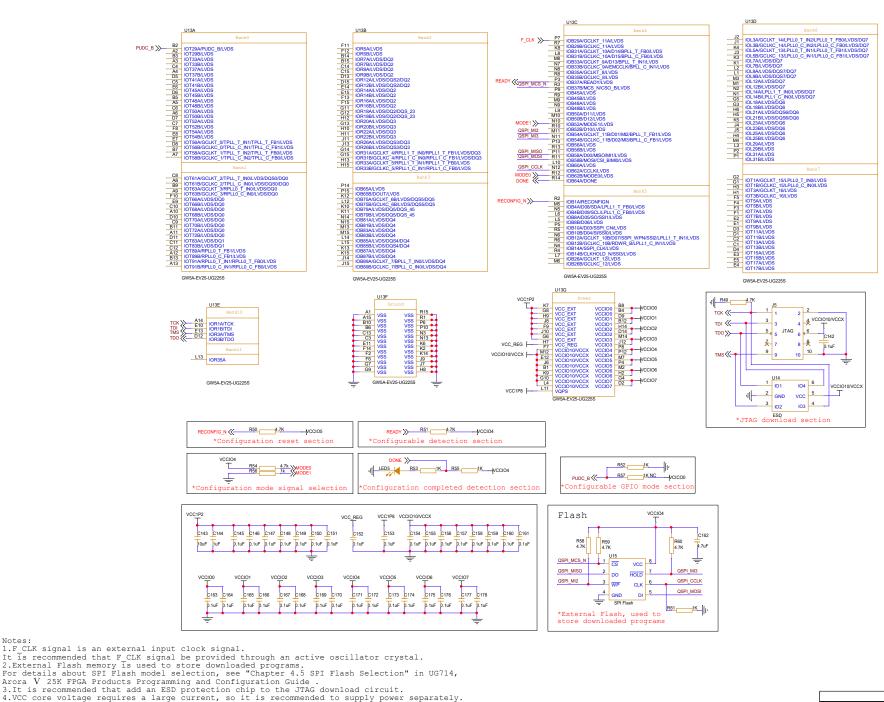
GW5A-EV25PG256S U10C IOB29A/GCLKT_11A/LVDS IOB29B/GCLKC_11A/LVDS IOB31A/GCLKT_10A/D14/BPLL_T_FB0/D14/LVDS ORSALVIDS ORSELVIDS ORSELVIDS ORRIALVIDSOD2 ORRIALVIDSOD3 IOR5A/LVDS IOB65A/LVDS IOB65B/DOUT/LVDS IOR5B/LVDS PUDC B >> E7 E8 E10 C10 D8 C8 C11 A11 F9 D9 B12 IOT29A/PUDC B/I VDS IOT61A/GCLKT 2/TPLL T IN0/LVDS/DQS0/DQ0 IOB31B/GCLKC_10A/D15/BPLL_C_FB0/D15/BPLL_C_FB0/LVDS IOB33A/GCLKT_9A/D13/BPLL_T_IN1/LVDS IOT29B/LVDS IOT31A/LVDS IOT61B/GCLKC_2/TPLL_C_IN0/LVDS/DQS0/DQ0 IOT63A/GCLKT_3/RPLL0_T_IN0/LVDS/DQ0 IOB69A/LVDS/DQ5 IOB69B/LVDS/DQ5 L13 R12 T12 T14 T13 R14 T15 R16 P15 P16 L14 L16 M15 M16 N14 | WALFOCK | WALF IOB33B/GCLKC_9A/EMCCLK/BPLL_C_IN1/LVDS IOB35B/GCLKT_8/LVDS IOB35B/GCLKC_8/LVDS IOT63B/GCLKC_3/RPLL0_C_IN0/LVDS/DQ0 IOT66A/LVDS/DQ0 IOT66B/LVDS/DQ0 IOB71A/LVDS/DQS IOB71B/LVDS/DQS IOB73A/LVDS/DQS IOT31B/LVDS IOT35A/LVDS IOTEBALVISCIOIO OTTOBBALVISCIOIO OTTOBALVISCIOIO OTTOBALVISCIOIO OTTOBALVISCIOI OTTSALVISCIOI OTTSBALVISCIOI OTTSBARPLIO C FRILVISCIOI OTTSBARPLIO C FRILV IOT68A/LVDS/DQ0 IOT35B/LVDS IOT37A/LVDS OTS/ALVOS OTS/BALVOS A12 C13 A13 F10 E11 B14 A14 D11 D12 F15 F16 G14 G16 H15 H16 MODE1 >>-QSPI_MI2 QSPI_MI3 G12 H11 H13 H14 J11 QSPI_CCLK GW54-FV25-PG256S GW54-FV25-PG256S MODE0 >> GW5A-EV25-PG256S GW5A-EV25-PG256S GW5A-EV25-PG256S IOL3A/GCLKT 14LPLL0 T INZLPLL0 T FB0LVDS/DOZ-IOL3B/GCLKC 14LPLL0 C INZLPLL0 C FB0LVDS/DOZ-IOL5A/GCLKT 13LPLL0 T INJLPLL0 T FB1LVDS/DOZ-IOL5B/GCLKC 13LPLL0 C INJLPLL0 C FB1/LVDS/DOZ-IOL7ALVDS/DOZ-IOL7BLVDS/DOZ-VCCIO1 B13 VCCIO1 D10 P0 VCC_REG VCCIO0 VCCIO1 VCCIO1 VCCIO1 VCCIO2 VCCIO2 VCCIO2 VCCIO3 VCCIO3 VCCIO3 VCCIO4 VCCIO4 VCCIO5 VC K10 K8 G7 H10 G9 J7 J9 A1 A16 B11 B7 D13 D4 E9 G15 G2 G8 H7 H9 VCCIO2 D15 G13 IOR2A/LVDS -VCC1P2 | IOBZA/LVDS | IOBZA/LVDS | IOBA/ID08/SDA/LPLL1_T_FB0/LVDS | IOBA/ID09/SCI./PLL1_C_FB0/LVDS | IOBBA/ID05/SO/SS11/LVDS | IOBBA/ID05/LVDS OLBALVUSSIOGS/DOG* OLBALVUSSIOG* OL128LVUSSIOG* OL128LVUSSIOG* OL128LVUSSIOG* OL128LVUSSIOG* OL128LVUSSIOG* OL148LVUSSIOG* OL148LVUSSIOG* OL148LVUSSIOG* OL148LVUSSIOG* OL148LVUSSIOG* OL128LVUSSIOG* OL248LVUSSIOG* OL248LVUSSIOG* OL248LVUSSIOG* OL248LVUSSIOG* OL258LVUSSIOG* IOL9A/LVDS/DQS7/DQ7 IOR1A/TCK IOR1B/TDI IOR3A/TMS IOR3B/TDO VCCIO3 K13 N15 R13 N10 E5 VCCIO10/VCCX K2 K1 L3 L1 M2 M1 N3 N1 P2 P1 R2 R1 M4 M3 M5 VCCIO10MCCX JOBBAIDUBLIVDS OBTOADUSSEPI CNILVDS OBTOADUSSEPI CNILVDS OBTOBEDOMSISSIOLIVDS OBTOBE VCCIO10/VCCX VCCIO10/VCCX VCCIO10/VCCX VCCIO4 R8 X P14 IOR35A VCCIO5 | N7 R4 VCCIO6 | N2 K4 J2 VCCIO7 | D2 G4 VCCIO10/VCCX VCCIO6 VCCIO6 VCCIO6 VCCIO7 VCCIO10/VCCX G10 GW5A-EV25-PG256S GW5A-EV25-PG256S RECONFIG_N >>-VCCIO10/VCCX H12 VCC1P8 VQPS VCCIO7 GW5A-EV25-PG256S GW5A-EV25-PG256S GW5A-FV25-PG256S GW5A-EV25-PG256S .[R36 TCK << VCCIO4 Flash R37 1K 4 VCCIO10/VCCX TDI <<-PUDC_B R38 KNC VCICOO JTAG TDO >> C102 8 8 *Configurable GPIO mode section R40 4.7K R42 READY NCCIO4 0.1uF 4 7K 4 7K 10 10 TMS << *Configurable detection section U11 RECONFIG_N (R43 VCCIO5 CS VCC 8 QSPI_MISO QSPI MI3 *Configuration reset section HOLD DO U12 QSPI_MI2 QSPI_CCLK 3 WP 104 LED4 R44 1K R45 1K VCCIO4 CLK 101 VCCIO10/VCCX 4 GND VCC 5 QSPI MOSI 2 GND DI 5 VCCIO4 *Configuration completed R46 4.7k MODE0 R47 1k MODE1 SPI Flash IO3 4 102 detection section *External Flash, used to *JTAG download section *Configuration mode signal selection VCC1P2 VCC REG VCC1P8 VCCIO10VCCY VCIC00 VCICO1 VCICO4 VCICO5 VCICO6 VCICO7 C105 C106 C107 C108 C109 C110 C111 C103 C104 C112 C114 C115 C116 C117 C118 C119 C120 C121 C122 C123 C124 C125 C126 C127 C128 C129 C130 C131 C132 C133 C134 C135 C136 C137 C138 C139 C140 C141 10uF 1uF 0.1uF Notes: 1.F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora $\,V\,$ 25K FPGA Products Programming and Configuration Guide . 3.It is recommended that add an ESD protection chip to the JTAG download circuit. 4.VCC core voltage requires a large current, so it is recommended to supply power separately. 5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide. Rev 2.3

GW5A-EV25UG225S

5. The MODE pin is the GowinCONFIG configuration mode selection signal.

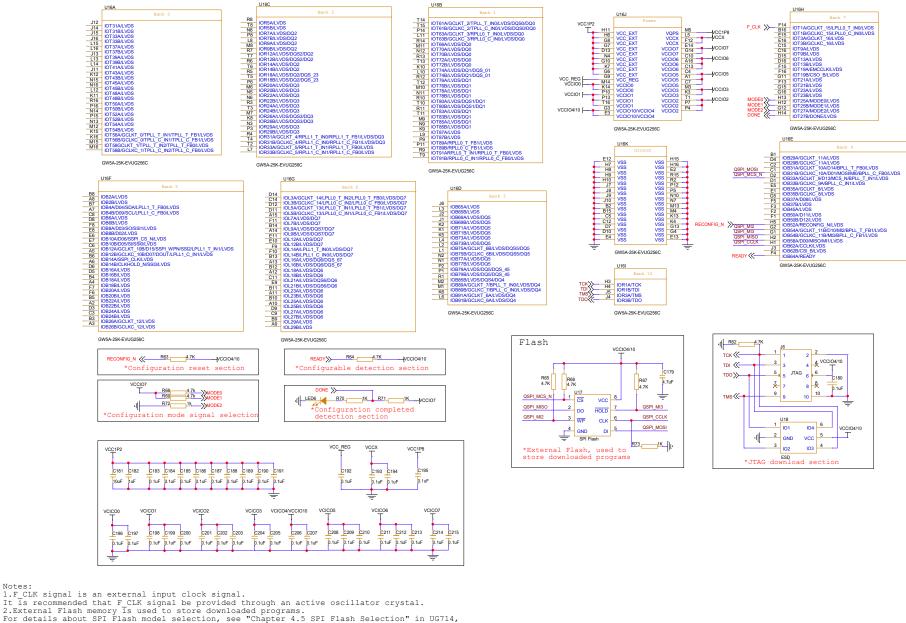
Arora V 25K FPGA Products Programming and Configuration Guide.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714,



| Title | G/OWIN Minimum System Diagram | Size | Document Number | C | GWISA-EV/SSU2025S | 2.3 | Date: Tuesday, May 07, 2024 | Sheet 5 of 15 |

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1.F CLK signal is an external input clock signal.

Arora $\,V\,$ 25K FPGA Products Programming and Configuration Guide .

3.It is recommended that add an ESD protection chip to the JTAG download circuit.

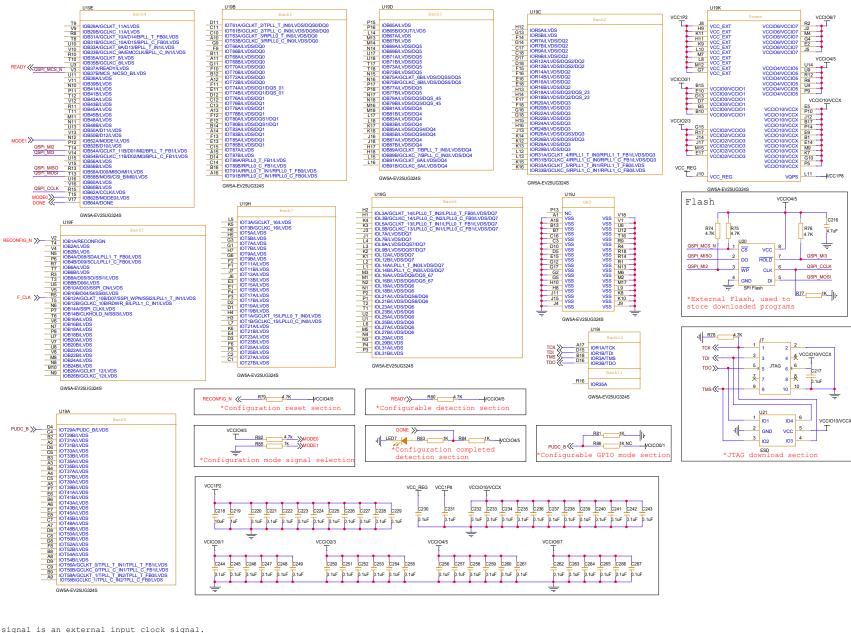
4.VCC core voltage requires a large current, so it is recommended to supply power separately.

5. The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

€ev 2.3 Tuesday, May 07, 2024

GW5A-EV25UG324S



Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2.External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora $\,V\,$ 25K FPGA Products Programming and Configuration Guide .

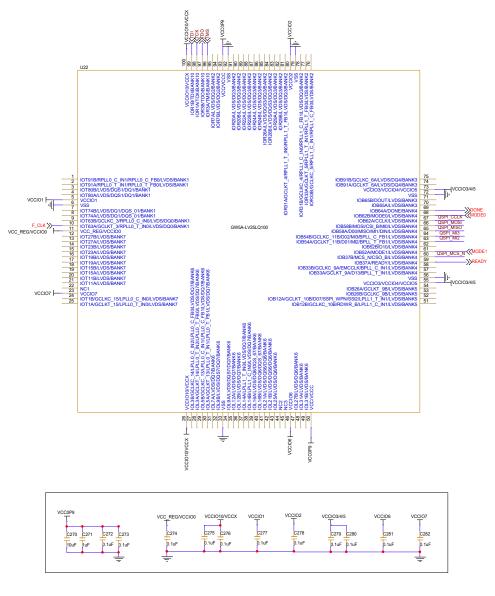
3.It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately. 5. The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

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GW5A-LV25L0100



1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

2.External rash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714,

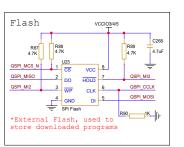
Arora V 25K FPGA Products Programming and Configuration Guide .

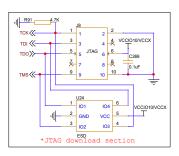
3.It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

5. The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.





READY >> R92 4.7K VCCIO3/4/5 *Configurable detection section

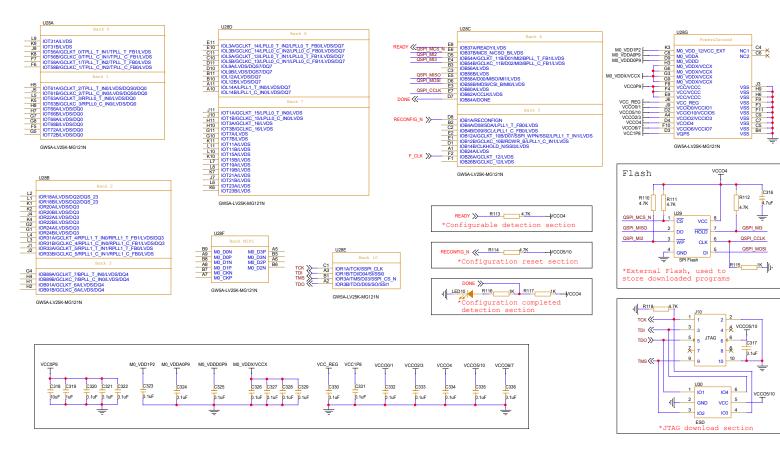


R95 4.7K VCCIO3/4/5 MODE0 <<-MODE1 (R96 IK *Configuration mode signal selection

Title GOWIN Minimum System Diagram							
Size C	Document Number GW5A-LV25LQ100					Rev 2.3	
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GW5A-LV25LQ144 R97 TCK << 4 VCCIO10/VCCX TDI ≪ TDO>> 8 8 0.1uF CONVOZON CONTROLO CON 104 6 VCCIO10/VCCX VCC 5 103 *JTAG download section 134.PLL0 T IN14.PLL0 T 134.PLL0 C IN14.PLL0 C 144.PLL0 T IN24.PLL0 T Flash VCC REG/VCCIO0/4 VCCOP9 VCC0P9 VCCVCCC VCC/VCCC VSS IOT3B/GCLKC 16/LVDS/BANK7 C284 | VCC/VCC| R100 4.7uF 4.7K 4.7K IOT3A/GCLKT_16/LVDS/BANK7 IOT5A/LVDS/BANK7 VCCIO5 U27 VCCIOS 10B12A/GCLKT_10B/D07/SSPI_WPN/SSI2/LPLL1_T_IN1/LVDS/BANK5 10B14A/SSPI_CLK/LVDS/BANK5 10B14B/CLKFIOLD_N/SSI3/LVDS/BANK5 VCCIO7 QSPI MCS N 1 CS QSPI MISO 2 DO QSPI MI3 I IOBHABICLHFOLD, INSISILITUSIDAMINA VICCIOS 10831AGCLAT, IOADHAIPPLL, T. FBULVDSBANKA 10831AGCLAC, IOADHAIPPLL, C. FBULVDSBANKA VICC. REGIVCCIOWCCIOA 10833AGCLAT, SADDISPPLL, T. INITLVDSBANKA 10833AGCLAT, SADDISPPLL, T. INITLVDSBANKA 10833AGCLAT, VOSBANKA 10837ARBADY, VOSBANKA 1083 VCCIO5 [HOLD -QSPI MI2 QSPI CCLK 3 WP CLK 6 DI 5 4 GND QSPI MOSI VCC REG/VCCIO0/4 GW5A-LV25LQ144 SPI Flash READY (COSPI MCS N VCC_REG/VCCIO0/4 VSS VCC_REG/VCCIO0/VCCIO4 IOB50A/D11/LVDS/BANK4 IOB50B/D12/LVDS/BANK4 IOB52A/MODE1/LVDS/BANK4 IOB52B/D10/LVDS/BANK4 VCC REG/VCCI00/4 *External Flash, used to store downloaded programs MODE1 >> IOBS4A/GCLKT_11B/D01/MI2/BPLL_T_FB1/LVDS/BANK4 IOBS4B/GCLKC_11B/D02/MI3/BPLL_C_FB1/LVDS/BANK4 IOBS8A/D00/DIN/MISO/MI1/LVDS/BANK4 -(/F CLK RECONFIG_N R102 4.7K VCCIO5 VCC_REG/VCCIO0/4 QSPI_MOSI VCC_REG/VCCIO0/VCCIO4 IOB58B/MOSI/MI0/CSI_B/LVDS/BANK4 *Configuration reset section IOB62A/CCLK/LVDS/BANK4 IOB62B/MODE0/LVDS/BANK4 IOB64A/DONE/BANK4 VCC/VCCC IOT70A/LVDS/DQ0/BANK1 IOT72A/LVDS/DQ0/BANK1 IOT72B/LVDS/DQ0/BANK1 VCCIO3 IOB65B/DOUT/LVDS/BANK3 VCCIO3 MODE0 KR103 4.7K VCC_REG/VCCIO0/4 VCCIO1 IOT91A/RPLL0_T_IN1/RPLL0_T_FB0/LVDS/BANK1 IOT91B/RPLL0_C_IN1/RPLL0_C_FB0/LVDS/BANK1 VCCIO3 F VCCIO3 IOB75A/GCLKT_6B/LVDS/DQS5/DQ5/BANK3 IOB75B/GCLKC_6B/LVDS/DQS5/DQ5/BANK3 VCC/VCCC MODE1 (R104 1K VSS VCC/VCCC VCC0P9 [*Configuration mode signal selection R105 1K R106 1K NC VCC_REG/VCCIO0/4 PUDC_B <<-*Configurable detection section READY >> R107 VCC REG/VCCIO0/4 Configurable detection section R108 1K VCC_REG/VCCIO0/4 DONE >> R109 1K LED9 VOC1P8 VCC0P9 「辛」 *Configuration completed detection section VCC0P9 VCC REG/VCCIO0/4 VCC1P8 C287 C288 C289 C290 C291 C292 C293 C294 1.F_CLK signal is an external input clock signal. C285 C286 C295 C296 C297 C298 C302 It is recommended that F CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide . 3.It is recommended that add an ESD protection chip to the JTAG download circuit. 4.VCC core voltage requires a large current, so it is recommended to supply power separately. 5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora $\,V\,$ 25K FPGA Products Programming and Configuration Guide. C304 C305 C306 C307 C308 C309 C310 C311 C312 C313 C314 C315 0.1uF Document Number GW5A-LV25LQ144 2.3

GW5A-LV25MG121N



Notes:

1.F CLK signal is an external input clock signal.

It $\bar{1}s$ recommended that F_CLK signal be provided through an active oscillator crystal.

2.External Flash memory Is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714,

Arora V 25K FPGA Products Programming and Configuration Guide .

3.It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

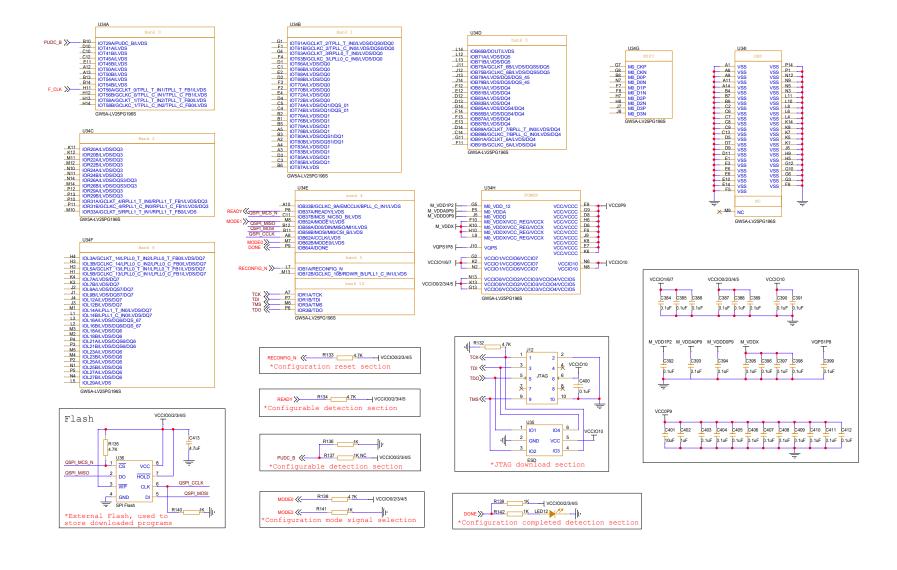
5. The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

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GW5A-LV25MG196S Bank2 PUDC B >> B2 A2 B3 A3 B4 A4 B5 A5 B6 A6 B7 C12 C13 D13 D14 E13 E14 F11 F12 J11 J12 F13 F14 G13 G14 IOT29A/PUDC B/LVDS ORSALVIDS ORSELVIDS ORSELVIDS ORVALVIDS ORVALVIDS ORVALVIDS ORVALVIDS ORSELVIDS ORSELV IOR5A/LVDS IOL3A/GCLKT 14/LPLL0 T IN2/LPLL0 T FB0/LVDS/DQ7 IOT29B/LVDS IOT35A/LVDS IOT35B/LVDS IOL3B/GCLKC 14/LPLL0 C IN2/LPLL0 C FB0/LVDS/DQ7 IOL5A/GCLKT 13/LPLL0 T IN1/LPLL0 T FB1/LVDS/DQ7 IOL5B/GCLKC 13/LPLL0 C IN1/LPLL0 C FB1/LVDS/DQ7 IOT39A/LVD IOT399ALVDS IOT39ALVDS IOT39ALVDS IOT45ALVDS IOT45ALVDS IOT56AAGCLKT_0TPLL_T_FB1/LVDS IOT56BAGCLKC_0TPLL_C_N1/TPLL_T_FB1/LVDS IOT58BAGCLKT_1/TPLL_T_N2/TPLL_T_FB0/LVDS IOT58BAGCLKT_1/TPLL_T_N2/TPLC_FB0/LVDS IOT61A/GCLKT_Z/TPLL_T_IN0/LVDS/DQS0/DQ0 IOT61B/GCLKC_Z/TPLL_C_IN0/LVDS/IDQS0/DQ0 IOT63A/GCLKT_3/RPL0_D_TN0/LVDS/DQ0 IOT63B/GCLKC_3/RPL0_C_IN0/LVDS/DQ0 IOT66A/LVDS/IDQ0 IOT66B/LVDS/IDQ0 IOT66B/LVDS/IDQ0 IOT76B/LVDS/IDQ0 M13 M14 IOB65A/LVDS IOB65B/DOUT/LVDS IOB75A/GCLKT_6B/LVDS/DQS5/DQ5 IOB75B/GCLKC_6B/LVDS/DQS5/DQ5 IOB75B/GCLKC_0B/LVDS/DQ55/DQ5 IOTZZALVDS/DQ0 IOTZZALVDS/DQ0 IOTZZALVDS/DQ0 IOTZZALVDS/DQ1 IOTZZA | 10885A/LVDSI/DG4/IDQ4 | 10885B/LVDSI/DQ4/IDQ4 | 10887A/LVDSI/DQ4 | 10887B/LVDSI/DQ4 | 10889B/GCLKT_7/IBPLL_T_IN0/LVDSI/DQ4 | 10889B/GCLKT_7/IBPLL_C_IN0/LVDSI/DQ4 | 10881A/GCLKT_6A/LVDSI/DQ4 IOB91B/GCLKC 6A/LVDS/DQ GW5AJI V25,MG196S U31C IOB31A/GCLKT_10A/D14/BPLL_T_FB0/LVDS IOB31B/GCLKC_10A/D15/BPLL_C_FB0/LVDS IOB33A/GCLKT_9A/D13/BPLL_T_IN1/LVDS IOB33A/GCLKC_9A/EM/CCLK/BPLL_C_IN1/LVDS IOB37A/READY/LVDS F_CLK >>-RECONFIG_N R119 4.7K VCCIO5 READY R120 4.7K VCCIO4 U31G *Configuration reset section *Configurable detection section READY (QSPI_MCS_N VCCI00 C4 C5 VCCI01 C10 IOB37A/READY/LVDS IOB37B/MCS_N/CSO_B/LVDS IOB50A/D11/LVDS IOB50B/D12/LVDS IOB52B/MODE1/LVDS IOB52B/D10/LVDS VCCIO0 VCCIO0 VCCIO1 VCCIO2 VCCIO2 VCCIO2 VCCIO2 VCC/VCCC VCC/VCCC VCC/VCCC VCC/VCCC VCC/VCCC VCC/VCCC VCCIO4 R122 R121 R121 R121 R121 MODE0 MODE1 DONE >> MODE1 >> LED11 R123 1K R124 1K VCCIO4 QSPI_MI2 QSPI_MI3 IOB54A/GCLKT_11B/D01/MI2/BPLL_T_FB1/LVDS IOB54B/GCLKC_11B/D02/MI3/BPLL_C_FB1/LVDS *Configuration completed IOBS6ALVDS IOBS6BLVDS IOBS6BLVDS IOBS6BLVDS IOBS8B/MOSI/CSI_B/MIO/LVDS IOBS0B/MOSI/CSI_B/MIO/LVDS IOB60ALVDS IOB60ALVDS VCCIO3 VCCIO3 VCCIO4 VCCIO4 VCCIO4 VCC/VCCC VCC/VCCC VCC/VCCC VCC/VCCC VCC/VCCC VCC/VCCC *Configuration mode signal selection detection section QSPI_CCLK 6 VCCIO10NCCX 15 VCCIO10NCCX 16 VCCIO10NCCX 16 VCCIO10NCCX 17 VCCIO10NCCX 18 VCCI MODEO SONE ((-IOB62B/MODE0/LVDS VCCIO5 VCCIO6 VCCIO6 VCCIO6 VCCIO7 VCCIO7 VCCIO7 R125 4.7K RECONFIG.N > NST OBHARECONFIGN Flash VCCIO4 тск <<-4 VCCIO10/VCCX TDI << VCC1P8 L11 VQPS JTAG TDO >> C337 R126 4.7K R128 R127 4.7K 8 8 4 7uF 0.1uF 4.7K GW5A-I V25-MG196S 10 10 U32 TMS< QSPI_MCS_N 1 CS VCC 8 QSPI_MISO 2 DO HOLD 7 QSPI_CCLK GW5A-LV25-MG196S 3 WP CLK 6 IO4 6 101 VCCIO10/VCCX DI 5 QSPI_MOSI 4 GND VCC 5 2 GND ÷ R129 1K IO3 4 3 102 PUDC_B R131 NK NC VCICO0/1 *External Flash, used to *JTAG download section store downloaded programs *Configurable GPIO mode section A1 A14 C2 C3 C6 C7 D10 D5 D6 D9 E11 F7 F8 G6 G7 G8 H10 G4 P14 M7 M3 M11 L9 L6 L5 L3 L10 K8 J8 J7 J10 H9 H8 H7 H4 VSS - VCC/0P9 VCCIO10/VCCX C341 C342 C343 C344 C345 C346 C347 C348 C349 C350 C351 C352 C353 C354 U31E C355 C356 C357 C358 C359 C360 C361 C362 C363 D.1uF D.1uF D.1uF D.1uF D.1uF D.1uF D.1uF D.1uF IOR1A/TCK IOR1B/TDI IOR3A/TMS IOR3B/TDO VCCI00 VCCIO6 VCCIO7 L12 IOR35A C376 C377 C364 C365 C366 C367 C368 C369 C370 C371 C372 C373 C374 C375 C378 C379 C380 C381 C382 C383 GW5A-LV25-MG196S 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF To tue To tue 0.1uF <u>‡</u> GW5A-LV25-MG196S 1.F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide . 3.It is recommended that add an ESD protection chip to the JTAG download circuit. 4.VCC core voltage requires a large current, so it is recommended to supply power separately. 5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, GOWIN Minimum System Diagram Arora V 25K FPGA Products Programming and Configuration Guide. Document Number GW5A-LV25MG196S 2.3

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1.F CLK signal is an external input clock signal. It Is recommended that F CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora $\,V\,$ 25K FPGA Products Programming and Configuration Guide .

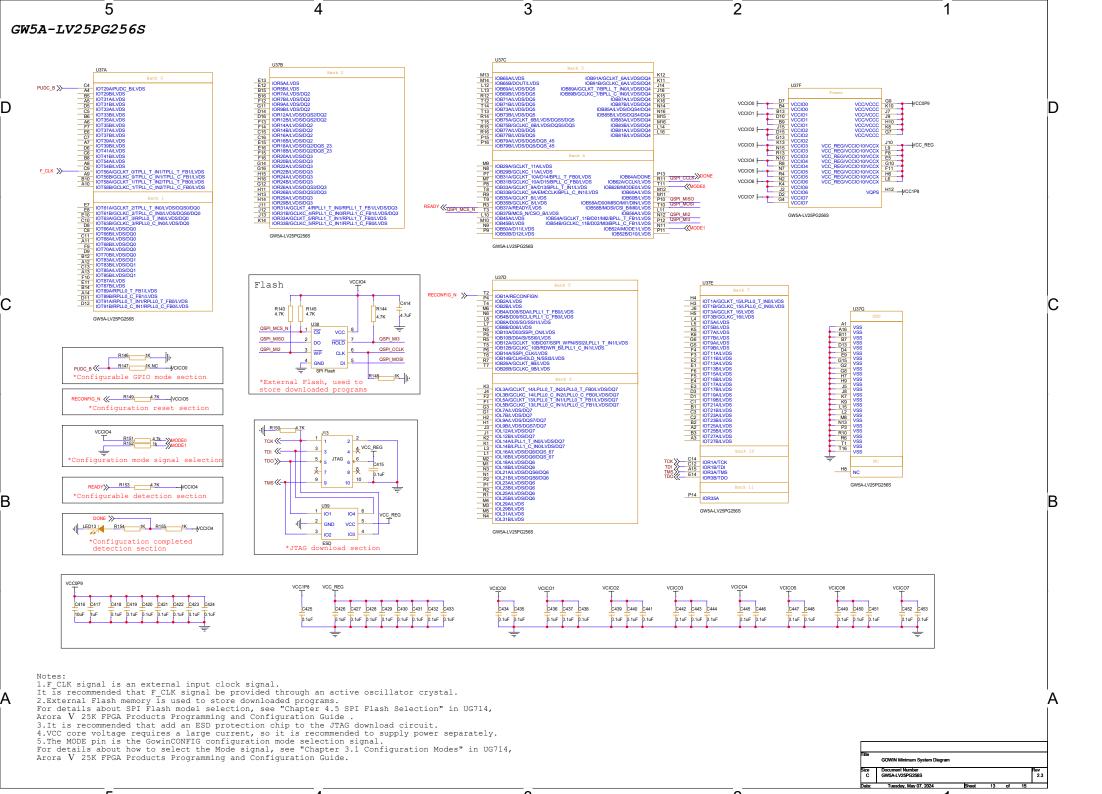
3.It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

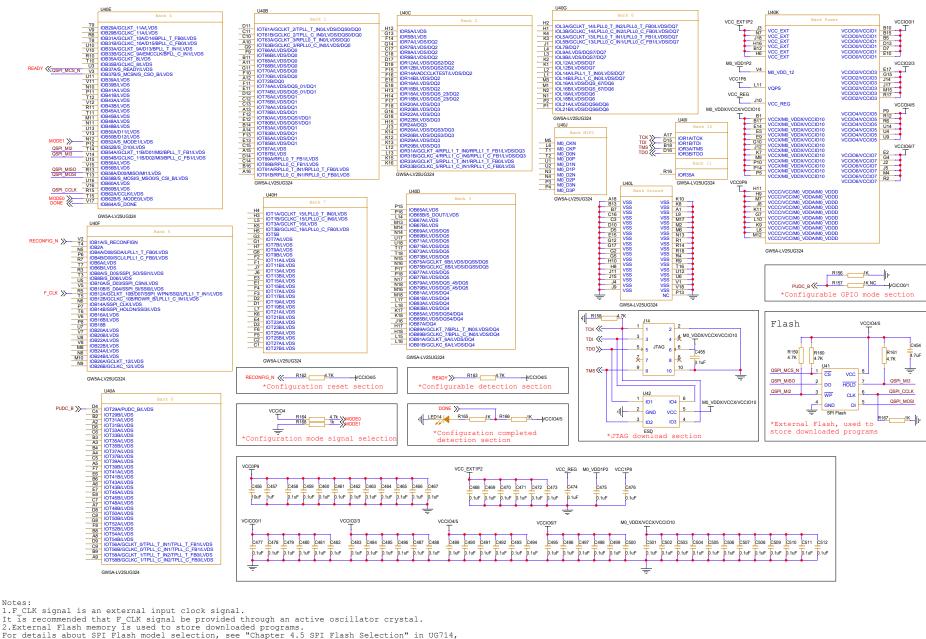
5. The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

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3.It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

5. The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

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GW5A-LV25UG324S 11434 U43D VCICO0/1 | 815 E10 D13 D13 D13 D13 B10 B10 VCCIO2/3 | R17 J14 J17 VCCIO4/5 | P9 R17 VCCIO4/5 | P9 | IOBBSALVDS | IOBSALVDS | IOBS IOT61A/GCLKT 2/TPLL T IN0/LVDS/DQS0/DQ0 P15 P16 L14 M13 M14 N14 U17 U18 T17 T18 N15 N16 P17 P18 N17 N18 M16 M18 L17 L18 K17 IOT29A/PUDC B/LVDS IOR5A/LVDS IOB65A/LVDS VCCI00/1 OT61B/GCLKC 2/TPLL C IN0/LVDS/DQS0/DQ0 OT63A/GCLKT 3/RPLL0 T IN0/LVDS/DQ0 IOR5B/LVDS IOR7A/LVDS/DQ2 VCCIO0/1 AND UNTERSCOLAR SHELL OF THE STATE OF THE ST IOR7B/LVDS/DQ2 IOR9A/LVDS/DQ2 IOT33B/LVDS IOT338/LVDS
IOT358/LVDS
IOT358/LVDS
IOT378/LVDS
IOT378/LVDS
IOT398/LVDS
IOT398/LVDS
IOT418/LVDS
IOT418/LVDS
IOT438/LVDS
IOT438/LVDS
IOT458/LVDS
IOT458/LVDS
IOT458/LVDS
IOT458/LVDS
IOT458/LVDS
IOT458/LVDS
IOT508/LVDS
IOT508/LVDS IOR9B/LVDS/DQ2 IOR12A/LVDS/DQS2/DQ2 IOR12B/LVDS/DQS2/DQ2 VCCIO2/3 | IOR128BLVDSIDOS2DD2 | IOR148LVDSIDO2 | IOR14BLVDSIDO2 | IOR148LVDSIDO2 | IOR168LVDSIDO2 | IOR168LVDSIDO2 | IOR168LVDSIDO2 | IOR168LVDSIDO3 | IOR168LVDSIDO3 | IOR20BLVDSIDO3 | IOR20BLVDSIDO3 | IOR20BLVDSIDO3 | IOR20BLVDSIDO3 | IOR24BLVDSIDO3 | IOR34BLVDSIDO3 | IOR34BLVDSIDO3 | IOR34BLVDSIDO3 | IOR34BLVDSIDO3 | IOR34BLVDSIDO3 | IOR34BLVDSIDO3 | VCCIO2/3 VCCIO2/3 VCCIO2/3 VCCIO4/5 VCCIO4/5 VCCIO4/5 VCCIO4/5 VCCIO4/5 VCCIO6/7 VCCIO6/7 VCCIO6/7 VCCIO6/7 VCC_REGIVCCID10VCCX
VCC_REGIVCCID10VCCX M9 E14 E5 G10 VCCIO6/7 J5 E2 G4 M4 J2 R2 - Fi3 OTSBALVDSD01
- Fi3 OTSBALVDSD01
- C15 OTSBALVDSD01
- C15 OTSBALVDSD01
- C17 OTSBALVDS
- C14 OTSBALVDS
- C18 OTSBALVDS
- C18 OTSBALVDS
- C18 OTSBARPLLD C FBILVDS
- C18 OTSBARPLLD C T MIRPLD C FBOLVDS
- C18 OTSBARPLLD C T MIRPLD C FBOLVDS
- C18 OTSBARPLLD C T MIRPLD C FBOLVDS IOT50B/LVDS IOT52A/LVDS IOT52B/LVDS IOT54A/LVDS IOT54B/LVDS IOR29ALVDS/DQ3 IOR29BLVDS/DQ3 IOR31A/GCLKT 4/RPLL1 T IN0/RPLL1 T FB1/LVDS/DQ3 IOR31B/GCLKC_4/RPLL1_C_IN0/RPLL1_C_FB1/LVDS/DQ3 IOR33B/GCLKT_5/RPLL1_T_IN1/RPLL1_T_FB0/LVDS IOR33B/GCLKC_5/RPLL1_C_IN1/RPLL1_C_FB0/LVDS GW5A-LV25UG324S F_CLK >> GW5A-LV25UG324S 07114ALVDS
07116LVDS
07116LVDS
07118ALVDS
07118ALVDS U43E J7 J6 E3 E1 A1 VSS A18 VSS B13 VSS B17 VSS C16 VSS G17 VSS IOB29A/GCLKT_11AIL/DS IOB29A/GCLKT_11AIL/DS IOB31A/GCLKT_10AD14/BPIL_T_FBUL/DS IOB31A/GCLKT_10AD14/BPIL_T_FBUL/DS IOB31A/GCLKT_9A/D13/BPIL_T_N1AIL/DS IOB33A/GCLKC_0AFEMCCLK/BPIL_C_N1/L/DS IOB33A/GCLKC_0AFEMCCLK/BPIL_C_N1/L/DS IOB35A/GCLKT_8/L/DS IOB35A/GCLKT_8/L/DS IOB35A/GCLKT_8/L/DS IOL3A/GCLKT_14/LPLL0_T_IN2/LPLL0_T_FB0IL/DS/DO7 IOL38/GCLKC_14/LPLL0_C_IN2/LPLL0_C_FB0IL/DS/DO7 IOL5A/GCLKT_13/LPLL0_T_IN1/LPLL0_T_FB1IL/DS/DO7 IOL58/GCLKC_13/LPLL0_C_IN1/LPLL0_C_FB1IL/DS/DO7 IOL7A/LVDS/BOQ7 IOL7A/LVDS/BOQ7 IOL7A/LVDS/BOQ7 IOL7A/LVDS/BOQ7 V2
T4
IOB1A/RECONFIGN
IOB2A/LVDS
NS
IOB2B/LVDS
P6
IOB2B/LVDS
IOB2B/LVDS
IOB2B/LVDS
IOB4A/DO8/SDA/LPLL1_T_FB0/LVDS
IOB4B/D09/SCL/LPLL1_C_FB0/LVDS V18
V1
U6
U12
T16
R9
R4
R18
R11
N13
M6
M2
M17
L9
K8
K10
J9 RECONFIG_N >>-F3
D2
D1
H4
H3
L7
K6
E4
D3
F6
F5
C2
C1
L5
K5
H6
H5
G3
G1
H7
G6 | IOB4B/IO09/SC/L/PLL1_C_FB | IOB6A/LVDS | IOB8B/LVDS | IOB8A/IO5/SO/SSI1/LVDS | IOB8B/IO6/LVDS | IOB10A/IO3/SSPI_CN/LVDS U. 10.781.VSSD0377007
U. 10.1003.VSSD0377007
U. 10.1003.VSSD0377007
U. 10.1281.VSSD0377007
U. 10.1281.VSSD037
U. 10.1481.PL.1.T. NOLVDSD037
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U. 10.1481.VSSD03 - IOBTOANDOSSEN CONTUDES - IOBTOBROUSINSSIOLVOS - IOBTOBROUSINSSIOLVOS - IOBTOBROCKIC TOBRODVIS BILPLL1_C_INTUVOS - IOBTOBROCKIC TOBRODVIS BILPLL1_C_INTUVOS - IOBTOBROCKIC TOBRODVIS - IOBTOBROCK IOB39A/LVDS IOB41B/LVDS IOB43A/LVDS IOB43B/LVDS Ţ | IOT27/ALVDS | IOT278/LVDS | IOT38/GCLKT_16/LVDS | IOT38/GCLKC_16/LVDS | IOT5A/LVDS | IOT5A/LVDS | IOT7A/LVDS | IOT7B/LVDS | IOT9B/LVDS | IOT9B/LVDS IOB45A/LVDS IOB45B/LVDS IOB16B/LVDS IOB18A/LVDS I OBBARALIVOS
OBSARADITA NOS
OBSARALIVOS
OBSARALIVOS IOB48A/LVDS | IOL23A/LVDS/IDQ6 | IOL25B/LVDS/IDQ6 | IOL25B/LVDS/IDQ6 | IOL25B/LVDS/IDQ6 | IOL27A/LVDS/IDQ6 | IOL27B/LVDS/IDQ6 | IOL29A/LVDS | IOL29B/LVDS | IOL21A/LVDS P13 MODE1 >> QSPI_MI2 QSPI_MI3 GW5A-LV25UG324S U15 V15 R13 IOR1A/TCK QSPI_MOSI T13 GW5A-I V25UG324S GW5A-LV25UG324S RECONFIG N (R169 4.7K VCCIO4/5 READY NCCIO4/5 R16 *Configuration reset section *Configurable detection section IOR35A DONE >> R171 1K 4.7k >>MODE0 R172 LED15 R173 1K R174 1K VCCIO4/5 PUDC B R176 1K NC VCICO0/1 R175 1k MODE1 Configuration completed Configurable GPIO mode section detection section Configuration mode signal selection VCCIO4/5 Flash TCK << C513 VCC0P9 VCC_REG VCC1P8 VCC_REG TDI <<-R179 4.7K R178 4.7K 4.7uF JTAG 6 TDO >> U44 8 × 10 QSPI MCS N C527 C528 C529 C530 C531 C532 C533 C534 C535 C536 C537 C538 C539 CS VCC C515 C516 C517 C518 C519 C520 C521 C522 C523 C524 C525 C526 0.1uF 2 DO QSPI_MISO QSPI_MI3 D.1uF 0.1uF HOLD TMS ((-QSPI MI2 3 WP QSPI_CCLK CLK GND DI 5 QSPI_MOSI VCICO0/1 VCCIO4/5 VCCIO6/7 U45 SPI Flash 104 6 101 VCC_REG VCC 5 *External Flash, used to C558 C559 C560 C561 C562 C563 GND C540 C541 C542 C543 C544 C545 C546 C547 C548 C549 C550 C551 C552 C553 C554 C555 C556 C557 store downloaded programs 103 4 3 IO2 0.1uF *JTAG download section I.F CLK signal is an external input clock signal.

It Is recommended that F_CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide . 3.It is recommended that add an ESD protection chip to the JTAG download circuit. 4.VCC core voltage requires a large current, so it is recommended to supply power separately. 5. The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

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