GW2AN-LV55UG676

U1B Bank1 — GW2AN-LV55UG676
U1D Bank3 — GW2AN-LV55UG676
U1F Bank5 — GW2AN-LV55UG676
U1A Bank0 — GW2AN-LV55UG676
U1I Power — GW2AN-LV55UG676
U1C Bank2 — GW2AN-LV55UG676
U1H Bank7 — GW2AN-LV55UG676
U1E Bank4 — GW2AN-LV55UG676
U1G Bank6 — GW2AN-LV55UG676
U1J Ground — GW2AN-LV55UG676

MODE0, MODE1, MODE2, RECONFIG_N, READY, DONE
MSPI_MISO, MSPI_MOSI, MSPI_CS, MSPI_CLK
JTAGSEL_N
F_CLK, TDI, TCK, TMS, TDO

Configuration completed detection section
DONE — LED1 — R1 1K — R2 4.7K — VCCO3

Configurable detection section
READY — R3 4.7K — VCCO3

Configuration reset section
RECONFIG_N — R6 4.7K — VCCO3

JTAG mode selection signal section
JTAGSEL_N — R9 1K

Configuration mode signal selection
R4 1K — MODE0
R5 1K — MODE1
R7 1K — MODE2

Flash
External Flash, used to store downloaded programs
MSPI_CS — CS, VCC
MSPI_MISO — DO, HOLD
WP, CLK — MSPI_CLK
R11 4.7K3, GND, DI — MSPI_MOSI
VCCO3, C80 0.1uF VCCO3, R10 4.7K, R12 1K
U2 SPI Flash

JTAG download section
R8 4.7K
TCK, TDI, TDO, TMS
J1 JTAG, C79 0.1uF, VCCO2
U3 ESD — IO1, IO4, GND, VCC, IO2, IO3, VCCO2

Notes:
1. F_CLK signal is an external input clock signal.
   It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
   For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.

Decoupling capacitors: C1 4.7uF, C2 0.01uF, C3–C39 0.1uF; C40–C78 0.1uF
VCC1P0, VCC, VCCPLLL, VCCPLLR, VCCX
VCCX, VCCO0, VCCO1, VCCO2, VCCO3, VCCO4, VCCO5, VCCO6, VCCO7
FB1, FB2, FB3