

Gowin FPGA Quad JTAG Interfaces Offline Programmer(OP720-4)

User Guide

UG301-1.4E,02/23/2024

Copyright © 2024 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

and are registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any denotes, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description	
07/10/2019	1.0E	Initial version.	
02/19/2020	1.1E	Programming security key added (GW2A).	
06/30/2022	1.2E	 The description of section 2.3.2 "Voltage Configuration Jumper Diagram" updated. The description of power supply updated. 	
11/07/2022	1.3E	 COM PORT option added on the interface of the updated Offline Programmer. The figures of external serial port cable connection added. 	
12/29/2023	1.3.1E	Supported products updated.	
02/23/2024	1.4E	 The descriptions of accessory list added. The descriptions of connecting offline programmer to PC updated. 	

Contents

C	ontents	i
Li	st of Figures	ii
Li	st of Tables	iii
1	About This Guide	1
	1.1 Purpose	1
	1.2 Supported Products	1
	1.3 Related Documents	1
	1.4 Terminology and Abbreviation	2
	1.5 Support and Feedback	2
2	Instructions for FPGA Offline Programmer	3
	2.1 Overview	3
	2.2 Using Offline Programmer	3
	2.2.1 Software Download and Driver Installation	4
	2.2.2 Connect Offline Programmer to PC	5
	2.2.3 Configuration Interface	8
	2.2.4 Configure to Programmer	10
	2.2.5 Password	11
	2.2.6 Program Four FPGA Devices Simultaneously	14
	2.2.7 Program One FPGA Automatically	15
	2.2.8 Program Security Key (GW2A)	16
	2.3 Diagram of Programmer Interface Connection and Description of Voltage Configuration	on17
	2.3.1 Programmer Interface Connection Diagram	17
	2.3.2 Voltage Configuration Jumper Diagram	17
	2.4 Instructions for FPGA Offline Programmer Firmware Update	19
	2.5 Notes	20
	2.6 Main Parameters	20
	2.7 Specification and Parameter	21
	2.8 Error code and Troubleshooting	21

List of Figures

jure 2-1 Accessory4	ŀ
jure 2-2 Driver Installation Completed5	5
jure 2-3 Version 1 Connection6	;
jure 2-4 Version 2 Connection (Sub-version A)7	,
jure 2-5 Version 2 Connection (Sub-version B)	}
jure 2-6 Software Configuration Interface9)
jure 2-7 Software Configuration Interface1	1
jure 2-8 Change Password1	2
jure 2-9 Password Change Completion1	3
jure 2-10 Password Configuration Interface1	4
jure 2-11 Programmer Exterior1	4
jure 2-12 Connecting Programmer to SocketBoard1	5
jure 2-13 Programming Security Key1	6
jure 2-14 Diagram of Programmer Interface Connection1	7
jure 2-15 Diagram of Vcc1 and Vcc2 Configuration Interface	7
jure 2-16 Vcc1 and Vcc2 Jumper1	8
jure 2-17 Diagram of Vcc1 and Vcc2 Configuration Completion	8
jure 2-18 Firmware Update1	9

UG301-1.4E ii

List of Tables

Table 1-1 Terminology and Abbreviations	2
Table 2-1 Firmware and Matched Programmer Type	20
Table 2-2 Reference Time of Programming	21
Table 2-3 Description of Error Code	21

UG301-1.4E iii

1 About This Guide 1.1 Purpose

1 About This Guide

1.1 Purpose

This guide includes two parts:

- 1. How to use FPGA Offline Programmer
- 2. Functional description of the Programmer

1.2 Supported Products

This guide describes quad JTAG interfaces offline programmer, and the type is OP720-4. The programmer in the guide applies to the following products:

- All products of LittleBee[®] family
- All products of Arora family (Arora V products excluded)

1.3 Related Documents

The latest user guides are available on our Website. Refer to the related documents at www.gowinsemi.com.

- DS100, GW1N series of FPGA Products Data Sheet
- DS117, GW1NR series of FPGA Products Data Sheet
- DS821, GW1NS series of FPGA Products Data Sheet
- DS861, GW1NSR series of FPGA Products Data Sheet
- DS841, GW1NZ series of FPGA Products Data Sheet
- DS891, GW1NSE series FPGA Products Data Sheet
- DS102, GW2A series of FPGA Products Data Sheet
- DS226, GW2AR series of FPGA Products Data Sheet
- DS971, GW2AN-18X & 9X Data Sheet

UG301-1.4E 1(22)

- DS976, GW2AN-55 Data Sheet
- DS961, GW2ANR series of FPGA Products Data Sheet

1.4 Terminology and Abbreviation

The terminology and abbreviations used in this manual are as shown in below Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DFU	Device Firmware Upgrade
FPGA	Field Programmable Gate Array
ID	Identification
JTAG	Joint Test Action Group

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com
E-mail: support@gowinsemi.com

UG301-1.4E 2(22)

2 Instructions for FPGA Offline Programmer

2.1 Overview

Offline programmer is a device that can program FPGA chips offline. It has the features of data confidentiality, portability, multi-interface programming, etc. It is suitable for large-scale, rapid production in factories, facilitating maintenance personnel when working remotely. The offline programmer can simultaneously program four FPGA devices or automatically detect and program devices through a single interface, greatly improving production efficiency.

The offline programmer employs the AES-128 advanced encryption algorithm to encrypt and store data securely. The encryption key is also stored after undergoing several rounds of encryption. AES is an internationally recognized, widely used, and secure encryption standard, ensuring the secure delivery of data.

2.2 Using Offline Programmer

Using the offline programmer software, you can manage the configuration of the offline programmer, including data stream file management, programming limit management, firmware upgrades for the programmer, etc. This software is compatible with Windows 7 and above operating systems. Once the configuration of the offline programmer is completed, it can be connected to the FPGA for programming.

Accessory List

- Offline programmer (OP720-4) x1
- 5V Power Supply x1 (Input: 100-240V-50/60Hz 0.6A, Output: DC 5V 2A)
- USB cable x1 (USB_A to USB_B)

UG301-1.4E 3(22)

• JTAG gray cable x1 (10-pin)

Figure 2-1 Accessory



2.2.1 Software Download and Driver Installation

The software and driver package can be downloaded at Gowin website: https://www.gowinsemi.com/en/support/devkits_detail/7/ or contact the local office or technical support. You can install the driver, and the path is driver\gowin_usb_driver.exe. After installation, use USB cable to connect the programmer and computer, and USB Serial Port (COMxx) appears on the port, that is, the driver is installed successfully, as shown in Figure 2-2.

Note!

If you have used Gowin USB programming download cable before, it does not need to install the driver.

UG301-1.4E 4(22)

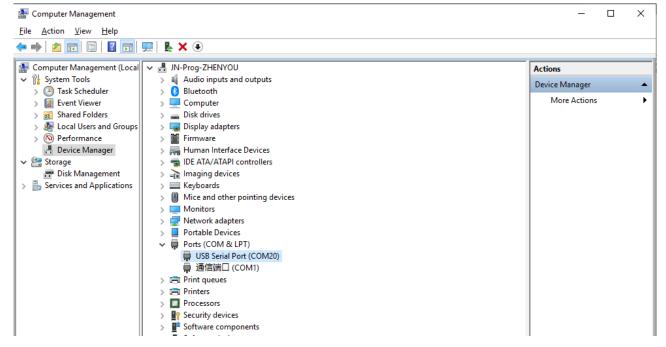


Figure 2-2 Driver Installation Completed

2.2.2 Connect Offline Programmer to PC

Version 1: Connect directly to the PC using the USB cable provided in the accessory, the PC can recognize the port number of the offline programmer.

UG301-1.4E 5(22)



Figure 2-3 Version 1 Connection

Version 2: Connect directly to the PC using the USB cable provided in the accessory, the PC can recognize the port number of the offline programmer.

Note!

Version 2 includes two sub-versions: Sub-version A and Sub-version B. The connection for Sub-version A is shown in Figure 2-5, which directly uses a USB cable to connect to the PC. For Sub-version B, you need to use the USB to TTL cable provided in the accessory to connect to the PC, and the connection is shown in Figure 2-5. Only three wires RXD, TXD, and GND are required.

UG301-1.4E 6(22)



Figure 2-4 Version 2 Connection (Sub-version A)

UG301-1.4E 7(22)

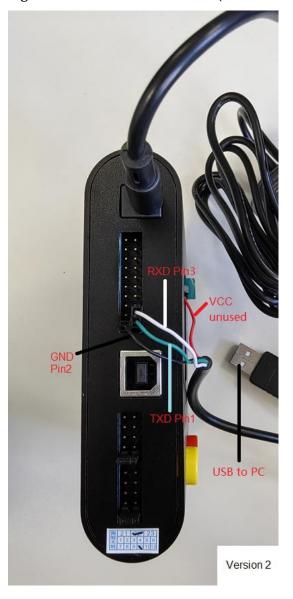


Figure 2-5 Version 2 Connection (Sub-version B)

2.2.3 Configuration Interface

OPmanager.exe is the associated software in the "bin" directory. Open OPmanager.exe, and the configuration options are shown in Figure 2-6.

UG301-1.4E 8(22)

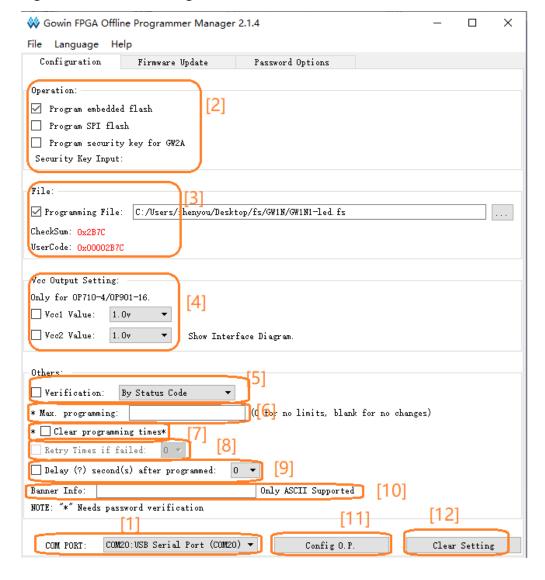


Figure 2-6 Software Configuration Interface

- 1. Select a port.
- Operation: Program embedded Flash, program external SPI Flash, or program security key. The checked is the operation performed by the programmer. If you choose to program the security key (only the GW2A series is supported), you need to enter the security key, which cannot be changed after it is written.
- 3. Programming File: The selected one is GW1N1-led.fs. Open the management tool and generate the key randomly, encrypt the data stream files and store them in the programmer.
- 4. Vcc1 and Vcc2 output setting requires manual adjustment of jumper. After adjustment, the boot interface will display the configured Vcc1 and Vcc2 voltage.

Note!

UG301-1.4E 9(22)

The output can be: 1.2V 1.5V 1.8V 2.5V 3.3V, and the default is 1.0v without adjusting jumper. Vcc2 configuration is the same as Vcc1, as shown in Figure 2-15.

5. Verification: Status code, Read-back, and No verification.

Note!

- Status code: Determine whether the programming is successful or not according to the status code read from the FPGA after finishing programming data stream files.
- Read-back: Determine whether the programming is successful or not according to the consistency of writing and reading after finishing programming data stream files.
- No verification, that is, only prompting the finishing of programming
- 6. The max. programming times: If it sets 100, "programming times: Error" will pop up on the LCD of the offline programmer if the programming times are greater than 100. This is valid only if the password is configured correctly.
- 7. Clear programming times: Check to clear programming times, which is valid with password configuration.
- 8. Retry times if failed: Retry x times automatically if failed, and error will be reported if x times fails.

Note!

Retry times settings are not supported for the time being.

- 9. Delay after programmed: Delay x seconds after programmed; Vcc1 and Vcc2 power off, and the result of programming is prompted.
- 10. Customized information: Any entering customized character will be displayed on the programmer screen after configuration.
- 11. Configure to programmer: Configure the checked information items to programmer.
- 12. Restore factory settings: You can clear the password, clear fs file information, and the number of programming times.

2.2.4 Configure to Programmer

The associated software is required to configure the programmer. Open OPManaer.exe software to configure, as shown in Figure 2-7. The steps are as follows:

- 1. Select operation content (that is, press the programming button of the Programmer).
- 2. Select data stream file (only support .fs format at present).
- 3. Verification selection: Select according to the status code.

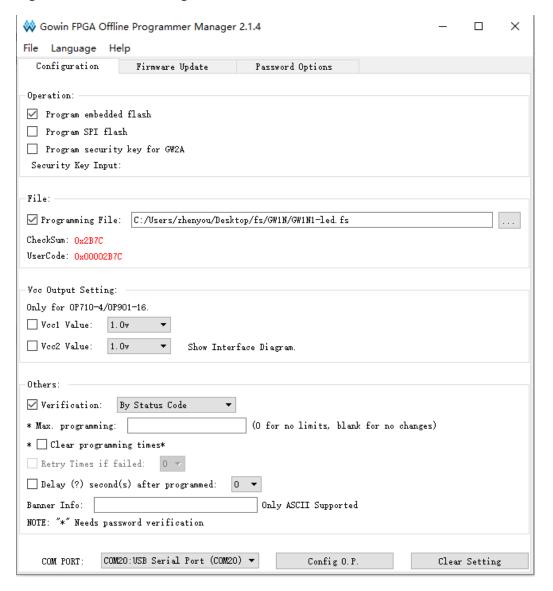
UG301-1.4E 10(22)

- 4. Set the max. programming times or leave it blank.
- 5. Click the "Config O.P." button.
- Reboot the programmer after configuration.

Note!

For the item with *, it needs correct password check to configure to the programmer. If the password is not correct, it will show that the password check fails, but the configuration of other items to the programmer will not be affected.

Figure 2-7 Software Configuration Interface



2.2.5 Password

Configure the max. programming times and clear programming times, it needs to enter the password of the current offline programmer and update it to the local before configuring to the programmer. If the password is incorrect, there is no permission to configure the max. programming

UG301-1.4E 11(22)

times and clear programming times. For the first time to use, steps are as follows:

- 1. When the new offline programmer is first used, the default factory password is 00000000.
- 2. Enter the original password 00000000, then enter the new password such as 12345678, confirm the password.

Note!

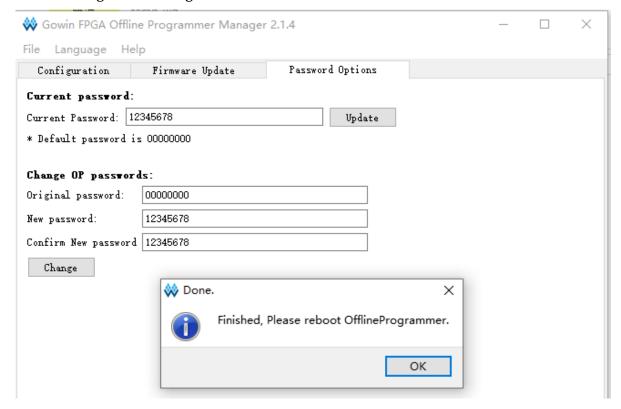
The new password can be set to any 8 digits.

- 3. Click "Change" to change the password of the offline programmer.
- 4. Click "Update" to obtain permission: Set the max. programming times and clear the programming times.

A password has been set for the programmer. The steps are as follows:

- 1. Enter the password of the programmer, such as: 1111111, click "Update".
- 2. Configure the max. programming times and clear programming times.
- 3. If the password is incorrect, the programming times and clearing programming times can not be configured, and other configuration items are not affected.

Figure 2-8 Change Password



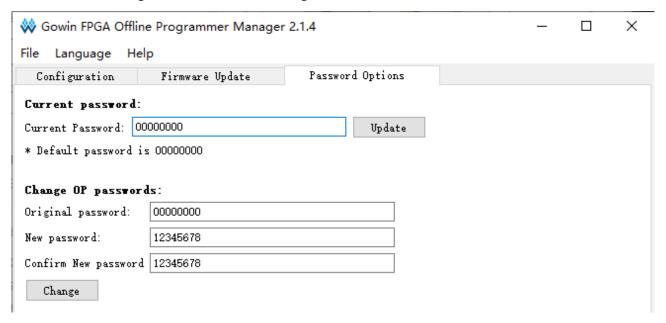
UG301-1.4E 12(22)

W Gowin FPGA Offline Programmer Manager 2.1.4 File Language Help Firmware Update Configuration Password Options Operation: Program embedded flash Program SPI flash Program security key for GW2A Security Key Input: Programming File: C:/Users/zhenyou/Desktop/fs/GW1N/GW1N1-led.fs CheckSum: 0x2B7C W Done. Х UserCode: 0x00002B7C Finished, Please reboot OfflineProgrammer. Vcc Output Setting: Only for OP710-4/OP901-16. ОК Vcc1 Value: 1.0v Vcc2 Value: 1.0v Show Interface Diagram. Others: ✓ Verification: By Status Code * Max. programming: 100 (O for no limits, blank for no changes) *
Clear programming times* Retry Times if failed: 0 🔻 ☐ Delay (?) second(s) after programmed: Banner Info: Only ASCII Supported NOTE: "*" Needs password verification COM20:USB Serial Port (COM20) ▼ Config 0.P. Clear Setting COM PORT:

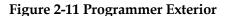
Figure 2-9 Password Change Completion

UG301-1.4E 13(22)

Figure 2-10 Password Configuration Interface



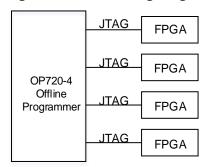
2.2.6 Program Four FPGA Devices Simultaneously





UG301-1.4E 14(22)

Figure 2-12 Connecting Programmer to SocketBoard



Note!

The four FPGAs are of the same type.

The quad JTAG programming interfaces share the TCK, TDI, and TMS signal lines. After the programmer sends commands, the four FPGAs responds and can be programmed simultaneously. Operation steps of programing four FPGA devices simultaneously are as follows:

- 1. Power up and boot the programmer (support USB power supply or 5V power supply).
- 2. Connect four FPGAs to the programmer.
- Press the green Program key, the screen displays detecting the device and the corresponding ID CODE is displayed after the device is detected. The corresponding indicator turns green after the programming is done successful.

Note!

In this mode, n (<=4) FPGAs can be programmed if they are connected. The programming interfaces of 1.2.3.4 can be selected as desired.

2.2.7 Program One FPGA Automatically

In the automatic programming mode, the programmer can automatically detect the new FPGA. It will program automatically if a new FPAG is connected. Currently, automatically programming only supports one FPGA, and only interface 1 of the programmer supports detecting and programming automatically. Operation steps of programing one FPGA automatically are as follows:

- 1. Power up and boot the programmer (Support USB power supply or 5V power supply).
- 2. "AUTO-PRO-MODE" will be displayed after pressing the program key for 5 seconds, and then the programmer enters the auto programming mode.
- 3. Connect one FPGA to interface 1.

UG301-1.4E 15(22)

- 4. The screen displays detecting the device and the corresponding ID CODE is displayed after the device is detected. The corresponding indicator turns green after the programming is done successful.
- 5. Disconnect the FPGA from the interface1, and then connect it to the interface 1 again. The programmer will automatically program the stream file to the FPGA device, and you do not need to press the green programming key.

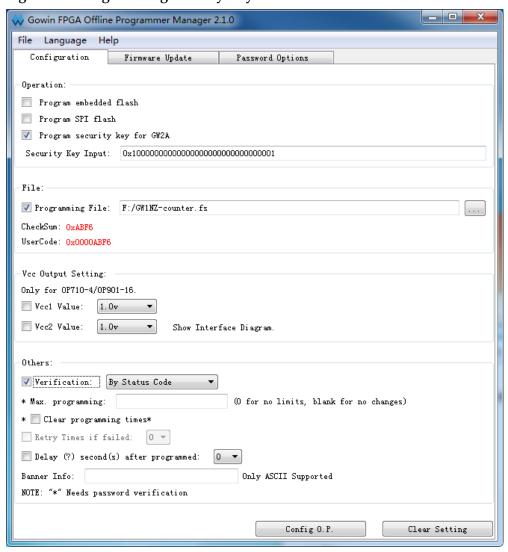
Note!

The automatic detection is used to detect whether there is a device connecting the programmer; if a device is connected, it will be programmed automatically. If not, the programmer will continue detecting and waiting for the new device.

2.2.8 Program Security Key (GW2A)

Only support single interface to program the security key, and the first access one is valid.

Figure 2-13 Programming Security Key



UG301-1.4E 16(22)

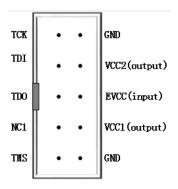
The steps are as follows:

- 1. Check "Program security key for GW2A" (AES) and enter the security key.
- 2. Click "Config O.P."
- 3. Reboot the device.
- 4. Connect the FPGA to the first interface.
- 5. Press program button, after programming finishing, re-program is not allowed.

2.3 Diagram of Programmer Interface Connection and Description of Voltage Configuration

2.3.1 Programmer Interface Connection Diagram

Figure 2-14 Diagram of Programmer Interface Connection

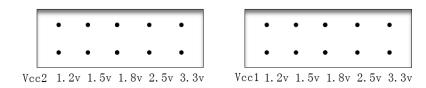


Note!

- The voltage output for the FPGA device is set to 3.3V.
- EVCC is the input voltage, which is the VCCIO voltage of the FPGA chip.
- Vcc1 and Vcc2 are configurable output voltage.

2.3.2 Voltage Configuration Jumper Diagram

Figure 2-15 Diagram of Vcc1 and Vcc2 Configuration Interface



UG301-1.4E 17(22)

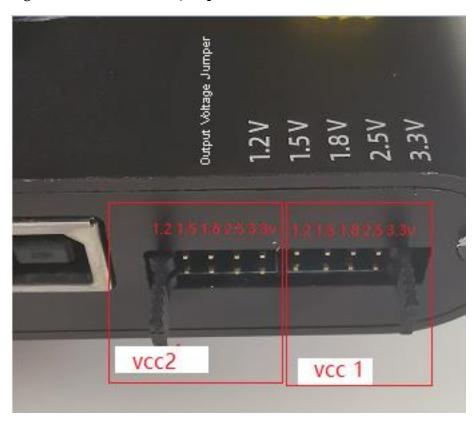
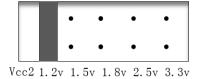
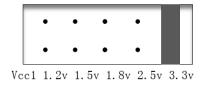


Figure 2-16 Vcc1 and Vcc2 Jumper

The programmer can configure Vcc output voltage by jumper. If jumper is not used, the default output is 1.0V. The output can be configured as 1.2V, 1.5V, 1.8V, 2.5V, 3.3V by using jumper. As shown in Figure 2-17, Vcc1 jumper is inserted at 1.2V and Vcc2 is inserted at 3.3V, that is, Vcc1 is configured as 1.2V and Vcc2 as 3.3V. After the jumper is inserted, restart the programmer, and the second screen upon startup will display Vcc1 as 1.2V and Vcc2 as 3.3V.

Figure 2-17 Diagram of Vcc1 and Vcc2 Configuration Completion

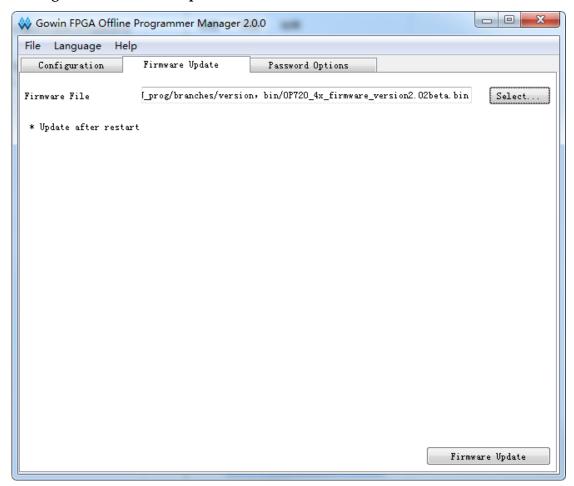




UG301-1.4E 18(22)

2.4 Instructions for FPGA Offline Programmer Firmware Update

Figure 2-18 Firmware Update



The firmware update steps are shown below:

- 1. Connect the programmer to PC with USB cable
- 2. Select firmware to update, such as OP720_4x_firmware_version2.02beta.bin.
- 3. Click the firmware update, wait for the prompt box to restart device, and reboot the offline programmer to complete the update.

Note!

Firmware update is to update the offline programmer so that the latest features can be used

The link for the latest firmware:

https://www.gowinsemi.com/en/support/devkits_detail/7/

UG301-1.4E 19(22)

The downloaded firmware should match the offline programmer, as shown in Table 2-1.

Table 2-1 Firmware and Matched Programmer Type

Firmware Name	Matched Programmer Type
OP710_4x_firmware_version1.9x.bin	OP710-4 (Blue Shell)
OP720_4x_firmware_version2.0x.bin	OP720-4 (Balck Shell)
OP901_16x_firmware_version2.0x.bin	OP901-16

2.5 Notes

- 1. If the firmware is upgraded with mismatched firmware, resulting in abnormal programmer, it needs to follow the steps as below to fix:
 - a). The programmer powers off and shuts down
 - b). Press the programming button to start and the indicator turns red
 - c). Select the correct firmware and re-upgrade.
- When multiple devices are programed simultaneously, only the same series of devices are supported. For example, all the GW1N-1 devices or all the GW1N-4 devices.
- 3. The data stream file is configured in the offline programmer. Select the FPGA to be programmed according to the screen prompt: "currently support: GW1N(R)-x", to avoid other damage to the FPGA.

2.6 Main Parameters

Power Supply

Operating voltage: DC5V±10%

- Power: 0.75 W

- Output voltage: Adjustable

Note!

The power supply needs to meet 5V1A, otherwise there will be a problem that Vcc1 and Vcc2 are equal to 0.

Memory

Embedded memory: 8MByte

Reference time of programming

UG301-1.4E 20(22)

Table 2-2 Reference Time of Programming

Chip Type Supported	Programming Time (ms)
GW1N-1	5312
GW1N-2	5312
GW1N(R)-4	5312
GW1N(R)-9	6278
GW1NZ	4600
GW1NS-2	4500

Note!

- In JTAG mode, the data can be programed into the embedded Flash of the FPGA.
- The programming time is the sum of the time used for erasing the embedded Flash and the time used for successfully programming the data stream file into the FPGA's embedded Flash. The time required for programming a single interface is the same as the time required for programming four interfaces.

Vcc1 and Vcc2 output voltage can be configured as: 1.0V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V.

2.7 Specification and Parameter

Operating environment: 0-60[°]C

Host Dimensions: 120 mm * 106 mm * 26 mm

• Screen: Resolution (128*160) size (32mm*38mm)

Host Net: 350g

2.8 Error code and Troubleshooting

After programming or if programming is successful, it will prompt: Programmed successfully and displayed STA: 0x1f020 or STA:0x3f020. If the device is abnormal, an error code will be reported, and the meaning of error code is shown in Table 2-3.

Note!

STA is the abbreviation of status code.

Table 2-3 Description of Error Code

Error Code	Description	Troubleshooting
E01	POR error	_
E02	Gowin VLD error	-
E03	Device error	Detects whether the connected device matches the data stream file.

UG301-1.4E 21(22)

Error Code	Description	Troubleshooting
E04	No access device	Checks whether the device is connected and the device is powered.
E05	Failed to open data stream file	Reconfigures the data stream file to the programmer.
E06	Programming failure	Reprogram, retry 3 times.
E07	The programming is completed, and the device is disconnected.	Failure in reading back due to JTAG multiplexing.

UG301-1.4E 22(22)

