

GW5RAT-LV15MG132P QSPI_MI2 P8
QSPI_MISO N8
QSPI_CCLK P9
QSPI_MCS_N N9
QSPI_MGS_N N9
QSPI_MI3 P10
QSPI_MOSI N10
M8 IOB3A/D02/MI2/LVDS IOB5A/CCLK/LVDS IOB5B/MCS_N/LVDS M0_CKP M0_CKN M0_D0P M0_D0N M0_D1P M0_D1N M0_D2P M0_D2N M0_D3P M0_D3N IOB7A/D03/MI3/LVDS B3 C3 B6 C6 B8 C8 B12 C12 Q0_LN0_TXP_O Q0_LN0_TXM_O Q0_LN1_TXP_O Q0_LN1_TXM_O Q0_LN2_TXM_O Q0_LN2_TXM_O Q0_LN3_TXP_O Q0_LN3_TXP_O Q0_LN3_TXM_O Q0_LN0_RXP_I Q0_LN0_RXM_I Q0_LN1_RXM_I Q0_LN1_RXM_I Q0_LN2_RXM_I Q0_LN2_RXM_I Q0_LN3_RXM_I Q0_LN3_RXM_I A2 A4 A5 A10 A11 A13 A14 L3 M3 M1 M2 N1 N2 P1 P2 IOL29A/DONELVDS
IOL29B/RECONFIG NLVDS
IOL39B/RECONFIG NLVDS
IOL314B/GCLT S/MODE/ILVDS
IOL314B/GCLT S/MODE/ILVDS
IOL314B/GCLT S/MODE/ILVDS
IOL33B/GCLT A/PLL_T NIPLPL_T FB0/CSO_B/DOUT/SCLL/VDS
IOL33B/GCLT A/PLL_T C NIPLPL_C FB0/CS/B/SDAL/VDS
IOL33B/GCLT A/PLL_C NIPLPL_C FB0/CS/B/SDAL/VDS RECONFIG N >> MODE1 >> MODE0 >> A8 Q0_REFCLKP_0 Q0_REFCLKM_0 Q0_REFCLKP_1 Q0_REFCLKM_1 IOL35R/D05/SSPI CS N/LVDS GW5ART-LV15-MG132F GW5ART-LV15-MG132P Q0_VDDA(Q0_VDDRC_LN0/1/2/3/Q0_VDDTC/Q0_VDDTC_LN0/1/2/3 Q0_VDDA(Q0_VDDRC_LN0/1/2/3/Q0_VDDTC/Q0_VDDTC_LN0/1/2/3 Q0_VDDA(Q0_VDDRC_LN0/1/2/3/Q0_VDDTC/Q0_VDDTC_LN0/1/2/3 Q0_VDDA(Q0_VDDRC_LN0/1/2/3/Q0_VDDTC/Q0_VDDTC_LN0/1/2/3 Q0 VDDA0P9 [-R23 Flash тск 🔆 Q0_VDDT0P9 GU_B4 Q0_VDDT_LN0/Q0_VDDT_LN1/Q0_VDDT_LN2/Q0_VDDT_LN3 Q0_VDDT0P9 C7
Q0_VDDHA1P8 C7
Q0_VDDHA
Q0_VDDHA 4 VCCIO4 C84 B1 B5 B7 B9 B11 B14 D3 E12 L2 M6 JTAG 6 6 VSS VSS VSS VSS VSS VSS VSS VSS VSS R24 4.7K R25 4 7K R26 4.7K TDO>>> 4.7uF C85 VCCIO2 M9 --- VCCIO2 8 8 10.1uF E2 M1_VDDA_LN0/M1_VDDA_LN1/M1_VDDA_LN2 Z 7 VCCIO3 M4 VCCIO3 U9 ÷ M_VDDX C2 M0_VDDX/M1_VDDX QSPI_MCS_N 1 CS 10 VCCIO4 F3 VCCIO4 vcc M0_VDDA0P9 M5 M0_VDDA QSPI_MISO 2 DO QSPI MI3 VCCX VCCX VCCX VCCX HOLD 3 WP QSPI CCLK QSPI MI2 CLK QSPI_MOSI IO4 6 4 GND DI 101 VQPS L12 VQPS1P8 VCCIO4 SPI Flash GW5ARTJ V15JMG132P 2 GND VCC 5 VCC_REG F12 VCC_REG *External Flash, used to 3 IO2 IO3 4 DPHY_VDD12 M7 ____DPHY_VDD1P2 store downloaded programs *JTAG download section VCC/VCCB/VCC GW5ART-LV15-MG132P READY >> R28 4.7K VCCIO2 *Configurable detection section В RECONFIG_N R29 4.7K VCCIO3 M1_VDDA0P9 M_VDDX M0_VDDA0P9 VQPS1P8 VCC_REG DPHY_VDD1P2 PSRAM VDD1P8 Q0 VDDA0P9 Q0 VDDHA1P8 *Configuration reset section C98 C99 C86 C87 C103 C104 C93 C94 C95 C96 C97 C100 C101 C102 n tuE 0.1uF 0.1uE 0.1uF 0.1uF 100uF 10uF 1uF n tuE 100uF 10uF 1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF MODE0 (R30 4.7K VCCIO3 R31 1K MODE1 << VCC0P9 VCCX VCCIO2 Q0 VDDT0P9 *Configuration mode signal selection C106 C107 C108 C109 C110 C111 C112 C113 C114 C115 C116 C117 C118 C119 C120 C122 C123 C124 C125 C121 0.1uF 100uF 10uF 1uF 0.1uF R32 1K VCCIO3 ÷ ÷ DONE >> R33 1K LED3 *Configuration completed detection section Notes: 1.F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
4.VCC core voltage requires a large current, so it is recommended to supply power separately. 5. The MODE pin is the GowinCONFIG configuration mode selection signal.

3

5

