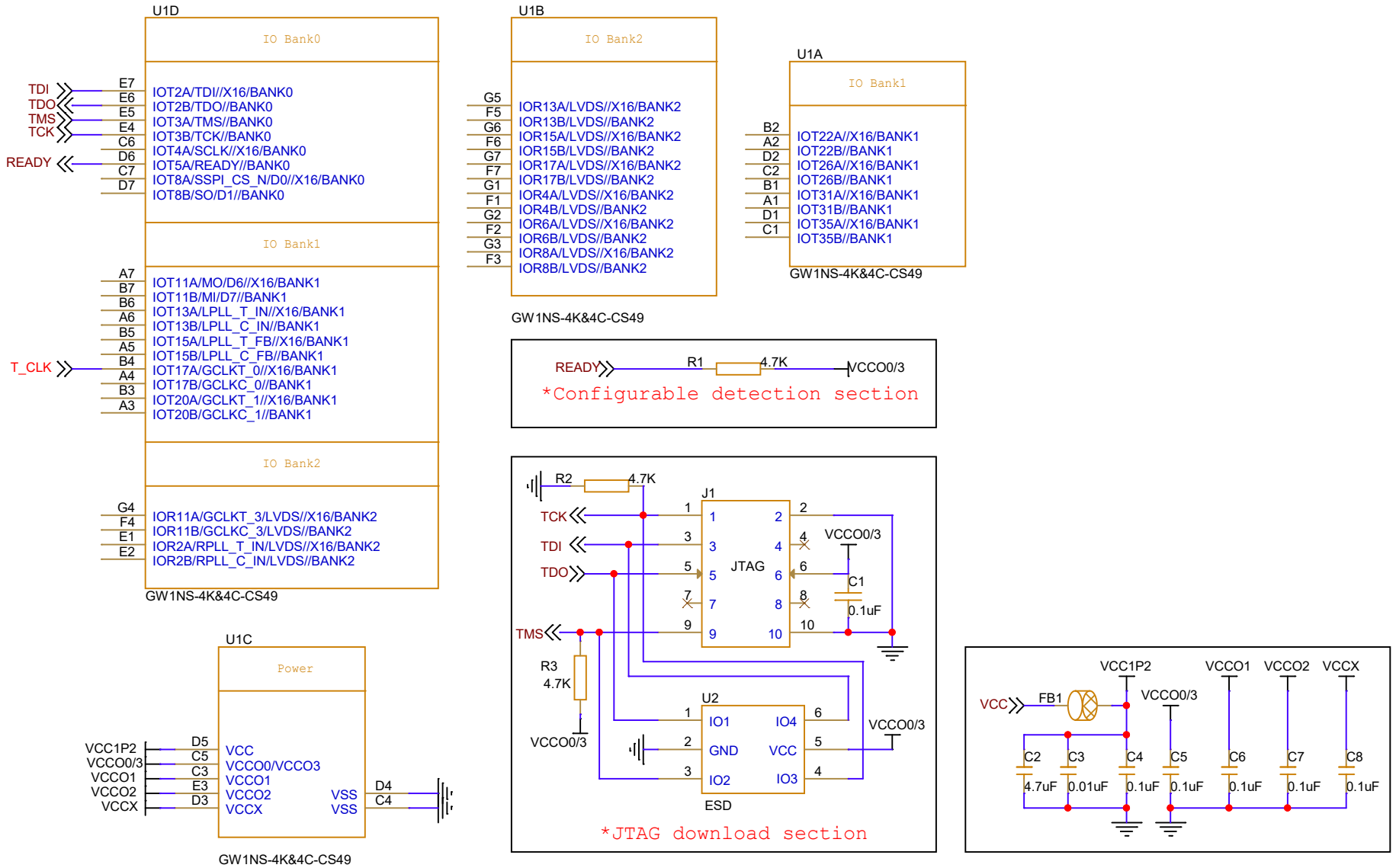
GW1NS-LV4CS49 & GW1NS-LV4CCS49

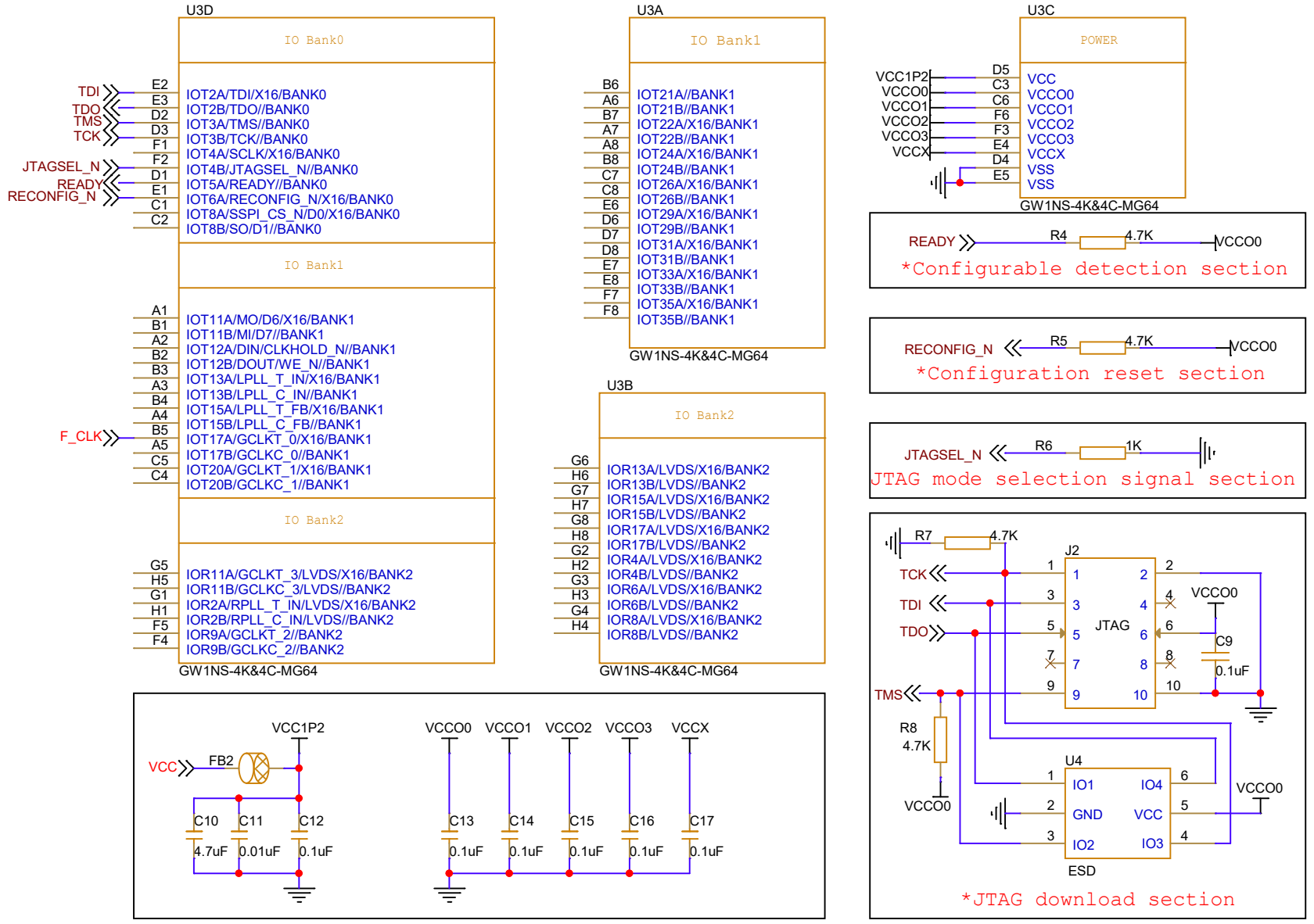


Notes:

1. F_CLK signal is an external input clock signal.
   It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.
3. The CS49 package supports GW1NS-4 & GW1NS-4C.

Title	GOWIN Minimum System Diagram	
Size A4	Document Number GW1NS-LV4CS49 & GW1NS-LV4CCS49	Rev 2.2
Date: Tuesday, April 16, 2024	Sheet 1 of 4	

GW1NS-LV4MG64 & GW1NS-LV4CMG64

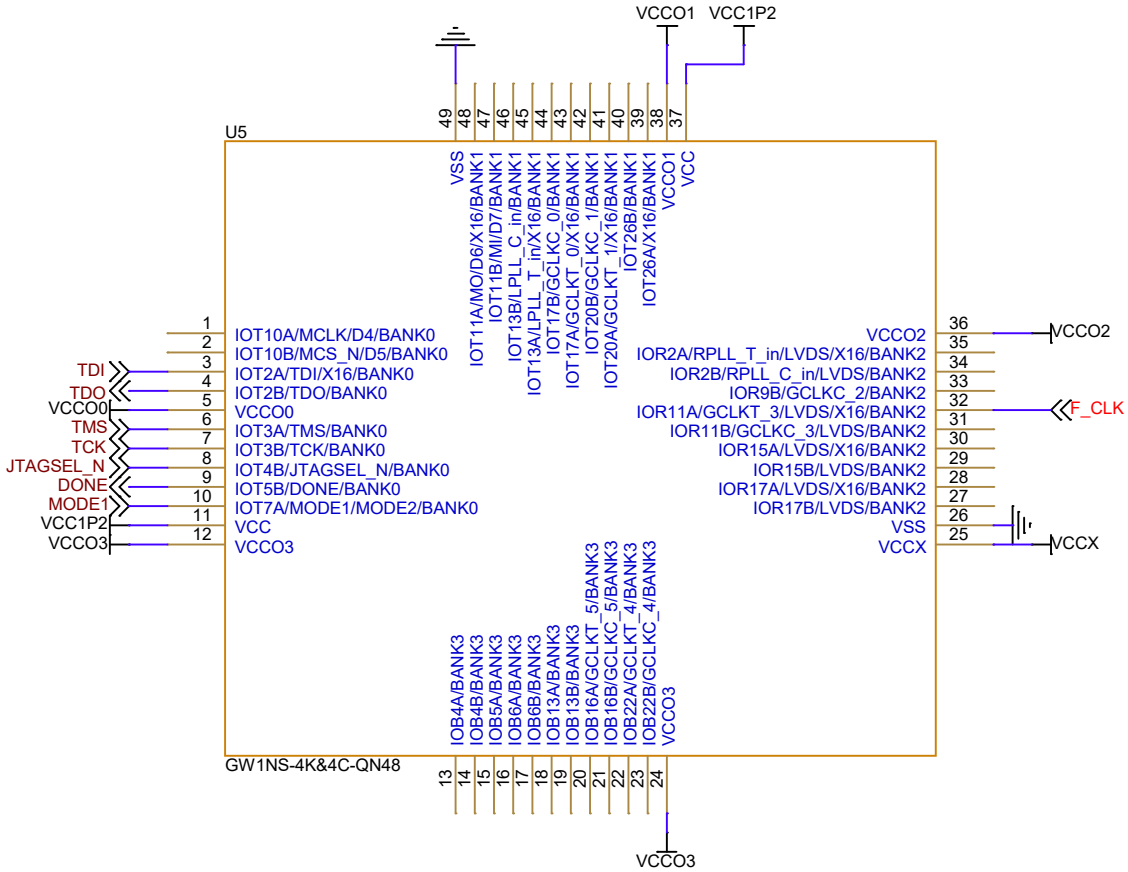


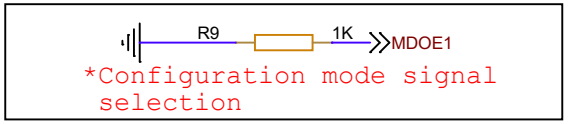
Notes:

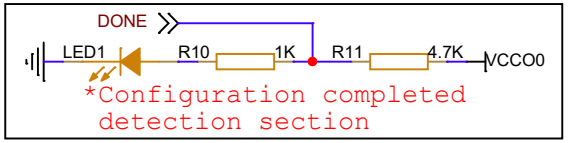
1. F_CLK signal is an external input clock signal.
   It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.
3. The MG64 package supports GW1NS-4 & GW1NS-4C.

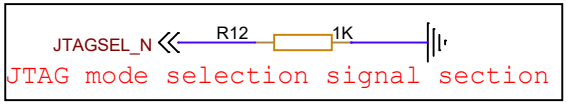
Title	GOWIN Minimum System Diagram	
Size A4	Document Number GW1NS-LV4MG64 & GW1NS-LV4CMG64	Rev 2.2
Date: Wednesday, April 10, 2024	Sheet 2 of 4	

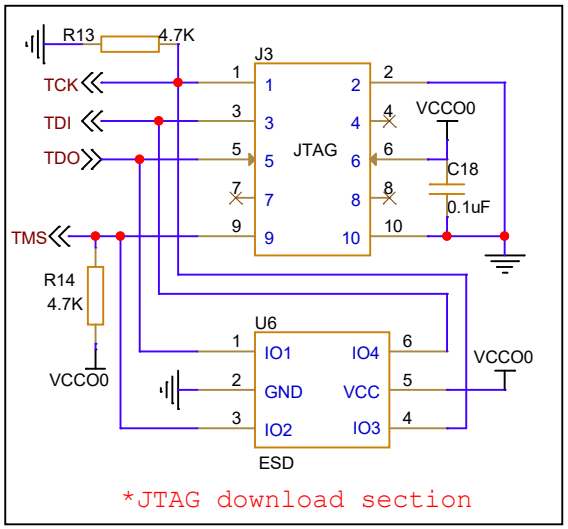
GW1NS-LV4QN48 & GW1NS-LV4CQN48

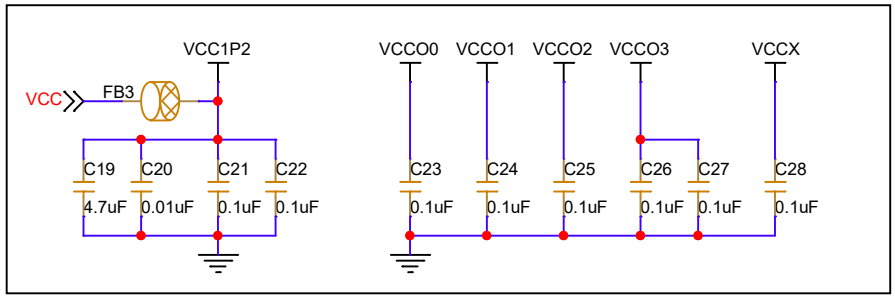








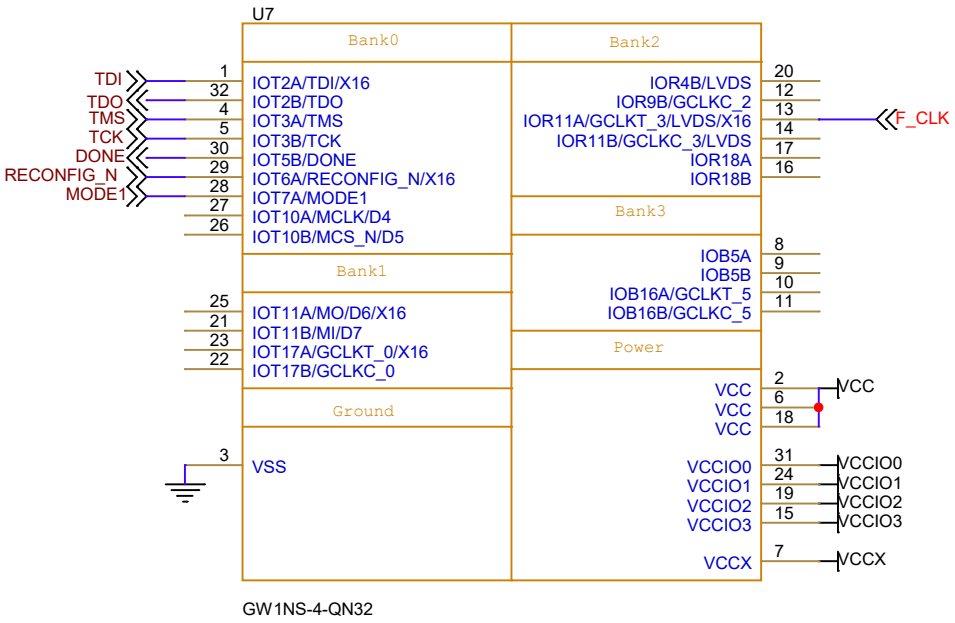


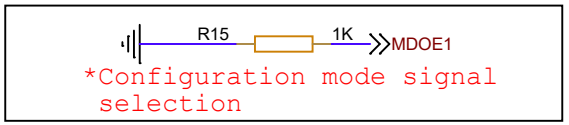


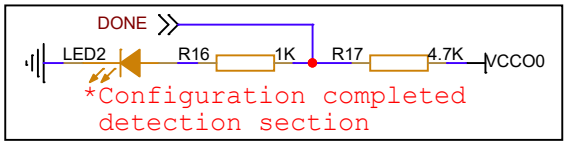
Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.
3.The QN48 package supports GW1NS-4 & GW1NS-4C.

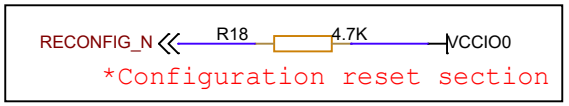
Title	GOWIN Minimum System Diagram	
Size A4	Document Number GW1NS-LV4QN48 & GW1NS-LV4CQN48	Rev 2.2
Date: Wednesday, April 10, 2024	Sheet 3 of 4	

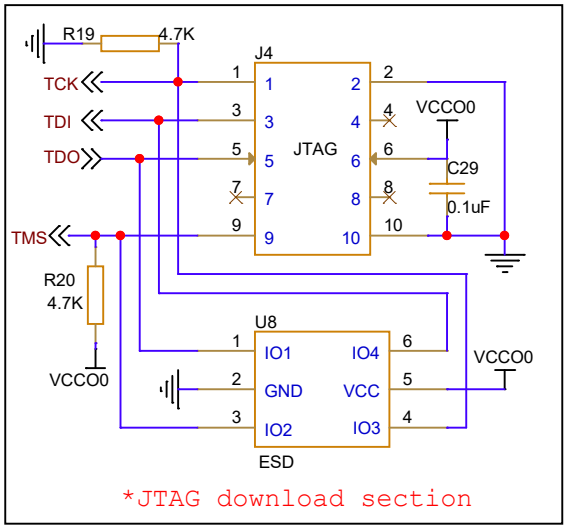
GW1NS-LV4QN32

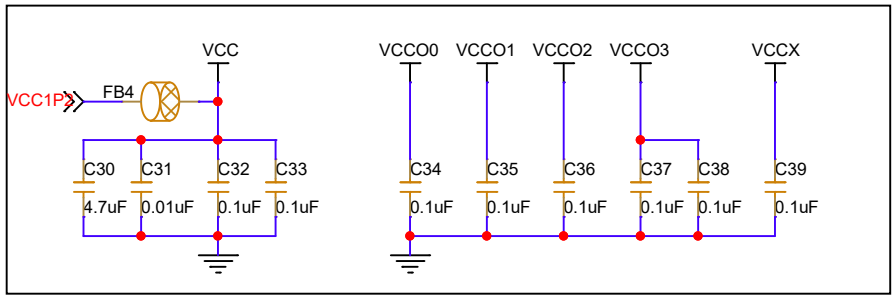












Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title: GOWIN Minimum System Diagram		
Size: A4	Document Number: GW1NS-LV4QN32	Rev: 2.2
Date: Wednesday, April 10, 2024	Sheet 4 of 4	