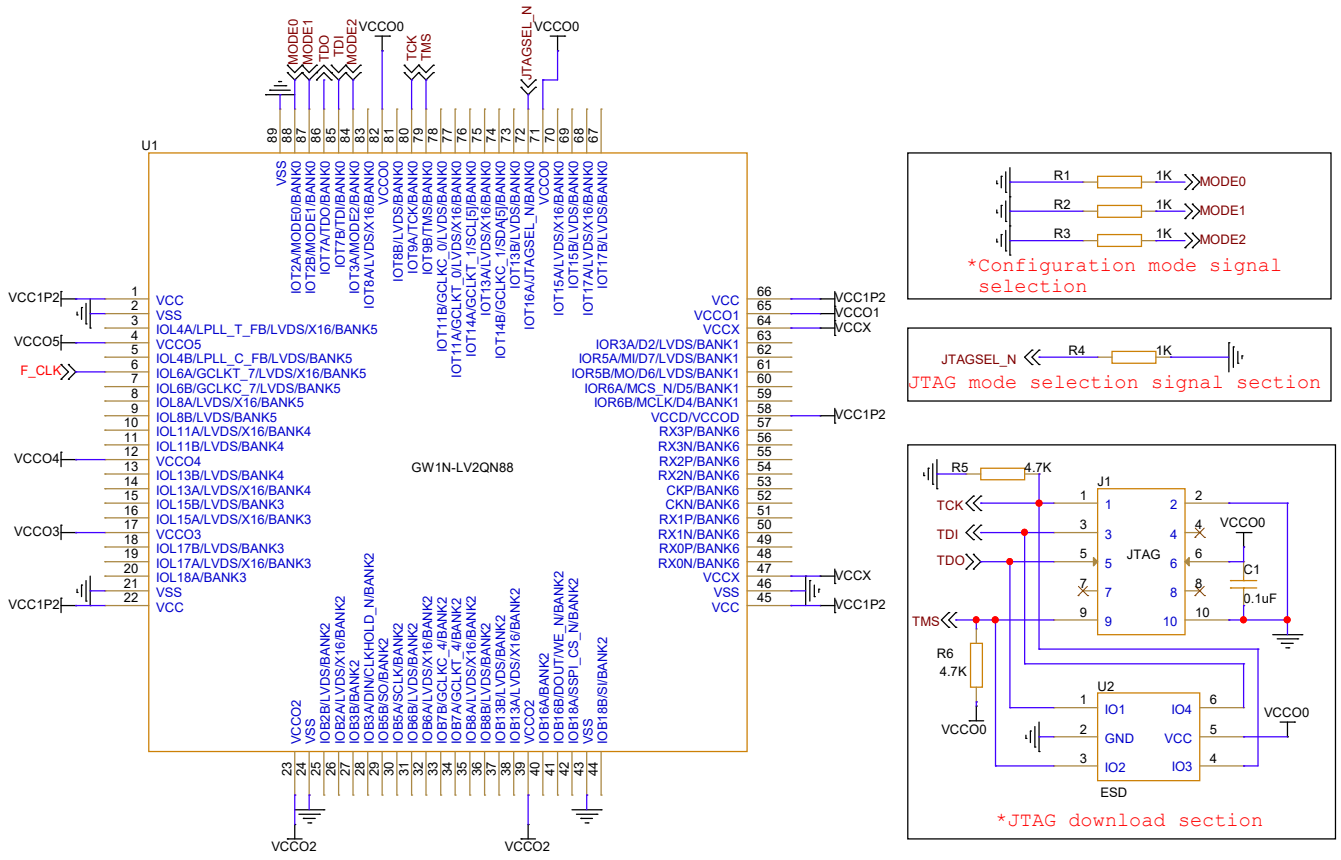
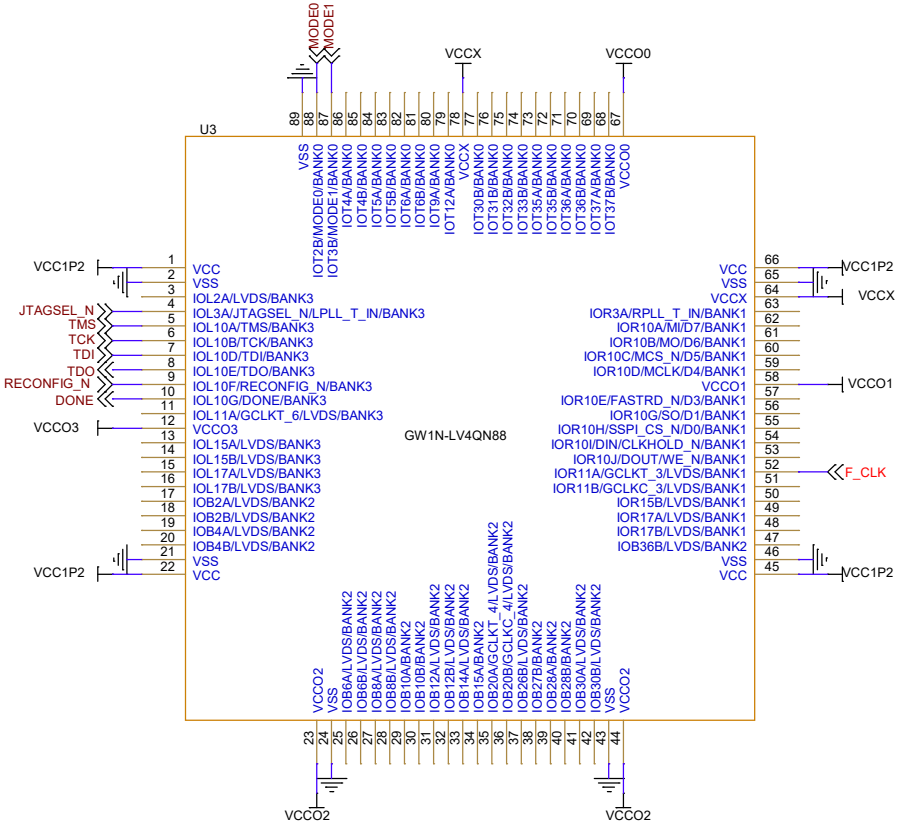
GW1N-LV2QN88

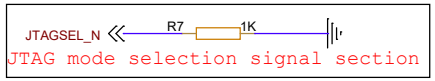


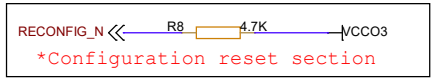
Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

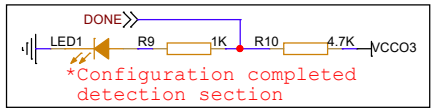
Title	GOWIN Minimum System Diagram	
Size B	Document Number GW1N-LV2QN88	Rev 2.8
Date: Wednesday, May 08, 2024	Sheet 1 of 11	

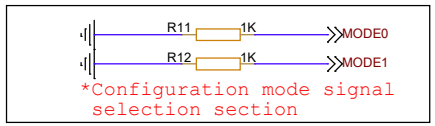
GW1N-LV4QN88

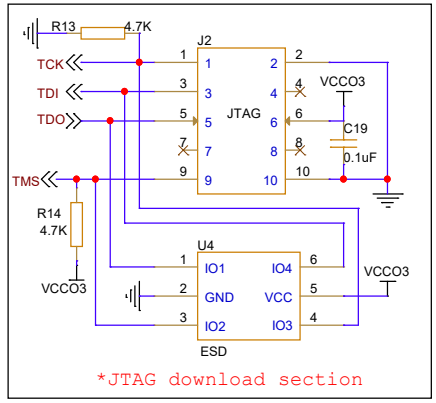


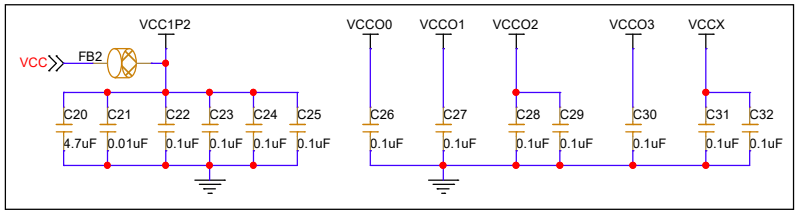








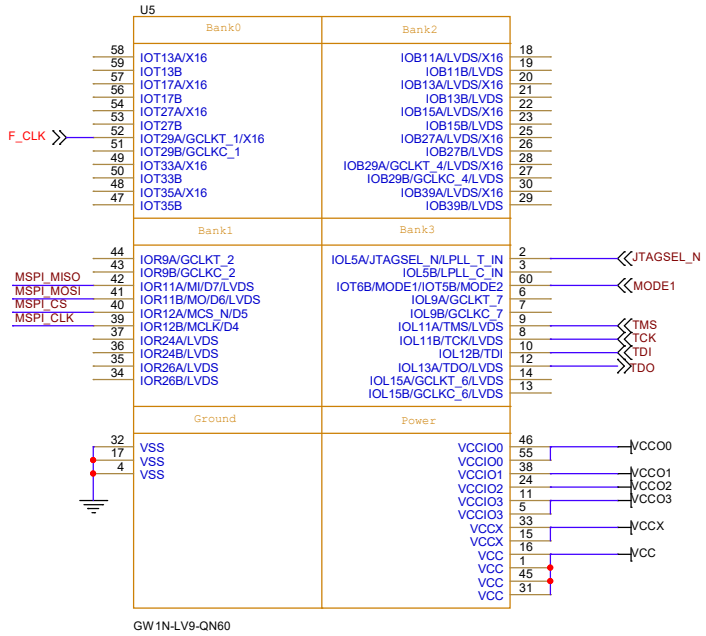


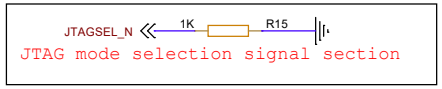


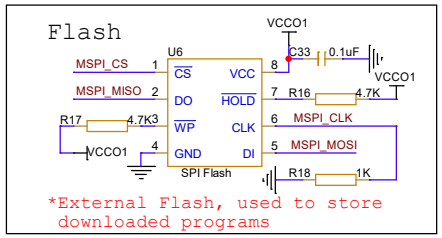
Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

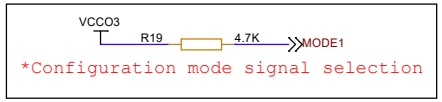
Title: Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size: B	Document Number: GW1N-LV4QN88	Rev: 2.8
Date: Wednesday, May 08, 2024	Sheet 2 of 11	

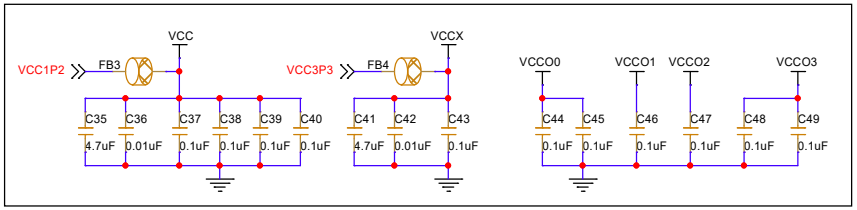
GW1N-LV9QN60

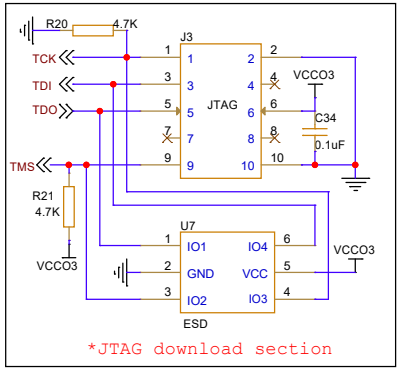








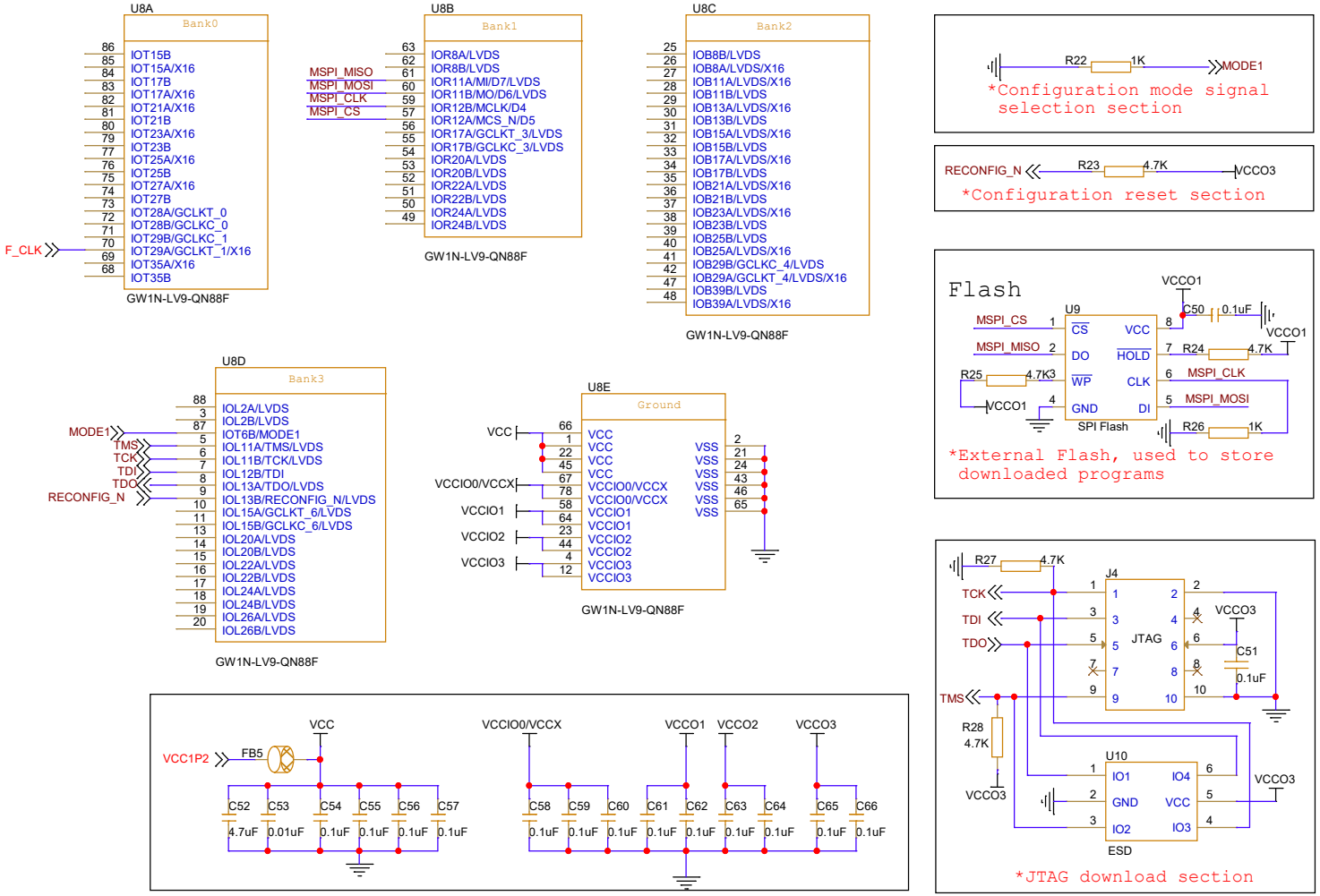




Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
  For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	Gowin FPGA-AOTOMOTIVE Minimum System Diagram	
Size A3	Document Number GW1N-LV9QN60	Rev 2.8
Date: Wednesday, May 08, 2024	Sheet 3 of 11	

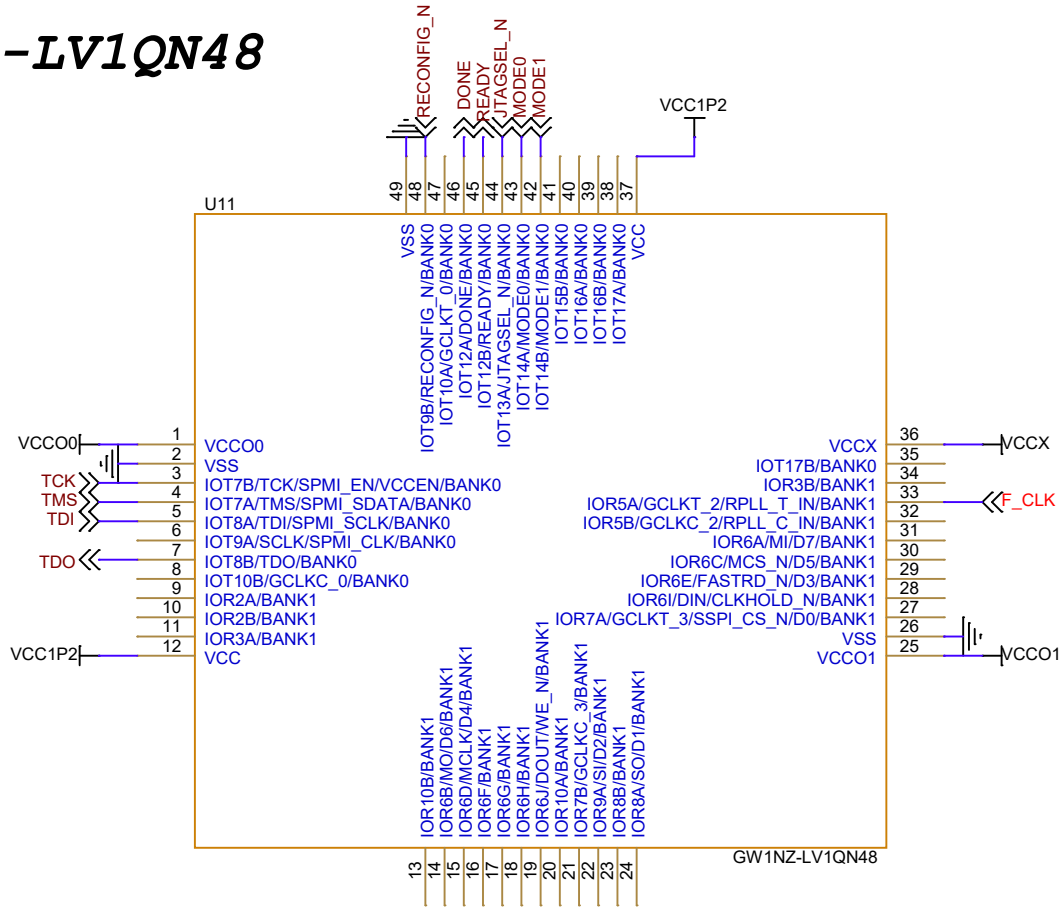
GW1N-LV9QN88F

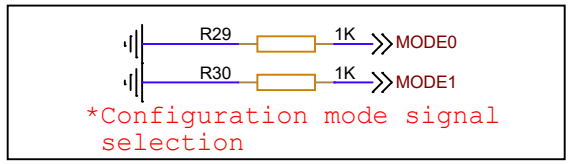


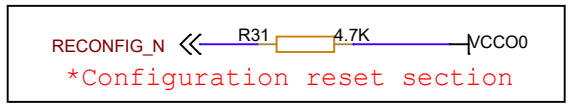
Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

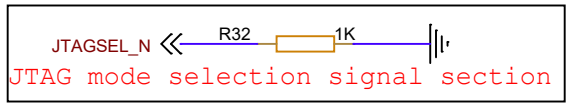
Title	GOWIN Minimum System Diagram	
Size B	Document Number GW1N-LV9QN88F	Rev 2.8
Date: Wednesday, May 08, 2024	Sheet 4 of 11	

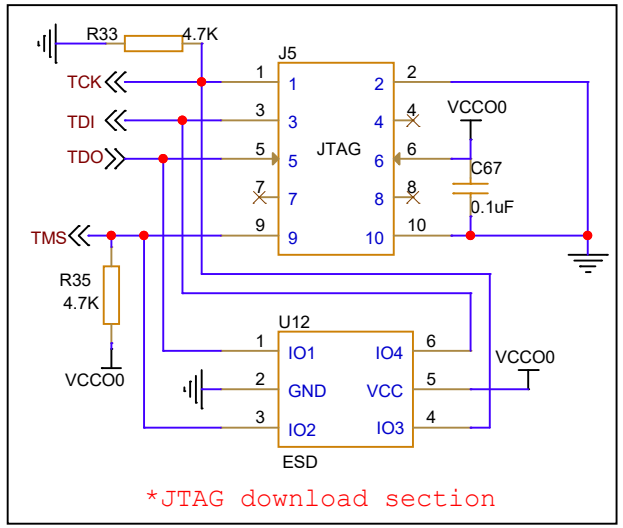
GW1NZ-LV1QN48

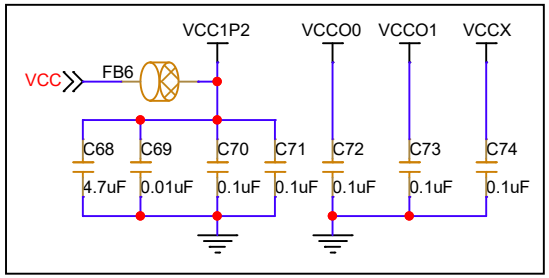


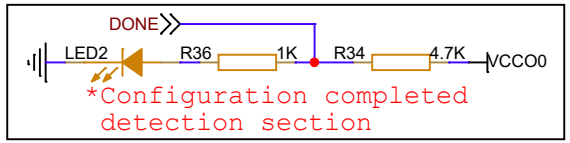


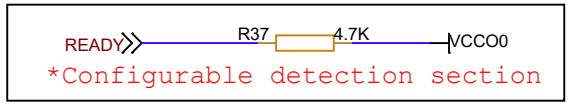








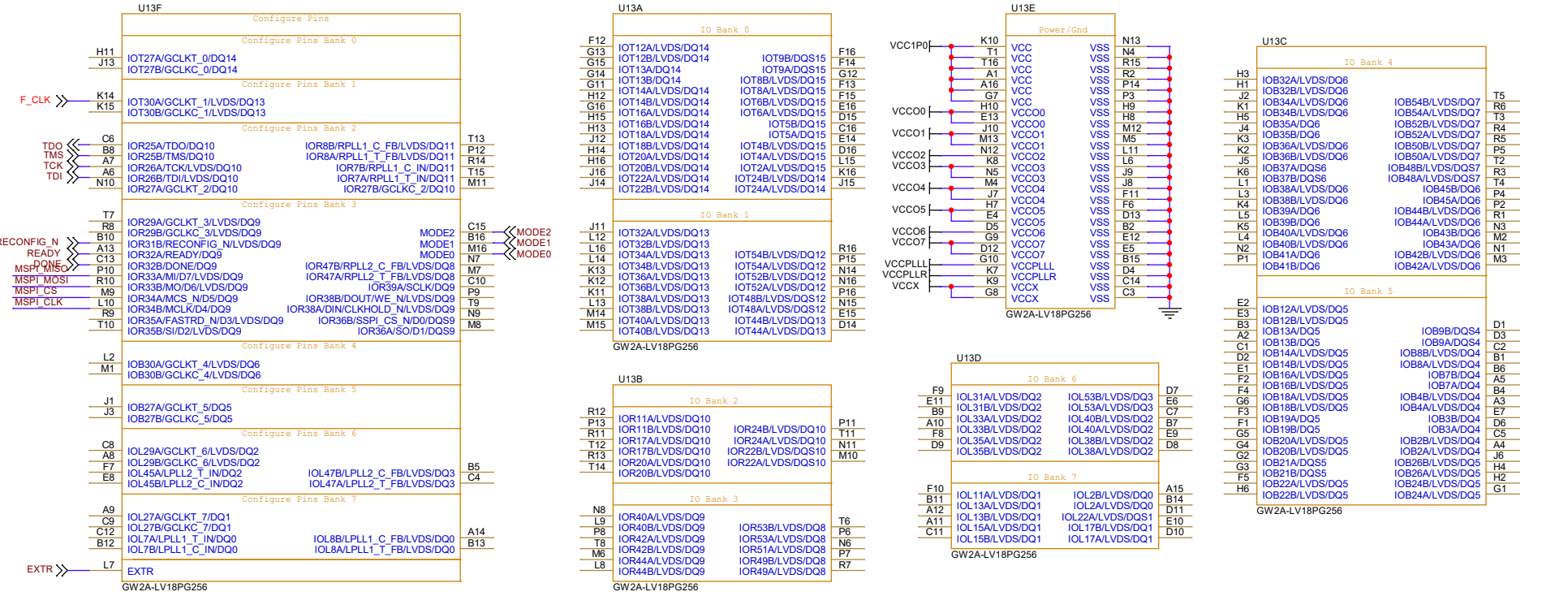


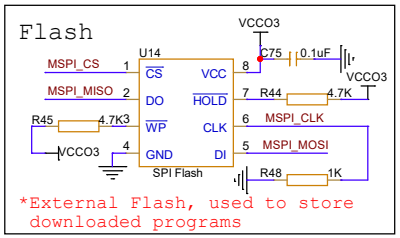


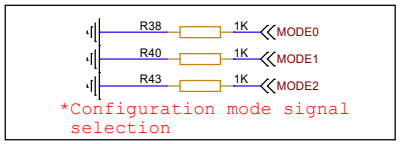
Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.It is recommended that add an ESD protection chip to the JTAG download circuit.

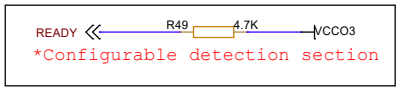
Title: Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size: A4	Document Number: GW1NZ-LV1QN48	Rev: 2.8
Date: Wednesday, May 08, 2024	Sheet 5 of 11	

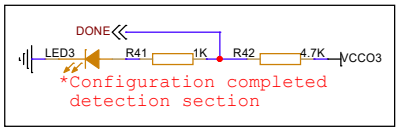
GW2A-LV18PG256

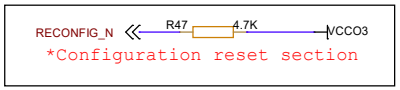


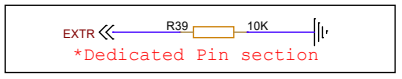


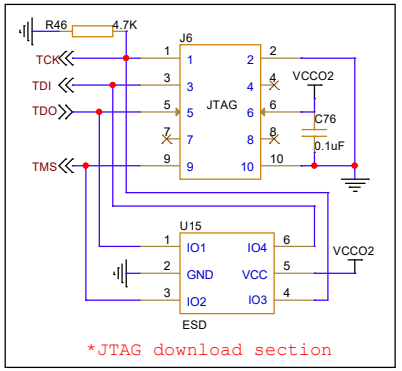


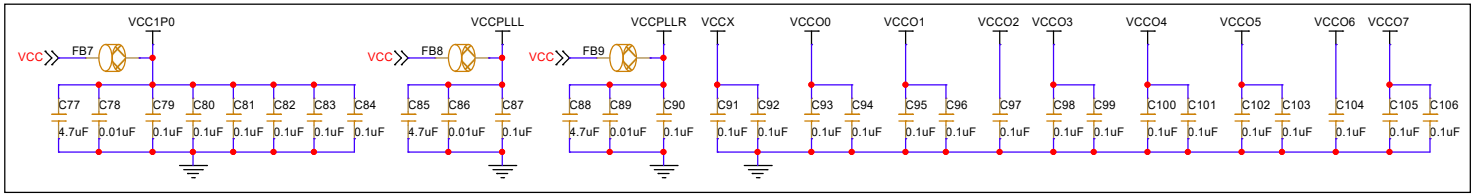








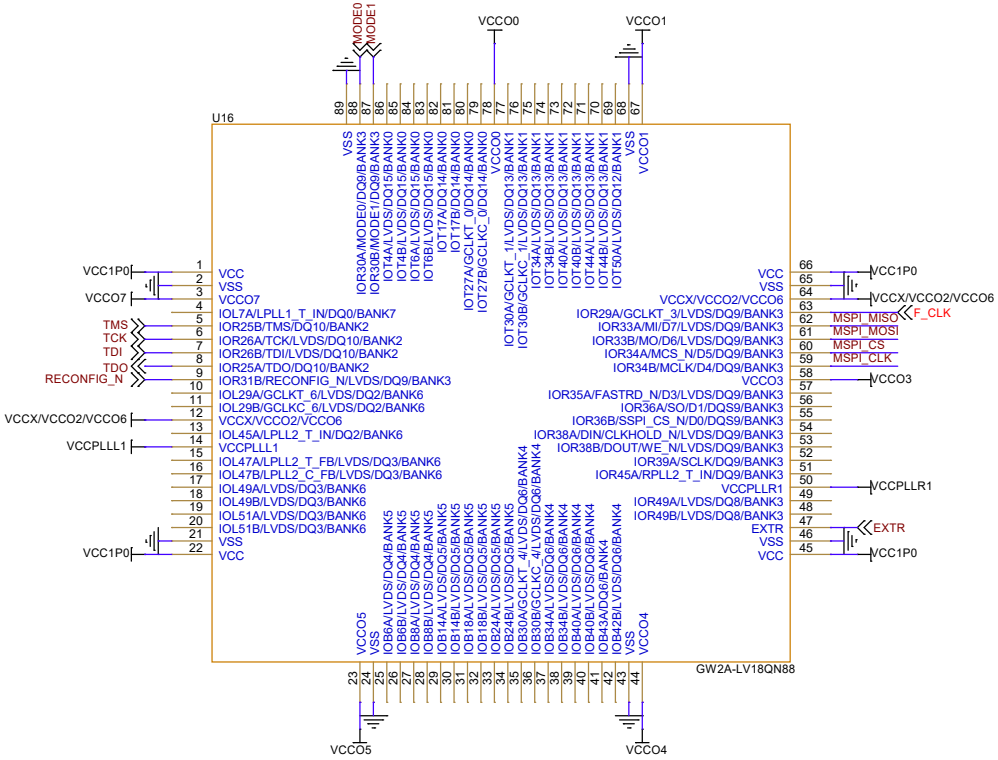


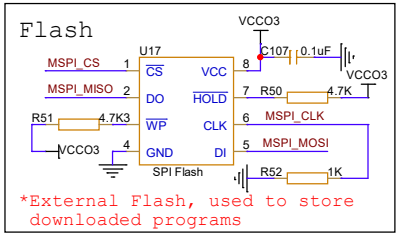


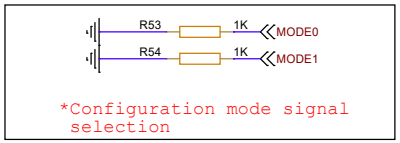
Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
  For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3.It is recommended that add an ESD protection chip to the JTAG download circuit.

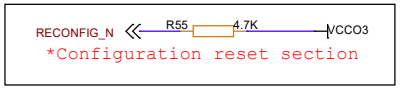
Title: Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size: A3	Document Number: GW2A-LV18PG256	Rev: 2.8
Date: Wednesday, May 08, 2024	Sheet 6 of 11	

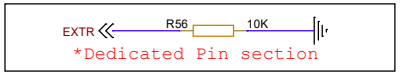
GW2A-LV18QN88

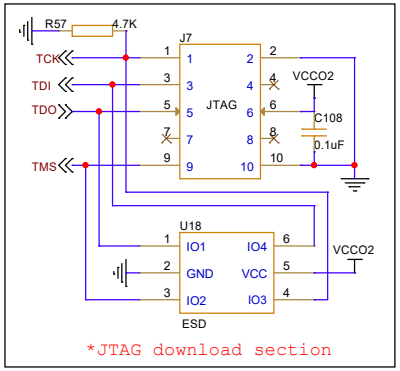


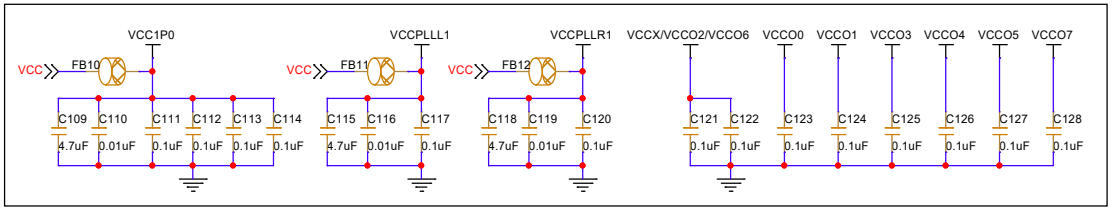








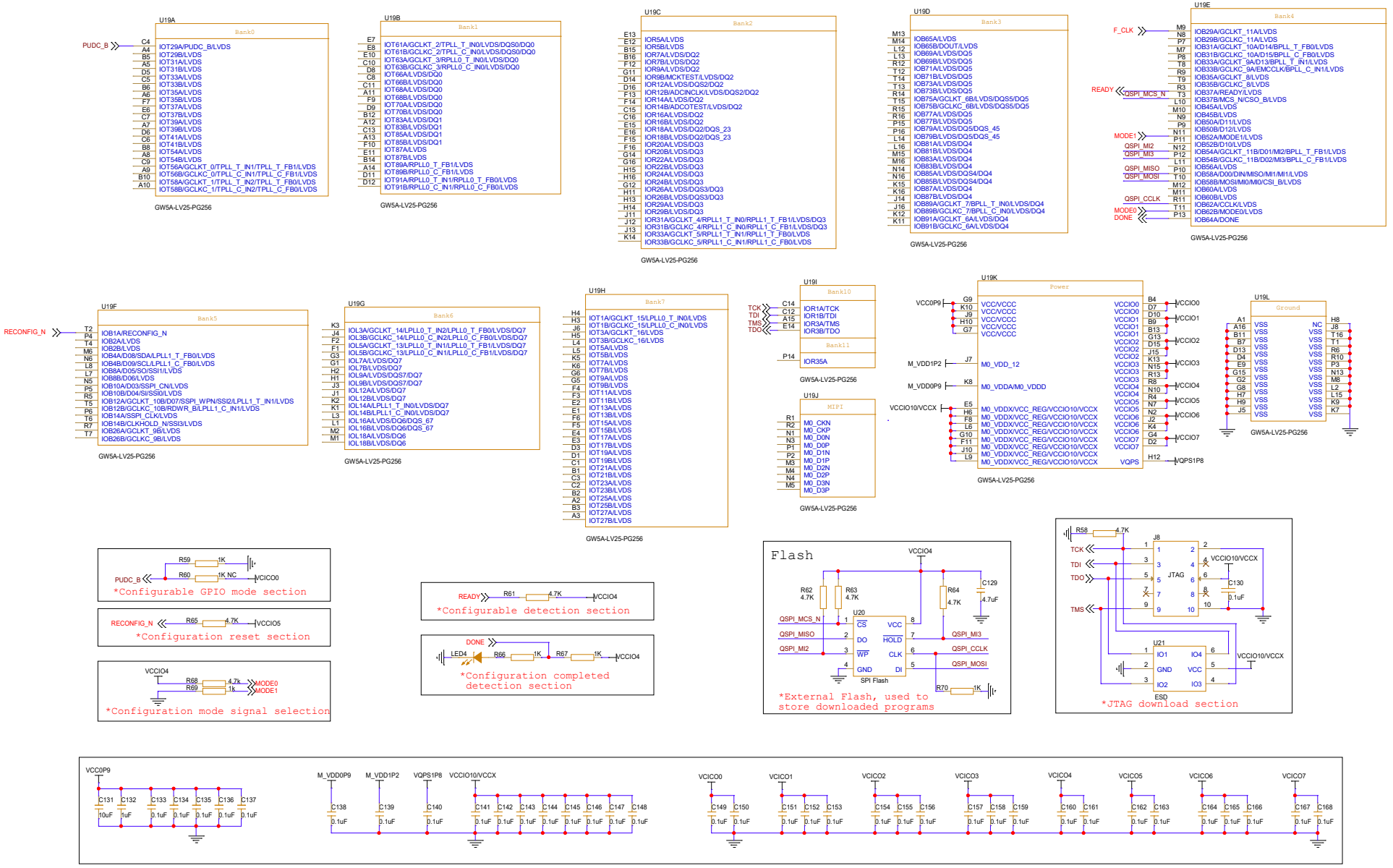




Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
  For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title: Gowin FPGA-AOTOMOTIVE Minimum System Diagram		
Size: A3	Document Number: GW2A-LV18QN88F	Rev: 2.8
Date: Wednesday, May 08, 2024	Sheet 7 of 11	

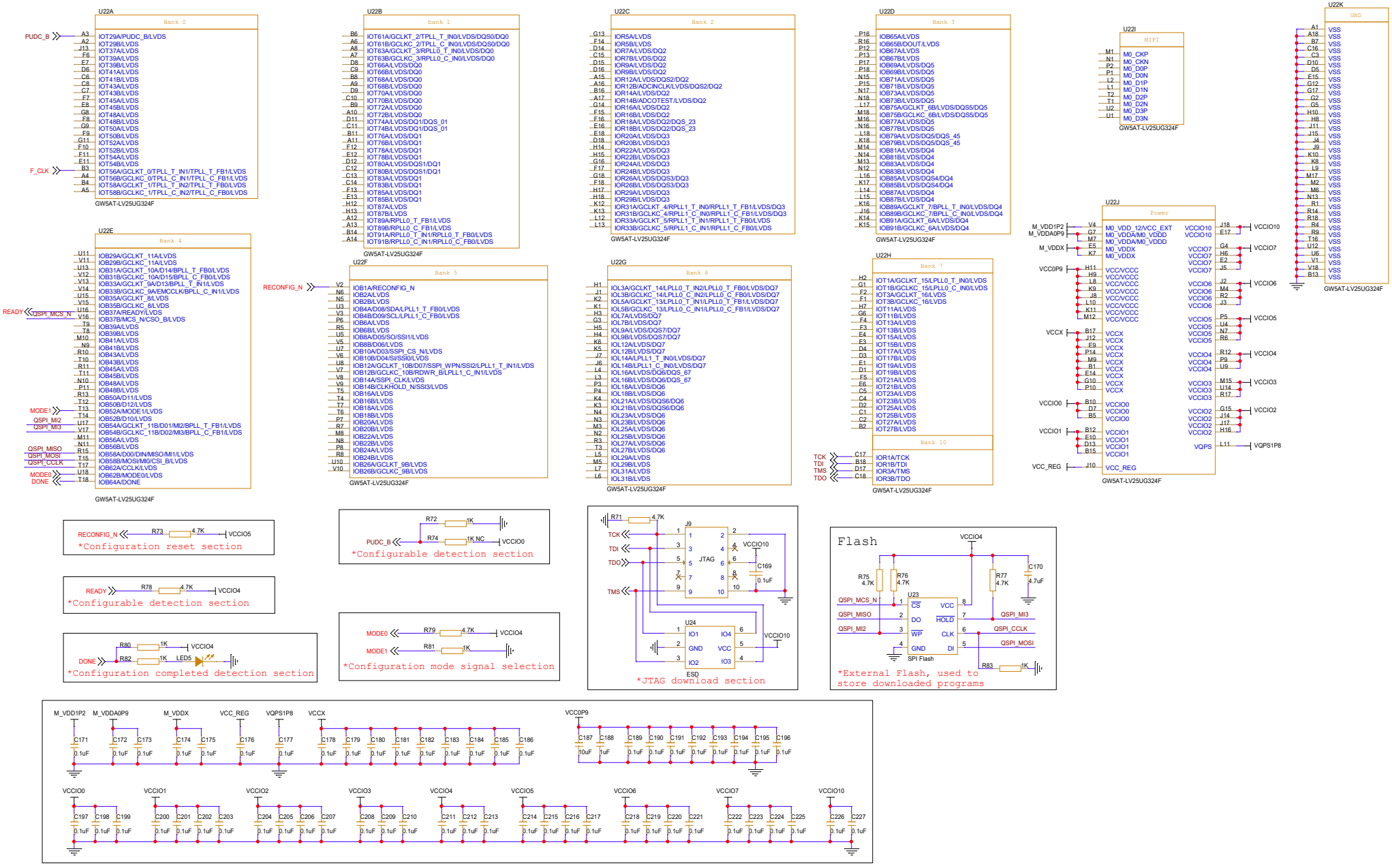
GW5A-LV25PG256



Notes:
1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
3.It is recommended that add an ESD protection chip to the JTAG download circuit.
4.VCC core voltage requires a large current, so it is recommended to supply power separately.
5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

Title	GOWIN Minimum System Diagram	
Size C	Document Number GW5A-LV25PG256	Rev 2.8
Date: Wednesday, May 08, 2024	Sheet 8 of 11	

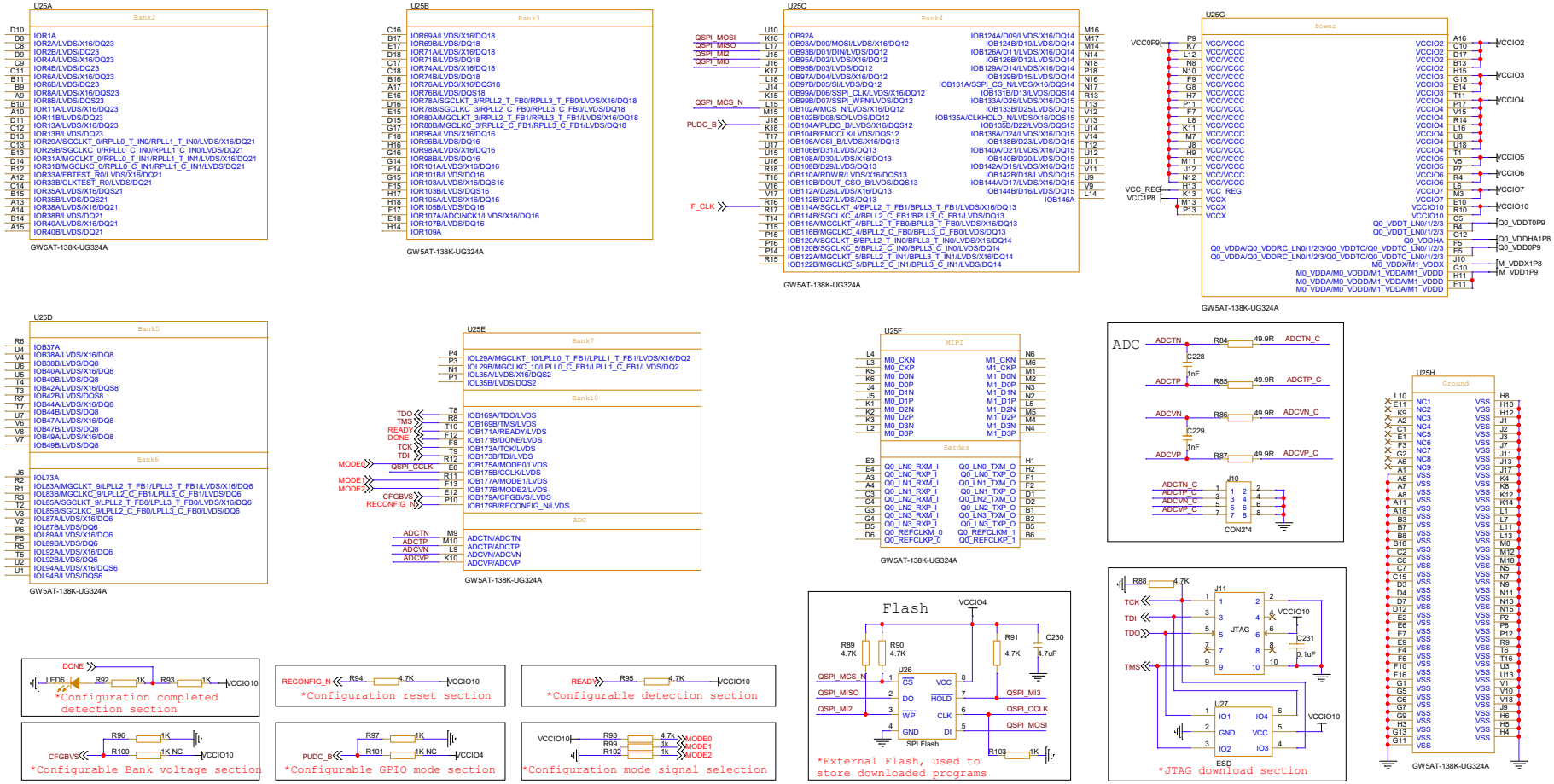
GW5A-LV25UG324F



Notes:
1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
3.It is recommended that add an ESD protection chip to the JTAG download circuit.
4.VCC core voltage requires a large current, so it is recommended to supply power separately.
5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

Title	GOWIN Minimum System Diagram	
Size C	Document Number GW5A-LV25UG324F	Rev 2.8
Date: Wednesday, May 08, 2024	Sheet 9 of 11	

GW5AT-LV138UG324A

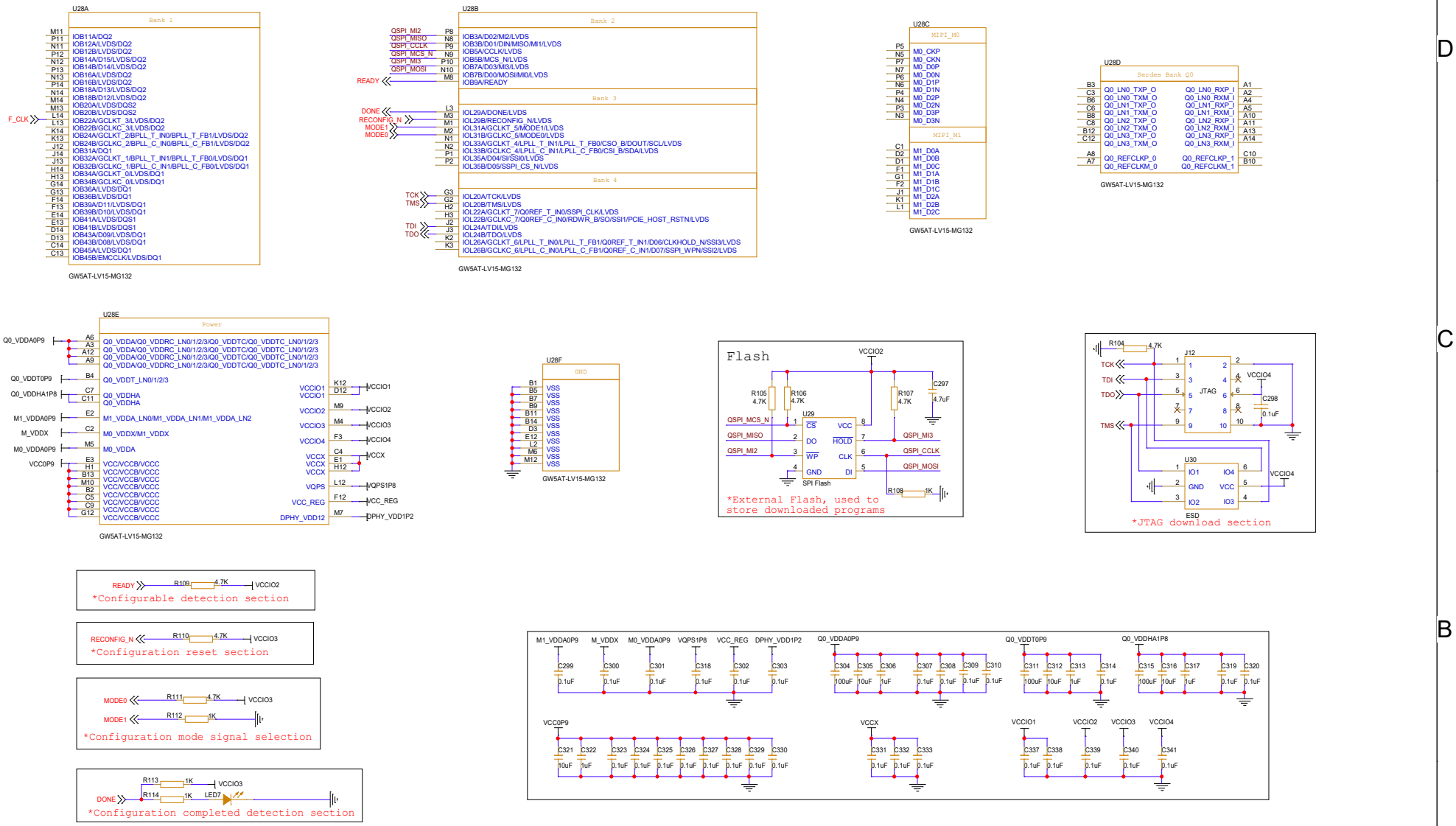


Notes:

1. F_CLK signal is an external input clock signal.
   It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
   For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.

Title	GOWIN Minimum System Diagram		
Size A2	Document Number GW5AT-LV138UG324A		Rev 2.8
Date: Wednesday, May 08, 2024	Sheet 10 of 11		

GW5AT-LV15MG132



Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
3.It is recommended that add an ESD protection chip to the JTAG download circuit.
4.VCC core voltage requires a large current, so it is recommended to supply power separately.
5.The MODE pin is the GowinCONFIG configuration mode selection signal.

Title	GOWIN Minimum System Diagram	
Size C	Document Number GW5AT-LV15MG132	Rev 2.8
Date: Wednesday, May 08, 2024	Sheet 11 of 11	