GW2AR-LV18EQ144 VCC00 VCCO1 VCC3P3 Flash C1 [ 0.1uF [] MSPI\_CS MSPI\_MISO 2 4.7K DO HOLD 4.7K3 MSPI\_CLK CLK VCC3P3 4 GNID SPI Flash \*External Flash, used to store downloaded programs -VCC1P0 VCC1P0 VCC/VCCPLLL1 VCC/VCCPLLL1 VSS VSS 1K (MODE0 IOL2A/LVDS/DQ0/BANK72 IOR7A/RPLL1\_T\_IN/DQ11/BANK2 IOL28/LVDS/DQ0/BANK2
VCCX/VCCO2/6/7
IOL7A/LPLL1\_T\_IN/DQ0/BANK7
IOL7B/LPLL1\_C\_IN/DQ0/BANK7 IOR7B/RPLL1\_C\_IN/DQ11/BANK2 VCCPLLR0 VCC3P3 VCCPLLR0 VCC3P3 VCCX/VCCO2/6/7 7<mark>─1K</mark> ≪MODE2 IOR20A/LVDS/DQ10/BANK2 VCCPLLL0F VCCPLLL0 IOL22A/LVDS/DQS1/BANK7 IOR20B/LVDS/DQ10/BANK2 \*Configuration mode signal IOR22A/LVDS/DQS10/BANK2 IOL22B/LVDS/DQS1/BANK7 IOL27A/GCLKT 7/DQ1/BANK7 IOR22B/LVDS/DQS10/BANK2 IOR27A/GCLKT 2/DQ10/BANK2 IOL27B/GCLKC\_7/DQ1/BANK7 IOR25B/TMS/DQ10/BANK2 IOR27B/GCLKC\_2/DQ10/BANK2 MSPI MISO TMS IOR33A/MI/D7/I VDS/DO9/BANK3 IOR26A/TCK/LVDS/DQ10/BANK2 IOR39A/SCLK/DQ9/BANK3 IOR33B/MO/D6/LVDS/DQ9/BANK3 IOR34A/MCS N/D5/DQ9/BANK3 DONE << MSPI CS MSPI\_CLK TDI >> IOR26B/TDI/LVDS/DQ10/BANK2 IOR34B/MCLK/D4/DQ9/BANK3 IOR35A/FASTRD\_N/D3/LVDS/DQ9/BANK3 Configuration completed VCC3P3 IOR25A/TDO/DQ10/BANK2 VCC3P3 GW2AR-LV18EQ144 IOR35B/SI/D2/LVDS/DQ9/BANK3 VCCX/VCCO2/6/7 IOR31B/RECONFIG\_N/LVDS/DQ9/BANK3 detection section RECONFIG\_N >> IOR36A/SO/D1/DQS9/BANK3
IOR36B/SSIP\_CS\_N/D0/DQS9/BANK3
IOR36B/SIN/CLKHOED\_N/LVDS/DQ9/BANK3
IOR38B/DOUT/WE\_N/LVDS/DQ9/BANK3 DONE SEADY IOR32B/DONE/DQ9/BANK3 IOR32A/READY/DQ9/BANK3 IOL32A/DQ2/BANK6 IOL32B/DQ2/BANK6 R9 4.7K IOL29A/GCLKT\_6/LVDS/DQ2/BANK6 IOL29B/GCLKC\_6/LVDS/DQ2/BANK6 IOR42A/LVDS/DQ9/BANK3 IOR42B/LVDS/DQ9/BANK3 \*Configurable detection section IOL33A/LVDS/DQ2/BANK6 IOL33B/LVDS/DQ2/BANK6 IOR45A/RPLL2\_T\_IN/DQ9/BANK3 VCCPLLR0 VCCPLLR1 IOL36A/DQS2/BANK6 IOR49A/LVDS/DQ8/BANK3 IOL36B/DQS2/BANK6 IOR49B/LVDS/DO8/BANK3 VCC3P3 VCCX/VCCO2/6/7 IOR50A/DQS8/BANK3 RECONFIG\_N 
R10 4.7K IOL42A/LVDS/DQ2/BANK6 IOL42B/LVDS/DQ2/BANK6 VCCO3 IOR50B/DQS8/BANK3 4/LVDS/DQ6/BANK4 \*Configuration reset section IOL45A/LPLL2\_T\_IN/DQ2/BANK6 IOL45B/LPLL2\_C\_IN/DQ2/BANK6 EXTR VSS **KEXTR** VCC1P0I VCC1P0 VCC/VCCPLLL1 R11 10K EXTR << GCLKT / GCLKC / JDG6/BAN \*Dedicated Pin section I R12 VCC3P3 TDI ≪ ÷ JTAG TDO>> 0.1uF TMS<< VCC1P0 VCCPLLR0 VCCPLLL0 VCC3P3 VCCO0 VCCO1 VCC3P3 VCCO4 VCCO5 VCC3P3 VCC>> FB1 FB3 U3 101 104 VCC3P3 GND VCC C3 C7 C9 C16 C17 C24 C25 C6 C10 C11 C12 C13 C18 C19 C20 C21 C22 C23 103 IO2 0.1uF 0.1uF 0.1uF 4.7uF 0.01uF 0.1uF 0.1uF 0.1uF 4.7uF 0.01uF 0.1uF 0.1uF 4.7uF 0.01uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF ÷ ÷ \*JTAG download section Notes: 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290. GOWIN Minimum System Diagram 3.It is recommended that add an ESD protection chip to the JTAG download circuit. Document Number GW2AR-LV18EQ144 Rev 2.0 ize A3

GW2AR-LV18EQ144P **\*\*\*** VCC00 VCC01 Flash MSPI\_CS CS vccoa MSPI\_MISO 2 HOLD 6 MSPI CLK 4.7K3 5 MSPI MOSI -VCC03 ÷ SPI Flash \*External Flash, used to store downloaded programs 108 107 VCC/VCCPLLL1 VCC1P0F VCC/VCCPLLL1 1K (MODE0 IOR7A/RPLL1\_T\_IN/DQ11/BANK2 VSS IOL2A/LVDS/DQ0/BANK7 IOR7B/RPLL1\_C\_IN/DQ11/BANK2 \_\_\_1K\_\_\_((MODE1 IOL2B/LVDS/DQ0/BANK7 VCCO2/VCCO7 VCCPLLR0 VCCO2/VCCO7 VCC1P8L VCC1P8 1K (MODE2 IOL7A/LPLL1 T IN/DQ0/BANK7 IOR20A/LVDS/DQ10/BANK2 IOR20B/LVDS/DQ10/BANK2 IOL7B/LPLL1\_C\_IN/DQ0/BANK7 \*Configuration mode signal VCCPLLL0F VCCPLLL0 IOL22A/LVDS/DQS1/BANK7 IOR22A/LVDS/DQS10/BANK2 IOR22B/LVDS/DQS10/BANK2 selection IOR27A/GCLKT\_2/DQ10/BANK2 IOR27B/GCLKC\_2/DQ10/BANK2 IOR33A/MI/D7/LVDS/DQ9/BANK3 ⟨F\_CLK IOL22B/LVDS/DQS1/BANK7 IOL27A/GCLKT 7/DQ1/BANK7 MSPI\_MISO IOL27B/GCLKC\_7/DQ1/BANK7 MSPI MOSI DONE << TMS IOR25B/TMS/DO10/BANK2 IOR33B/MO/D6/LVDS/DO9/BANK3 IOR34A/MCS\_N/D5/DQ9/BANK3 IOR34B/MCLK/D4/DQ9/BANK3 IOR26A/TCK/LVDS/DQ10/BANK2 MSPI\_CLK IOR39A/SCLK/DQ9/BANK3 \*Configuration completed TDI >>> IOR26B/TDI/LVDS/DQ10/BANK2 IOR35A/FASTRD\_N/D3/LVDS/DQ9/BANK3 GW2AR-LV18EQ144P VSS VCCO3 IOR25A/TDO/DQ10/BANK2 IOR35B/SI/D2/LVDS/DQ9/BANK3 detection section VCC1P8 VCCO2/VCCO7 RECONFIG\_N IOR31B/RECONFIG\_N/LVDS/DQ9/BANK3 IOR36A/SO/D1/DQS9/BANK3 IOR32B/DONE/DQ9/BANK3 IOR32A/READY/DQ9/BANK3 IOR36B/SSPI\_CS\_N/D0/DQS9/BANK3
IOR38A/DIN/CLKHOLD N/LVDS/DQ9/BANK3 DONE READY < R21 4.7K IOL32A/DQ2/BANK6 IOL32B/DQ2/BANK6 IOR38B/DOUT/WE\_N/LVDS/DQ9/BANK3 IOR42A/LVDS/DQ9/BANK3 READY << \*Configurable detection section IOL29A/GCLKT\_6/LVDS/DQ2/BANK6 IOL29B/GCLKC\_6/LVDS/DQ2/BANK6 IOR42B/LVDS/DQ9/BANK3 IOR45A/RPLL2\_T\_IN/DQ9/BANK3 IOL33A/LVDS/DQ2/BANK6 VCCPLLR0 IOR49A/LVDS/DQ8/BANK3 IOI 33B/I VDS/DQ2/BANK6 IOL36A/DQS2/BANK6 IOL36B/DOS2/BANK6 IOR50A/DOS8/BANK3 RECONFIG\_N 
R22
4.7K VCCX/VCC4/6 VCCX/VCCO4/VCCO6 VCCO3 VCC03 IOL 42A/LV/DS/DO2/BANKS IOR50B/DQS8/BANK3 IOL42B/LVDS/DQ2/BANK6 EXTR \*Configuration reset section IOL45A/LPLL2\_T\_IN/DQ2/BANK6 IOL45B/LPLL2\_C\_IN/DQ2 VCC/VCCPLLL1 VCC1P0 VCC/VCCPLLL1 EXTR << R23 10K \*Dedicated Pin section VCC1P8 √cc05 C27 0.10F TMS<< VCCPLLR0 VCCPLLL0 VCCX/VCC4/6 VCCO0 VCCO1 VCC1P8 VCCO3 VCC05 VCC>> FB4 101 104 VCC1P8 GND VCC C32 C41 C42 C28 C29 C31 C33 C34 C35 C36 C37 C38 C39 C43 C44 C45 C46 C47 C48 C49 C50 102 103 0.01uF 4.7uF 0.01uF 4.7uF 0.01uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF FSD ÷ ÷ \*JTAG download section 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290. GOWIN Minimum System Diagram 3.It is recommended that add an ESD protection chip to the JTAG download circuit. Document Number GW2AR-LV18EQ144P Rev 2.0 ize A3

GW2AR-LV18EQ144PF VCC01 VCC00 Flash C51 [ 0.1uF ]], MSPL CS VCC MSPI\_MISO 2 7 R25 4.7K T DO MSPI\_CLK 4.7K3 MSPI\_MOSI VCCO3 DI GND rl R27 \*External Flash, used to store downloaded programs 108 107 106 105 VCC1P0F VCC/VCCPLLL1 VCC/VCCPLLL1 VCC1P0 IOT30A/ IOT30B/( VSS VSS 7—1K ≪MODE0 IOL2A/LVDS/DQ0/BANK7 IOR7A/RPLL1\_T\_IN/DQ11/BANK2 IOL2B/LVDS/DQ0/BANK7 IOR7B/RPLL1 C IN/DQ11/BANK2 <mark>1K ≪MODE</mark>1 VCC1P8 VCCPLLR0 VCCO/ IOL7A/LPLL1\_T\_IN/DQ0/BANK7 IOL7B/LPLL1\_C\_IN/DQ0/BANK7 VCCPLLL0 IOL22A/LVDS/DQS1/BANK7 VCCO2 VCCO2 IOR20A/LVDS/DQ10/BANK2 IOR20B/LVDS/DQ10/BANK2 IOR22A/LVDS/DQS10/BANK2 1K (MODE2 VCCPLLL0 \*Configuration mode signal IOL22B/LVDS/DQS1/BANK7 IOL27A/GCLKT 7/DQ1/BANK7 IOR22B/LVDS/DOS10/BANK2 selection IOR27A/GCLKT 2/DQ10/BANK2 </F\_CLK IOL27B/GCLKC\_7/DQ1/BANK7 IOR25B/TMS/DQ10/BANK2 IOR27B/GCLKC\_2/DQ10/BANK2 IOR33A/MI/D7/LVDS/DQ9/BANK3 MSPI MISO TMS IOR26A/TCK/LVDS/DQ10/BANK2 IOR39A/SCLK/DQ9/BANK3 IOR33B/MO/D6/LVDS/DQ9/BANK3 IOR34A/MCS N/D5/DQ9/BANK3 DONE << MSPI CS MSPI\_CLK LED3 R31 1K R32 TDI >>> IOR34B/MCLK/D4/DQ9/BANK3 IOR35A/FASTRD\_N/D3/LVDS/DQ9/BANK3 IOR26B/TDI/LVDS/DQ10/BANK2 VSS Configuration completed IOR25A/TDO/DQ10/BANK2 -VCCO3 TDO VCC1P8 GW2AR-LV18EQ144PF IOR35B/SI/D2/LVDS/DQ9/BANK3 detection section VCCO7 RECONFIG\_N IOR31B/RECONFIG\_N/LVDS/DQ9/BANK3 IOR32B/DONE/DQ9/BANK3 IOR32A/READY/DQ9/BANK3 IOR36A/SO/D1/DOS9/BANK3 DONE IOR36A/SO/D1/DQS9/BANK3
IOR36B/SSPI\_CS. N/D0/DQS9/BANK3
IOR38A/DIN/CLKHOLD\_N/LVDS/DQ9/BANK3
IOR38B/DOUT/WE\_NLVDS/DQ9/BANK3
IOR32B/ALVDS/DQ9/BANK3
IOR42B/LVDS/DQ9/BANK3 READY & IOL32A/DQ2/BANK6 IOL32B/DQ2/BANK6 R33 4.7K IOL29A/GCLKT\_6/LVDS/DQ2/BANK6 IOL29B/GCLKC\_6/LVDS/DQ2/BANK6 \*Configurable detection section IOL33A/LVDS/DQ2/BANK6 IOL33B/LVDS/DQ2/BANK6 IOR45A/RPLL2\_T\_IN/DQ9/BANK3 VCCPLLR0 VCCPLLR1 IOR49A/LVDS/DQ8/BANK3 IOR49B/LVDS/DQ8/BANK3 IOL36A/DQS2/BANK6 IOI 36B/DOS2/BANK6 VCCX/VCC4/6 VCCX/VCCO4/VCCO6 IOR50A/DQS8/BANK3 RECONFIG\_N 
R34
A.7K VCC03 IOI 42A/I VDS/DO2/BANK6 VCCO3 IOL42B/LVDS/DQ2/BANK6 IOL42B/LVDS/DQ2/BANK6 IOL45A/LPLL2\_T\_IN/DQ2/BANK6 IOL45B/LPLL2\_C\_IN/DQ2/BANK6 IOR50B/DQS8/BANK3 \*Configuration reset section **≪**EXTR EXTR VSS 36 VCC1P0 VCC1P0 VCC/VCCPLLL1 VCC/VCCPLLL1 \*Dedicated Pin section R36 TDI ≪ TDO>>> VCCX/VCC4/6 √CC05 0.1uF TMS<< VCCO5 VCCO2 VCC1P8 VCC1P0 VCCPLLR0 VCCPLLL0 VCCX/VCC4/6 VCCO0 VCCO1 VCCO3 VCC>> FB7 VCC>> FB8 VCC>> FB9 IO1 IO4 VCCO2 GND VCC C53 C56 C57 C59 C63 C66 C70 C71 C74 C75 C54 C55 C58 C60 C61 C62 C64 C67 C68 C69 C72 C73 103 IO2 0.1uF 0.1uF 0.10F 4 7uF 0 01uF 0 1uF 0.1uE 0.1uE 4 7uF 0 01uF 0 1uF 4.7uF 0.01uF 0.1uF 0.1uF 0 1uF 0 1uF 0.1uF 0.1uF ÷ \*JTAG download section 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290. 3.It is recommended that add an ESD protection chip to the JTAG download circuit. GOWIN Minimum System Diagram Document Number GW2AR-LV18EQ144PF Rev 2.0 ize A3

GW2AR-LV18EQ176 VCC00 VCCX VCCO1 VCC2P5 Flash C76 0.1uF MSPI CS MSPI\_MISO 2 DO 4.7K3 MSPI CLK CNID SPI Flash ŧ VCC1P0 → VCC1P0 \*External Flash, used IOL2A/LVDS/DO0/BANK7 129 128 127 IOL2B/LVDS/DQ0/BANK7 IOR7A/RPLL1 T IN/DQ11/BANK2 downloaded programs VCC2P5 VCCO2/VCCO3/VCCO6/VCCO7 IOL11A/LVDS/DQ1/BANK7 IOR7B/RPLL1\_C\_IN/DQ11/BANK2 VCCPLLR0 VCCPLLR0 IOR14A/DQ10/BANK2 IOL14B/DQ1/BANK7 IOL15A/LVDS/DO1/BANK7 IOR20A/LVDS/DO10/BANK2 T\_1K ≪MODE0 IOL15B/LVDS/DQ1/BANK7 IOR20B/LVDS/DQ10/BANK2 IOR22A/I V/DS/DOS10/BANK2 IOI 17A/I VDS/DQ1/BANK7 7<mark>−1K</sub> ((MODE1</mark> IOL17B/LVDS/DQ1/BANK7 IOL18A/DQ1/BANK7 VCCO2/VCCO3/VCCO6/VCCO7 IOR25A/TDO/DQ10/BANK2 IOR26A/TCK/LVDS/DQ10/BANK2 □ 1K ((MODE2 VCC2P5L IOL23A/DQ1/BANK7 IOR25B/TMS/DQ10/BANK2 TMS \*Configuration mode signal IOL24A/LVDS/DQ1/BANK7 VCCO2/VCCO3/VCCO6/VCCO7 VCC2P5 IOL24B/LVDS/DQ1/BANK7 IOL26A/LVDS/DQ1/BANK7 IOR26B/TDI/LVDS/DQ10/BANK2 IOR27A/GCLKT\_2/DQ10/BANK2 TDI selection IOL25B/DQ1/BANK7 VCCX. IOR29A/GCLKT 3/LVDS/DQ9/BANK3 IOI 26B/I VDS/DO1/BANK7 DONE ((-IOL27B/GCLKT\_7/DQ1/BANK7 IOL27B/GCLKC\_7/DQ1/BANK7 IOR30A/MODE0/DQ9/BANK3 IOR31A/MODE2/LVDS/DQ9/BANK3 MODE2 MODE1 VCC2P5 ILED4 GW2AR-I V18FO176 1K R44 VCC2P5 VCCO2/VCCO3/VCCO6/VCCO7 IOR30B/MODE1/DQ9/BANK3 VCCX VCCO2/VCCO3/VCCO6/VCCO7 Configuration completed IOL38A/LVDS/DQ2/BANK6 IOR32A/READY/DQ9/BANK3 READY RECONFIG\_N IOR31B/RECONFIG\_N/LVDS/DQ9/BANK3 IOL38B/LVDS/DO2/BANK6 detection section MSPI MISO DONE IOL40A/LVDS/DQ2/BANK6 IOR32B/DONE/DQ9/BANK3 IOL40B/LVDS/DQ2/BANK6 IOL42A/LVDS/DQ2/BANK6 IOR33A/MI/D7/LVDS/DQ9/BANK3 IOR33B/MO/D6/LVDS/DQ9/BANK3 MSPI MOSI IOL42B/LVDS/DQ2/BANK6 IOL44A/LVDS/DQ2/BANK6 IOR34A/MCS\_N/D5/DQ9/BANK3 IOR34B/MCLK/D4/DQ9/BANK3 MSPI CLK R45 102 101 100 IOR35A/FASTRD\_N/D3/LVDS/DQ9/BANK3 IOR35B/SI/D2/LVDS/DQ9/BANK3 IOL44B/LVDS/DQ2/BANK6 \*Configurable detection section IOL45A/LPLL2 T IN/DQ2/BANK6 IOL45B/LPLL2\_C\_IN/DQ2/BANK6 IOR36A/SO/D1/DQS9/BANK3 IOR36B/SSPI CS N/D0/DQS9/BANK3 VCCPLLL0 VCCPLLL1 IOL47A/LPLL2\_T\_FB/LVDS/DQ3/BANK6 IOL47B/LPLL2\_C\_FB/LVDS/DQ3/BANK6 IOL49A/LVDS/DQ3/BANK6 IOR38A/DIN/CLKHOLD N/LVDS/DQ9/BANK3 IOR38B/DOUT/WE\_N/LVDS/DQ9/BANK3 IOR39A/SCLK/DQ9/BANK3 R46 RECONFIG N <<-IOL50A/DOS3/BANKS VCCO2/VCCO3/VCCO6/VCCO7 VCCPLLR1 IOL50B/DQS3/BANK6 VCCPLLR0 IOR45A/RPLL2\_T\_IN/DQ9/BANK3 IOR47A/RPLL2\_T\_FB/LVDS/DQ8/BANK3 \*Configuration reset section VCC2P5 VCCO2/VCCO3/VCCO6/VCCO7 IOL53A/LVDS/DQ3/BANK6 41 42 IOL53B/LVDS/DQ3/BANK6 EXTR VSS **EXTR** 43 44 VCC1P0 VCC1P0 R47 10K EXTR << \*Dedicated Pin section R48 TDI < JTAG 8 8 VCC05 VCC04 VCC05 vccx 0.1uF TMS<< VCCPLLL0 VCC00 VCCO1 VCC2P5 VCCO4 VCC2P5 VCC>> FB10 FB1 FB12 U12 101 104 ∨СС2Р5 Т GND VCC C100 C101 0.1uF C103 C104 C105 C106 C107 C108 C109 C11 C82 C78 C79 CRO C81 C83 C84 C85 C87 C88 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99 103 102 p.1uF 4.7uF 0.01uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1 0.1uF 0.1uF 0.1uF 4.7uF 0.01uF 0.1uF 0.1uF 4.7uF 0.01uF 0.1uF 0.1uF 0.1uF ESD ÷ ÷ \*JTAG download section Notes: 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal. 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290. GOWIN Minimum System Diagram 3.It is recommended that add an ESD protection chip to the JTAG download circuit. Document Number GW2AR-LV18EQ176 Rev 2.0 ize A3





