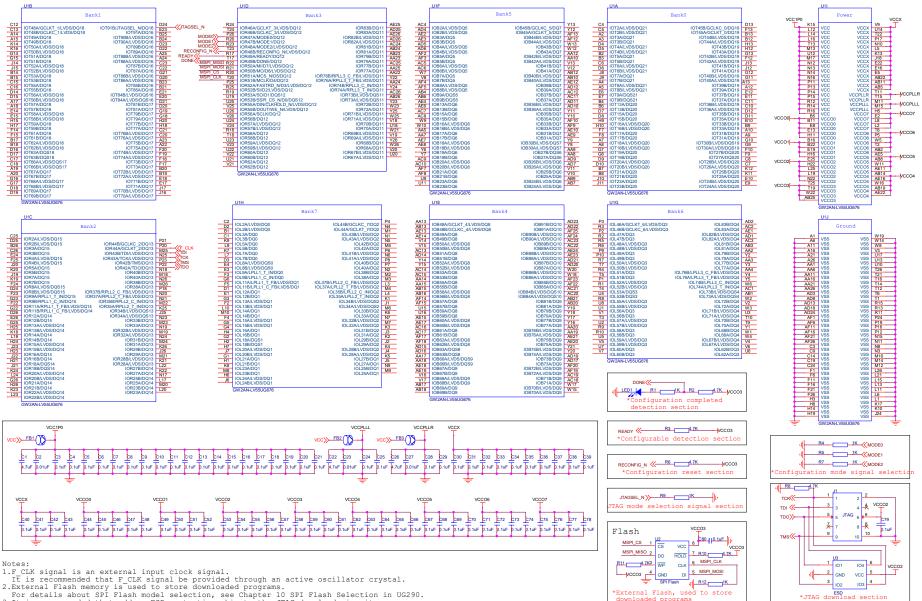
GW2AN-LV55UG676 3 2 4 1



1.F CLK signal is an external input clock signal.

For details about SPI Flash model selection, see Chapter 10 SPI Flash Selection in UG290.

3.It is recommended that add an ESD protection chip to the JTAG download circuit.

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