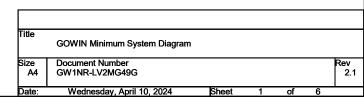


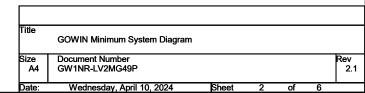
Notes:

- 1.F CLK signal is an external input clock signal.
 - It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2. It is recommended that \overline{add} an \overline{ESD} protection chip to the JTAG download circuit.



Notes:

- 1.F CLK signal is an external input clock signal.
 - It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



U5A

B5

A6

В6

В7

A3

В3

F5

G1

D1

D2

E6

E7

G6

G7 F6

F7

D7

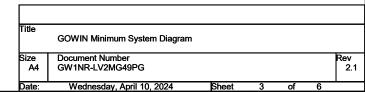
C6 C7

Notes:

1.F CLK signal is an external input clock signal.

U5C

- $\overline{\text{It}}$ is recommended that F CLK signal be provided through an active oscillator crystal.
- 2. It is recommended that add an ESD protection chip to the JTAG download circuit.

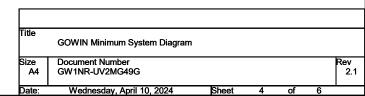


U7D

U7C

Notes:

- 1.F CLK signal is an external input clock signal.
 - $\overline{\text{It}}$ is recommended that F CLK signal be provided through an active oscillator crystal.
- 2. It is recommended that add an ESD protection chip to the JTAG download circuit.



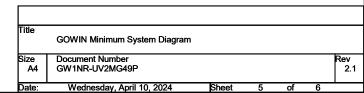
U9A

U9D

U9C

Notes:

- 1.F CLK signal is an external input clock signal.
 - It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



vccx

U11A

B5

A6

В6

В7

A3

В3

F5

G1

D1

D2

E6

E7

G6

G7 F6

F7

D7

C6 C7

U11B

IOT13A/LVDS/X16/BANK0

IOT15A/LVDS/X16/BANK0

IOT17A/LVDS/X16/BANK0

IOT8A/LVDS/X16/BANK0

IOB13A/LVDS/X16/BANK2

IOB4A/LVDS/X16/BANK2 IOB4B/LVDS/BANK2 GW1NR-UV2MG49PG

Bank3

IOL17A/LVDS/X16/BANK3

Bank4

IOL13A/LVDS/X16/BANK4 IOL13B/LVDS/BANK4

CKN/BANK6

CKP/BANK6

RX0N/BANK6

RX1N/BANK6

RX1P/BANK6

RX2N/BANK6

RX2P/BANK6

RX3N/BANK6

RX3P/BANK6 GW1NR-UV2MG49PG

RX0P/BANK6

IOL17B/LVDS/BANK3

IOB13B/LVDS/BANK2

IOT13B/LVDS/BANK0

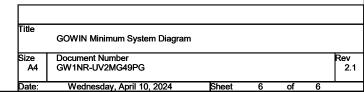
IOT15B/LVDS/BANK0

IOT17B/LVDS/BANK0

IOT8B/LVDS/BANK0

Notes:

- 1.F CLK signal is an external input clock signal.
 - $\overline{\text{It}}$ is recommended that F CLK signal be provided through an active oscillator crystal.
- 2. It is recommended that add an ESD protection chip to the JTAG download circuit.



Power

JTAG

101

GND

102

ESD

*JTAG download section

2

VCC

VSS C4

VSS

VCC00

10

5

10

104

VCC

103

C46

0.1uF

VCC00

VCCX

vccx