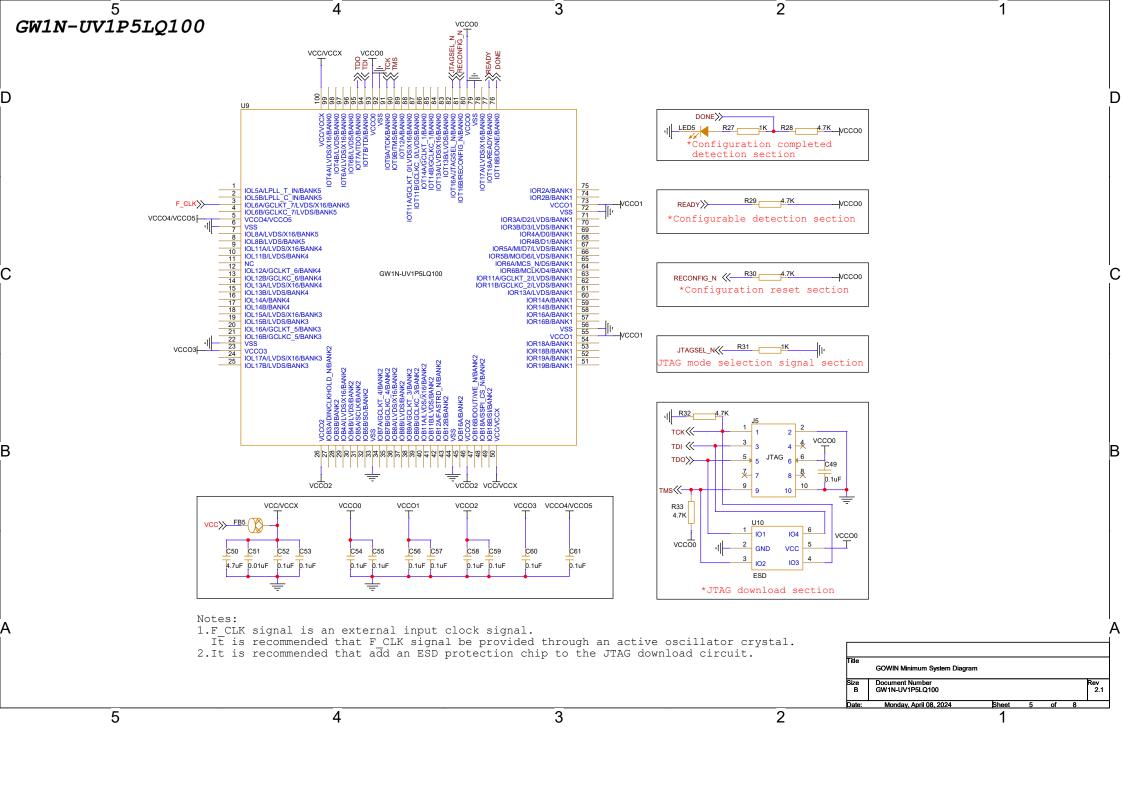
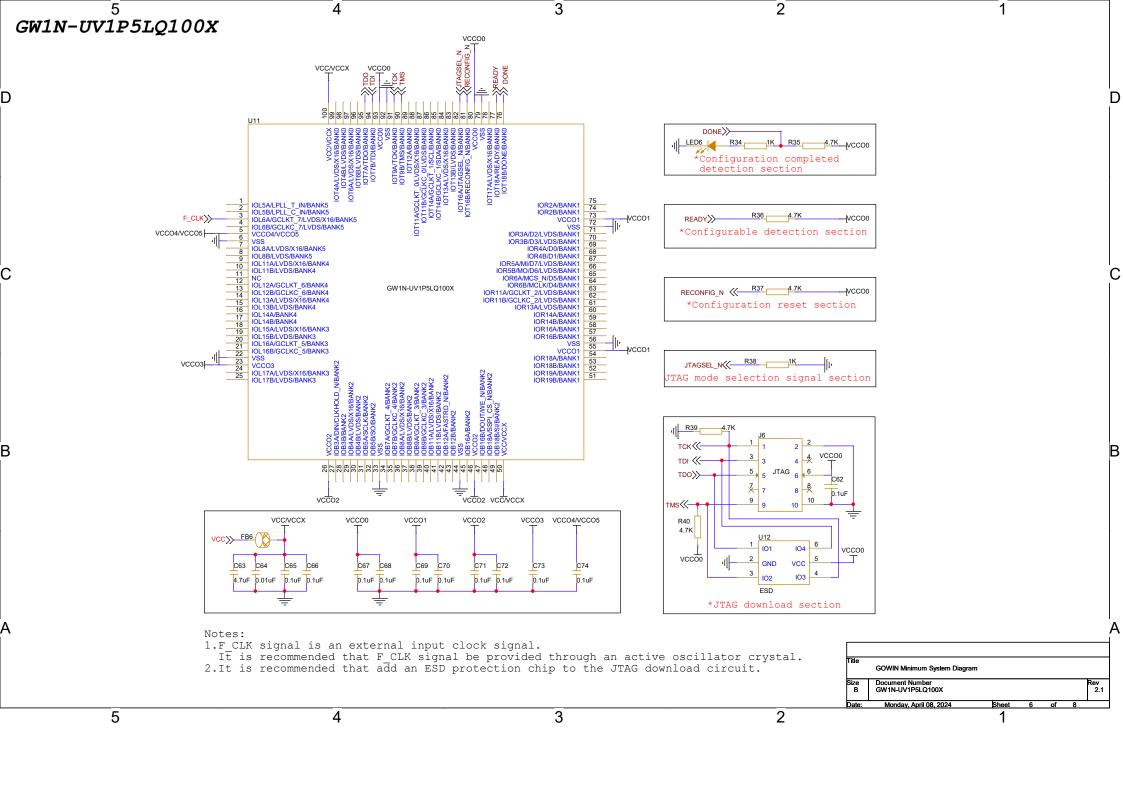


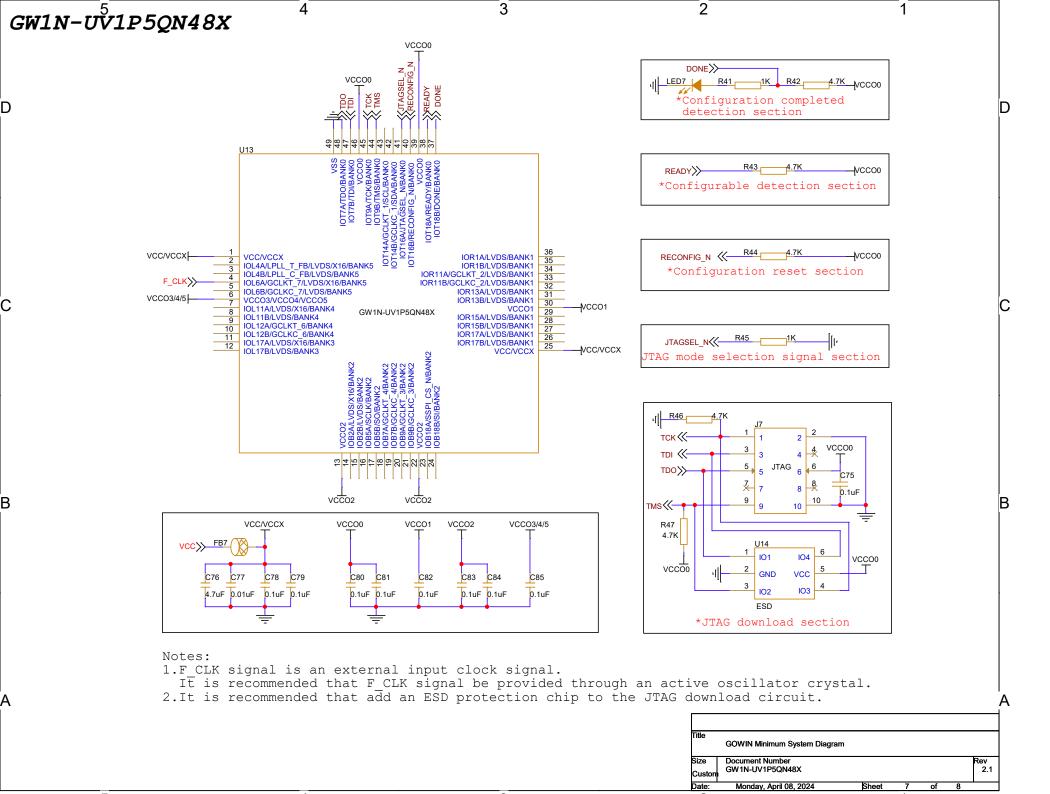
 $GW1N-LV{5}$ 3 VCC00 DONE R23 *Configuration completed detection section VCC1P2 IOR1A/LVDS/BANK1 IOL4A/LPLL_T_FB/LVDS/X16/BANK5 IOR1B/LVDS/BANK1 IOL4B/LPLL_C_FB/LVDS/BANK5 IOL6A/GCLKT_7/LVDS/X16/BANK5 IOR11A/GCLKT_2/LVDS/BANK1 F_CLK>> IOR11B/GCLKC_2/LVDS/BANK1 IOL6B/GCLKC_7/LVDS/BANK5 IOR13A/LVDS/BANK1 VCCO3/4/5 READY >> VCCO3/VCCO4/VCCO5 IOR13B/LVDS/BANK1 VCCO1/VCCX IOL11A/LVDS/X16/BANK4 VCCO1/VCCX GW1N-LV1P5QN48XF 29 *Configurable detection section IOL11B/LVDS/BANK4 IOR15A/LVDS/BANK1 IOL12A/GCLKT 6/BANK4 IOR15B/LVDS/BANK1 IOL12B/GCLKC 6/BANK4 IOR17A/LVDS/BANK1 IOL17A/LVDS/X16/BANK3 IOR17B/LVDS/BANK1 VCC1P2 IOL17B/LVDS/BANK3 R25 VCC00 TDI ≪ TDO>> C38 0.1uF VCC02 VCC02 10 TMS<< VCC1P2 VCC00 VCCO1/VCCX VCCO2 VCCO3/4/5 R26 4.7K VCC>> FB4 101 104 VCC00 VCC00 GND VCC C46 C39 C40 C43 C41 C45 C47 C48 3 103 102 0.1uF 0.1uF 0.1uF 0.1uF 4.7uF 0.01uF 0.1uF 0.1uF 0.1uF 0.1uF ESD *JTAG download section Notes: 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal. 2.It is recommended that add an ESD protection chip to the JTAG download circuit. Title **GOWIN Minimum System Diagram**

> Rev 2.1

Document Number GW1N-LV1P5QN48XF Monday, April 08, 2024







GW1N-UV1P5QN48XF3 VCC00 VCC00 DONE *Configuration completed detection section VCC/VCCX VCC/VCCX IOR1A/LVDS/BANK1 IOR1B/LVDS/BANK1 IOL4A/LPLL T FB/LVDS/X16/BANK5 IOL4B/LPLL_C_FB/LVDS/BANK5 IOL6A/GCLKT_7/LVDS/X16/BANK5 IOR11A/GCLKT 2/LVDS/BANK1 F_CLK> IOR11B/GCLKC 2/LVDS/BANK1 IOL6B/GCLKC 7/LVDS/BANK5 IOR13A/LVDS/BANK1 VCCO3/4/5 IOR13B/LVDS/BANK1 READY VCCO3/VCCO4/VCCO5 VCC01 IOL11A/LVDS/X16/BANK4 VCC01 GW1N-UV1P5QN48XF *Configurable detection section IOR15A/LVDS/BANK1 IOL11B/LVDS/BANK4 IOR15B/LVDS/BANK1 IOR17A/LVDS/BANK1 IOL12A/GCLKT_6/BANK4 IOL12B/GCLKC_6/BANK4 10 11 IOL12B/GCLKC_6/BANK4 12 IOL17A/LVDS/X16/BANK3 IOR17B/LVDS/BANK1 -vcc/vccx IOL17B/LVDS/BANK3 VCC/VCCX R51 TCK << VCC00 TDI ≪ TDO>> 0.1uF VCC02 VCC02 10 гмѕ≪− VCC/VCCX VCC00 VCCO1 VCCO2 VCCO3/4/5 R52 4.7K VCC>> FB8 101 104 VCC00 VCC00 **GND** VCC C89 C94 C87 C90 C91 C92 C93 C95 C96 102 103 0.1uF 0.1uF 0.01uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF ÷ ÷ *JTAG download section Notes: 1.F CLK signal is an external input clock signal. $\overline{\text{It}}$ is recommended that F_CLK signal be provided through an active oscillator crystal. 2.It is recommended that add an ESD protection chip to the JTAG download circuit. Title **GOWIN Minimum System Diagram** Rev 2.1 Document Number GW1N-UV1P5QN48XF

Monday, April 08, 2024