U1B

H6

G6

H5

G5

F5

G3

G2

H1

G1

D6

E6

B7

A8

VCC1P2

VCCO0/2

VCCO1/3

VCCX

TMS\

TCK 1

TDIS

JTAGSEL\_N >>

IO Bank2

IOB29A/GCLKT\_4/LVDS/X16

IOB29B/GCLKC\_4/LVDS

IOB13A/LVDS/X16

IOB17A/LVDS/X16

IOB23A/LVDS/X16

IOB27A/LVDS/X16

IOB33A/LVDS/X16

IOB39A/LVDS/X16

IOB41A/LVDS/X16

IOB8A/LVDS/X16

IOL11A/TMS/LVDS

IOL11B/TCK/LVDS

IOL13A/TDO/LVDS

IOL15A/GCLKT 6/LVDS

IOL15B/GCLKC\_6/LVDS

IOL5A/JTAGSEL N/LPLL T IN

VCC E5 VCC

VCCX F6 VCCX D5 VSS E4 VSS GW1N-LV9CM64

C6

C3

Power/Gnd

VCCO0/VCCO2

VCCO1/VCCO3

IOB13B/LVDS

IOB17B/LVDS

IOB23B/LVDS

IOB27B/LVDS

IOB33B/LVDS

IOB39B/LVDS

IOB41B/LVDS

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IOL12B/TDI

IOL22A/LVDS

IOL22B/LVDS

A7 IOL5B/LPLL\_C\_IN

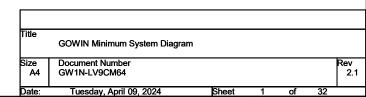
IOT11A/X16

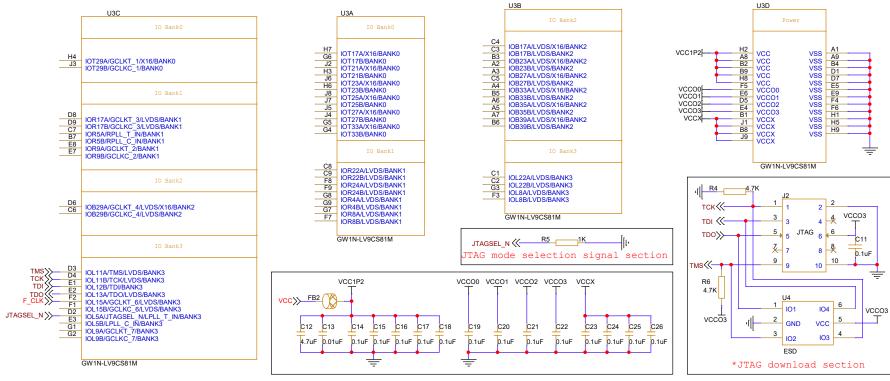
IOT8A/X16 IOT8B GW1N-LV9CM64

IOT11B

### Notes:

- 1.F CLK signal is an external input clock signal.
- $\overline{\text{It}}$  is recommended that F CLK signal be provided through an active oscillator crystal.
- 2. It is recommended that add an ESD protection chip to the JTAG download circuit.





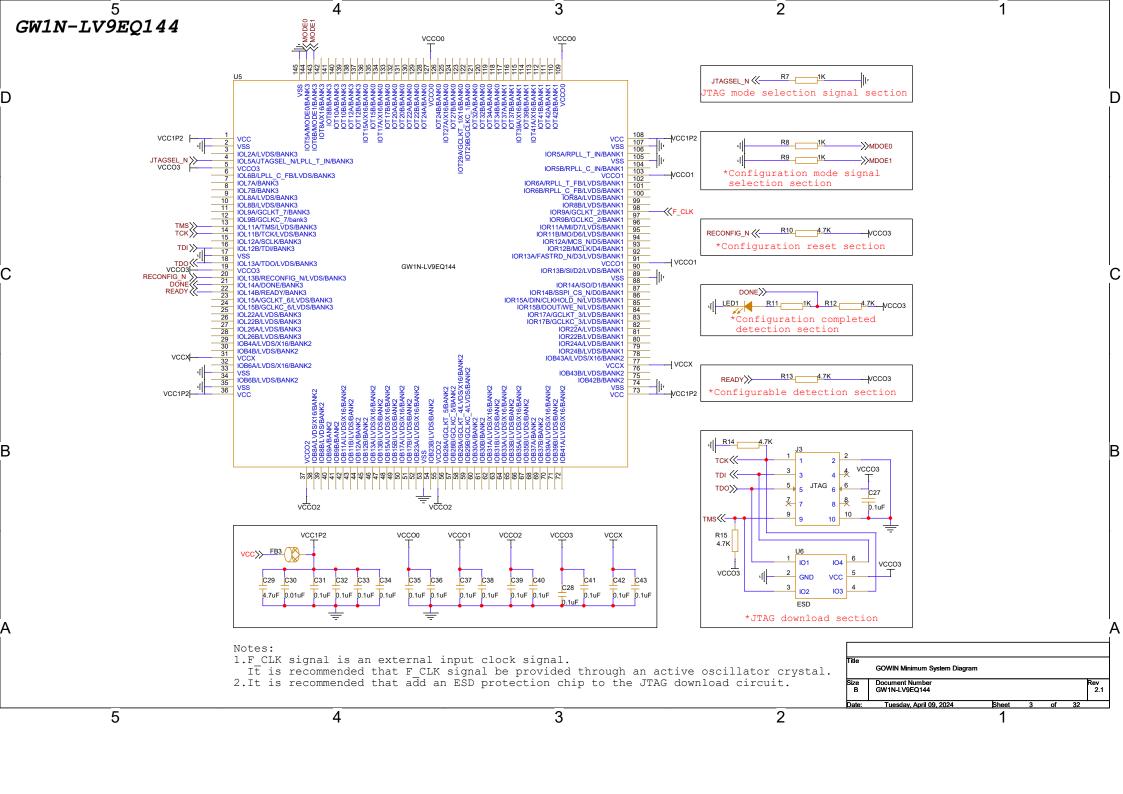
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- 1.F CLK signal is an external input clock signal.
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- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

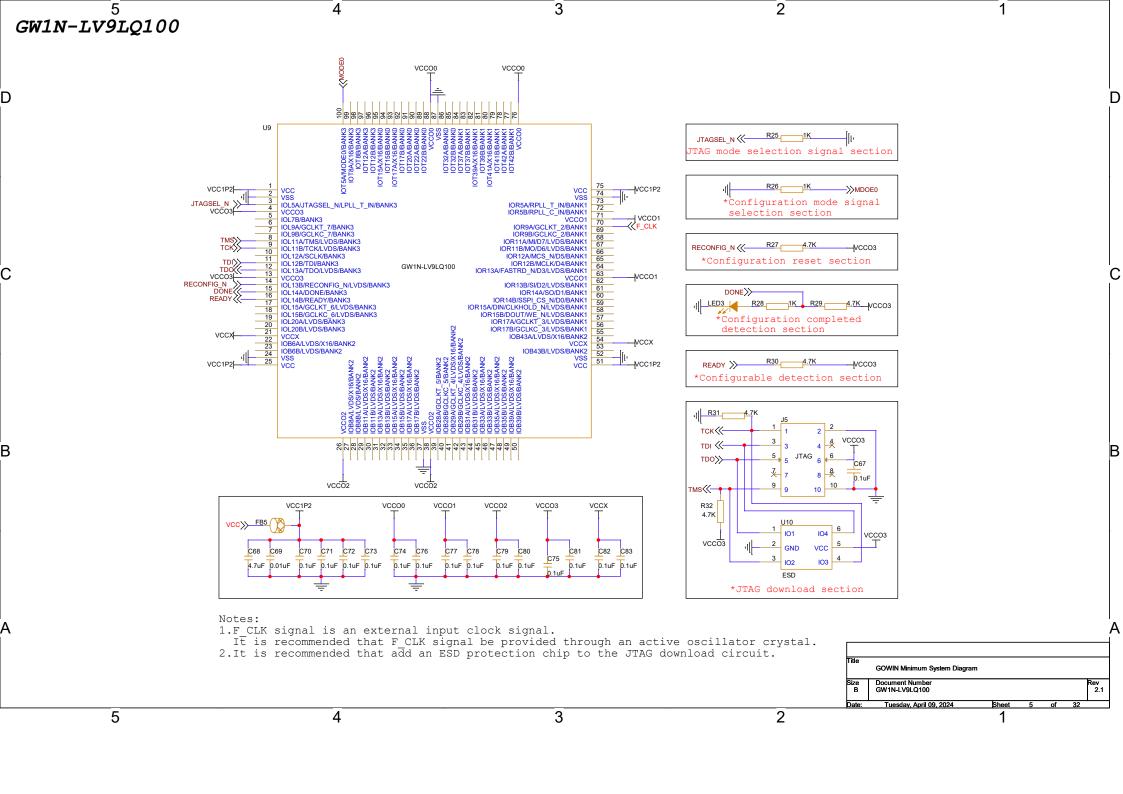
GOWIN Minimum System Diagram Document Number GW1N-LV9CS81M Rev 2.1 Tuesday, April 09, 2024

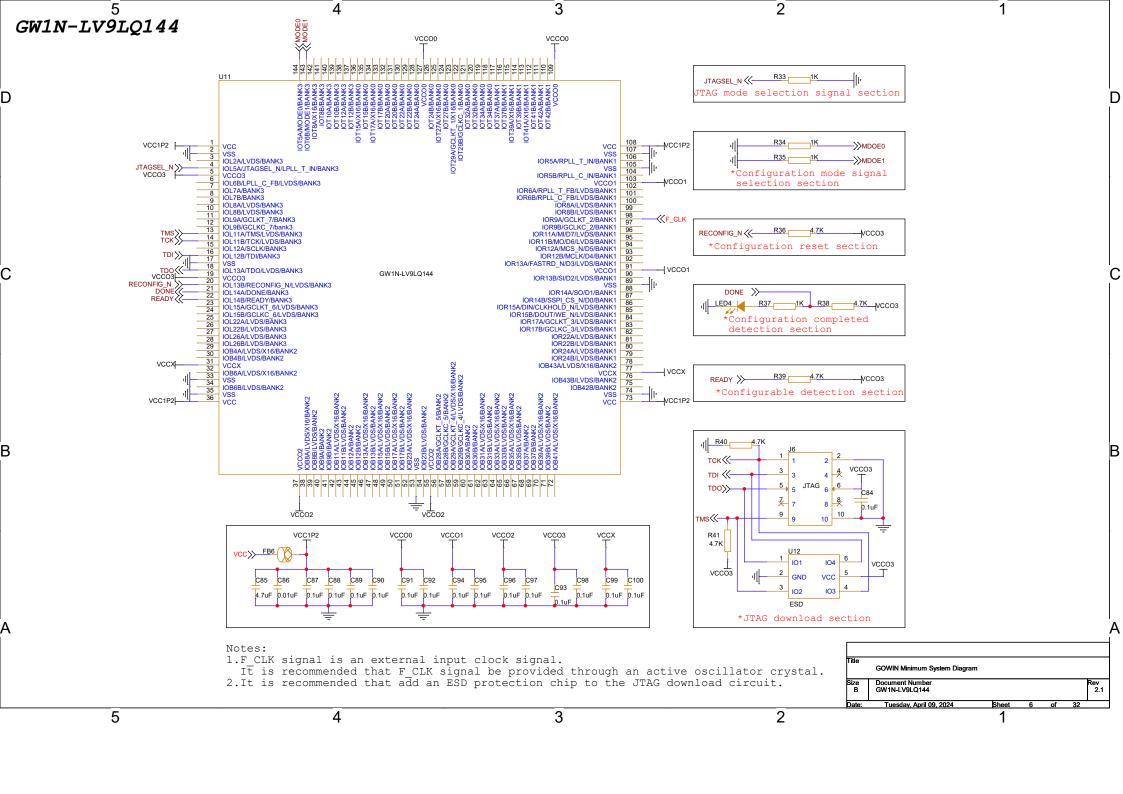
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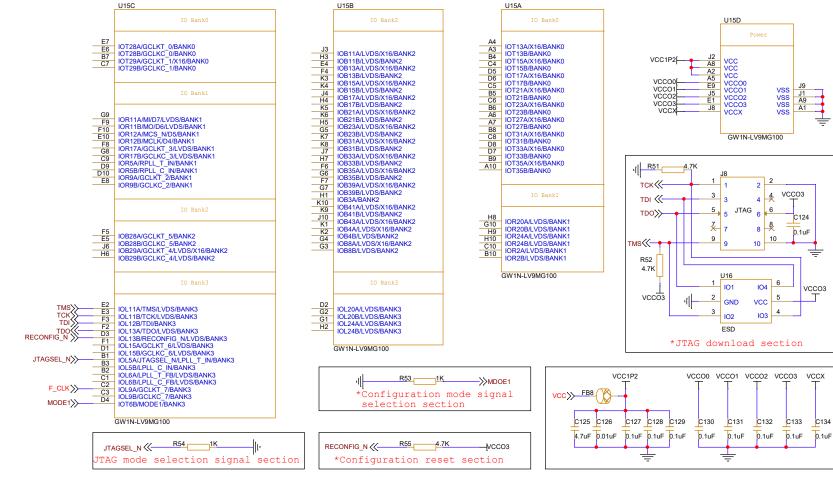


3 GW1N-LV9EQ176 VCC00 VCC00 vccx VCC00 ->>MDOE0 R17 ->>MDOE1 132 131 130 VCC1P2 VCC VSS VCC1P2 ->>MDOE2 IOL2A/LVDS/BANK3 VCCX 129 128 127 \*Configuration mode signal IOL2B/LVDS/BANK3 IOR5A/RPLL T IN/BANK1 IOR5B/RPLL\_C\_IN/BANK1 IOR6A/RPLL\_T\_FB/LVDS/BANK1 IOR6B/RPLL\_C\_FB/LVDS/BANK1 IOL3A/BANK3 selection section IOL3B/BANK3 IOL4A/LVDS/BANK3 IOL4B/LVDS/BANK3 TORSB/I VDS/BANK1 JTAGSEL\_N >>> IOL5A/JTAGSEL\_N/LPLL\_T\_IN/BANK3 IOR9A/GCLKT\_2/BANK1 IOL5B/LPLL\_C\_IN/BANK3 IOL6A/LPLL\_T\_FB/LVDS/BANK3 IOR9B/GCLKC\_2/BANK1 IOR11A/MI/D7/LVDS/BANK1 122 IOL6B/LPLL\_C\_FB/LVDS/BANK3 IOR11B/MO/D6/LVDS/BANK1 VCC03 IOR12A/MCS N/D5/BANK1 VCCO3 IOL9A/GCLKT 7/BANK3 IOR12B/MCLK/D4/BANK1 RECONFIG\_N 
R19
4.7K IOL9B/GCLKC 7/BANK3 IOR13A/FASTRD N/D3/LVDS/BANK1 VCC03 TMS IOL11A/TMS/LVDS/BANK3 IOL11B/TCK/LVDS/BANK3 IOR13B/SI/D2/LVDS/BANK1 IOR14A/SO/D1/BANK1 \*Configuration reset section IOL12A/SCLK/BANK3 VCC01 IOR14B/SSPI\_CS\_N/D0/BANK1 IOI 12B/TDI/BANK3 TDO RECONFIG\_N IOL13A/TDO/LVDS/BANK3 IOL13B/RECONFIG\_N/LVDS/BANK3 IOR15A/DIN/CLKHOLD\_N/LVDS/BANK1
IOR15B/DOUT/WE\_N/LVDS/BANK1 GW 1N-I V9FO176 VCCO3 IOR17A/GCLKT\_3/LVDS/BANK1 IOL14A/DONE/BANK3 VCC01 VCC01 IOL15A/GCLKT\_6/LVDS/BANK3 IOL15B/GCLKC\_6/LVDS/BANK3 IOR22A/LVDS/BANK1 IOR22B/LVDS/BANK1 IOL17A/LVDS/BANK3 IOR24A/LVDS/BANK1 DONE >> IOL17B/LVDS/BANK3 IOL20A/LVDS/BANK3 IOR24B/LVDS/BANK1 IOR26A/LVDS/BANK1 1K R21 4.7K VCCO3 \*Configuration completed IOL20B/LVDS/BANK3 IOL22A/LVDS/BANK3 IOR26B/LVDS//BANK1 IOR27A/BANK1 IOL22B/LVDS/BANK3 IOR27B/BANK1 IOB46A/BANK2 detection section IOL24B/LVDS/BANK3 IOB46B/BANK2 vcco3F IOB45A/I VDS/X16/BANK2 VCCO3 IOL27A/BANK3 IOB45B/LVDS/BANK2 IOB2A/LVDS/X16/BANK2 IOR44A/RANK2 IOB2B/LVDS/BANK2 IOB44B/BANK2 IOB4A/LVDS/X16/BANK2 IOB4B/LVDS/BANK2 VCCO1 IOB43A/LVDS/X16/BANK2 40 41 42 R22 VCCX VCCX IOB6A/LVDS/X16/BANK2 IOB43B/LVDS/BANK2 IOB42A/BANK2 JTAGSEL\_N <<-TAG mode selection signal section IOB6B/LVDS/BANK2 IOB42B/BANK2 VSS 43 44 VCC1P2 .[ R23 r TDI << ÷ ŧ TDO>>> VCC02 VCC02 VCC02 мs<<-R24 VCC00 VCC01 VCCO2 VCCO3 vccx 4.7K VCC>> FB4 IO1 IO4 **VCCO3** VCC03 GND VCC C45 C48 C49 C50 C52 C53 C55 C56 C58 C59 C60 C61 C62 C63 103 IO<sub>2</sub> 0.1uF 0.1uF 0.1uF ESD \*JTAG download section 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal. 2.It is recommended that add an ESD protection chip to the JTAG download circuit. GOWIN Minimum System Diagram Document Number GW1N-LV9EQ176 Rev 2.1 ize A3





GW1N-LV9LQ176 VCC00 VCCO0 VCCX VCC00 R42 →>>MDOE0 ->>MDOE1 VCC1P2L 6 VCC1P2 VCC VSS ->>MDOE2 VSS 130 129 128 127 IOL2A/LVDS/BANK3 VCCX MCCX IOR5A/RPLL\_T\_IN/BANK1 IOR5B/RPLL\_C\_IN/BANK1 IOR6A/RPLL\_T\_FB/LVDS/BANK1 IOR6B/RPLL\_C\_FB/LVDS/BANK1 \*Configuration mode signal IOL2B/LVDS/BANK3 IOL3A/BANK3 selection section IOL3B/BANK3 IOL4A/LVDS/BANK3 125 124 123 122 121 120 TORNELL C FB/LVDS/BANK1
TOR8B/LVDS/BANK1
TOR9A/GCLKT 2/BANK1
TOR9B/GCLKC 2/BANK1
TOR11A/MI/D7/LVDS/BANK1
TOR11B/MO/D6/LVDS/BANK1 IOL4B/LVDS/BANK3 JTAGSEL\_N >> IOL5A/JTAGSEL N/LPLL T\_IN/BANK3
IOL5B/LPLL C\_IN/BANK3
IOL6A/LPLL\_T\_FB/LVDS/BANK3
IOL6B/LPLL\_C\_FB/LVDS/BANK3 < VCC03 VCCO3 IOR12A/MCS N/D5/BANK1 119 118 117 IOL9A/GCLKT 7/BANK3 IOR12B/MCLK/D4/BANK1 R45 4.7K RECONFIG N <<--VCCO3 IOL9B/GCLKC\_7/BANK3 IOL11A/TMS/LVDS/BANK3 IOR13A/FASTRD\_N/D3/LVDS/BANK1 IOR13B/SI/D2/LVDS/BANK1 TMS \*Configuration reset section IOL11B/TCK/LVDS/BANK3 IOR14A/SO/D1/BANK1 IOI 12A/SCLK/BANK3 VCCO1 IOR14B/SSPI\_CS\_N/DO/BANK1
IOR15A/DIN/CLKHOLD\_N/LVDS/BANK1
IOR15B/DOUT/WE\_N/LVDS/BANK1
IOR17A/GCLKT\_3/LVDS/BANK1 TDI \ IOL12B/TDI/BANK3 IOL13A/TDO/LVDS/BANK3 TDO RECONFIG N VCCO3 GW 1N-I V9I O176 IOL13B/RECONFIG\_N/LVDS/BANK3 VCCO3 DONE ( IOL14A/DONE/BANK3 VCC01 VCC01 109 108 107 106 IOL15A/GCLKT\_6/LVDS/BANK3 IOL15B/GCLKC\_6/LVDS/BANK3 IOR22A/LVDS/BANK1 IOR22B/LVDS/BANK1 IOL17A/LVDS/BANK3 IOL17B/LVDS/BANK3 IOR24A/LVDS/BANK1 IOR24B/LVDS/BANK1 DONE >> LED5 R46 \_\_1K \_\_R47 \_\_ 4.7K VCCO3 IOL20A/LVDS/BANK3 IOL20B/LVDS/BANK3 IOR26A/LVDS/BANK1 IOR26B/LVDS//BANK1 \*Configuration completed IOL22A/LVDS/BANK3 IOL22B/LVDS/BANK3 IOR27A/BANK1 IOR27B/BANK1 detection section IOL24A/LVDS/BANK3 IOB46A/BANK2 IOB46B/BANK2 IOL24B/LVDS/BANK3 VCCO3L IOB45A/LVDS/X16/BANK2 IOI 27A/BANK3 IOB45B/LVDS/BANK2 IOB2A/LVDS/X16/BANK2 IOB44A/BANK2 IOB2B/I VDS/BANK2 IOB44B/BANK2 VCCO1 IOB43A/LVDS/X16/BANK2 IOB43B/LVDS/BANK2 IOB4B/LVDS/BANK2 R48 vccx-VCCX JTAGSEL N <<-IOB6A/LVDS/X16/BANK2 IOB6B/LVDS/BANK2 IOB42A/BANK2 IOB42B/BANK2 42 43 44 JTAG mode selection signal section VCC1P2 VCC1P2 VCC VCCO3 TDI << ÷ C101 VCC02 VCC02 vccx VCC02 0.1uF гмѕ<<-R50 VCC1P2 VCC00 VCCO2 VCC03 VCCX 4.7K VCC>> FB7 101 104 VCCO3 VCCO3 GND VCC C114 C115 C116 C104 C105 C106 C107 C108 C109 C110 C111 C112 C113 C117 C118 C119 C120 C121 C122 C123 C102 C103 102 103 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 4.7uF 0.01uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF .1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF FSD \*JTAG download section 1.F CLK signal is an external input clock signal.  $\overline{\text{It}}$  is recommended that F CLK signal be provided through an active oscillator crystal. 2.It is recommended that add an ESD protection chip to the JTAG download circuit. GOWIN Minimum System Diagram Rev 2.1 ize A3 GW1N-LV9LQ176



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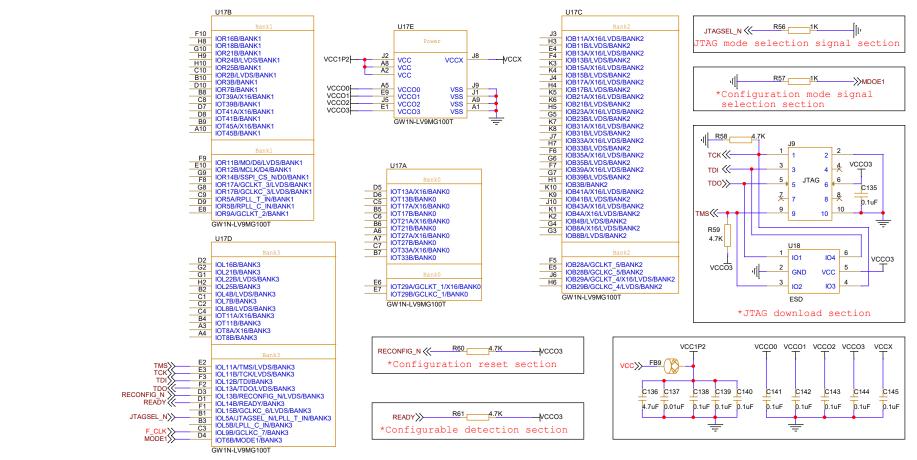
- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title **GOWIN Minimum System Diagram** Document Number GW1N-LV9MG100 Rev 2.1 Wednesday, April 10, 2024

3 4

D

Α



5

- 1.F CLK signal is an external input clock signal.
  - It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

**GOWIN Minimum System Diagram** Document Number GW1N-LV9MG100T Rev 2.1 Tuesday, April 09, 2024

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- 1.F CLK signal is an external input clock signal.
  - It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

**GOWIN Minimum System Diagram** Document Number Rev 2.1 GW1N-LV9MG160 Wednesday, April 10, 2024

3 4

2

U19C

VCC VCC

VCC

VCC00

VCC01

VCC01

VCCO2 VCCO2

VCCO3

VCCX

VCCX

VCCX

R62 -

selection section

U20 101

GND

102

**FSD** 

\*JTAG download section

104

vcc

103

GW1N-LV9MG160

\*Configuration mode signal

VSS VSS VSS

VSS

VSS

VSS VSS

VSS

VSS VSS VSS

N13

M3 M12

L11 D4 D11

C3 C12 B2 B13

÷

->>MDOE0

>>MDOE1

->>MDOE2

VCCO3

C146

0.1uF

ŧ

VCCO3

L4

A1 A14

C11

C4 D12

L12

M11 M4

D3 L3

C13 C2 M13

M2

4

3

GOWIN Minimum System Diagram Document Numbe Rev 2.1 GW1N-I V9PG256 Tuesday, April 09, 2024

2

4

VCCO0/3

JTAGSEL\_N

RECONFIG N

VCC1P2

TCK

TDI

TDO

DONE

\*JTAG download section

## Notes:

VCC>> FB13

C239 C240

4.7uF 0.01uF

1.F CLK signal is an external input clock signal.

VCCO0/3

C243

0.1uF

VCC1P2

MODE1

U25

VCCO0/VCCO3

IOL12B/TDI/BANK3

IOL14A/DONE/BANK3

VCC1P2

C241 C242

0.1uF 0.1uF

IOL13A/TDO/LVDS/BANK3

11 IOL15A/GCLKT\_6/LVDS/BANK3

12 IOL15B/GCLKC\_6/LVDS/BANK3

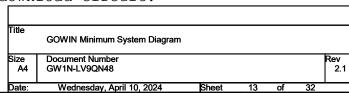
IOL5A/JTAGSEL\_N/LPLL\_T\_IN/BANK3 IOL11A/TMS/LVDS/BANK3

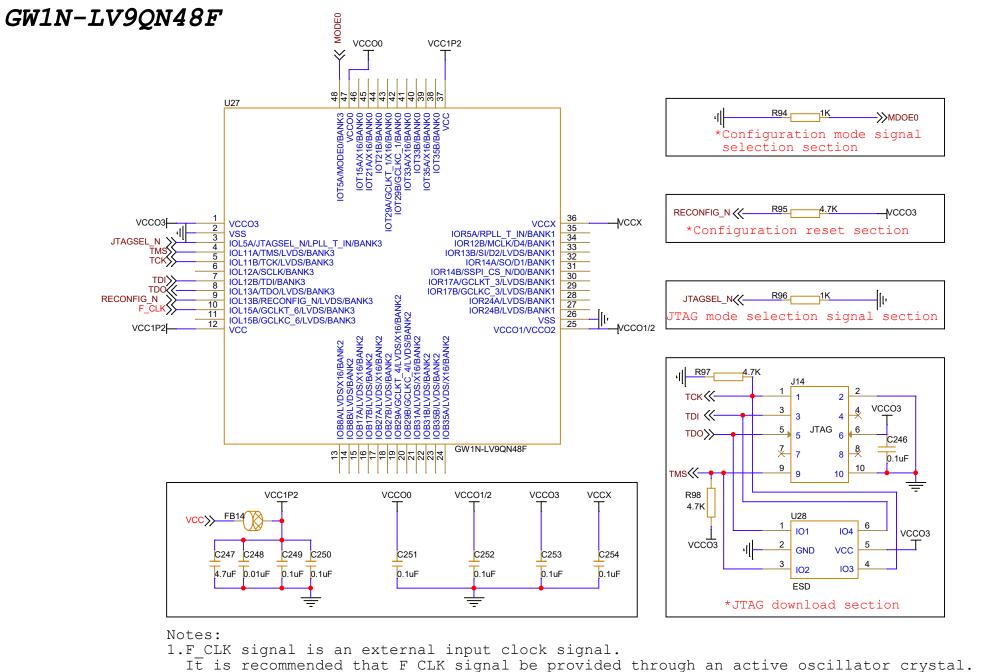
IOL13B/RECONFIG\_N/LVDS/BANK3

IOL11B/TCK/LVDS/BANK3 GW1N-LV9QN48

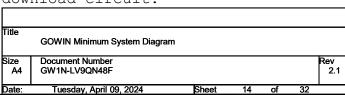
VSS

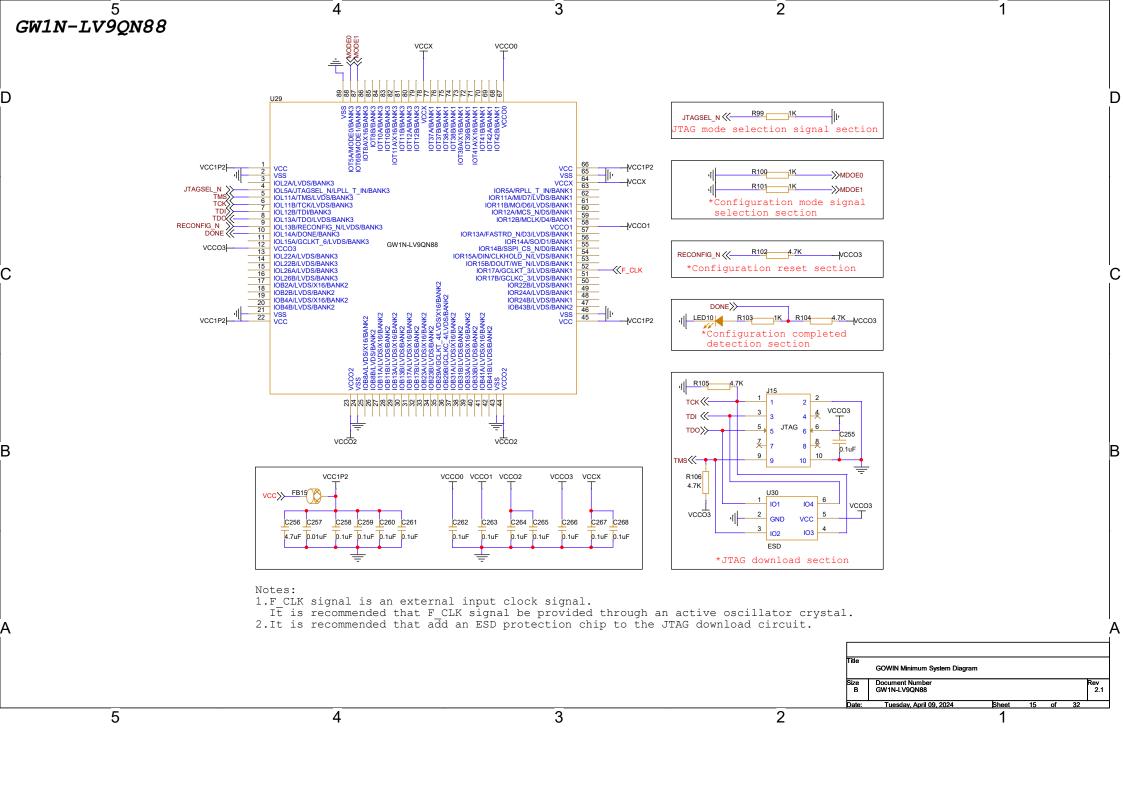
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

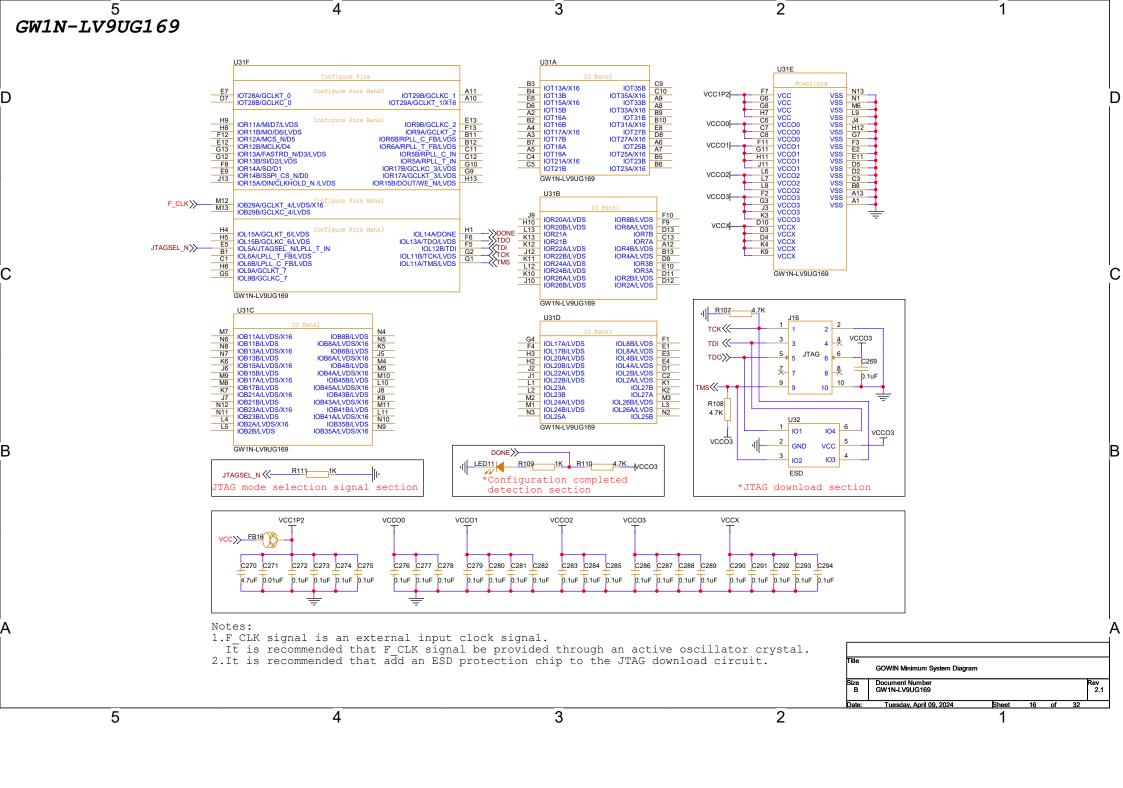




2. It is recommended that add an ESD protection chip to the JTAG download circuit.









1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.

2.It is recommended that  $\overline{add}$  an ESD protection chip to the JTAG download circuit.

GOWIN Minimum System Diagram Document Number ₹ev 2.1 GW1N-I V9LIG332 Tuesday, April 09, 2024

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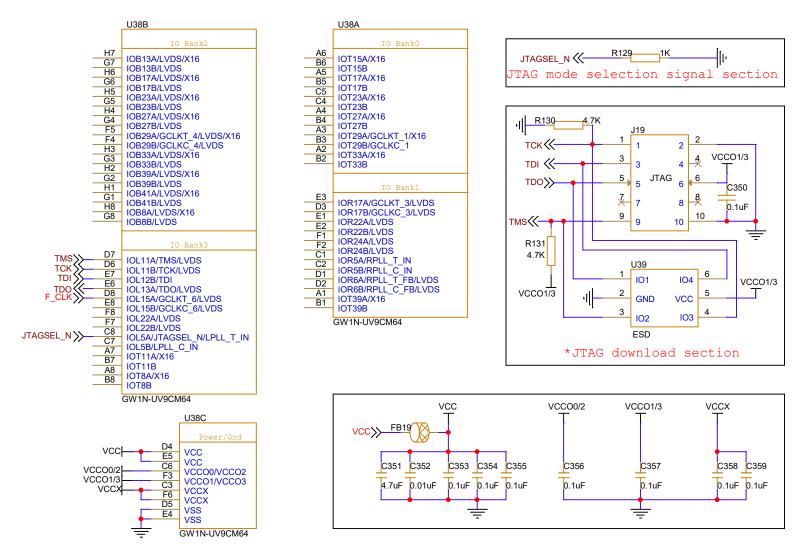
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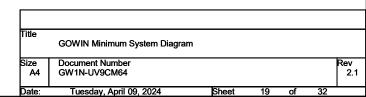
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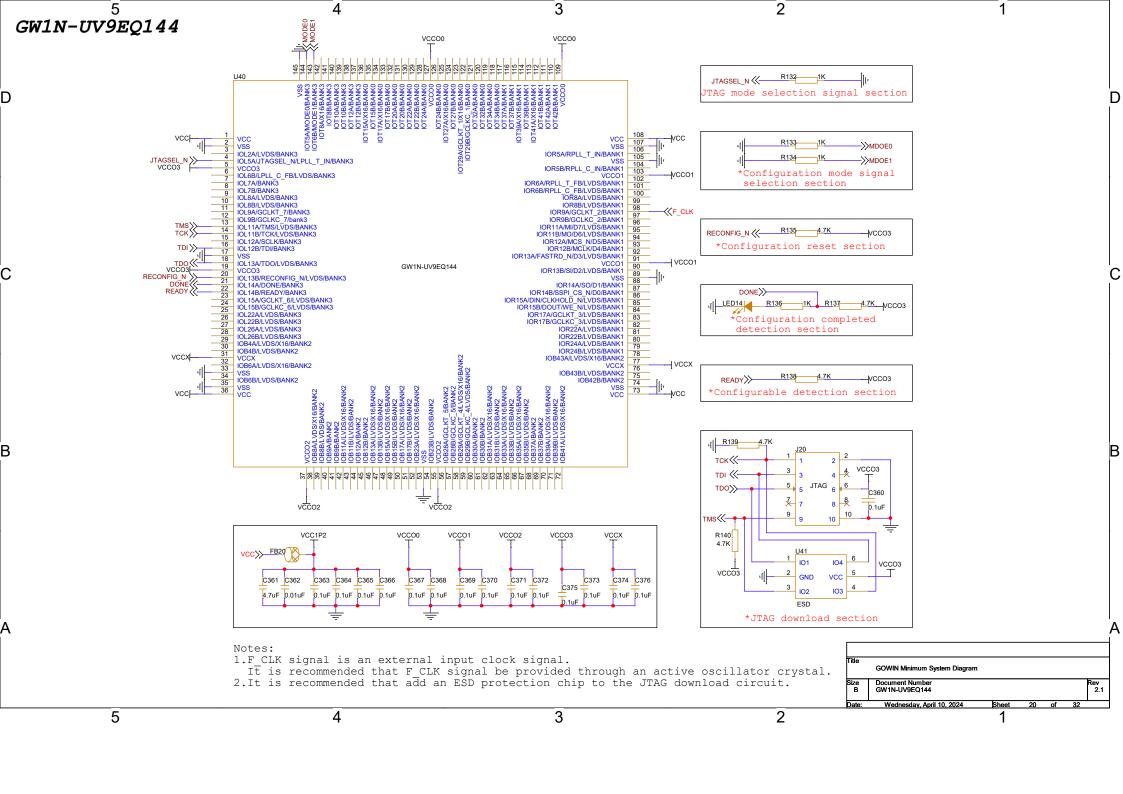
FSD

\*JTAG download section

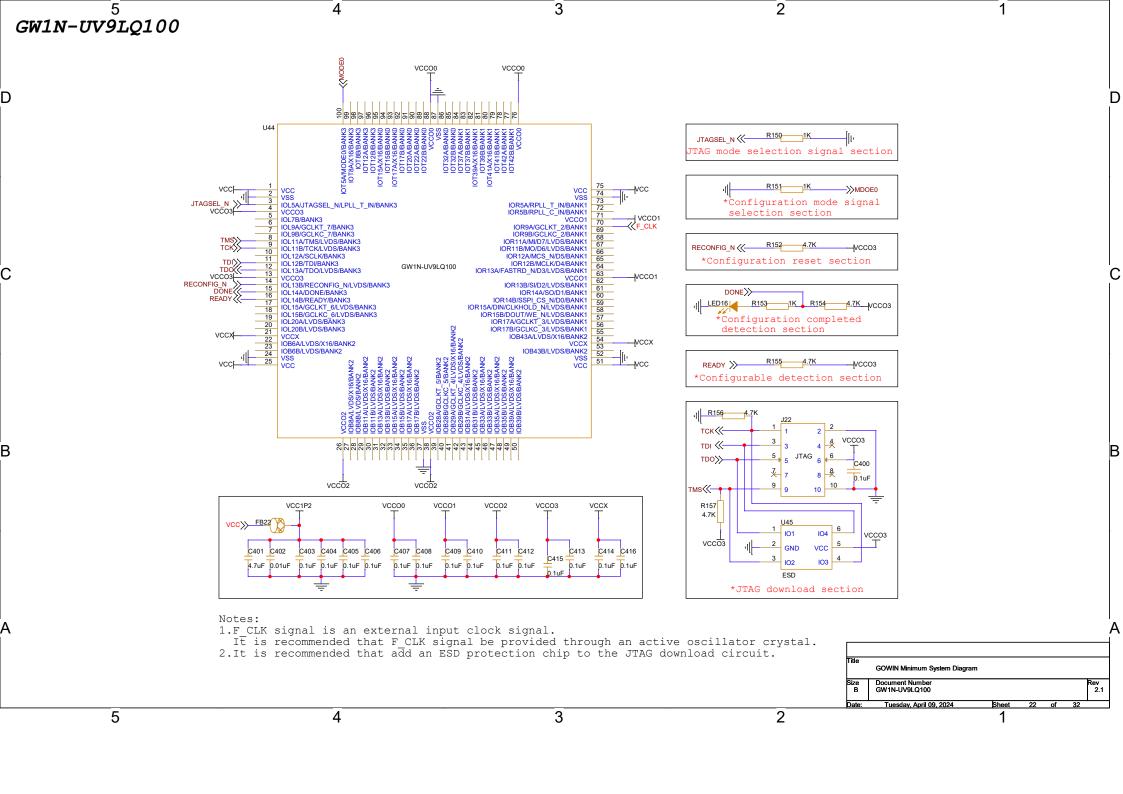


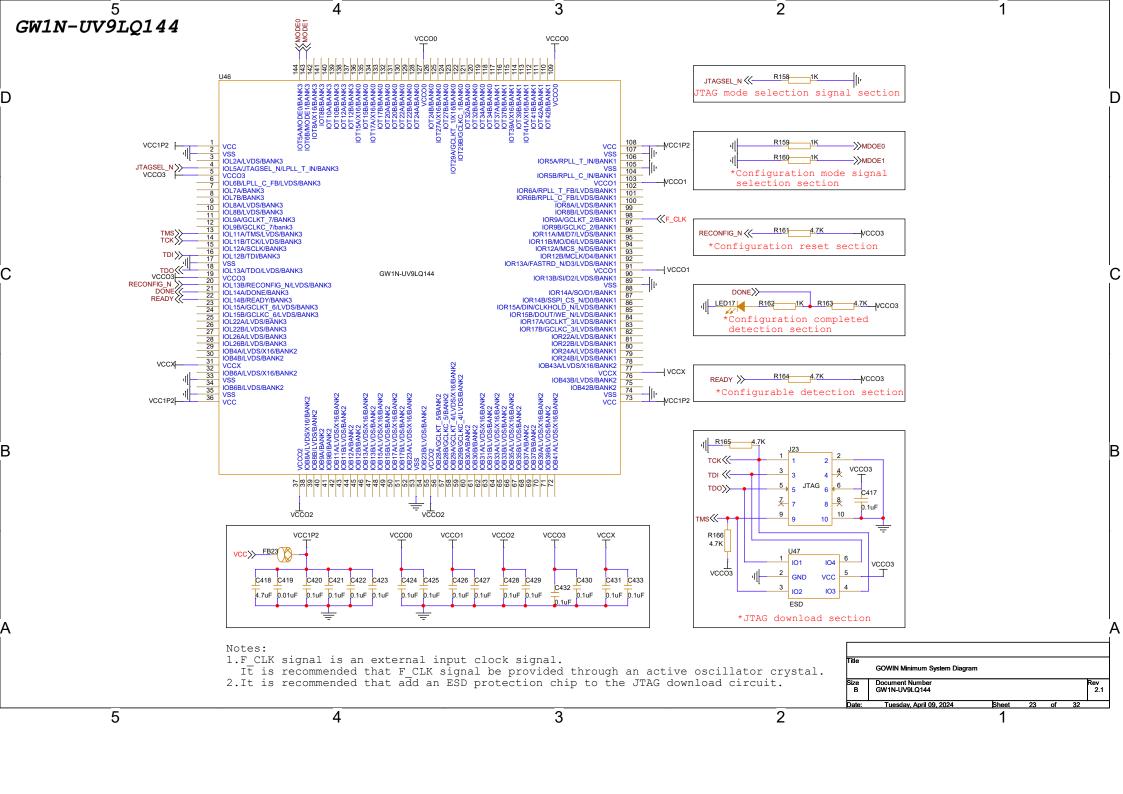
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- 2. It is recommended that add an ESD protection chip to the JTAG download circuit.



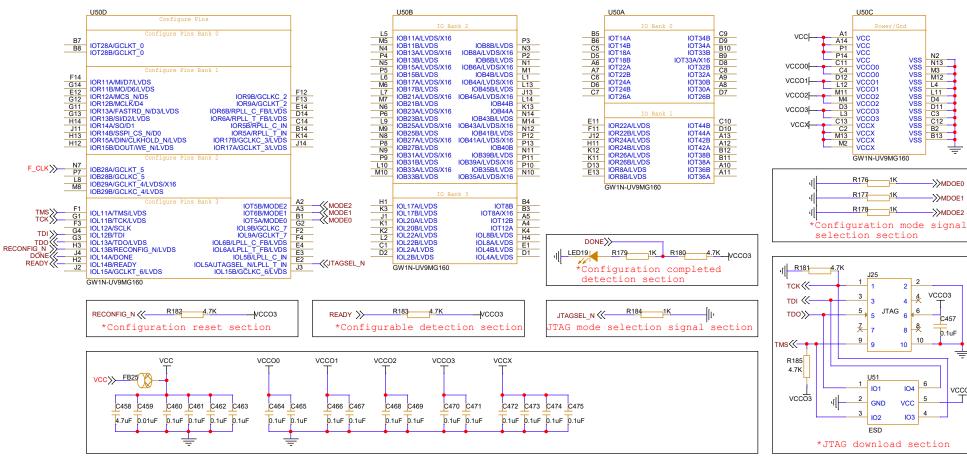


3 GW1N-UV9EQ176 VCC00 VCC00 vccx VCC00 ->>MDOE0 R142 ->>MDOE1 VCC VSS ->>MDOE2 VSS IOL2A/LVDS/BANK3 VCCX 129 128 127 IOL2B/LVDS/BANK3 IOR5A/RPLL T IN/BANK1 \*Configuration mode signal IOR5B/RPLL\_C\_IN/BANK1 IOR6A/RPLL\_T\_FB/LVDS/BANK1 IOR6B/RPLL\_C\_FB/LVDS/BANK1 IOL3A/BANK3 selection section IOL3B/BANK3 IOL4A/LVDS/BANK3 IOL4B/LVDS/BANK3 TORSB/I VDS/BANK1 JTAGSEL\_N >>> IOL5A/JTAGSEL\_N/LPLL\_T\_IN/BANK3 IOR9A/GCLKT\_2/BANK1 IOL5B/LPLL\_C\_IN/BANK3 IOL6A/LPLL\_T\_FB/LVDS/BANK3 IOR9B/GCLKC\_2/BANK1 IOR11A/MI/D7/LVDS/BANK1 122 IOL6B/LPLL\_C\_FB/LVDS/BANK3 IOR11B/MO/D6/LVDS/BANK1 VCC03 IOR12A/MCS N/D5/BANK1 VCCO3 IOL9A/GCLKT 7/BANK3 IOR12B/MCLK/D4/BANK1 RECONFIG\_N 
R144
4.7K IOL9B/GCLKC 7/BANK3 IOR13A/FASTRD N/D3/LVDS/BANK1 VCC03 TMS IOL11A/TMS/LVDS/BANK3 IOL11B/TCK/LVDS/BANK3 IOR13B/SI/D2/LVDS/BANK1 IOR14A/SO/D1/BANK1 \*Configuration reset section IOL12A/SCLK/BANK3 VCC01 IOR14B/SSPI\_CS\_N/D0/BANK1 IOI 12B/TDI/BANK3 RECONFIG\_N IOL13A/TDO/LVDS/BANK3 IOL13B/RECONFIG\_N/LVDS/BANK3 IOR15A/DIN/CLKHOLD\_N/LVDS/BANK1
IOR15B/DOUT/WE\_N/LVDS/BANK1 GW1N-UV9FO176 VCCO3 IOR17A/GCLKT\_3/LVDS/BANK1 DONE ( IOL14A/DONE/BANK3 VCC01 VCC01 IOL15A/GCLKT\_6/LVDS/BANK3 IOL15B/GCLKC\_6/LVDS/BANK3 IOR22A/LVDS/BANK1 IOR22B/LVDS/BANK1 IOL17A/LVDS/BANK3 IOR24A/LVDS/BANK1 DONE >> IOL17B/LVDS/BANK3 IOL20A/LVDS/BANK3 IOR24B/LVDS/BANK1 IOR26A/LVDS/BANK1 1K R146 4.7K VCCO3 \*Configuration completed IOL20B/LVDS/BANK3 IOL22A/LVDS/BANK3 IOR26B/LVDS//BANK1 IOR27A/BANK1 IOL22B/LVDS/BANK3 IOR27B/BANK1 IOB46A/BANK2 detection section IOL24B/LVDS/BANK3 IOB46B/BANK2 vcco3F IOB45A/I VDS/X16/BANK2 VCCO3 IOL27A/BANK3 IOB45B/LVDS/BANK2 IOB2A/LVDS/X16/BANK2 IOR44A/RANK2 IOB2B/LVDS/BANK2 IOB44B/BANK2 IOB4A/LVDS/X16/BANK2 IOB4B/LVDS/BANK2 VCCO1 IOB43A/LVDS/X16/BANK2 40 IOB4B/LVDS/BANK2 VCCX IOB6A/LVDS/X16/BANK2 10B6B/LVDS/X16/BANK2 R147 VCCX IOB43B/LVDS/BANK2 IOB42A/BANK2 JTAGSEL\_N <<-TAG mode selection signal section IOB6B/LVDS/BANK2 IOB42B/BANK2 VSS 43 44 vcc| <u>| R148</u> TDI << ÷ ŧ TDO>>> VCC02 VCC02 VCC02 0.1uF мs<<-R149 VCC00 VCC01 VCCO2 VCCO3 vccx 4.7K U43 VCC>> FB21 101 IO4 **VCCO3** VCC03 GND VCC C380 C381 C382 C383 C384 C385 C386 C388 C389 C390 C391 C392 C393 C394 C395 C396 C397 C398 C399 103 IO<sub>2</sub> 0.1uF 0.1uF 0.1uF .1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF ESD \*JTAG download section 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal. 2.It is recommended that add an ESD protection chip to the JTAG download circuit. GOWIN Minimum System Diagram Rev 2.1 ize A3 GW1N-UV9EQ176



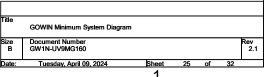


3 GW1N-UV9LQ176 VCC00 VCCO0 VCCX VCC00 R167 →>>MDOE0 ->>MDOE1 VCCI-6 VCC VSS R169 ->>MDOE2 VSS 130 129 128 127 IOL2A/LVDS/BANK3 VCCX \*Configuration mode signal IOR5A/RPLL\_T\_IN/BANK1 IOR5B/RPLL\_C\_IN/BANK1 IOR6A/RPLL\_T\_FB/LVDS/BANK1 IOL2B/LVDS/BANK3 IOL3A/BANK3 selection section IOL3B/BANK3 IOL4A/LVDS/BANK3 IOR6B/RPLL C FB/LVDS/BANK1 125 124 123 122 121 120 TORNELL C FB/LVDS/BANK1
TOR8B/LVDS/BANK1
TOR9A/GCLKT 2/BANK1
TOR9B/GCLKC 2/BANK1
TOR11A/MI/D7/LVDS/BANK1
TOR11B/MO/D6/LVDS/BANK1 IOL4B/LVDS/BANK3 JTAGSEL\_N >> IOL5A/JTAGSEL N/LPLL T\_IN/BANK3
IOL5B/LPLL C\_IN/BANK3
IOL6A/LPLL\_T\_FB/LVDS/BANK3
IOL6B/LPLL\_C\_FB/LVDS/BANK3 < VCC03 VCCO3 IOR12A/MCS N/D5/BANK1 119 118 117 IOL9A/GCLKT 7/BANK3 IOR12B/MCLK/D4/BANK1 R170 4.7K RECONFIG N <<--VCCO3 IOL9B/GCLKC\_7/BANK3 IOL11A/TMS/LVDS/BANK3 IOR13A/FASTRD\_N/D3/LVDS/BANK1 IOR13B/SI/D2/LVDS/BANK1 TMS \*Configuration reset section IOL11B/TCK/LVDS/BANK3 IOR14A/SO/D1/BANK1 IOI 12A/SCLK/BANK3 VCCO1 IOR14B/SSPI\_CS\_N/DO/BANK1
IOR15A/DIN/CLKHOLD\_N/LVDS/BANK1
IOR15B/DOUT/WE\_N/LVDS/BANK1
IOR17A/GCLKT\_3/LVDS/BANK1 TDI \ IOL12B/TDI/BANK3 IOL13A/TDO/LVDS/BANK3 RECONFIG\_N VCC03 GW1N-UV9L0176 IOL13B/RECONFIG\_N/LVDS/BANK3 VCCO3 DONE ( VCC01 -VCCO1 109 108 107 106 IOL15A/GCLKT\_6/LVDS/BANK3 IOL15B/GCLKC\_6/LVDS/BANK3 IOR22A/LVDS/BANK1 IOR22B/LVDS/BANK1 IOL17A/LVDS/BANK3 IOL17B/LVDS/BANK3 IOR24A/LVDS/BANK1 IOR24B/LVDS/BANK1 DONE LED18 R171 1K R172 4.7K VCCO3 IOL20A/LVDS/BANK3 IOL20B/LVDS/BANK3 IOR26A/LVDS/BANK1 IOR26B/LVDS//BANK1 \*Configuration completed IOL22A/LVDS/BANK3 IOL22B/LVDS/BANK3 IOR27A/BANK1 IOR27B/BANK1 detection section IOL24A/LVDS/BANK3 IOB46A/BANK2 IOB46B/BANK2 IOL24B/LVDS/BANK3 VCCO3L IOB45A/LVDS/X16/BANK2 IOL27A/BANK3 IOB45B/LVDS/BANK2 IOB2A/LVDS/X16/BANK2 IOB44A/BANK2 IOB2B/I VDS/BANK2 IOB44B/BANK2 VCCO1 -VCCO1 IOB43A/LVDS/X16/BANK2 IOB43B/LVDS/BANK2 IOB4B/LVDS/BANK2 R173 VCCX-VCCX JTAGSEL N <<-IOB6A/LVDS/X16/BANK2 IOB6B/LVDS/BANK2 IOB42A/BANK2 IOB42B/BANK2 42 43 44 TAG mode selection signal section VCC| VCC VCCO3 TDI << ÷ C434 vc<del>c</del>02 VCC02 vccx VCC02 0.1uF гмs<< 10 R175 VCC1P2 VCC00 VCCO2 VCC03 VCCX 4.7K VCC>> FB24 101 104 VCCO3 VCCO3 GND VCC C437 C438 C439 C440 C441 C442 C443 C444 C445 C446 C447 C448 C449 C450 C451 C452 C453 C454 C455 C456 C435 C436 102 103 0.1uF 0.1uF 0.1uF 0.1uF 4.7uF 0.01uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF .1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF FSD \*JTAG download section 1.F CLK signal is an external input clock signal.  $\overline{\text{It}}$  is recommended that F CLK signal be provided through an active oscillator crystal. 2.It is recommended that add an ESD protection chip to the JTAG download circuit. GOWIN Minimum System Diagram Document Number GW1N-UV9LQ176 Rev 2.1 ize A3



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- 1.F CLK signal is an external input clock signal.
  - It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



VSS VSS VSS

VSS

VSS

VSS VSS

VSS

VSS VSS VSS

N13

M3 M12

L11 D4 D11

C3 C12 B2 B13

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->>MDOE0

>>MDOE1

->>MDOE2

VCCO3

104

vcc

103

C457

0.1uF

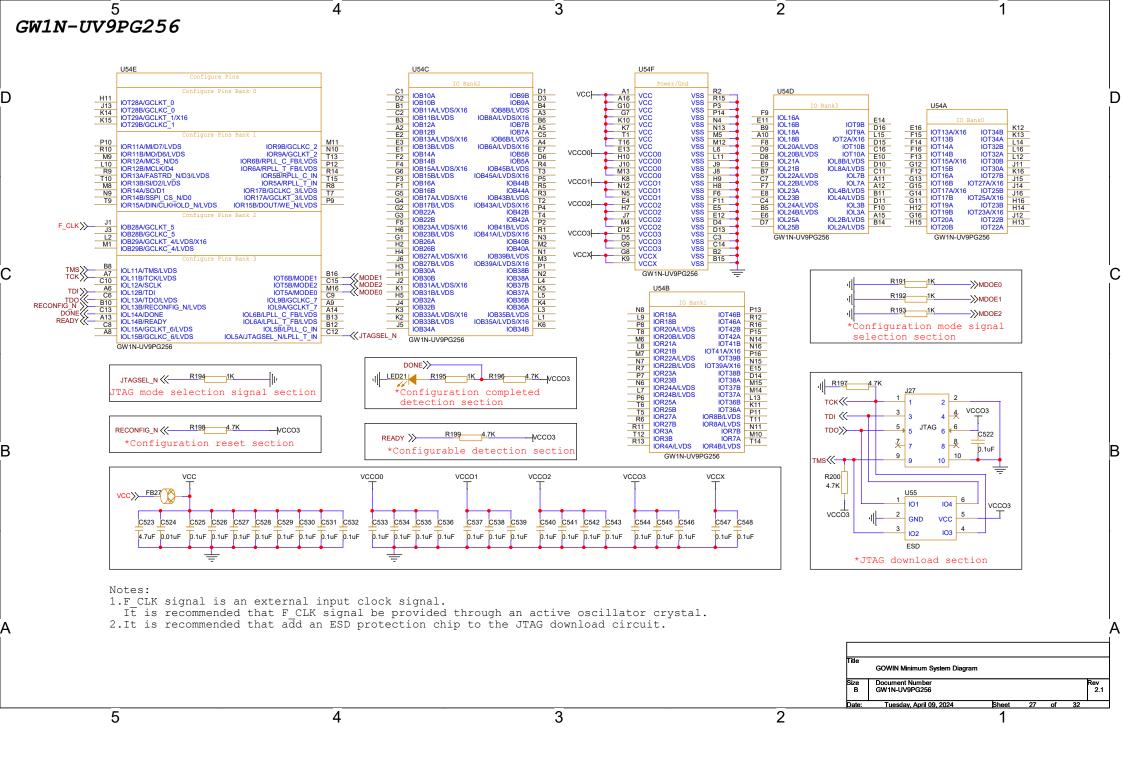
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VCCO3

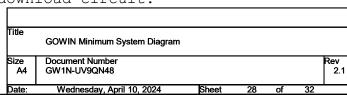
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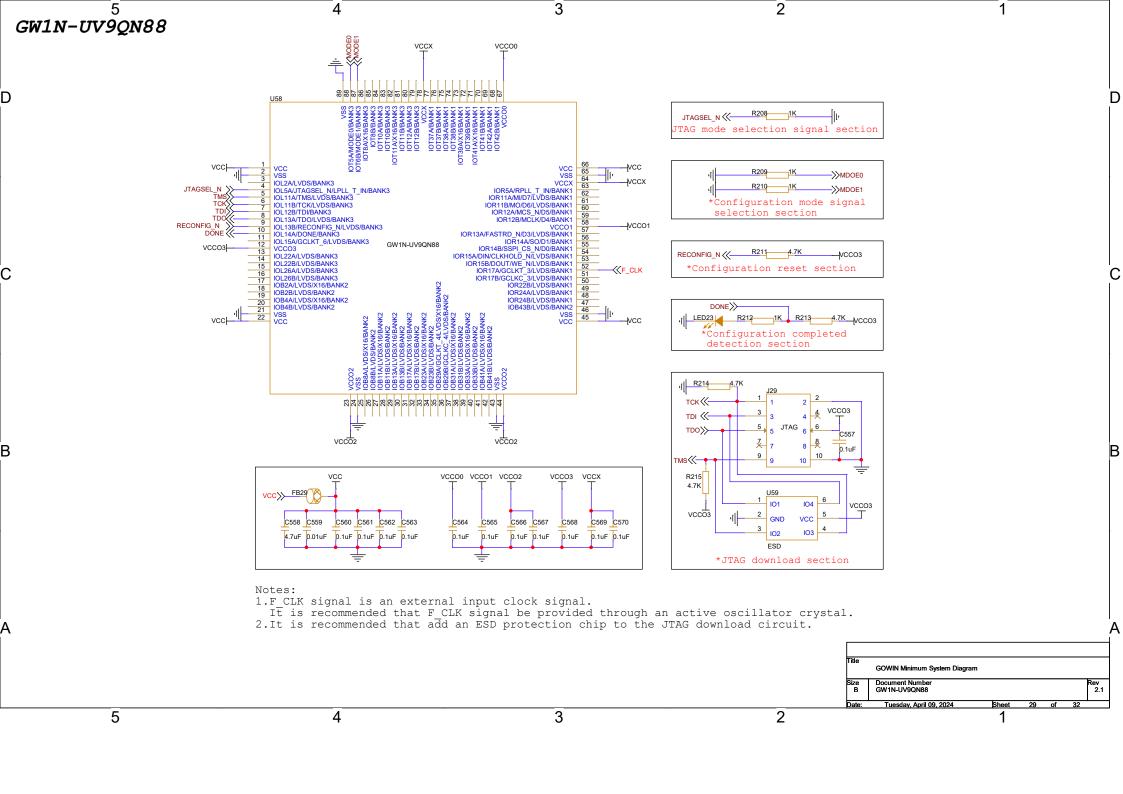
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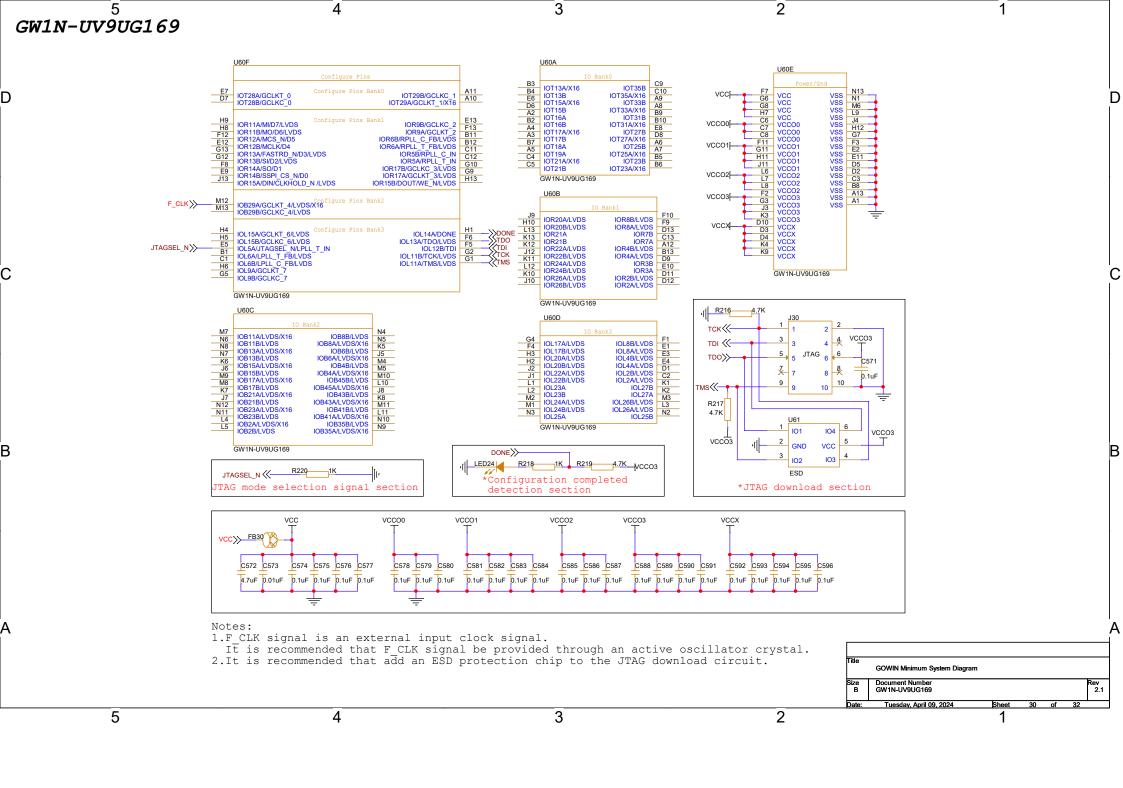
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- 1.F CLK signal is an external input clock signal.
  - It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.







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- 1.F CLK signal is an external input clock signal.
  - IT is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that  $\overline{add}$  an ESD protection chip to the JTAG download circuit.

GOWIN Minimum System Diagram Document Numbe ₹ev 2.1 GW1N-UV9UG332 Tuesday, April 09, 2024

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