

## Notes:

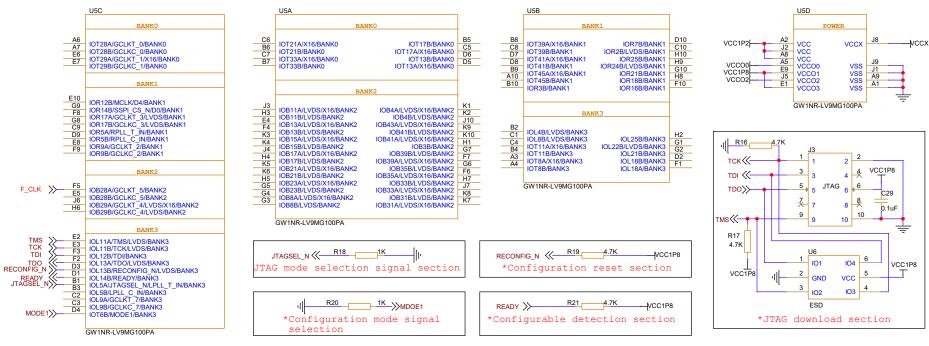
- 1.F CLK signal is an external input clock signal.
  - It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

GOWIN Minimum System Diagram Document Number GW1NR-LV9MG100P Rev 2.2 Wednesday, April 10, 2024

4

3

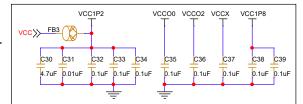
2



# Notes:

5

- 1.F CLK signal is an external input clock signal.
- It is recommended that F\_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



GOWIN Minimum System Diagram Document Number GW1NR-LV9MG100PA Rev 2.2 Wednesday, April 10, 2024

4

3

2

U7E

A7 E6

E7

F8 G8 C9

E8 F9

F5 E5 J6

F3

D1

B1 B3 C2

TCK

TDI

MODE1>>

5

TDO
RECONFIG\_N
READY
JTAGSEL\_N

IOT28A/GCLKT\_0/BANK0 IOT28B/GCLKC\_0/BANK0

IOR12B/MCLK/D4/BANK1

IOR5A/RPLL\_T\_IN/BANK1

IOR5B/RPLL\_C\_IN/BANK1

IOR9A/GCI KT 2/BANK1

IOR9B/GCLKC 2/BANK1

IOB28A/GCLKT\_5/BANK2

IOB28B/GCLKC\_5/BANK2

IOL11A/TMS/LVDS/BANK3

IOL11B/TCK/LVDS/BANK3

IOL12B/TDI/BANK3 IOL13A/TDO/LVDS/BANK3

IOL14B/READY/BANK3

IOL9B/GCLKC\_7/BANK3

IOT6B/MODE1/BANK3

GW1NR-LV9MG100PF

IOB29B/GCLKC 4/LVDS/BANK2

IOR14B/SSPI\_CS\_N/D0/BANK1 IOR17A/GCLKT\_3/LVDS/BANK1 IOR17B/GCLKC\_3/LVDS/BANK1

IOT29A/GCLKT\_1/X16/BANK0 IOT29B/GCLKC\_1/BANK0

1.F CLK signal is an external input clock signal.

4

 $\overline{\text{It}}$  is recommended that F CLK signal be provided through an active oscillator crystal.

3

2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title GOWIN Minimum System Diagram Document Number GW1NR-LV9MG100PF Rev 2.2 Wednesday, April 10, 2024

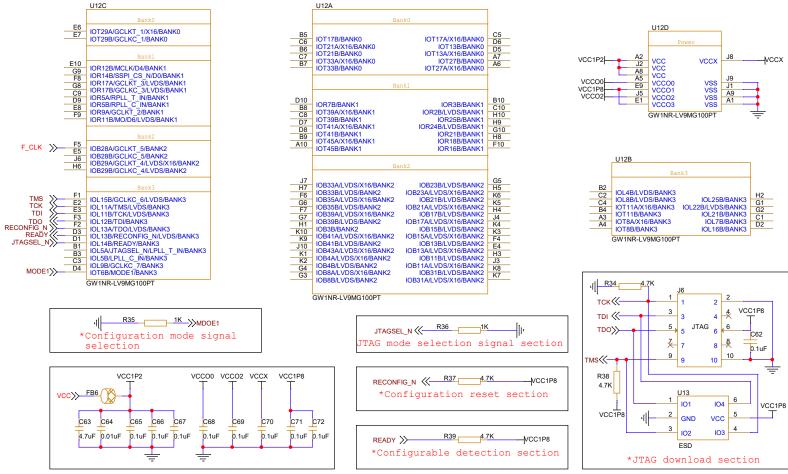
4

2

**GOWIN Minimum System Diagram** Document Number GW1NR-LV9MG100PS Rev 2.2 Wednesday, April 10, 2024

3 4

5

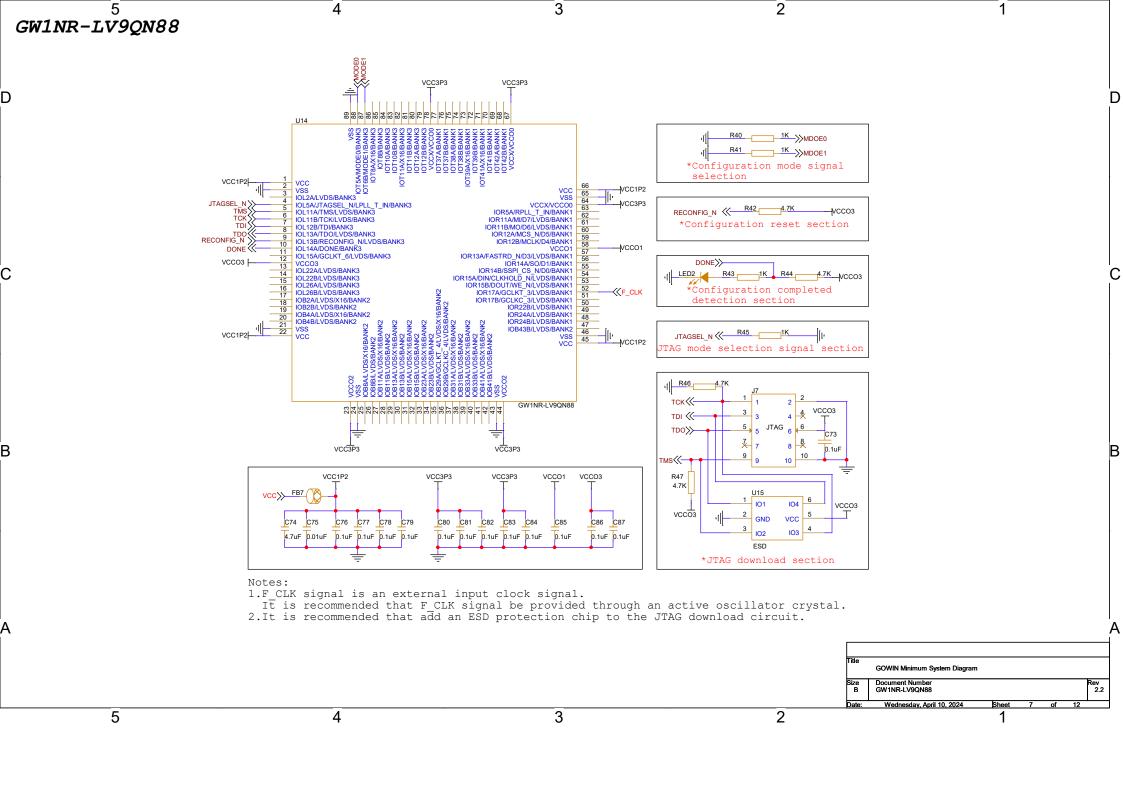


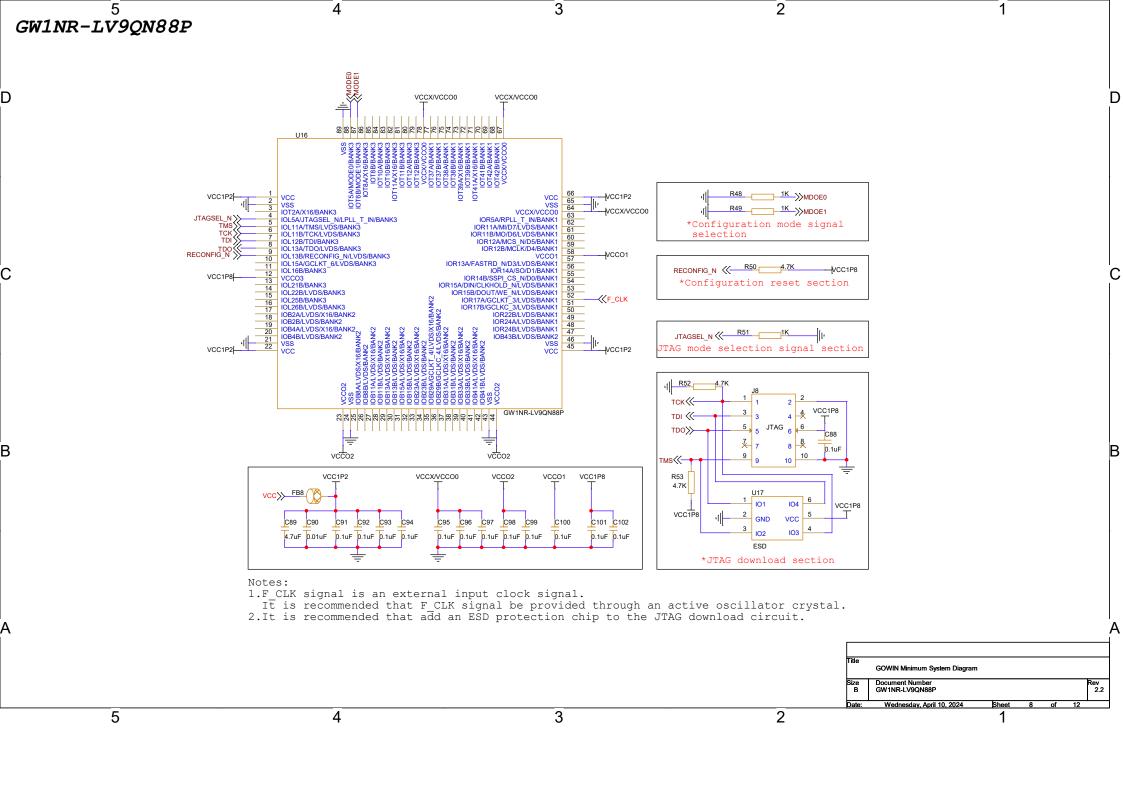
- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

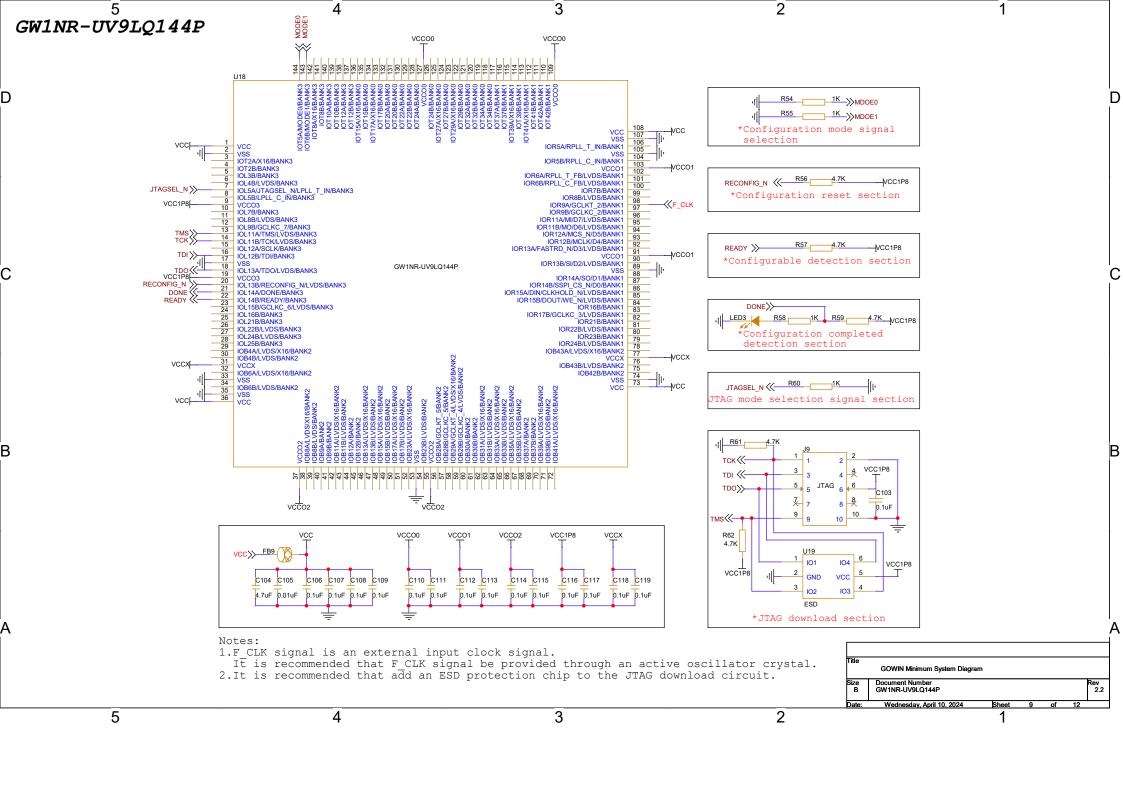
**GOWIN Minimum System Diagram** Document Number GW1NR-LV9MG100PT Rev 2.2 Wednesday, April 10, 2024

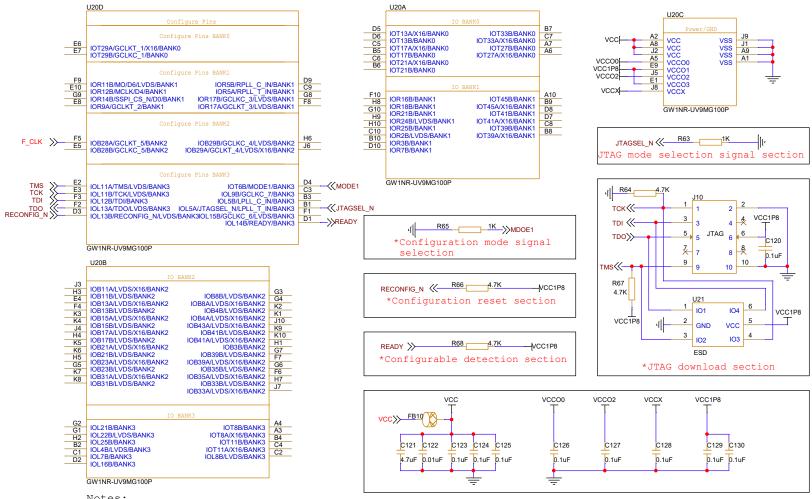
3 4

2









## Notes:

5

- 1.F CLK signal is an external input clock signal.
  - It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

GOWIN Minimum System Diagram Document Number GW1NR-UV9MG100P Rev 2.2 Wednesday, April 10, 2024

4

3

