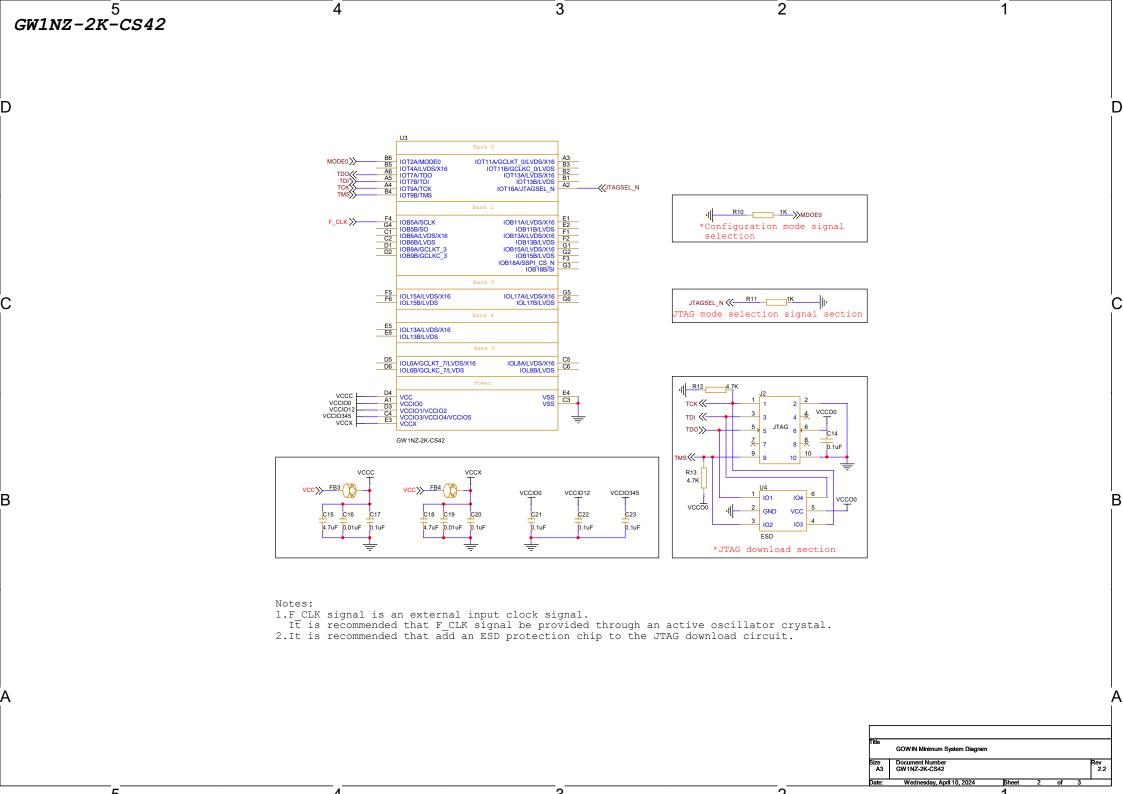
5 3 4 GW1NZ-2K-CS100H U1A U1C MODE0>> U1B □_1K_>>>MDOE0 IOT2A/MODE0 IOT3A/MODE2 B10 Bank1 J10 H8 K9 IOB2A/LVDS/X16 A9 B9 A8 IOT6A/LVDS/X16 IOT6B/LVDS IOB2B/LVDS IOB4B/LVDS □ 1K >>MDOE2 IOR1A/LVDS A2 B1 B2 C3 D4 D3 E3 G3 F3 H1 H2 H3 IOT7A/TDO IOT7B/TDI IOR1B/LVDS IOR3A/D2/LVDS IOB5A/SCLK IOB5B/SO B8 C8 D8 A7 J9 K8 *Configuration mode signal IOR3B/D3/LVDS IOR5A/MI/D7/LVDS IOR5B/MO/D6/LVDS IOB6A/LVDS/X16 IOB6B/LVDS IOB7A/GCLKT_4 IOT8A/LVDS/X16 IOT8B/LVDS selection IOT9A/TCK B7 D7 B6 C7 A6 A4 A5 B5 B4 C6 D5 A3 B3 C5 IOT9A/TCK IOT9B/TMS IOT11A/GCLKT_0/LVDS/X16 IOT11B/GCLKC_0/LVDS IOT12A IOB/A/GCLKT_4 IOB7B/GCLKC_4 IOB8A/LVDS/X16 IOB8B/LVDS IOB9A/GCLKT_3 IOR6A/MCS N/D5 F_CLK >> IOR6B/MCLK/D4 H6 K6 J6 K5 J5 H5 G5 K4 IOR11A/GCLKT_2/LVDS IOR11B/GCLKC_2/LVDS RECONFIG_N(R3 | IOT12A | IOT13A/LVDS/X16 | IOT13B/LVDS | IOT14A/GCLKT_1/SCL | IOT14B/GCLKC_1/SDA IOR13A/LVDS IOR13B/LVDS IOR14A IOR15A/LVDS IOB9B/GCLKC_3 IOB11A/LVDS/X16 IOB11B/LVDS IOB13A/LVDS/X16 *Configuration reset section J1 J2 K1 | IOB13A/LVDS/X16 | IOB13B/LVDS | IOB15A/LVDS/X16 | IOB15B/LVDS | IOB17A/LVDS/X16 | IOB17B/LVDS | IOB18A/SSPI_CS_N | IOB18B/SI IOT15A/LVDS/X16 IOT16A/JTAGSEL N IOR15B/LVDS IOR17A/LVDS JTAGSEL_N RECONFIG_N K2 J4 H4 G4 K3 R4 4.7K IOT16A/JTAGSEL N IOT16B/RECONFIG_N IOT18A/READY IOT18B/DONE IOT19A IOT19B IOR17B/LVDS READY *Configurable detection section GW1NZ-2K-CS100H J3 DONE GW1NZ-2K-CS100H GW1NZ-2K-CS100H ·[| LED1 R5 1K R6 U1D Configuration completed detection section E9 H10 H9 G8 IOL15B/LVDS IOL16A/GCLKT_5 IOL16B/GCLKC_5 JTAGSEL_N ≪ R7 1K U1E TTAG mode selection signal section IOL12A/GCLKT_6 IOL12B/GCLKC_6 IOL13A/LVDS/X16 IOL13B/LVDS IOL14A IOL14B VCC/VCCPLL VCCD/VCCIOD VCCD G10 F8 E8 R8 D6 E4 G6 G7 F7 E7 VCCIO0 VCCIO1 VCCO2 VCCIO2 VCCIO3 VCCO Bank5 VCCO4 VCCIO4 VCCIO5 TDI ≪ VCCO TDO>>> IOL4A/LPLL_T_FB/LVDS/X16 IOL4B/LPLL_C_FB/LVDS IOL6A/GCLKT_7/LVDS/X16 C9 D10 D9 E10 VCCX VCCX 0.1uF IOL6B/GCLKC_7/LVDS IOL8B/LVDS E6 10 VSS гмs<< F6 VSS ÷ R9 E2 CKN
G2 RX0N
F2 RX0P
F1 RX1P
D2 RX1P
C2 RX2N
C1 RX3P GW1NZ-2K-CS100H CKN CKP RX0N RX0P RX1N RX1P RX2N RX2P 4.7K U2 101 104 VCC00 vccoo GND VCC 103 *JTAG download section GW1NZ-2K-CS100H VCC_0P9>> FB1 VCC_3P3 VCC00 VCCO1 VCCO2 VCC03 VCCO4 VCC05 C2 C3 C5 C6 C10 C11 C12 C13 4.7uF 0.01uF 4.7uF 0.01uF 0.1uF 0.1uF .1uF 0.1uF ÷ ÷ Notes: 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal. 2.It is recommended that \overline{add} an ESD protection chip to the JTAG download circuit.

GOWIN Minimum System Diagram

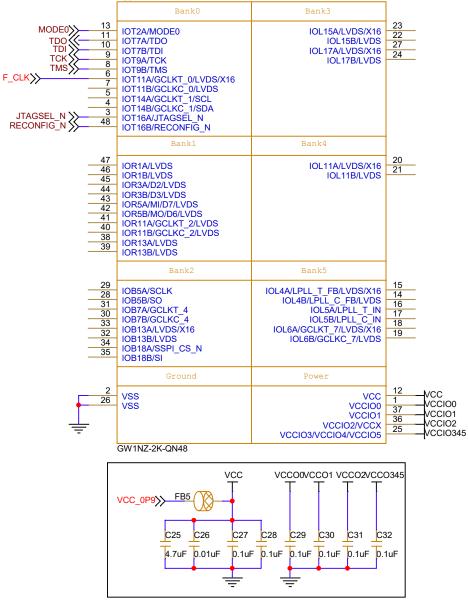
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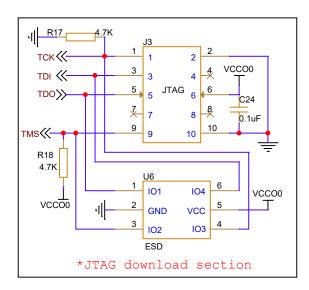
 $GW1NZ-\frac{5}{2}K-QN48$



*Configuration mode signal selection

RECONFIG_N

RECO



Notes:

1.F CLK signal is an external input clock signal.

 $\overline{\text{It}}$ is recommended that F CLK signal be provided through an active oscillator crystal.

A2.It is recommended that $a\overline{d}d$ an ESD protection chip to the JTAG download circuit.

| Title | COMINIA Minimum Control Discours | | | | | |
|-------|----------------------------------|-------|---|----|---|-----|
| | GOWIN Minimum System Diagram | | | | | |
| Size | Document Number | | | | | Rev |
| A4 | GW1NZ-2K-QN48 | | | | | 2.2 |
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| Date: | Wednesday, April 10, 2024 | Sheet | 3 | of | 3 | |