GW1NS & GW1NSR & GW1NSE & GW1NSER series of FPGA Products Schematic Manual

Introduction

You should follow some rules for circuit board design when using GW1NS & GW1NSR & GW1NSE & GW1NSER series of FPGA products. This manual describes the characteristics of GW1NS & GW1NSR & GW1NSE & GW1NSER series of FPGA products. The main contents of this manual are as follows:

- Power Supply
- JTAG
- MSPI
- Clock Pin
- Differential Pin
- RECONFIG_N, READY, DONE
- MODE
- JTAGSEL_N
- FASTRD_N
- Dual-purpose Pin
- FPGA External Crystal Oscillator Circuit Reference
- Bank Voltage
- Configuration Modes Supported by Each Device
- MIPI
- Pinout

Power Supply

Overview

GW1NS & GW1NSR & GW1NSE & GW1NSER series of FPGA products support LV version. The voltage includes core voltage (V_{CC}), auxiliary voltage (V_{CCX}) and bank voltage (V_{CCIO}).

There is no linear voltage regulator in devices of LV version, and V_{CCX} can be set to 1.8V, 2.5V or 3.3V. The I/O Bank voltage V_{CCIO} can be set to 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V as required.

V_{CC} is 1.2V. V_{CCX} is the auxiliary power, which is used to supply some circuits in the chip, supporting 1.8V, 2.5V and 3.3V. After the chip powers on, V_{CCX} can be turned off. V_{CCIO} Bank can be set to 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V as required.

Power DC Voltage Requirement

GW1NS & GW1NSR & GW1NSE & GW1NSER series devices have several different power rails, V_{CC}, V_{CCX} and some V_{CCIO}s. In order to release the Power On Reset, V_{CC}, V_{CCX} and some special V_{CCIO}s have to be powered. Please refer to the "Power Rails Monitored by POR Circuits of Different Devices" table in Chapter 6.1 Power-up Sequence of *UG290, Gowin FPGA Products Programming and Configuration Guide* for required V_{CCIO} rails of different devices. V_{CCX} should be always no less than V_{CCIO}, or there will be some unexpected leakage on V_{CCIO}.

For the recommended operating range for each power voltage, refer to the "Power" sheet in the following pinouts.

- UG824-1.3.2E_GW1NS-4&4C Pinout
- UG864-1.1.1E_GW1NSR-4 Pinout
- UG865-1.1.1E_GW1NSR-4C Pinout
- UG883-1.1E_GW1NSER-4C Pinout

Power Sequence

Theoretically the devices can be powered up and powered down by any sequence. But during the power ramping procedure, if V_{CCX} is lower than V_{CCIO}, V_{CCIO} could have high current (hundreds of mA). This high current could maintain until V_{CCX} is no less than V_{CCIO}. To prevent this unexpected current, we recommend power on V_{CCX} before/with V_{CCIO}s.

No special power sequence requirement for V_{CC}.

Recommended Reference Range of Power-up Time

Recommended reference range of power-on time for V_{CC} is 0.2ms~2ms. And the power supply ramping rate of V_{CCIO} and V_{CCX} is as shown in “Power Supply Ramp Rate” table in Chapter 3.1.3 “Power Supply Ramp Rate” of *DS821, GW1NS series of FPGA Products Datasheet*. You can ignore the reference range of power-on time and recommendations in

the “Power Supply Ramp Rate” table mentioned above (except V_{CCIO}) if you can meet the following calculation method in Power Supply Ramping Rate.

Note!

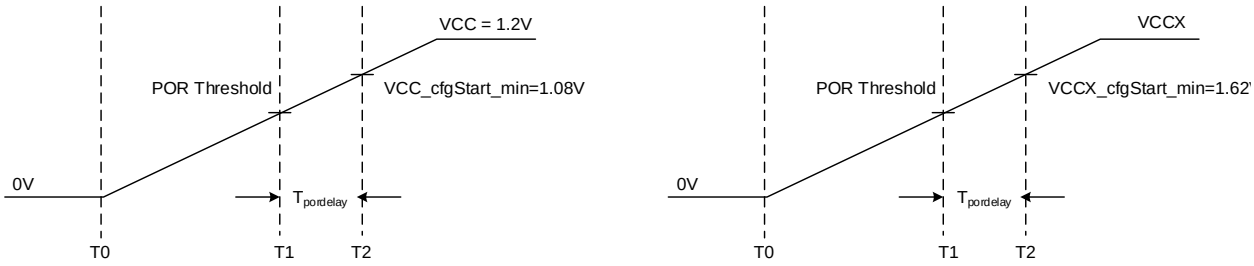
- If the power-on time is more than 2ms, you need to ensure that the power-on in sequence is V_{CC}, and then V_{CCX}/V_{CCIO}; Or you need to calculate the safe ramping time by the following formula in Power Supply Ramping Rate.
- If the power-on time is less than 0.2ms, it is recommended to increase the capacitance to prolong the power-on time.

Power Supply Ramping Rate

For GW1NS & GW1NSR & GW1NSE & GW1NSER devices, after the POR is released, the config logic will access the internal flash to read out the manufacture data for initializing. To make sure the internal flash is ready before this read operation, we have power ramping rate requirement.

The internal flash is powered by V_{CC} and V_{CCX}. As in the flash spec, $V_{CC} \geqslant 1.08V$ & $V_{CCX} \geqslant 1.62V$ is required for the reading operation. The system power rails have to meet this condition when the device starts to initializing.

Figure 1 Power Ramping Waveform



POR threshold voltage of V_{CC} and V_{CCX} is as shown in “POR Voltage” table in Chapter 3.1.5 “POR Feature” of *DS821, GW1NS series of FPGA Products Datasheet*. POR delay time: $T_{pordelay\text{-}min}$=500us, $T_{pordelay\text{-}typ}$=750us, $T_{pordelay\text{-}max}$=1ms.

To calculate the ramping time requirement, first we need to know which power rail will achieve the POR trip point at last. This is T1, when system POR will be released. Then we can get T2 which equals to T1 + $T_{pordelay}$, when the device starts to access the internal flash. We need to guarantee $V_{CC} \geqslant 1.08V$ & $V_{CCX} \geqslant 1.62V$ at T2.

Take GW1N-4 as an example, assuming V_{CC} is powered on at last and V_{CCX} and V_{CCIO}s are stable before V_{CC}, the POR release time will depend on V_{CC} rail. If the ramping time is 3.3ms, V_{CC} POR threshold is around 0.9V of GW1N-4 per “POR Voltage” table in Chapter 3.1.5 “POR Feature” of *DS100, GW1N series of FPGA Products Data Sheet*.

T1 = 3.3ms * 0.9V/1.2V = 2.475ms

T2 = T1 + $T_{pordelay\text{-}min}$ = 2.975ms,

Thus, we can get $V_{CC\_cfgstart}$ = 1.2V * 2.975ms/3.3ms = 1.08V bigger than minimum=1.08V requirement. Then it is a safe ramping rate.

Note!

The above calculation is based on the fact that the power supply is linearly lifted.

If V_{CCX} is the last rail powered on. We have to make sure it meets the $V_{CCX\_cfgstart\_min}$ =1.62V requirement.

For UV devices, please use 0.3V voltage drop of the internal LDO to calculate the V_{CC} ramping time requirement, i.e. at T2, the minimum voltage should be 1.08 + 0.3 = 1.38V.

Total Power

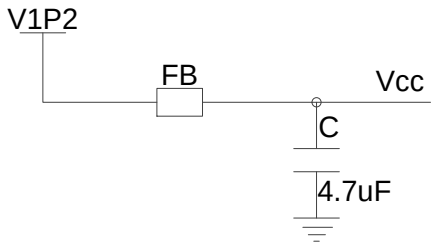
For specific density, packages, and resource utilization, GPA tools can be used to evaluate and analyze the power consumption.

Power Filter

Each FPGA power input pin is connected to the ground with a 0.1uF ceramic capacitor.

Noise processing should be noted at the input end of the V_{CC}, and the specific is as follows:

Figure 1 Noise Processing



FB is a ferrite bead, and the reference model is MH2029-221Y. The ceramic capacitance is 4.7uF, and It offers an accuracy of more than ±20%.

JTAG

Overview

JTAG interface is used for downloading the bitstream to SRAM, on-chip flash or off-chip flash of FPGA.

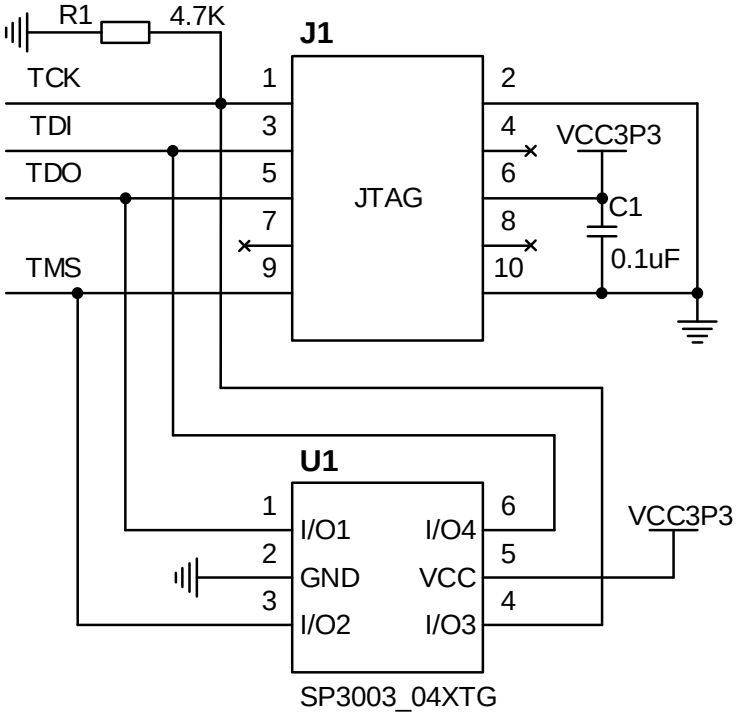
Signal Description

Table 1 Signal Description

Name	I/O	Description
TCK	I	JTAG serial clock input
TMS	I, internal weak pull-up	JTAG serial mode input
TDI	I, internal weak pull-up	JTAG serial data input
TDO	O	JTAG serial data output

JTAG Circuit Reference

Figure 2 JTAG Circuit Reference



Note!

- The power of JTAG 6th pin can be set to VCC1P2, VCC1P5, VCC1P8, VCC2P5 as required.
- It is recommended to add ESD protection chip on JTAG signal for better protection of JTAG pins from electrostatic damage, optional model: SP3003_04XTG.

MSPI

Overview

FPGA as a master device, MSPI reads the data automatically from the off-chip flash then transmits it to the FPGA SRAM.

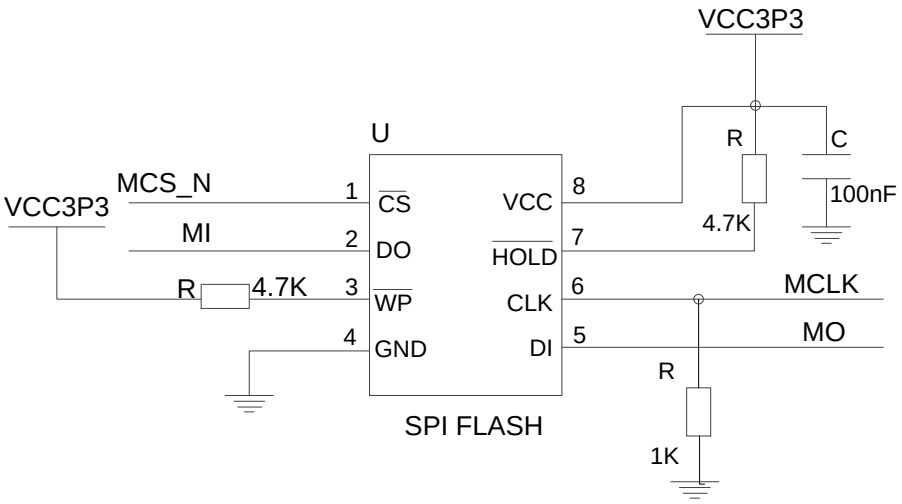
Signal Description

Table 2 Signal Description

Name	I/O	Description
MCLK	O	Clock output in MSPI mode
MCS_N	O	Enable signal in MSPI mode, low-active
MI	I	Data input in MSPI mode
MO	O	Data output in MSPI mode

MSPI Circuit Reference

Figure 3 MSPI Circuit Reference



Note!

MCLK signal requires 1K pull-down resistor.

Clock Pin

Overview

The clock pins include GCLK global clock pins and PLL clock pins.

- GCLK: GCLK in FPGA products distributes in L and R quadrants. Each quadrant provides eight GCLK nets. The clock source of each GCLK can be dedicated pin or CRU, and the dedicated pin can provide better performance.
- PLL: Frequency (multiplication and division), phase, and duty cycle can be adjusted by configuring the parameters.

Signal Description

Table 3 Signal Description

Name	I/O	Description
GCLKT_[x]	I/O	Pins in global clock input, T(True), [x]: global clock No.
GCLKC_[x]	I/O	Pins for Global clock input, C(Comp), [x]: global clock No.
LPLL_T_FB/RPLL_T_FB	I	Left/Right PLL feedback input pins, T(True)
LPLL_C_FB/RPLL_C_FB	I	Left/Right PLL feedback input pins, C(Comp)
LPLL_T_IN/RPLL_T_IN	I	Left/Right PLL clock input pin, T(True)
LPLL_C_IN/RPLL_C_IN	I	Left/Right PLL clock input pin, C(Comp)

Clock Input Selection

If the external clock as PLL clock, it is recommended to input from PLL_T.

GCLK is the global clock and is connected to all resources in the device. It is recommended to input from GCLK_T.

Differential Pin

Overview

Differential transmission is a kind of signal transmission, which is different from the traditional signal line and ground line. Differential transmission signals are transmitted on these two lines. These two signals are with same amplitude, phase and opposite polarity.

Differential Type

Table 4 Differential Type

I/O Output Standard	Single/Differ	Bank VCCIO (V)	Output Driver Strength (mA)
MIPI	Differential（MIPI）	1.2	N/A
LVDS25	Differential（True LVDS）	2.5/3.3	N/A
RSDS	Differential（True LVDS）	2.5/3.3	N/A
MINILVDS	Differential（True LVDS）	2.5/3.3	N/A
PPLVDS	Differential（True LVDS）	2.5/3.3	N/A
SSTL15D	Differential	1.5	8
SSTL25D_I	Differential	2.5	8
SSTL25D_II	Differential	2.5	8
SSTL33D_I	Differential	3.3	8
SSTL33D_II	Differential	3.3	8
SSTL18D_I	Differential	1.8	8
SSTL18D_II	Differential	1.8	8
HSTL18D_I	Differential	1.8	8
HSTL18D_II	Differential	1.8	8
HSTL15D_I	Differential	1.5	8
LVCMOS12D	Differential	1.2	4,8
LVCMOS15D	Differential	1.5	4,8
LVCMOS18D	Differential	1.8	4,8,12
LVCMOS25D	Differential	2.5	4,8,12,16
LVCMOS33D	Differential	3.3	4,8,12,16,24

Note!

See pinout manuals for specific differential pin positions.

RECONFIG_N, READY, DONE

Overview

RECONFIG_N, equivalent to the reset function of FPGA programming configuration, FPGA cannot perform any configuration operation when RECONFIG_N is pulled down.

As a configuration pin, a low level with a pulse width of not less than 25ns is required for GowinCONFIG configuration mode to enable the device to reload the bitstream. You can control the pin by writing logic to trigger the device to reconfigure as required.

You can configure FPGA only when the READY signal is high. The device should be restored by power on or triggering RECONFIG_N when the READY signal is low.

As an output configuration pin, it can indicate whether the FPGA can be configured currently. If the device is ready, READY signal is high. If the device fails to configure, the READY signal changes to low. As an input configuration pin, you can delay the configuration by its own logic or pulling down the READY signal.

DONE signal indicates that the FPGA is configured successfully. The signal is high after successful configuration.

As an output configuration pin, it can indicate whether FPGA configuration is successful. If configured successfully, DONE is high, and the device enters into an operating state. If the device failed to configure, the DONE signal remains low. As the input, you can delay the entry into user mode by manually pulling down the DONE signal via the logic.

When RECONFIG_N or READY signals are low, DONE signal is also low. When configuring SRAM using JTAG circuit, it does not need to take DONE signal into account.

Signal Description

Table 5 Signal Description

Name	I/O	Description
RECONFIG_N	I, internal weak pull-up	Low level pulse: start new GowinCONFIG configuration
READY[1]	I/O	High-level pulse: The device can be programmed and configured
		Low-level pulse: The device cannot be programmed and configured
DONE[1]	I/O	High-level pulse: Successfully programmed and configured
		Low-level pulse: Programming and configuration uncompleted or failed

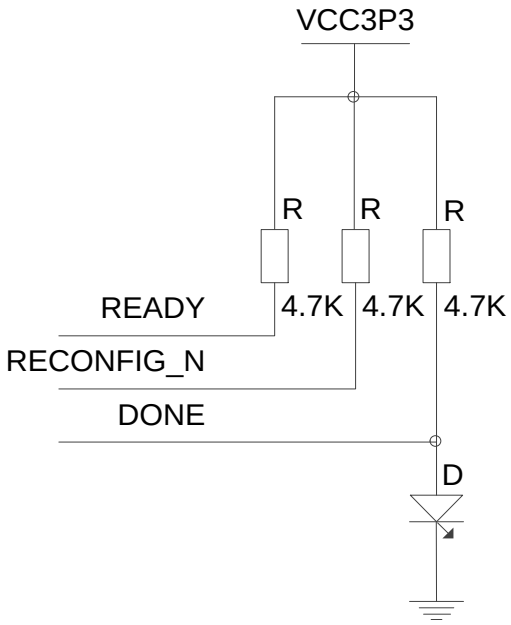
Note!

[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE

outputs 0 during configuration.

READY, RECONFIG_N, DONE Reference Circuit

Figure 4 READY, RECONFIG_N, DONE Reference Circuit



Note!

The pull-up power supply is the bank voltage value VCCIO0 of the corresponding pin.

MODE

Overview

MODE includes MODE0, MODE1, MODE2, and GowinCONFIG. When FPGA powers on or a low pulse triggers RECONFIG_N, the device enters the corresponding GowinCONFIG state according to the MODE value. MODE [2:0] is used to select the GowinCONFIG programming configuration mode. The configuration mode can be fixed by using pull-up or pull-down resistors. It is recommended to use a 4.7K resistor for pull-up or a 1K resistor for pull-down. As the number of pins for each package is different, some MODE pins are not all packaged, and the unpacked MODE pins are grounded inside. Please refer to the corresponding pinout manual for further details.

Signal Description

Table 6 Signal Description

Name	I/O	Description
MODE2	I, internal weak pull-up	GowinCONFIG mode selection pin
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin
MODE0	I, internal weak pull-up	GowinCONFIG mode selection pin

Mode Selection

Table 7 Mode Selection

Configuration Modes		MODE[2:0][1]	Description
JTAG		XXX[2]	The LittleBee® Family of FPGA products are configured via JTAG interface by external Host
GowinCONFIG	AUTO BOOT	000	FPGA reads data from embedded Flash for configuration
	SSPI[3]	001	FPGA products of LittleBee® Family are configured via SPI interface
	MSPI[3]	010	As a Master, FPGA reads data from external Flash (or other devices) via the SPI interface
	DUAL BOOT	110	FPGA reads data from external Flash first and if the external Flash configuration fails, it reads from the Internal Flash
	SERIAL[4]	101	External Host configures FPGA products of LittleBee® Family via DIN interface
	CPU[4]	111	External Host configures FPGA products of LittleBee® Family via DBUS interface

Note!

- [1] The unbound mode pins are grounded or internally connected to the power supply by default.
- [2] The JTAG configuration mode is independent of MODE value.
- [3] The SPI interfaces of the SSPI and MSPI modes are independent of each other.
- [4] The CPU configuration mode and SERIAL configuration mode share SCLK, WE_N and CLKHOLD_N. The data bus pins for the CPU configuration mode share pins with MSPI and SSPI configuration modes.

JTAGSEL_N

Overview

JTAGSEL_N is JTAG mode selection signal. If the JTAG pin is set to GPIO in Gowin software, the JTAG pin changes to GPIO after the device is powered on to configure successfully. If JTAG configuration fails, you can recover by pulling down JTAGSEL_N. If you do not set JTAG multiplexing, the JTAG configuration function is always available.

Signal Description

Table 8 Signal Description

Pin Name	I/O	Description
JTAGSEL_N	I, internal weak pull-up	Change JTAG pin from GPIO to configuration pin, active-low

Note!

The JTAGSEL_N pin and four JTAG pins (TCK, TMS, TDI, and TDO) configured as GPIO are exclusive. JTAG pins can only be used as configuration pin if JTAGSEL_N is set to GPIO. JTAGSEL_N can only be used as a configuration pin if JTAG pins are set to GPIOs.

FASTRD_N

Overview

It is the SPI Flash read speed selection signal in MSPI configuration mode. When FASTRD_N is high, it is normal read mode. When FASTRD_N is low, it is high speed read mode. Different manufacturers have different high-speed read operation instructions, please refer to the corresponding Flash datasheet.

Signal Description

Table 9 Signal Description

Pin Name	I/O	Description
FASTRD_N	I/O	As a configuration pin, internal weak pull-up, READY signal rising edge samples MSPI configuration speed mode; As a GPIO, it can be used as input or output.

Note!

- High level: Normal Flash mode, clock frequency should not be higher than 30MHz.
- Low level: High speed Flash mode, clock frequency should be > 30MHz and < 80MHz.

Dual-purpose Pin

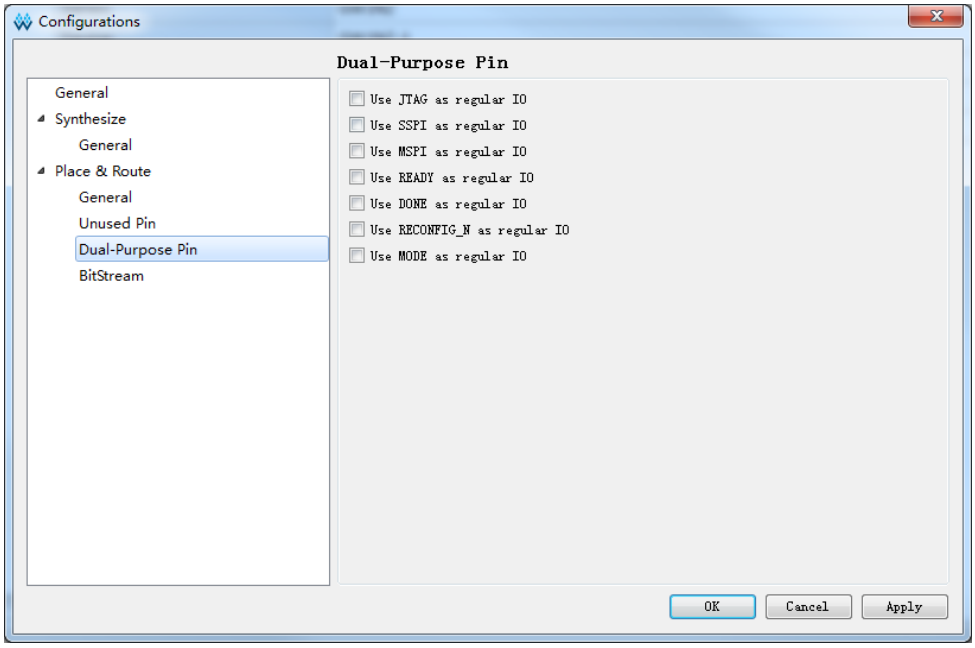
Overview

Dual-purpose pin configuration refers to performing configuration function at the moment of power-on. After downloading bitstream files, it is used as general I/O.

The steps are as follows:

1. Open the project in Gowin Software.
2. Select "Project > Configuration > Dual-Purpose Pin" from the menu, as shown in Figure 5.
3. Check the corresponding options.

Figure 5 Configure Dual-purpose Pin



Dual-purpose Pin

- SSPI: As a GPIO, SSPI can be used as input or output.
- MSPI: As a GPIO, MSPI can be used as input or output.
- RECONFIG_N GPIO can only be used as an output. Set the initial value of RECONFIG_N as high when multiplexing it.
- READY: As a GPIO, READY can be used as input or output. As an input GPIO, the initial value of READY should be 1. Otherwise, the FPGA will fail to configure.
- As a GPIO, DONE can be used as an input or output. If DONE is used as an input GPIO, the initial value of DONE should be 1. Otherwise, the FPGA will fail to enter the user mode after configuring.
- As a GPIO, JTAG can be used as an input or output.

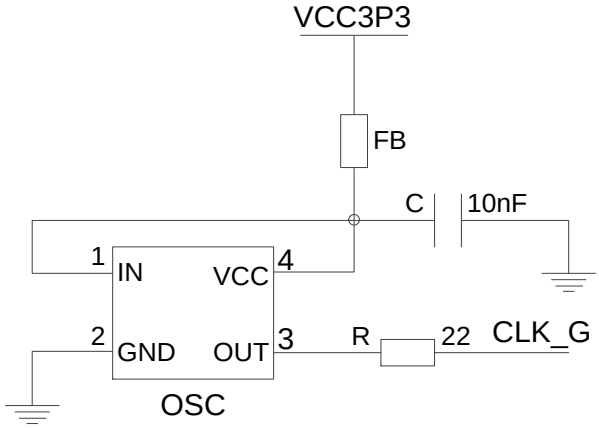
- As a GPIO, JTAGSEL_N can be used as an input or output.
- As a GPIO, JTAG can be used as an input or output. You multiplex MODE pin, the correct value is needed to provided during configuration (power-on or low-level pulse triggers RECONFIG_N). Up to three pins can be multiplexed in MODE. Unpackaged pins are grounded internally. Please refer to pinout manuasl for details. For the MODE value corresponding to different configuration modes, please refer to the corresponding device manual.

Note!

If the number of I/O ports is sufficient, use non-multiplexed pins first.

FPGA External Crystal Oscillator Circuit Reference

Figure 6 FPGA External Crystal Oscillator Circuit



FB is a ferrite bead, and MH2029-221Y is the reference model. The resistance accuracy is not less than ±5%, and capacitance accuracy is not less than ±20%.

Bank Voltage

For the Bank power supply requirements of the devices, please refer to the Power section of the following documents.

- UG824, GW1NS-4 & 4C Pinout
- UG864, GW1NSR-4 Pinout
- UG865, GW1NSR-4C Pinout
- UG883, GW1NSER-4C Pinout

Configuration Modes Supported by Each Device

GW1NS-4/4C

Table 10 GW1NS-4/4C Configuration Modes

Package	JTAG	AUTO BOOT	MSPI
CS49	Yes	Yes	No
QN48	Yes	Yes	No
MG64	Yes	Yes	No
QN32	Yes	Yes	Yes

Note!

QN32 package is for GW1NS-4 devices.

GW1NSER-4C

Table 11 GW1NSER-4C Configuration Modes

Package	JTAG	AUTO BOOT
QN48G	Yes	Yes
QN48P	Yes	Yes

GW1NSR-4

Table 12 GW1NSR-4 Configuration Mode

Package	JTAG	AUTO BOOT
MG64P	Yes	Yes

GW1NSR-4C

Table 13 GW1NSR-4C Configuration Modes

Package	JTAG	AUTO BOOT	MSPI	DUAL BOOT
QN48P	Yes	Yes	Yes	Yes
QN48G	Yes	Yes	No	Yes
MG64P	Yes	Yes	No	No

MIPI

GW1NS series of FPGA products support embedded MIPI interface modules. BANK0/BANK1 of GW1NS-4 is MIPI input and BANK2 supports MIPI output.

Note!

When BANK0/BANK1 of GW1NS-4C/4 is used as MIPI input, $V_{CCIO}0$/$V_{CCIO}1$ need to be set to 1.2V, and when BANK2 is used as MIPI output, $V_{CCIO}2$ needs to be set to 1.2V; When V_{CCX} is set to 1.8 V, the speed of MIPI can only reach 60% of the speed of MIPI when V_{CCX} is set to 2.5V/3.3V.

Pinout

Before the design of the circuit, you should take the FPGA pinout into consideration, and a reasonable choice should be made for IO LOGIC, global clock resource, PLL and differential signals, etc.

Note!

During configuration, all GPIOs of the device are high-impedance with internal weak pull-ups. After the configuration is complete, the I/O state is controlled by user programs and constraints. The state of CONFIG-related I/Os varies depending on the configuration mode.

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

Revision History

Date	Version	Description
07/28/2020	1.0E	Initial version published.
12/06/2021	1.1E	● The value described in Table 1 Recommended Range fixed. ● The configuration modes supported by each device updated.
07/15/2022	1.1.1E	The note in “JTAG Circuit Reference” updated.
10/20/2022	1.2E	GW1NS-2, GW1NS-2C, GW1NSR-2, GW1NSR-2C, and GW1NSE-2C series removed.
03/10/2023	1.3E	● “Power Supply” updated. ● “Figure 2 JTAG Circuit Reference” in “JTAG” updated. ● The data of GW1N-4 example in “Power Supply Ramping Rate” updated.
03/17/2023	1.3.1E	● The note in “Pinout” updated.
06/29/2023	1.3.2E	● “Table 10 GW1NS-4/4C Configuration Modes” in “Configuration Modes Supported by Each Device” updated. ● The overview in “MODE” updated.
08/10/2023	1.3.3E	● The note in “Pinout” optimized. ● The mode supported by QN48 package of GW1NS-4/4C devices in “Configuration Modes Supported by Each Device” updated.
02/22/2024	1.3.4E	The note of “Table 5 Signal Description” in “RECONFIG_N, READY, DONE” added.

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