

CYPD4126-24LQXI Firmware Release Notes

Version 3.2.1 Build 1658, June 27, 2018

Thank you for your interest in the CYPD4126-24LQXI CY-PD® CCG4 product family. This document contains release notes for the CYPD4126-24LQXI firmware. It also describes key updates and known issues.

Introduction

EZ-PD™ CCG4 is a dual USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG4 provides a complete dual USB Type-C and USB-Power Delivery port control solution for notebooks, power adapters and docking stations. It can also be used in dual role and downstream facing port applications. EZ-PD CCG4 uses Cypress's proprietary M0S8 technology with a 32-bit, 48-MHz ARM® Cortex®-M0 processor with 128-KB flash and integrates two complete Type-C Transceivers including the Type-C termination resistors RP and RD.

The CYPD4126-24LQXI device is a single port version of CCG4 which supports all the other device feature enhancements over previous versions of Cypress Type-C controllers. This device support USB-PD protocol revision 3.0 specification.

Key application level requirements

- Integrated USB-PD controller per PD 3.0 spec.
- Integrated Rp, Rd resistor on CC1/2 pins.
- Support dead battery termination.
- Integrated system level ESD protection for exposed pins.
- Integrated boot loader to support firmware update over I2C.
- Integrated VCONN FETS to provide power to EMCA cables.
- Support fast role swap.
- Support USB-PD extended messages.

Firmware Features

This version of the CYPD4126-24LQXI firmware supports the following key application level features:

- USB-PD Protocol as per PD 3.0 spec.
- USB-PD power contract negotiation as provider or consumer.
- Automatic consumer configuration when dead battery condition is detected.
- Support for VBus Over-Voltage protection based on internal comparator.
- Support for VBus Over-Current protection based on external current limited load switch.
- Support for DisplayPort alternate mode with PS8740B MUX for data path switching between USB-SS and DisplayPort.
- I2C based interface for status reporting and configuration updates from an Embedded Controller in the system.
- Selectable I2C slave address based on I2C_CFG pin status.
- Capability of in-system firmware upgrade through the I2C interface from Embedded Controller.
- Capability to update USB-PD profiles and change operating conditions through the I2C interface from Embedded Controller.
- Fast Role swap receive support.
- USBPD Extended messages support.

Default Device Configuration

Parameter	Supported Settings
Source PDOs	5V @ 3.0A, 9V @ 3.0A, 15V @ 3.0A, 20V @ 3.0A
Sink PDOs	5V @ 0.9A / 0.9A, 7V-21V @ 0.9A / 0.9A

Default SVDM Response

When the CYPD4126-24LQXI device functions as a UFP device, it will provide the following responses for the structured vendor defined message (SVDM) requests.

No SVIDs or Modes are supported as the device does not support any data transfers while functioning as a UFP.

DISCOVER_ID Response

0xFF008041, 0x920004B4, 0x00000000, 0xF6D40000

VDM header		
B31..16	Standard or Vendor ID (SVID)	0xFF00
B15	VDM Type	1b
B14..13	Structured VDM Version	00b
B12..11	Reserved	00b
B10..8	Object Position	000b
B7..6	Command Type	01b
B5	Reserved	0b
B4..0	Command	00001b
ID header		
B31	Data Capable as USB Host	1b
B30	Data Capable as a USB Device	0b
B29..27	Product Type is Peripheral	010b
B26	Modal Operation Supported	0b
B25..23	Product Type (DFP) is Alternate Mode Controller	100b
B22..16	Reserved. Shall be set to zero.	0x0
B15..0	16-bit USB Vendor ID	0x04B4
Cert Stat VDO		
B31..20	Reserved, shall be set to zero.	0
B19..0	20-bit unsigned integer	0
Product VDO		
B31..16	USB Product ID	0xF6D4
B15..0	bcdDevice	0x0000

DISCOVER_SVID Response

None.

DISCOVER_MODES Response

None.

Limitations and Known Problems of Firmware version 3.2.1

1. I2C slave address used for Host Processor Interface (HPI) is based on the I2C_CFG GPIO (pin 2). This pin should be held steady (high, low or floating with no subsequent changes) for about 200 ms when the CCG3 is powering up or being reset.
2. CCG4 requires a worst-case delay of 1 ms from the point where the EC writes to the INTR_REG to clear an interrupt, to the point where the HPI interrupt gets cleared. EC is expected to use the HPI in edge triggered mode. CCG4 will ensure that a new edge will be provided if the event queue already has more data at the time when EC clears the first interrupt.
3. Vendor Defined Message (VDM) and extended message requests with wrong arguments to the HPI results in `Transaction Failed` error code instead of `Invalid Arguments`.
4. The device does not enter low power mode when Fast Role Swap (FRS) receive is enabled and acting as a sink.
5. The Provider FET turn-on during Fast Role Swap (FRS) from Sink to Source is done through firmware intervention as this CCG4 package does not support hardware based control of the Provider FET. This could lead to failures in completing the FRS in the unlikely case of the CM0 controller on the device being loaded with other tasks at the time of receiving the FRS request.
6. The VBus OVP detection threshold used in CCG4 firmware has a minimum value of 6.5 V independent of the threshold selection made in the firmware configuration table. This is done to avoid false OVP detection due to inrush current at the time of Type-C connection.

Technical Support

For assistance, go to <http://www.cypress.com/go/support> for support.

Additional Information

For more information about the CCG4 Type-C controller, visit the web page:

<http://www.cypress.com/products/ez-pd-ccg4-two-port-usb-type-c-controller-power-delivery>

For more information about the CCG4 Evaluation Kit from Cypress, visit the web page:

<http://www.cypress.com/documentation/development-kitsboards/cy4541-ez-pd-ccg4-evaluation-kit>

For more information about the Cypress Type-C controller family, visit the web page:

<http://www.cypress.com/products/usb-type-c-and-power-delivery>

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