CYPD4126-40LQXI Firmware Release Notes

Version 3.2.1 Build 1658, June 27, 2018

Thank you for your interest in the CYPD4126-40LQXI CY-PD® CCG4 product family. This document contains release notes for the CYPD4126-40LQXI firmware. It also describes key updates and known issues.

Introduction

EZ-PD™ CCG4 is a dual USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG4 provides a complete dual USB Type-C and USB-Power Delivery port control solution for notebooks, power adapters and docking stations. It can also be used in dual role and downstream facing port applications. EZ-PD CCG4 uses Cypress's proprietary M0S8 technology with a 32-bit, 48-MHz ARM® Cortex®-M0 processor with 128-KB flash and integrates two complete Type-C Transceivers including the Type-C termination resistors RP and RD.

The CYPD4126-40LQXI device is a single port version of CCG4 which supports all of the other device feature enhancements over previous versions of Cypress Type-C controllers. This device support USB-PD protocol revision 3.0 specification.

Key application level requirements

- Integrated USB-PD controller per PD 3.0 spec.
- Integrated Rp, Rd resistor on CC1/2 pins.
- Support dead battery termination.
- Integrated system level ESD protection for exposed pins.
- Integrated boot loader to support firmware update over I2C.
- Integrated VCONN FETS to provide power to EMCA cables.
- Support fast role swap.
- Support USB-PD extended messages.

Firmware Features

This version of the CYPD4126-40LQXI firmware supports the following key application level features:

- USB-PD Protocol as per PD 3.0 spec.
- USB-PD power contract negotiation as provider or consumer.
- Automatic consumer configuration when dead battery condition is detected.
- Support for VBus Over-Voltage protection based on internal comparator.
- Support for VBus Over-Current protection based on external current limited load switch.
- Support for DisplayPort alternate mode with PS8740B MUX for data path switching between USB-SS and DisplayPort.
- I2C based interface for status reporting and configuration updates from an Embedded Controller in the system.
- Selectable I2C slave address based on I2C_CFG pin status.
- Capability of in-system firmware upgrade through the I2C interface from Embedded Controller.
- Capability to update USB-PD profiles and change operating conditions through the I2C interface from Embedded Controller.
- Fast Role swap receive support.
- USBPD Extended messages support.

Default Device Configuration

Parameter	Supported Settings
Source PDOs	5V @ 3.0A, 9V @ 3.0A, 15V @ 3.0A, 20V @ 3.0A
Sink PDOs	5V @ 0.9A / 0.9A, 7V-21V @ 0.9A / 0.9A

Default SVDM Response

When the CYPD4126-40LQXI device functions as a UFP device, it will provide the following responses for the structured vendor defined message (SVDM) requests.

No SVIDs or Modes are supported as the device does not support any data transfers while functioning as a UFP.

DISCOVER_ID Response

0xFF008041, 0x920004B4, 0x00000000, 0xF6D10000

VDM header		
B31..16	Standard or Vendor ID (SVID)	0xFF00
B15	VDM Type	1b
B14..13	Structured VDM Version	00b
B12..11	Reserved	00b
B10..8	Object Position	000b
B7..6	Command Type	01b
B5	Reserved	0b
B4..0	Command	00001b
ID header		
B31	Data Capable as USB Host	1b
B30	Data Capable as a USB Device	0b
B29..27	Product Type is **Peripheral**	010b
B26	Modal Operation Supported	0b
B25..23	Product Type (DFP) is **Alternate Mode Controller**	100b
B22..16	Reserved. Shall be set to zero.	0x0
B15..0	16-bit USB Vendor ID	0x04B4
Cert Stat VDO		
B31..20	Reserved, shall be set to zero.	0
B19..0	20-bit unsigned integer	0
Product VDO		
B31..16	USB Product ID	0xF6D1
B15..0	bcdDevice	0x0000

DISCOVER_SVID Response

None.

DISCOVER_MODES Response

None.

Changes in Firmware version 3.2.1

1. Updated PD stack for compliance with USB-PD Specification Revision 3.0, Version 1.1; and USB Type-C Specification Revision 1.2.
2. Updated fault (Over-voltage, Over-current) handling code to allow for automated recovery when the faulty partner device is physically detached.
3. Updated Over-Voltage detection code to avoid false fault detection when a 5V contract is in place.
4. Added new event notifications for Type-C attach detection and other Type-C state transitions. These events can be used to control external circuits which may require additional time to get enabled.
5. Enabled a soft watch-dog which resets the CCG4 controller if the firmware is not responsive for a programmable (default of 1.5 seconds) duration.
6. Added user defined HPI registers associated with the PD port in addition to the device level registers.
7. Increased number of wait states used when accessing device flash with the CPU clock running at 48 MHz. This is the recommended clock configuration for the CM0 core used in the CCG4 device family.
8. Updated project to the latest PSoC Creator release version (4.2).

Limitations and Known Problems of Firmware version 3.2.1

1. I2C slave address used for Host Processor Interface (HPI) is based on the I2C_CFG GPIO (pin 2). This pin should be held steady (high, low or floating with no subsequent changes) for about 200 ms when the CCG3 is powering up or being reset.
2. CCG4 requires a worst-case delay of 1 ms from the point where the EC writes to the INTR_REG to clear an interrupt, to the point where the HPI interrupt gets cleared. EC is expected to use the HPI in edge triggered mode. CCG4 will ensure that a new edge will be provided if the event queue already has more data at the time when EC clears the first interrupt.
3. Vendor Defined Message (VDM) and extended message requests with wrong arguments to the HPI results in `Transaction Failed` error code instead of `Invalid Arguments`.
4. The device does not enter low power mode when Fast Role Swap (FRS) receive is enabled and acting as a sink.
5. The VBus OVP detection threshold used in CCG4 firmware has a minimum value of 6.5 V independent of the threshold selection made in the firmware configuration table. This is done to avoid false OVP detection due to inrush current at the time of Type-C connection.

Changes in Firmware version 3.0.2

1. USB-PD eye diagram fix: Disabled checks for Rp change while PD message transmission is in progress.
2. Updated PD HAL to select the correct pull-up current source configuration for Rp across device variations, instead of using a static configuration for all devices.
3. Updated configuration table parameter attributes to ensure that fields like swap response control and billboard configuration parameters work when the default configuration is changed.
4. Re-enabled user defined registers in HPI library. This feature was disabled in firmware version 3.0.0 due to lack of flash space.
5. Enabled usage of project with PSoC Creator 4.0 release.

Limitations and Known Problems of Firmware version 3.0.2

1. I2C slave address used for Host Processor Interface (HPI) is based on the I2C_CFG GPIO (pin 2). This pin should be held steady (high, low or floating with no subsequent changes) for about 200 ms when the CCG3 is powering up or being reset.
2. CCG4 requires a worst-case delay of 1 ms from the point where the EC writes to the INTR_REG to clear an interrupt, to the point where the HPI interrupt gets cleared. EC is expected to use the HPI in edge triggered mode. CCG4 will ensure that a new edge will be provided if the event queue already has more data at the time when EC clears the first interrupt.
3. Vendor Defined Message (VDM) and extended message requests with wrong arguments to the HPI results in `Transaction Failed` error code instead of `Invalid Arguments`.
4. The device does not enter low power mode when Fast Role Swap (FRS) receive is enabled and acting as a sink.
5. Try.SNK support has been disabled in the PD stack library due to flash constraints. Please contact Cypress support if Try.SNK support is needed in a specific application.

6. HPI based event notifications for the Over Voltage and Over Current error conditions detected by CCGx Notebook applications are not functional. The actual error handling including disabling the PD port is still functional. If notifying the EC about the error condition is required, the following code should be added in the `sln_pd_event_handler` function in main.c, immediately after the call to the `hpi_pd_event_handler` function:

```
/* Send over-voltage event notification to EC. */
if (evt == APP_EVT_VBUS_OVP_FAULT)
{
  hpi_reg_enqueue_event (port + 1, 0x83, 0, 0);
}

/* Send over-current event notification to EC. */
if (evt == APP_EVT_VBUS_OCP_FAULT)
{
  hpi_reg_enqueue_event (port + 1, 0x82, 0, 0);
}
```

Limitations and Known Problems of Firmware version 3.0.0

1. I2C slave address used for Host Processor Interface (HPI) is based on the I2C_CFG GPIO (pin 2). This pin should be held steady (high, low or floating with no subsequent changes) for about 200 ms when the CCG3 is powering up or being reset.
2. CCG4 requires a worst case delay of 1 ms from the point where the EC writes to the INTR_REG to clear an interrupt, to the point where the HPI interrupt actually gets cleared. EC is expected to use the HPI in edge triggered mode. CCG4 will ensure that a new edge will be provided if the event queue already has more data at the time when EC clears the first interrupt.
3. Vendor Defined Message (VDM) and extended message requests with wrong arguments to the HPI results in `Transaction Failed` error code instead of `Invalid Arguments`.
4. The device does not enter low power mode when Fast Role Swap (FRS) receive is enabled and acting as a sink.

Technical Support

For assistance, go to http://www.cypress.com/go/support for support.

Additional Information

For more information about the CCG4 Type-C controller, visit the web page:
http://www.cypress.com/products/ez-pd-ccg4-two-port-usb-type-c-controller-power-delivery

For more information about the CCG4 Evaluation Kit from Cypress, visit the web page:
http://www.cypress.com/documentation/development-kitsboards/cy4541-ez-pd-ccg4-evaluation-kit

For more information about the Cypress Type-C controller family, visit the web page:
http://www.cypress.com/products/usb-type-c-and-power-delivery

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