CYPD5225-96BZXI Firmware Release Notes

Version 3.2.1 Build 1658, June 27, 2018

Thank you for your interest in the CYPD5225-96BZXI CY-PD® CCG5 product family. This document contains release notes for the CYPD5225-96BZXI firmware. It also describes key updates and known issues.

Introduction

EZ-PD™ CCG5 is a dual USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG5 provides a complete dual USB Type-C and USB-Power Delivery port control solution for notebooks, power adapters and docking stations. It can also be used in dual role and downstream facing port applications. EZ-PD CCG5 uses Cypress's proprietary M0S8 technology with a 32-bit, 48-MHz ARM® Cortex®-M0 processor with 128-KB flash and integrates two complete Type-C Transceivers including the Type-C termination resistors RP and RD.

The CYPD5225-96BZXI device is the dual port version of CCG5. This device support USB-PD protocol revision 3.0 specification.

Key application level requirements:

- Integrated USB-PD controller per PD 3.0 spec.
- Integrated Rp, Rd resistor on CC1/2 pins.
- Support dead battery termination.
- Integrated system level ESD protection for exposed pins.
- Integrated boot loader to support firmware update over I2C.
- Integrated VCONN FETS to provide power to EMCA cables.
- Support fast role swap.
- Support USB-PD extended messages.
- High Voltage (25 V) tolerance on VBus and CC pins.
- Integrated SBU MUX to switch Type-C SBU pins between DP AUX connections and Thunderbolt LSX connections.
- Integrated USB 2.0 MUX to selectively connect system USB 2.0 (D+/D-) pins to the top or bottom side of the Type-C connector.
- BC 1.2 compliant legacy USB charger detect functionality.

Firmware Features

This version of the CYPD5225-96BZXI firmware supports the following key application level features:

- USB-PD Protocol as per PD 3.0 spec.
- USB-PD power contract negotiation as provider or consumer.
- Automatic consumer configuration when dead battery condition is detected.
- Support for VBus Over-Voltage protection based on internal comparator.
- Support for VBus Over-Current protection based on internal sense amplifier.
- Support for VConn Over-Current protection based on internal current detection (fixed threshold only).
- Selectable source voltage using NCP81239 buck-boost controller.
- Support for DisplayPort alternate mode with PI3DPX1205A MUX for data path switching between USB-SS and DisplayPort.
- I2C based interface for status reporting and configuration updates from an Embedded Controller in the system.
- Selectable I2C slave address based on I2C_CFG pin status.
- Capability of in-system firmware upgrade through the I2C interface from Embedded Controller.
- Capability to update USB-PD profiles and change operating conditions through the I2C interface from Embedded Controller.
- Fast Role swap receive support.
- USBPD Extended messages support.
- BC 1.2 source (Charging Downstream Port) support.

- Dual firmware binaries for redundancy and fail-safe firmware upgrades.

Since the available flash on the CCG5 device is insufficient to accommodate two full featured copies of the device firmware, the two firmware binaries used on the CCG5 device support different feature sets. The primary or full featured firmware supports all of the above listed features, while the backup or limited feature firmware supports a subset of features that allow basic system operation and firmware upgrades. Refer to the table below for a comparison of features supported in each firmware binary:

Feature	Support in Primary Firmware	Support in Backup Firmware
Dual Role Type-C v1.2 compliant port	Yes	Yes
Try.SRC configuration support	Yes	Yes
Try.SNK configuration support	Yes	Yes
USB-PD revision 2.0 support	Yes	Yes
USB-PD revision 3.0 support	Yes	No
Fast Role Swap Receive Support	Yes	No
DisplayPort source state machine	Yes	No
Thunderbolt (DFP/UFP) state machine	Yes	No
Firmware upgrade support through HPI	Yes	Yes
PD status and event reporting through HPI	Yes	Yes
PD command and VDM tunneling support through HPI	Yes	No
BC 1.2 (CDP) source support	Yes	No
VBus Over Voltage Protection	Yes	Yes
VBus Over Current Protection	Yes	Yes
VConn Over Current Protection	Yes	Yes

Default Device Configuration

Parameter	Supported Settings
Source PDOs	5V @ 3.0A, 9V @ 3.0A, 15V @ 3.0A, 20V @ 3.0A
Sink PDOs	5V @ 0.9A / 0.9A, 7V-21V @ 0.9A / 0.9A

Default SVDM Response

The structured vendor defined message (SVDM) responses provided by the CYPD5225-96BZXI device as an UFP are different for the primary and backup firmware binaries. These response differences are chosen to reflect the different feature sets supported by each firmware binary.

Primary Firmware

DISCOVER_ID Response

The device reports itself as an Alternate Mode Adapter (AMA) as UFP and an Alternate Mode Controller (AMC) as DFP.

Response data: 0xFF00A041, 0xAE0004B4, 0x00000000, 0xF6E00000, 0x0000000A

VDM header		
B31..16	Standard or Vendor ID (SVID)	0xFF00
B15	VDM Type	1b
B14..13	Structured VDM Version	01b
B12..11	Reserved	00b
B10..8	Object Position	000b
B7..6	Command Type	01b
B5	Reserved	0b
B4..0	Command	00001b
ID header		

B31	Data Capable as USB Host	1b
B30	Data Capable as a USB Device	0b
B29..27	Product Type (UFP) is **Alternate Mode Adapter**	101b
B26	Modal Operation Supported	1b
B25..23	Product Type (DFP) is **Alternate Mode Controller**	100b
B22..16	Reserved. Shall be set to zero.	0x0
B15..0	16-bit USB Vendor ID	0x04B4
Cert Stat VDO		
B31..0	32-bit unsigned integer, XID	0
Product VDO		
B31..16	USB Product ID	0xF6E0
B15..0	bcdDevice	0x0000
AMA VDO		
B31..28	HW Version	0000b
B27..24	Firmware Version	0000b
B23..21	VDO Version	000b
B20..8	Reserved	0
B7..5	VConn Power	000b
B4	VConn Required	0b
B3	VBus Required	1b
B2..0	USB SuperSpeed signaling support	010b

DISCOVER_SVID Response

The Thunderbolt Alternate Mode is supported when CCG5 is UFP.

Response data: 0xFF00A042, 0x80870000

VDM header		
B31..16	Standard or Vendor ID (SVID)	0xFF00
B15	VDM Type	1b
B14..13	Structured VDM Version	01b
B12..11	Reserved	00b
B10..8	Object Position	000b
B7..6	Command Type	01b
B5	Reserved	0b
B4..0	Command	00010b
VDO 1		
B31..16	SVID0	0x8087
B15..0	SVID1	0

DISCOVER_MODES Response

Mode response associated with Thunderbolt Alternate Mode. Refer to the Thunderbolt documentation from Intel for details.

Response data: 0x8087A043, 0x00000001

Backup Firmware

DISCOVER_ID Response

The device reports itself as a peripheral with no alternate modes as UFP. Since PD 3.0 is not supported, product type as DFP is not required.

Response data: 0xFF008041, 0x900004B4, 0x00000000, 0xF6E00000

VDM header

B31..16	Standard or Vendor ID (SVID)	0xFF00
B15	VDM Type	1b
B14..13	Structured VDM Version	00b
B12..11	Reserved	00b
B10..8	Object Position	000b
B7..6	Command Type	01b
B5	Reserved	0b
B4..0	Command	00001b
ID header		
B31	Data Capable as USB Host	1b
B30	Data Capable as a USB Device	0b
B29..27	Product Type (UFP) is **Peripheral**	010b
B26	Modal Operation Supported	0b
B25..16	Reserved. Shall be set to zero.	0x0
B15..0	16-bit USB Vendor ID	0x04B4
Cert Stat VDO		
B31..0	32-bit unsigned integer, XID	0
Product VDO		
B31..16	USB Product ID	0xF6E0
B15..0	bcdDevice	0x0000

DISCOVER_SVID Response

No SVIDs supported. NAK response shall be provided.

DISCOVER_MODES Response

No SVIDs supported. NAK response shall be provided.

Changes in Firmware version 3.2.1

1. Updated PD stack for compliance with latest USB Type-C and USB-PD test specifications.
2. Updated VConn OCP settings to increase fault detection threshold to the maximum supported value.
3. Fixed a defect in the VBus OCP detection code which could cause OCP faults to be missed if the load increases beyond the threshold gradually.
4. Updated CDP state machine to allow charger detection by sink to work even if the sink connects a long time after the Rd attach on the Type-C port happens. Firmware version 3.1.0 expected that the BC 1.2 detection is done within 30 seconds of the Rd attach.
5. Implemented HPI commands to query the Discover SVID and Discover Modes responses received from a UFP port partner.
6. Updated code to allow Alternate Mode discovery and operation to proceed even if VConn OCP has been detected.
7. Updated Type-C state machine code to detect detach of an audio accessory when the voltage on either CC line goes out of the VRa range.
8. Updated project to the latest PSoC Creator release version (4.2).

Limitations and Known Problems of Firmware version 3.2.1

1. The CCG5 firmware supports Intel Thunderbolt alternate mode negotiation, however, the evaluation kit hardware does not include the Thunderbolt controllers required for actual Thunderbolt data transfers.
2. I2C slave address used for Host Processor Interface (HPI) is based on the I2C_CFG GPIO (pin 2). This pin should be held steady (high, low or floating with no subsequent changes) for about 200 ms when the CCG5 is powering up or being reset.
3. CCG5 requires a worst-case delay of 1 ms from the point where the EC writes to the INTR_REG to clear an interrupt, to the point where the HPI interrupt gets cleared. EC is expected to use the HPI in edge triggered mode. CCG5 will ensure that a new edge will be provided if the event queue already has more data at the time when EC clears the first interrupt.
4. Vendor Defined Message (VDM) and extended message requests with wrong arguments to the HPI results in `Transaction Failed` error code instead of `Invalid Arguments`.
5. The device does not enter low power mode when Fast Role Swap (FRS) receive is enabled and acting as a sink.
6. CCG5 firmware manages the two USB-PD ports in a completely independent manner. If there are policy decisions to be implemented at a global basis, this will have to be done by the EC through the HPI interface.
7. When firmware update is performed through the bootloader, control is passed to the last flashed binary after a device reset. If it is desired that the primary firmware should always be loaded when available, firmware update should either be done in firmware mode or the primary firmware image should be programmed last.
8. The Current Sense Amplifier (CSA) circuit used to implement the VBus Over Current Protection (OCP) scheme has a non-linear error which is higher at low sense voltages than at high sense voltages. Firmware compensates for the worst-case CSA error by shifting the OCP thresholds higher so that a false OCP detection does not happen. This compensation causes the actual OCP detection to happen at higher currents (up to 1.5X) instead of the expected threshold (1.2X). If better accuracy is required, please update the OCP detection threshold to 5% in the device configuration table.
9. The Cortex-M0 core on the CCG5 is being run at 24 MHz. This lower clock speed results in high worst-case latencies in firmware response to commands issued through the HPI interface. Latencies of up to 1 ms may be seen before CCG5 responds to an HPI command from the Embedded Controller.

Limitations and Known Problems of Firmware version 3.1.0

10. The CCG5 firmware supports Intel Thunderbolt alternate mode negotiation, however, the evaluation kit hardware does not include the Thunderbolt controllers required for actual Thunderbolt data transfers.
11. I2C slave address used for Host Processor Interface (HPI) is based on the I2C_CFG GPIO (pin 2). This pin should be held steady (high, low or floating with no subsequent changes) for about 200 ms when the CCG5 is powering up or being reset.
12. CCG5 requires a worst case delay of 1 ms from the point where the EC writes to the INTR_REG to clear an interrupt, to the point where the HPI interrupt actually gets cleared. EC is expected to use the HPI in edge triggered mode. CCG5 will ensure that a new edge will be provided if the event queue already has more data at the time when EC clears the first interrupt.
13. Vendor Defined Message (VDM) and extended message requests with wrong arguments to the HPI results in `Transaction Failed` error code instead of `Invalid Arguments`.

14. The device does not enter low power mode when Fast Role Swap (FRS) receive is enabled and acting as a sink.
15. CCG5 firmware manages the two USB-PD ports in a completely independent manner. If there are policy decisions to be implemented at a global basis, this will have to be done by the EC through the HPI interface.
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17. The Current Sense Amplifier (CSA) circuit used to implement the VBus Over Current Protection (OCP) scheme has a non-linear error which is higher at low sense voltages than at high sense voltages. Firmware compensates for the worst case CSA error by shifting the OCP thresholds higher so that a false OCP detection does not happen. This compensation causes the actual OCP detection to happen at higher currents (up to 1.5X) instead of the expected threshold (1.2X). If better accuracy is required, please update the OCP detection threshold to 5% in the device configuration table.
18. The Cortex-M0 core on the CCG5 is being run at 24 MHz. This lower clock speed results in high worst case latencies in firmware response to commands issued through the HPI interface. Latencies of up to 400 us may be seen before CCG5 responds to an HPI command from the Embedded Controller.

Technical Support

For assistance, go to http://www.cypress.com/go/support for support.

Additional Information

For more information about the Cypress Type-C controller family, visit the web page:
http://www.cypress.com/products/usb-type-c-and-power-delivery

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