END-SEMESTER REPORT

Made by - Utkarsh Saboo

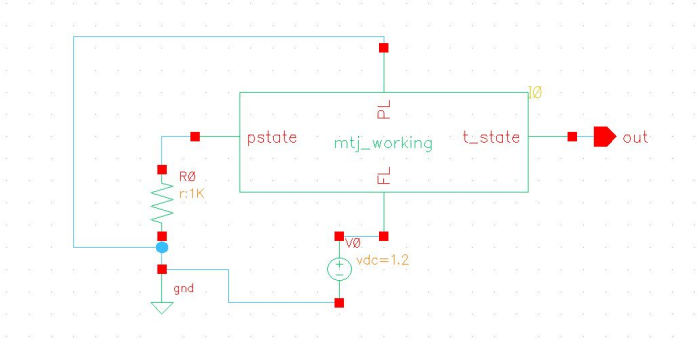
Project Title - Design of an MTJ based SR latch.

Aim - Design an MTJ based SR latch, feeding it's output to a Schmitt trigger and using it as an input to the dynamic CMOS logic.

Course Title - Study Oriented Project. (EEE F-266)

Theory -

MTJ - It exhibits a large magnetoresistive effect at room temperature. It works on the principle that we can reverse the magnetic moment of the metal by varying the direction of the local magnetic field. In a ferromagnetic material, an electric current consists of two partial currents, each with either spin-up or spin-down electrons.
Here the resistance depends on whether the magnetisation is parallel or anti-parallel.



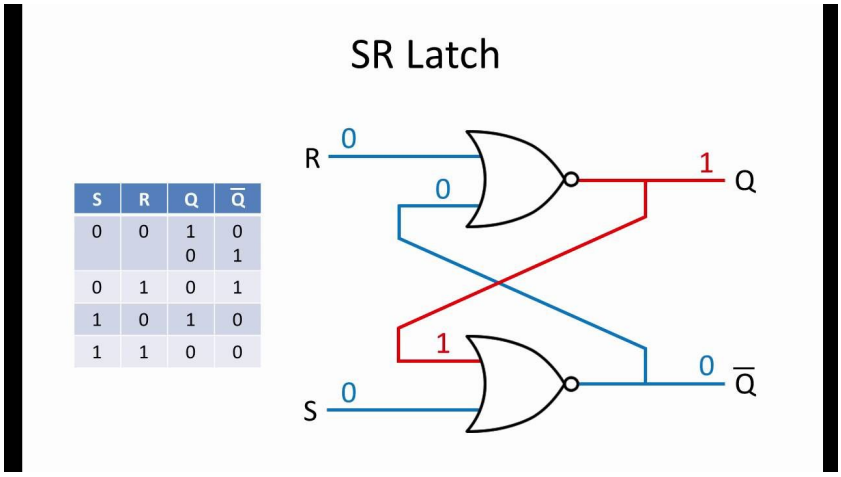
SR Latch

In an S-R latch, setting of just the S input activates the circuit hence setting Q = 1, while activation of the R input resets the circuit. If both S and R inputs are given at the same time, the circuit will be in an invalid condition.

The Q and not-Q outputs are supposed to be in opposite states.

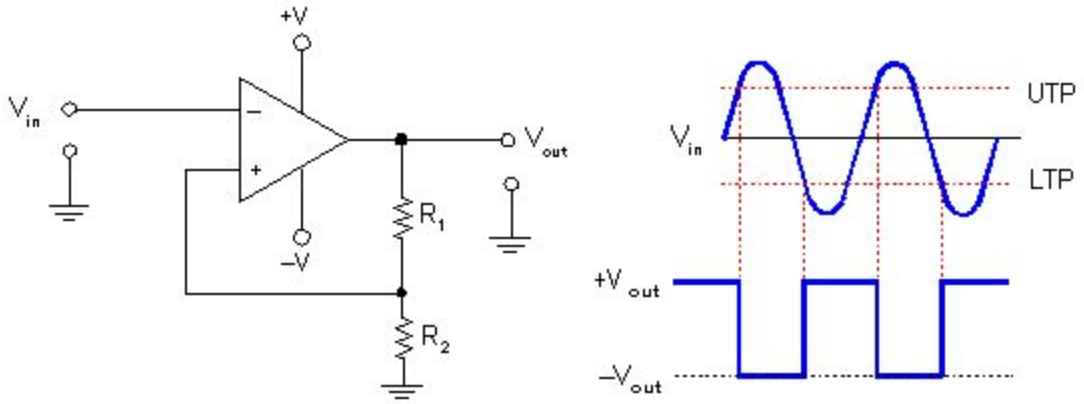
To create an S-R latch, we can wire two NOR Gates in such a way that the output of one feeds back to the input of another, and vice versa, like this:

Here is a diagram and working of an SR latch.

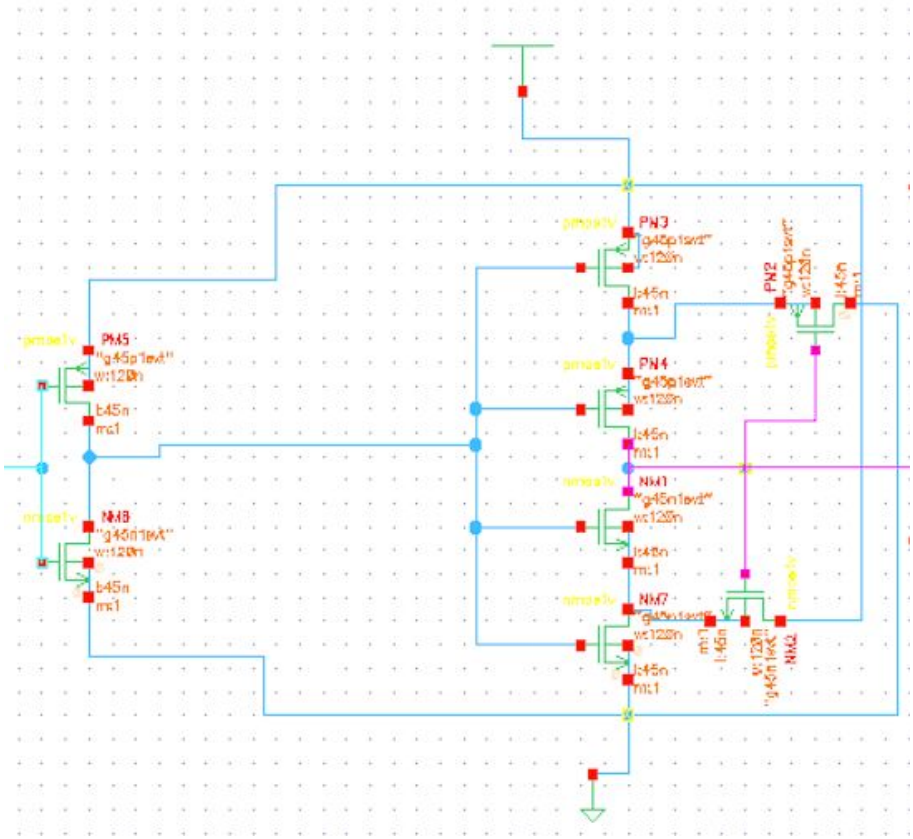


S	R	Q	$\overline{Q}$
0	0	1 0	0 1
0	1	0	1
1	0	1	0
1	1	0	0

SCHMITT TRIGGER CIRCUIT



CADENCE CIRCUIT



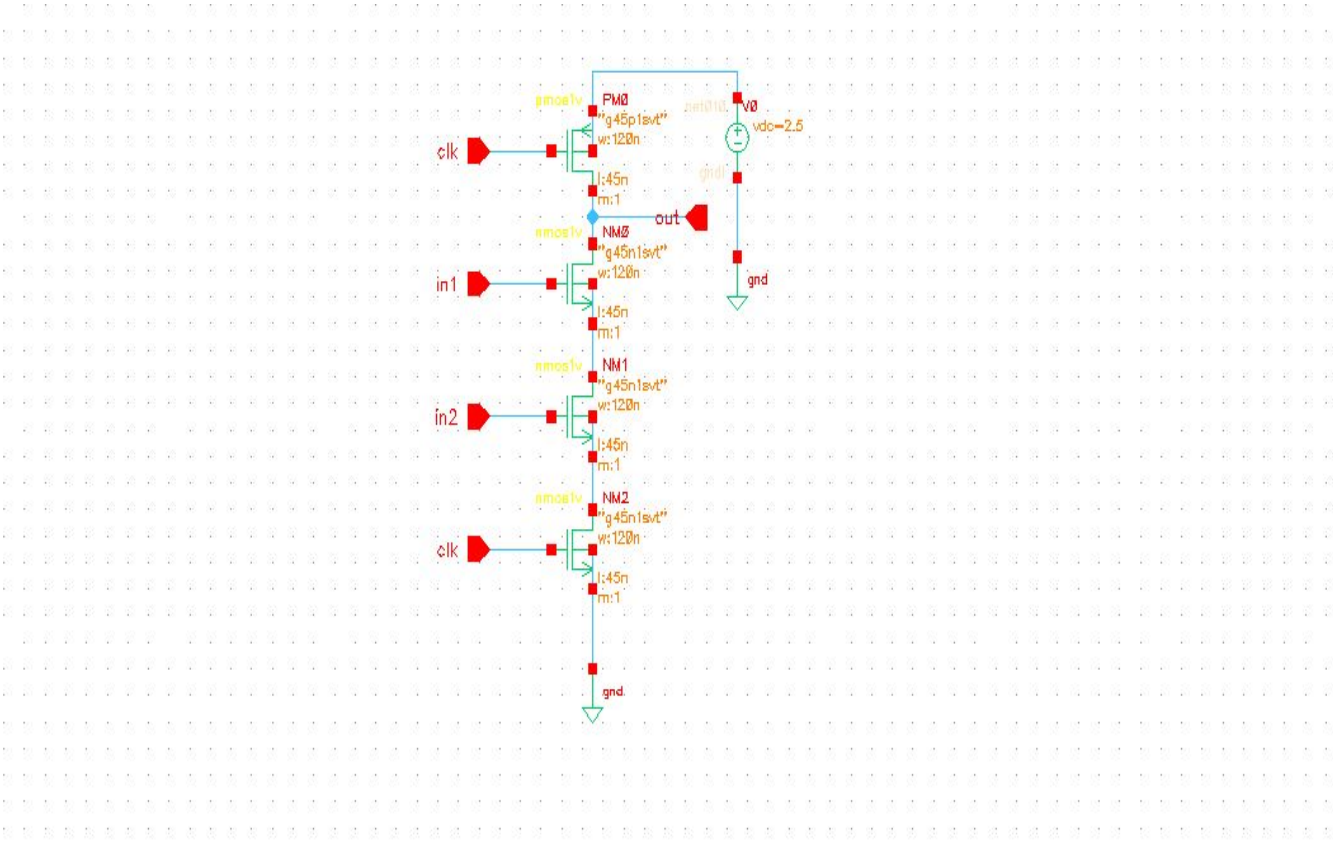
THEORY

The primal function of the Schmitt Trigger, to convert noisy square waves, sine waves or slow edges inputs into clean square waves.

In our MTJ circuit, the “S” output of the SR latch is not exactly 2.5 volts but somewhere around 1.6 V, so in order to restore the circuit to the value of 2.5V we use a Schmitt trigger circuit.

DYNAMIC CMOS LOGIC

We create a dynamic CMOS NAND gate which will receive the Schmitt trigger output, take in clock and another bit stream as in input as shown in the following figure.

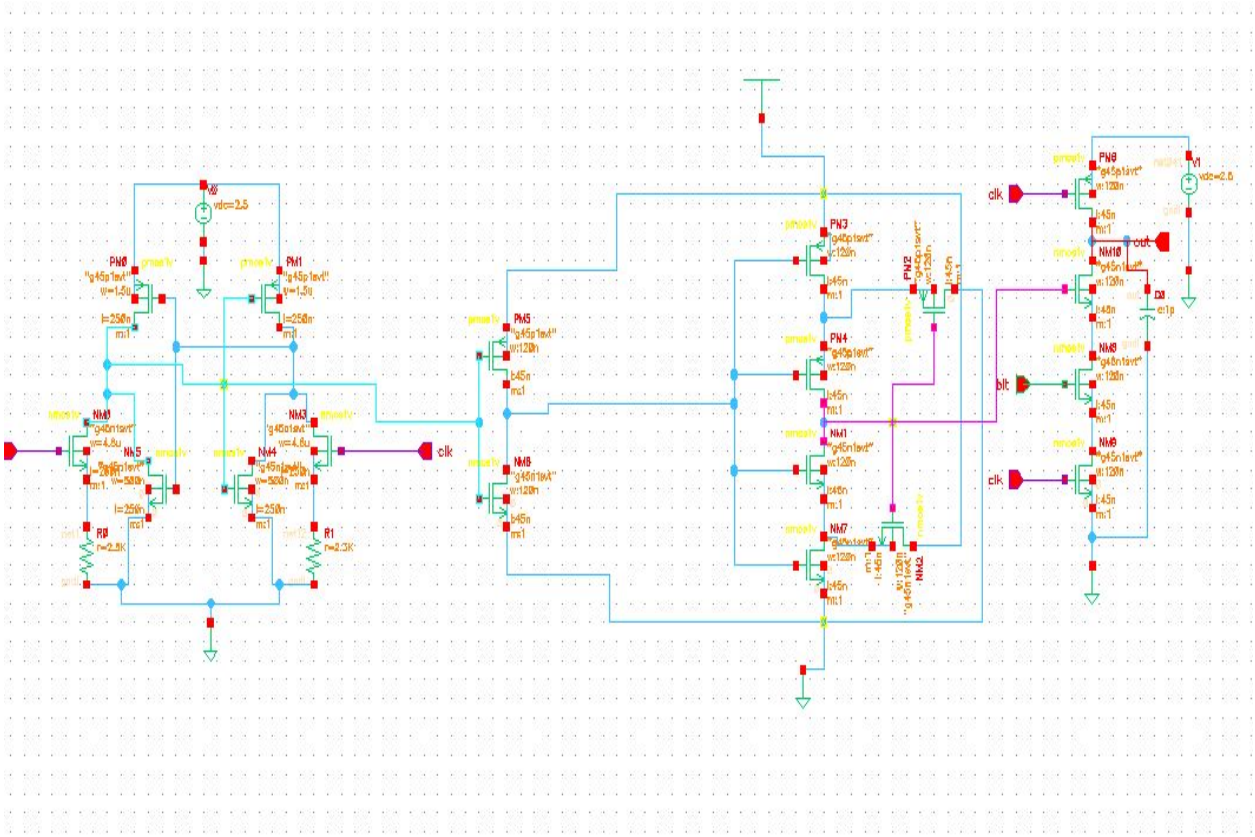


RESULTS :

The circuit has three parts :

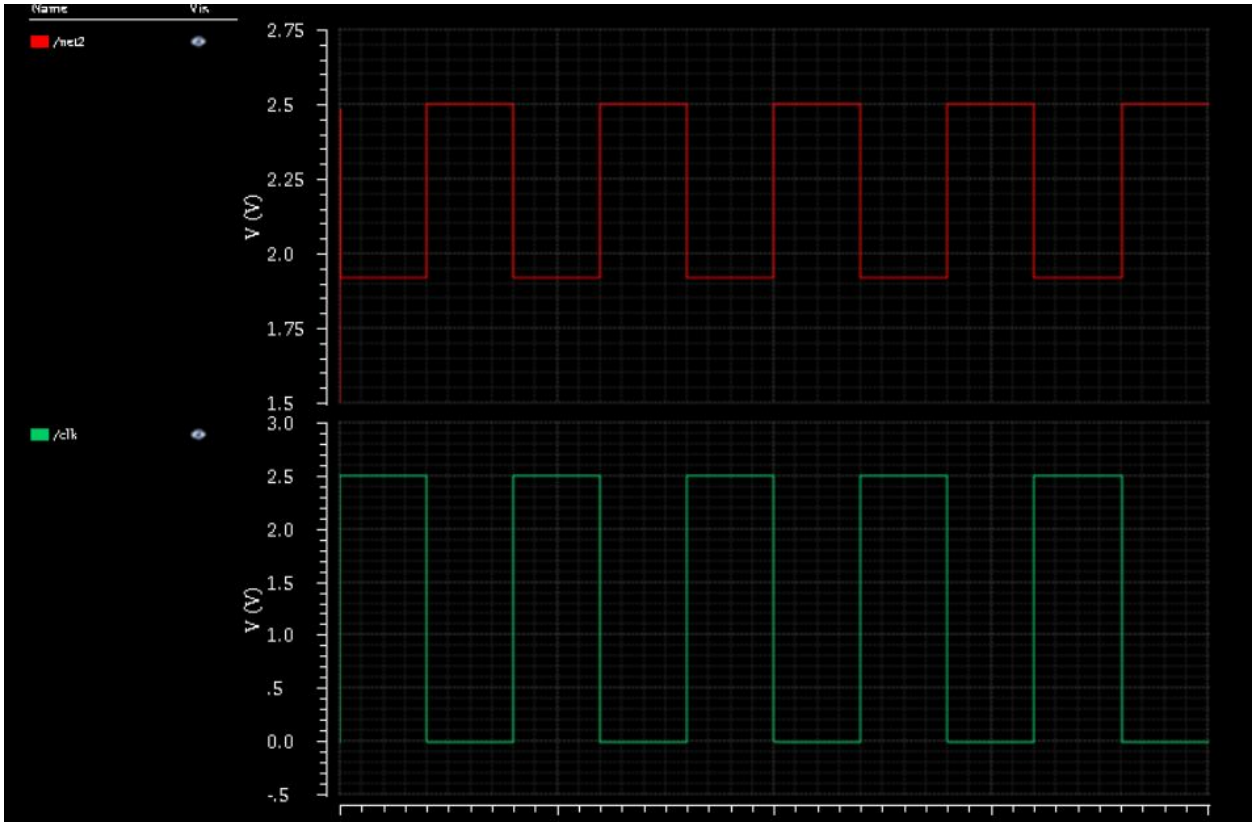
First part of the circuit has SR latch in which the output is given in the form of resistances . The higher resistance is considered to be 1 in the input and lower resistance is considered to be 0 as the input .

Following is the value of the output as the resistance of R input is varied from 0 to resistance at S input .



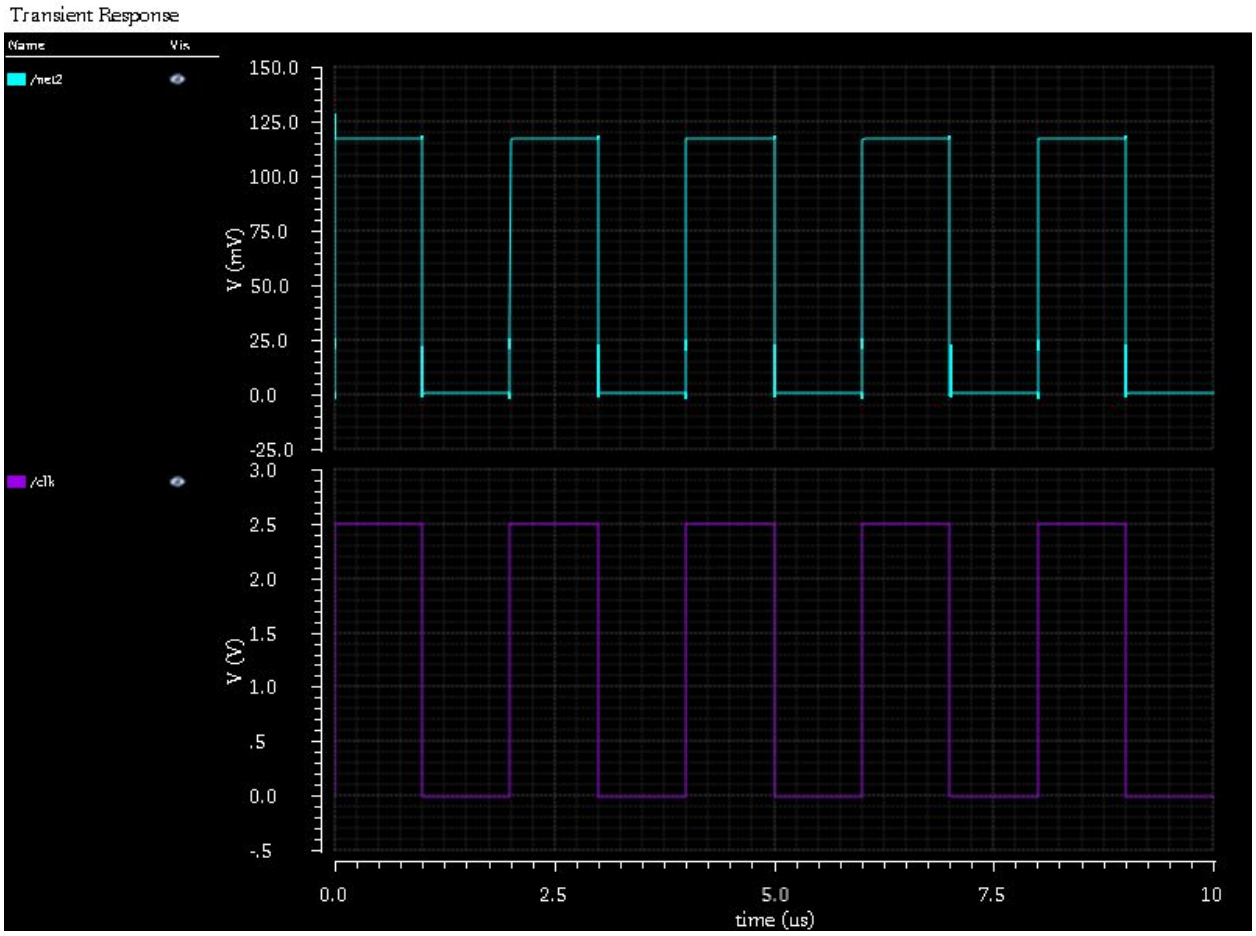
According to the parametric analysis if input at S resistance is 2.5k ohms , then the circuit gives us the correct result if the value of resistance at R is less than 2.3kohms .

According to SR latch logic , output =1 if S=1 . So the value of the output varies from 1.9v to 2.4v if we set the value of resistance at S to be 2.5kohms and value of resistance at R to be between 0 and 2.3kohms .



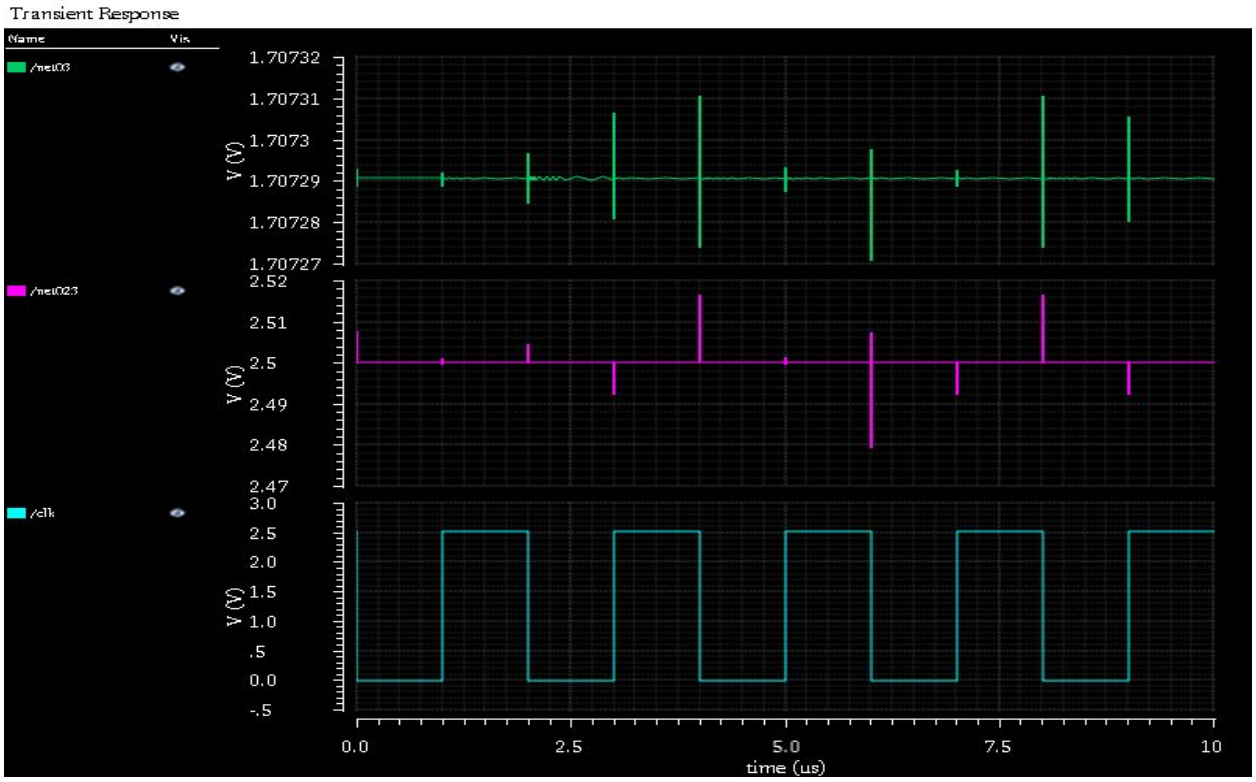
Green is the clock and red is the output Q when S=1 and R=0

Similarly if we set the value of resistance at S to be less than 2.3kohms and the value of resistance at R to be 2.5kohms , the output Q goes 0 and the output Q’ goes 1.



Purple is the clock and blue is the output of SR latch which is 0

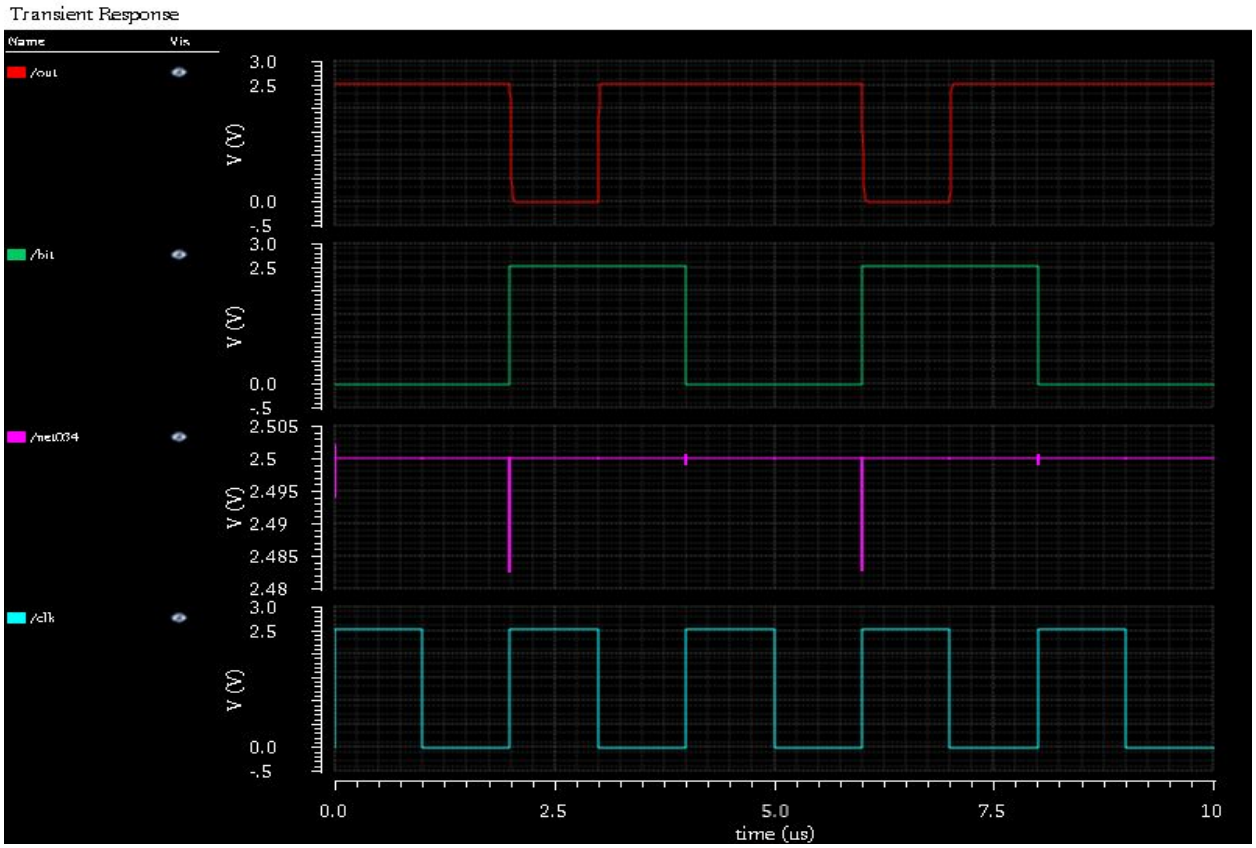
Second part of the circuit is Schmitt trigger which helps us to restore the value of the output to the value of VDD which we set because the output of the SR latch is somewhere around 1.9 to 2.4 but we want it to be equal to VDD which is 2.5 in our case . So the schmitt trigger is used which works as an inverter . if the value of the ouput is less than VDD/2 , it gives us the output as 1 and if the value is more than VDD/2 , the output is equal to 0 . As it works as an inverter , we have to use an inverter before giving the input to the schmitt trigger in order to get the correct results .



Here net023 is the output of the Schmitt trigger circuit. Net03(topmost) is the output of the SR latch. Clk is the clock with period of 2uS.

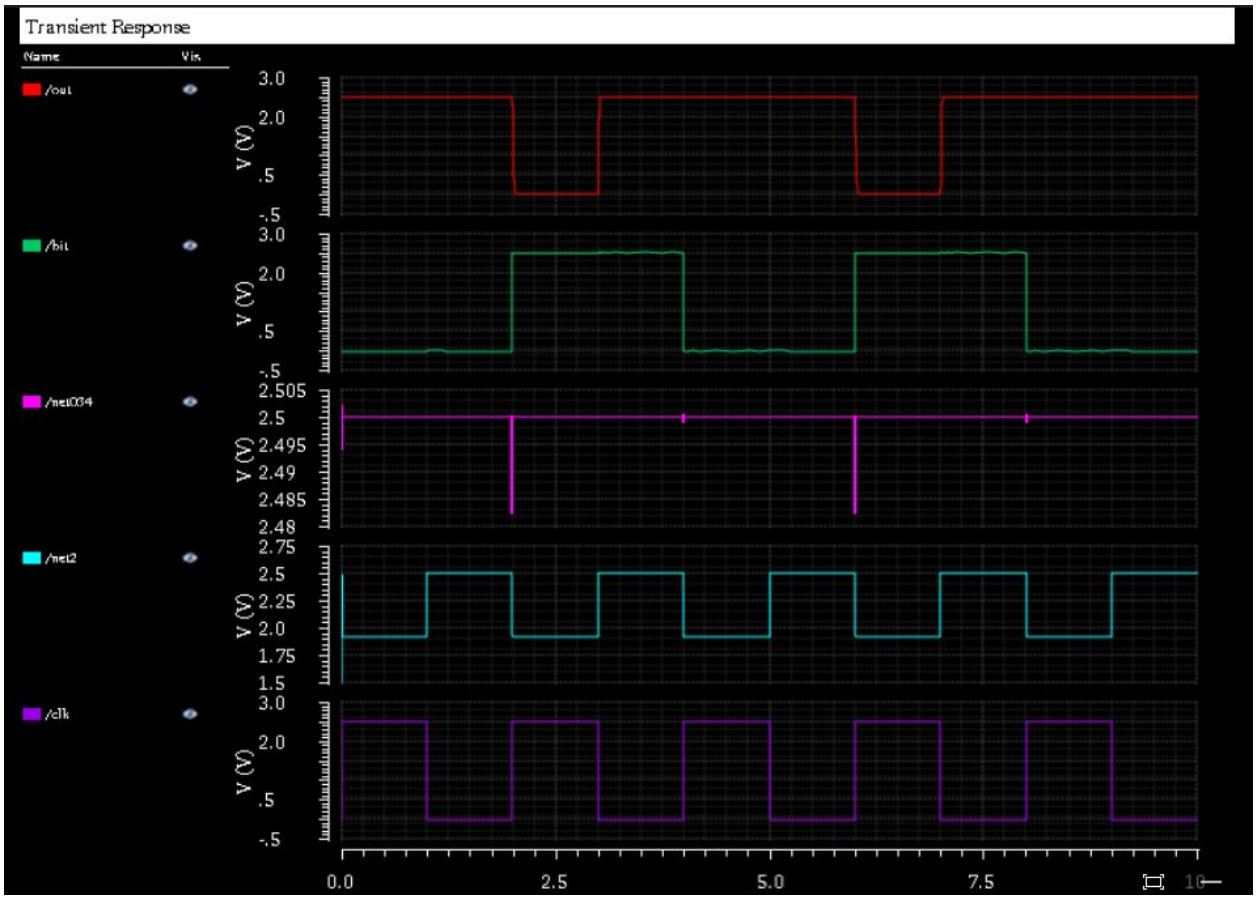
The third part of the circuit is a NAND gate with dynamic CMOS logic which is used to obtain the value from the sequential circuit . its a 2 input NAND gate . One input comes from the output of the Schmitt trigger and another is a random bit input given by us . when the clock is low , i.e. during the precharge period , the output is high irrespective of the inputs . when the clock is high , i.e the evaluative phase , the output varies according to the input

IF S=1 , one input of the nand gate will always be 1 , so the another input will monitor the output when the clock is high .



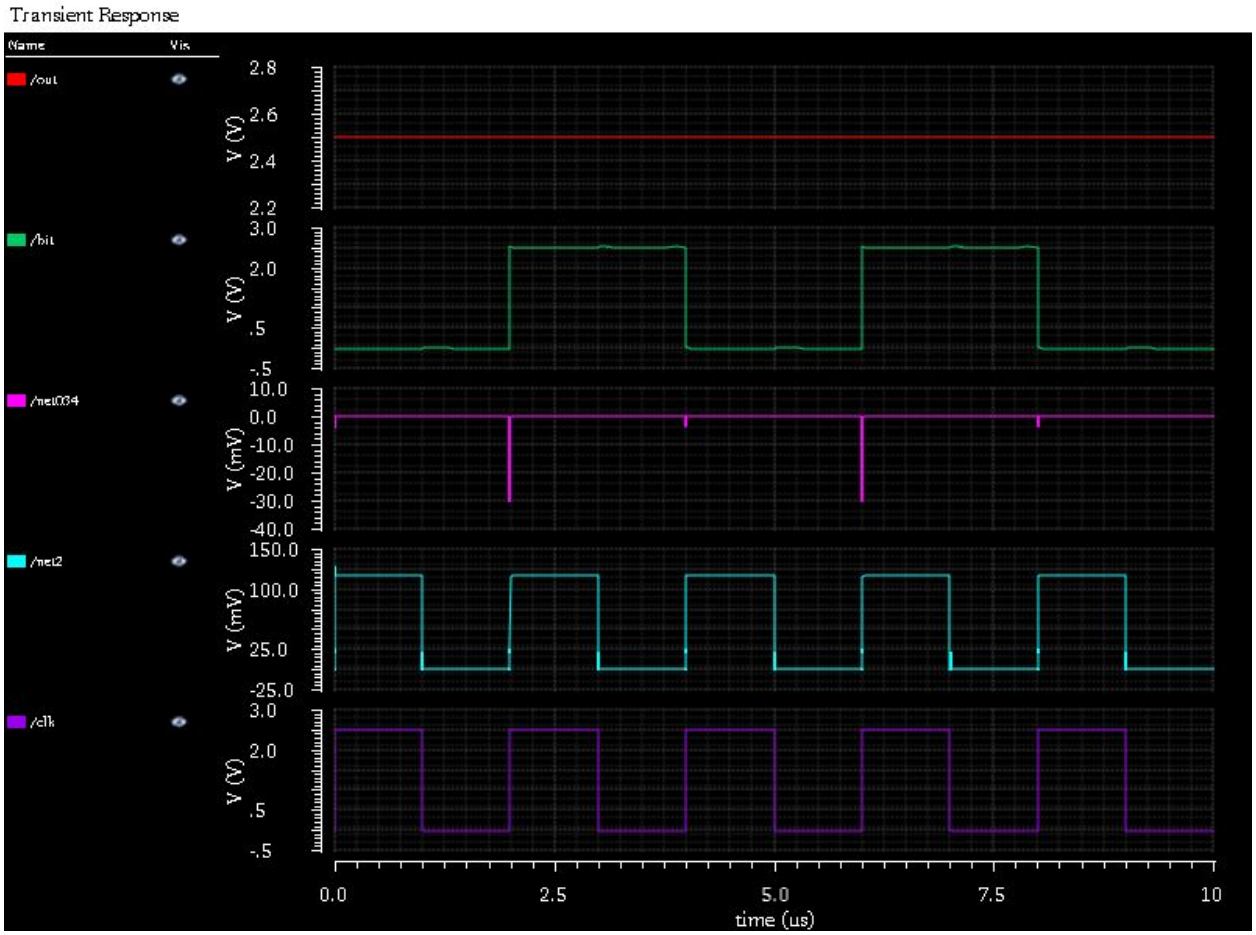
Here net034 is the output of the Schmitt trigger circuit. Bits is the pulse input we give. Clk is the clock with period of 2uS and out is the output.

The final output of the entire circuit when S = 1 and R = 0 is :



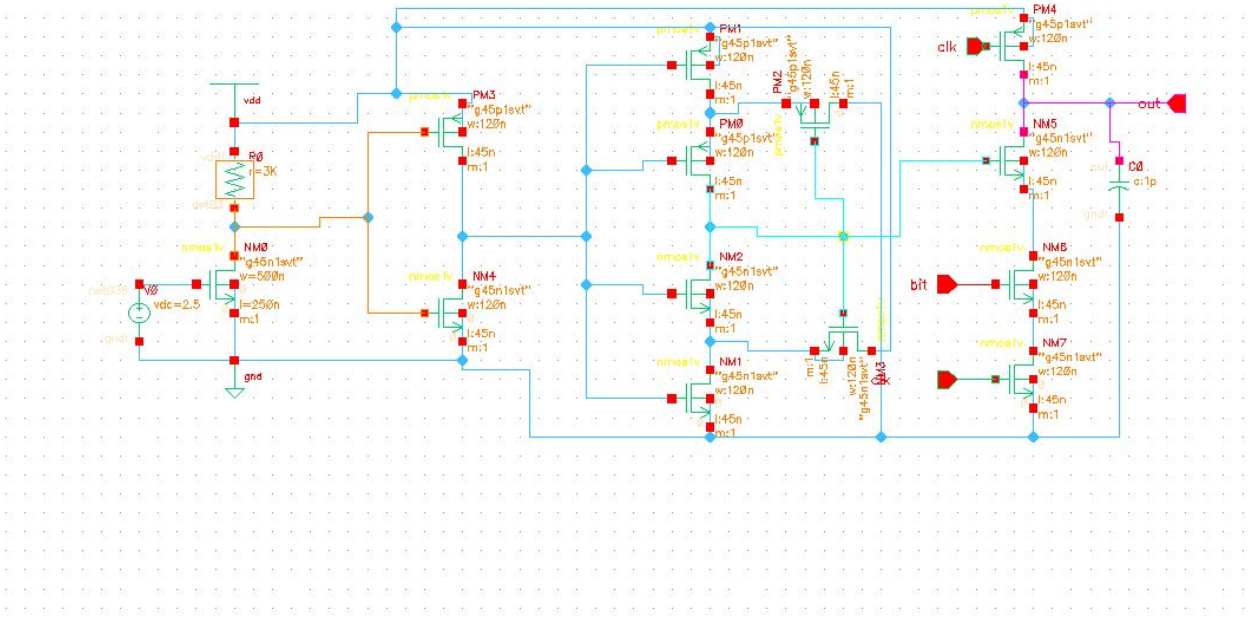
Starting from the last waveform , its the clock in purple.
Then blue waveform is the output of the SR latch when S=1 .
Pink is the output of the schmitt trigger which is equal to VDD as Q=1.
Green is the input given to NAND gate which is 0011001100.
Red is the final output of the circuit.

The final output of the entire circuit when S = 0 and R = 1 is :



Starting from the last waveform , its the clock in purple.
Then blue waveform is the output of the SR latch when S=0 .
Pink is the output of the schmitt trigger which is equal to 0 as Q=0.
Green is the input given to NAND gate which is 0011001100.
Red is the final output of the circuit.

CIRCUIT WITH NMOS AND RESISTANCE

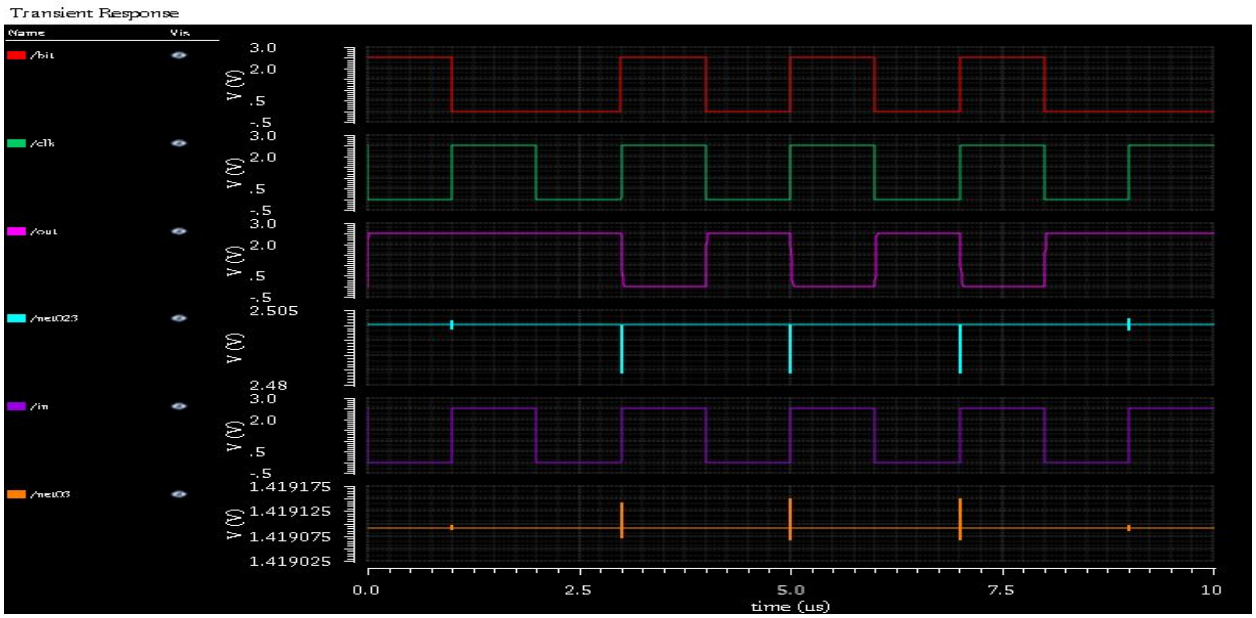


The second circuit involves a resistor and a MOS followed by schmitt trigger and dynamic CMOS logic NAND gate .
By setting the value of W/L of NMOS to be 1.5um /500nm , a parametric analysis is done on the value of resistance from 1k to 10k .
When the value of resistance is between 1k to 4k , it behaves as a pull up network and we get the output as VDD .
When the value of resistance varies from 4k to 10k , the output goes to 0 and it behaves as a pull down network because the resistance of the MOS is lower than the resistance given .

x	VDC("/net03") (V)
1K	2.17039
2K	1.85671
3K	1.56399
4K	1.30341
5K	1.09506
6K	936.801m
7K	815.564m
8K	720.793m
9K	645.125m
10K	583.518m

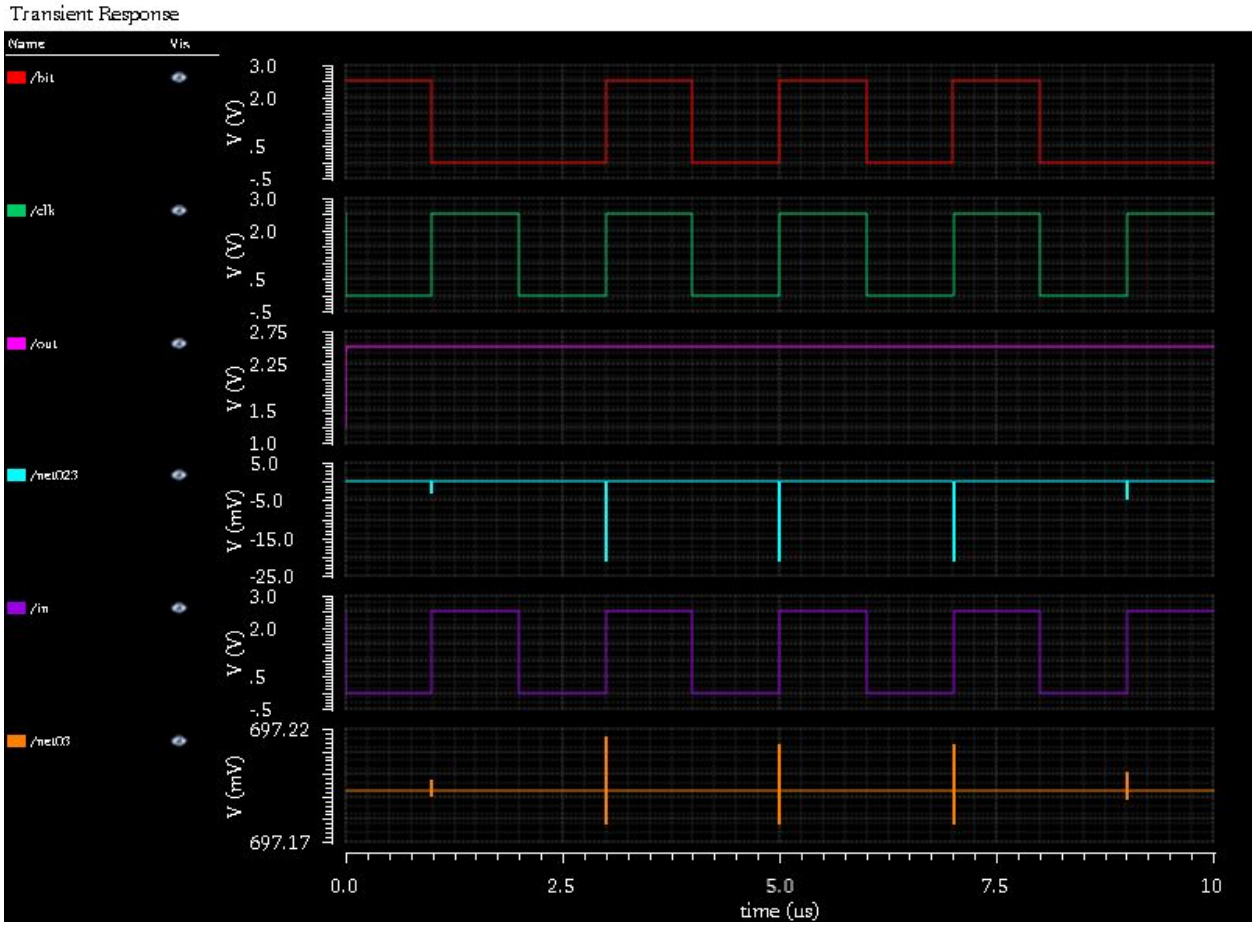
x	VDC("/net023") (V)
1K	2.49999
2K	2.49999
3K	2.5
4K	2.5
5K	20.568u
6K	20.1258u
7K	21.1138u
8K	22.0653u
9K	22.7947u
10K	23.2318u

The final output of the circuit when the circuit works as a pull up network is -



Orange waveform signifies the output at the first point which is high as it is acting as a pull up network .
Pink is final output of the circuit. Red it the bit stream we are giving to the NAND gate which is 10010101000. Blue is the output of the Schmitt trigger which is high.

The final output of the circuit when it works as a pull down network is -



Orange waveform signifies the output at the first point which is low as it is acting as a pull down network .
Pink is final output of the circuit. Red it the bit stream we are giving to the NAND gate which is 10010101000. Blue is the output of the Schmitt trigger which is low.