BITS Pilani
K K Birla Goa Campus

RESEARCH PRACTICE REPORT ON

SENSE AMPLIFIER FOR STTMRAM

Presented By:

UTKARSH SABOO

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Guided By:

Dr. C.K. Ramesha

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ABSTRACT

Spin-transfer torque magnetic random access memory(STT-MRAM) stores the data in magnetic tunnel junction(MTJ).It has very advantageous features like nonvolatility, scalability, high density, zero leakage and CMOS compatibility. MTJ has two states: a parallel state and anti parallel state, direction of the free layer decides the state. Date stores in the MTJ in the form of resistance. Sense amplifier requires to read that data. Sense amplifier senses the voltage across the MTJ block according to that it gives the output. Here in this project, sense amplifier designed using 45 nanometre CMOS technology and 15 nanometre FinFET technology.

Keywords : CMOS, FinFET, sense amplifier, CADENCE

INTRODUCTION

Due to shrinking device sizes, the old memory technologies are facing challenges like increasing leakage power and unreliability. To solve this issue, researchers are actively working for feasible solutions in the field of non-volatile memory technologies. Spin transfer torque magnetic random access memory(STTMRAM) is an emerging non-volatile magnetic memory. Magnetic tunnel junction(MTJ) has two stage: 1) parallel state and 2) anti parallel state. The state is the decided by magnetization direction of free layer. Here the sense amplifier senses the data according to the voltage across the (magnetic tunnel junction)MTJ block. Sense amplifier should have high read margin. The unique challenge in spin transfer torque magnetic random access memory (STTMRAM) is to avoid accidental write operation. While during the read operation, if current flows through magnetic tunnel junction(MTJ) is higher than particular threshold current, then there is higher probability of accidental write operation. Sense amplifier should be designed such that during the read operation, current flowing through the magnetic tunnel junction(MTJ) should be less than particular threshold current.

MTJ(Magnetic tunnel junction**)**

Magnetic tunnel junction consists three layers. Frist and third layers are made of feromagnet materials. Second layer is made of insulator. In Feromagnet materials layer, Frist layer is called free layer and third layer is reference layer. Free layer's magnetization direction can be changed but reference layer's magnetization direction can not be changed. If both layers magnetization direction are parallel, then resistance of MTJ block is less than the resistor of MTJ block when layers magnetization direction is anti parallel.

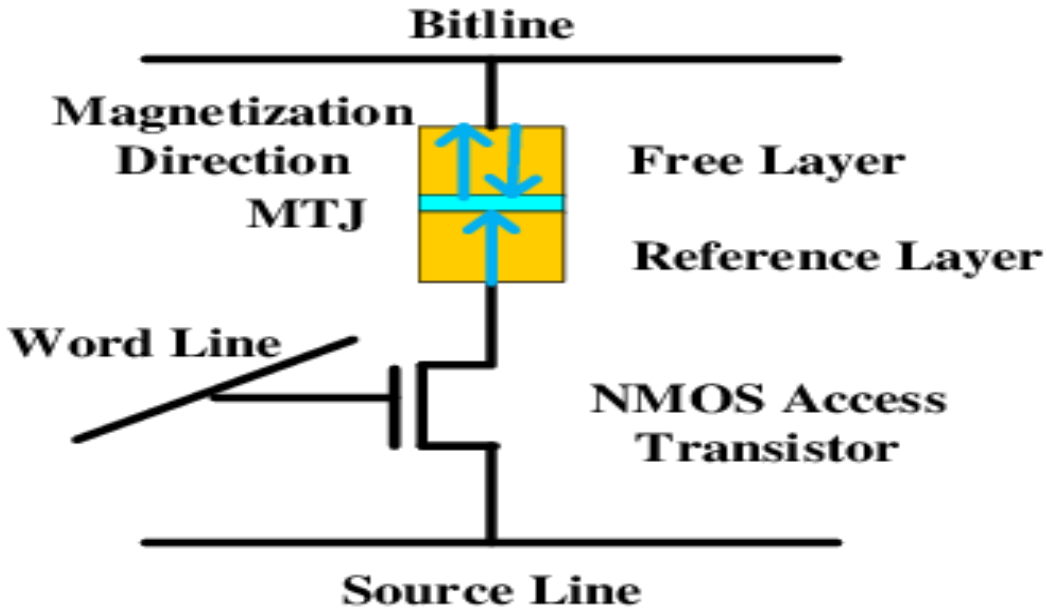

Figure: MJT block with access transistor

From the Verilog code of magnetic tunnel junction(MTJ), symbol and simulation are done in cadence virtuoso. For given MJT block resistances are 1.72kohm and 3.3k ohm for parallel and anti parallel state respectively.

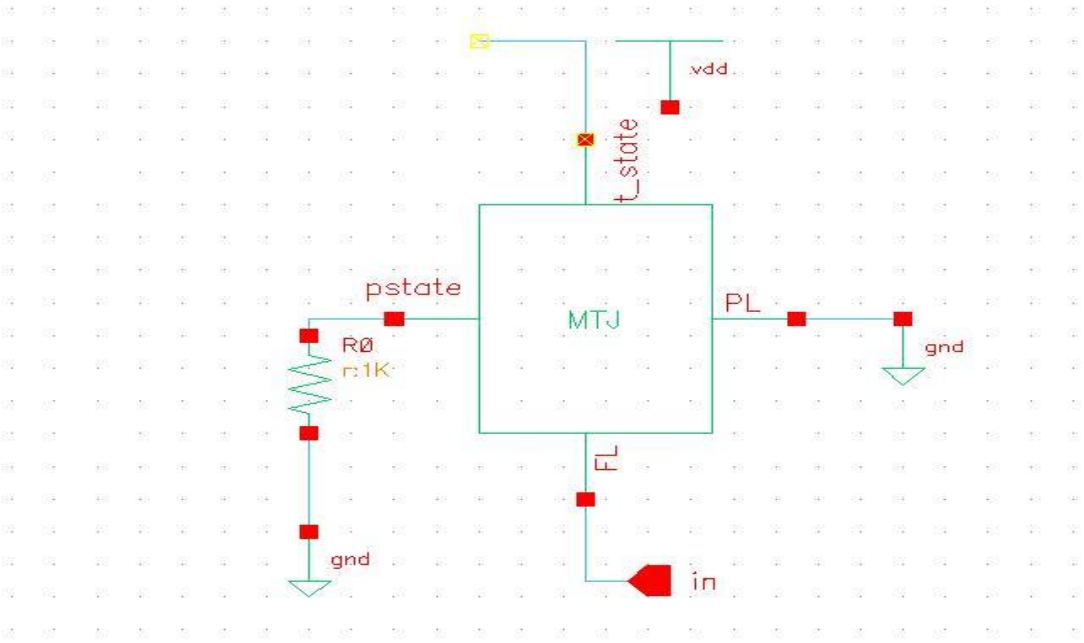

Figure: symbol of magnetic tunnel junction(MTJ)

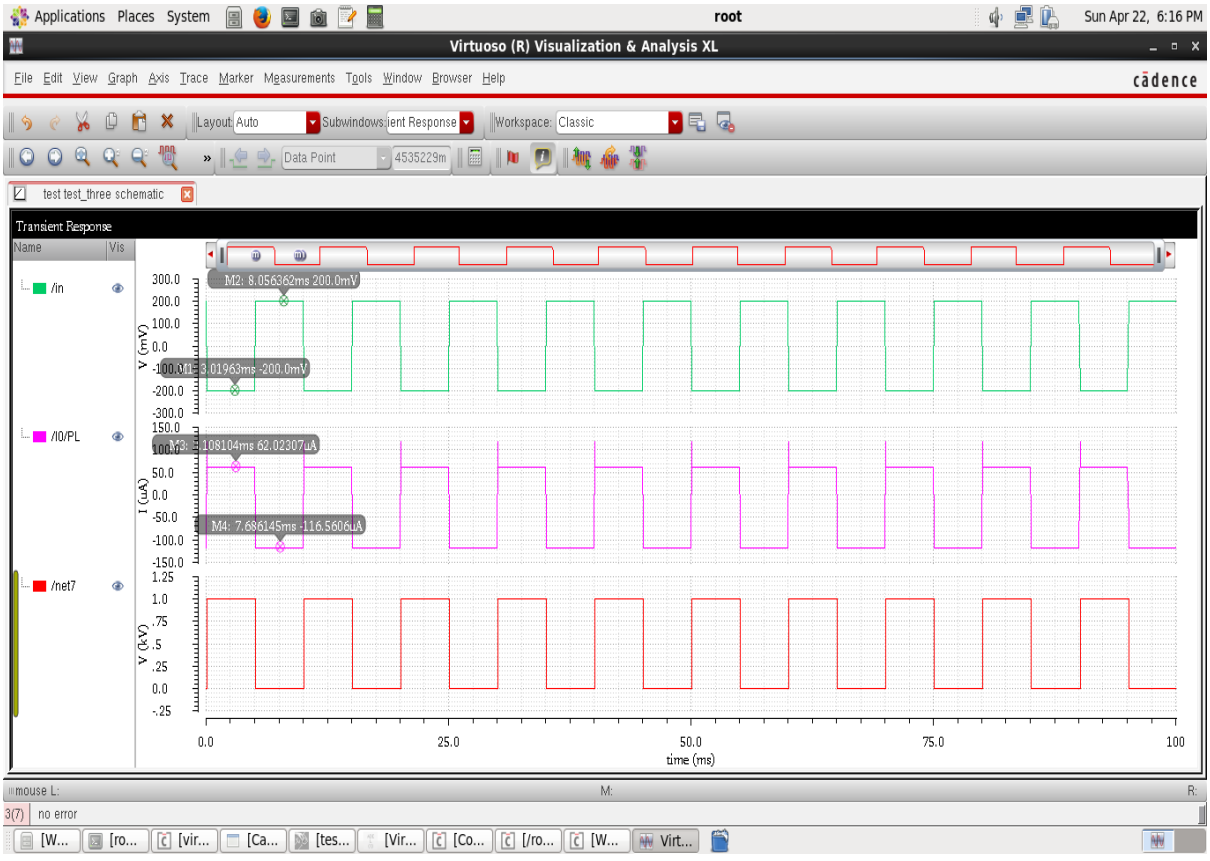

Figure: Waveforms of magnetic tunnel junction(MTJ)

Different topologies for sense amplifier

Frist three topology designed using cmos technology and fourth topology is designed using finfet technology.

1) Topology:-1

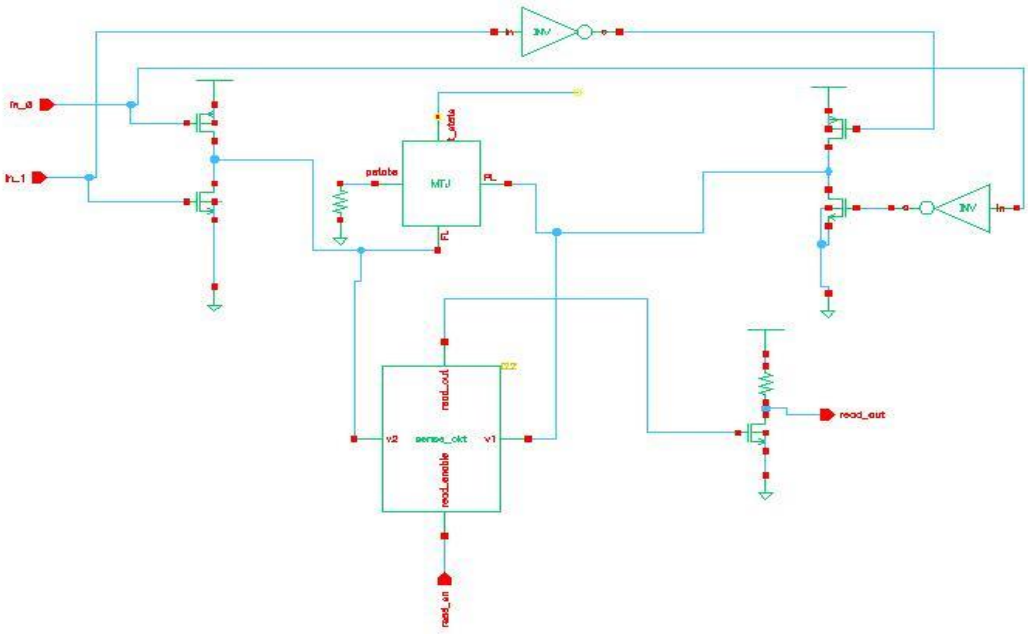

Figure: Schematic for topology1

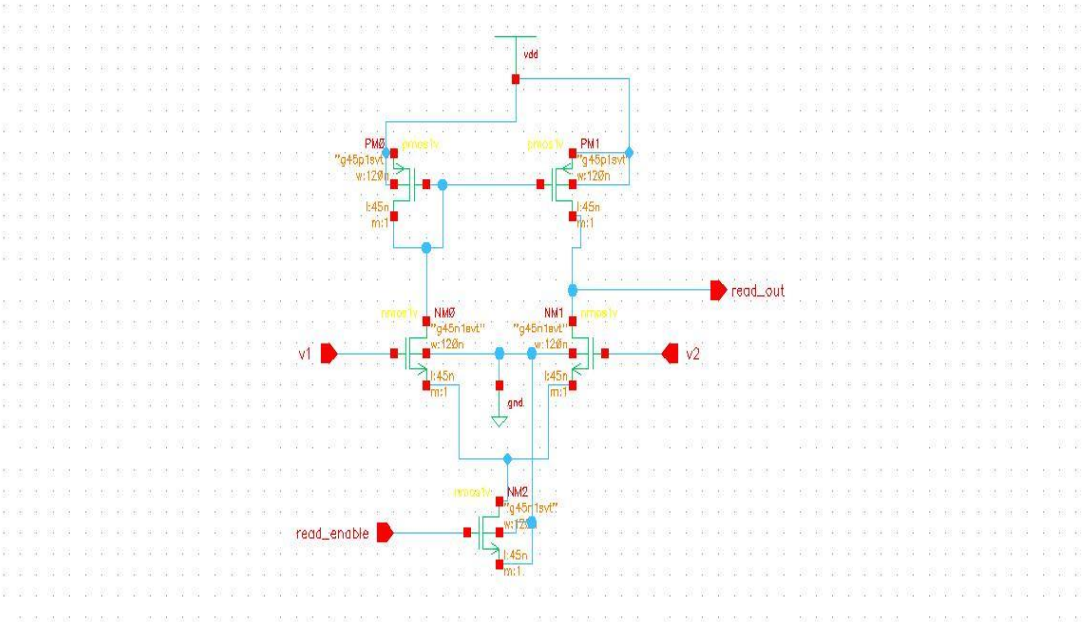

Figure: Schematic of reading circuitry(topology1)

In this sense amplifier, for writing circuit two inverter are used. By using the these two inverter, we can change the state of magnetic tunnel junction(MTJ). For reading circuitry, differential amplifier is used. The problem with this topology is that during read operation, current flowing through magnetic tunnel junction is higher than threshold current value.so there is the problem of accidental write operation. Accidental write operation is not acceptable.

2)Topology:-2

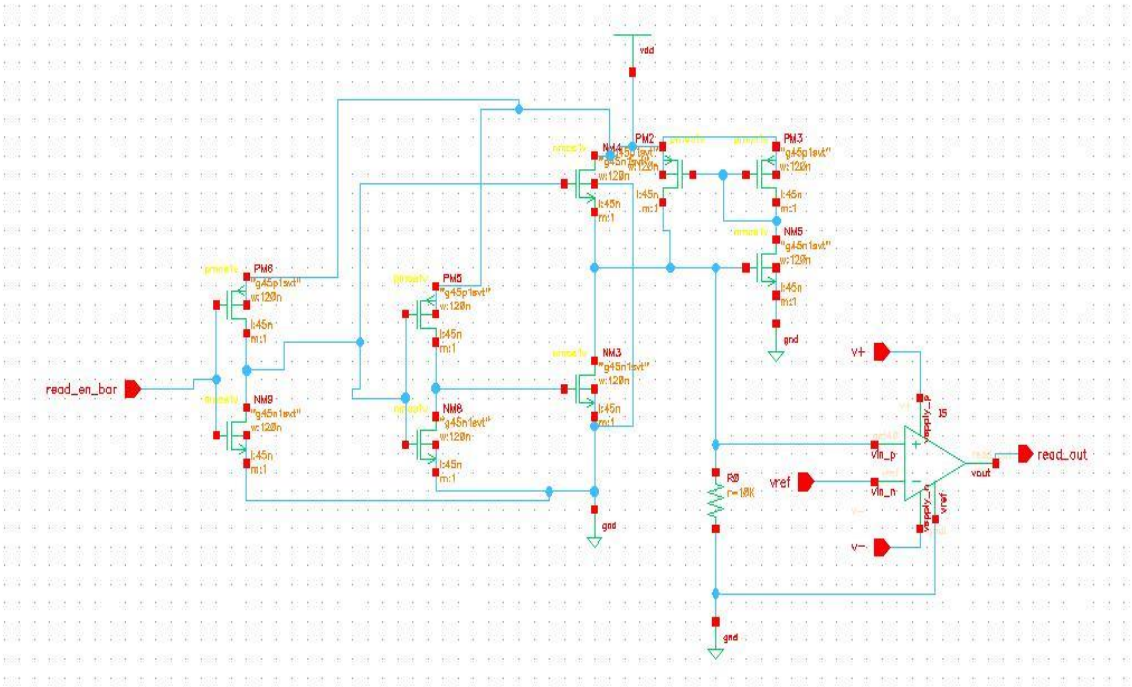

Figure: Schematic for topology2

In this sense amplifier, Resistor is taken in place of magnetic tunnel junction(MJT) block. For anti parallel state and parallel state resistance's values are 10k ohms and 5k ohms respectively. Current generated by current generation circuit will flow through resistance. Voltage across the resistance and vref voltage will be compared by amplifier. According to the difference between that voltage, amplifier will give the output.

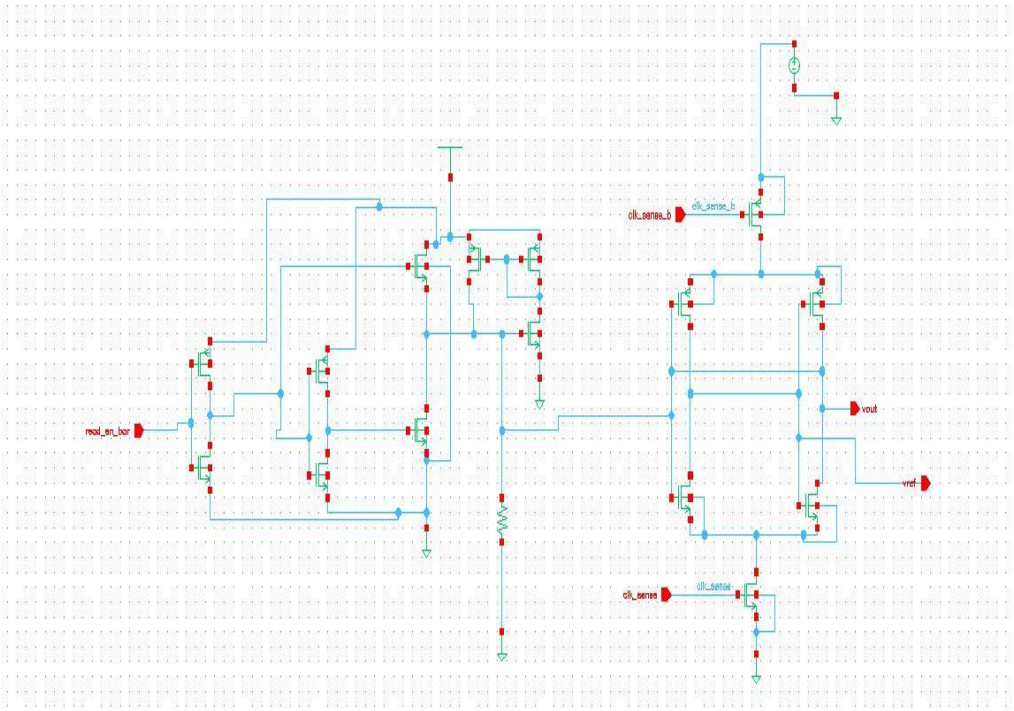

Figure: Schematic for topology2 with amplifier

Here back to back connected inverter are used as amplifier. This topology gives good read margin but current flowing through the resistance is higher than threshold current during read operation. So there will be accidental write operation during read operation.

3)Topology:-3

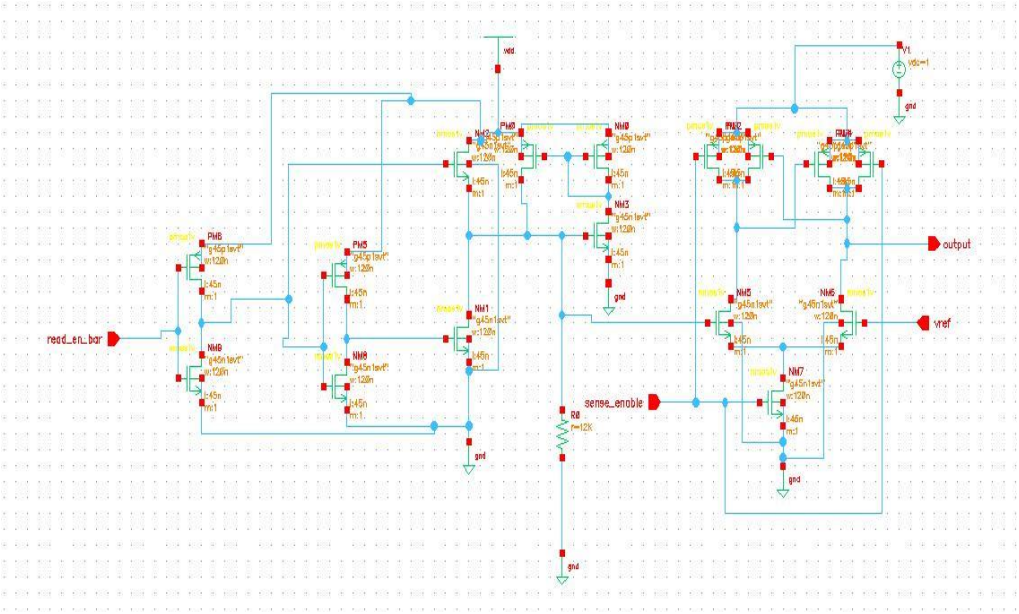

Figure: Schematic for topology3

In this sense amplifier, pmos back to back connected load amplifier is used for generating the output according to difference between voltage across resistance and vref voltage. This sense amplifier gives good read margin. In this topology, there is no chances of accidental write operation because current flowing through resistance is very less during read operation. Bandwidth of the circuit is around 25 KHz.

Input parameters:-

Vdd= 0.5 volt.

Vref= 4.195m volt.

Vdc= 1 volt.

MJT resistance = 5k ohm and 10k ohm

MTJ resistance(ohm)	Output voltage(volt.)	Power consumption(W)
5k	655m	280n
10k	1	277n

1) Pre layout simulation :-

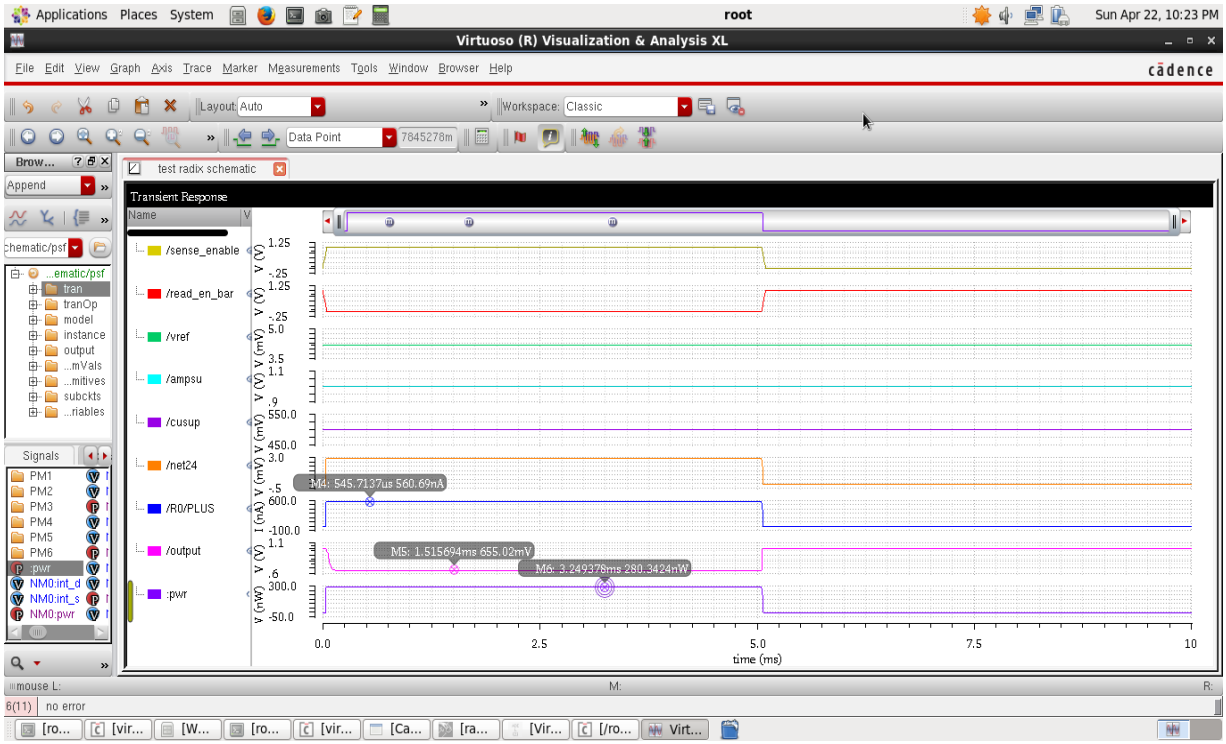

Figure: Waveforms of 5k ohm resistance

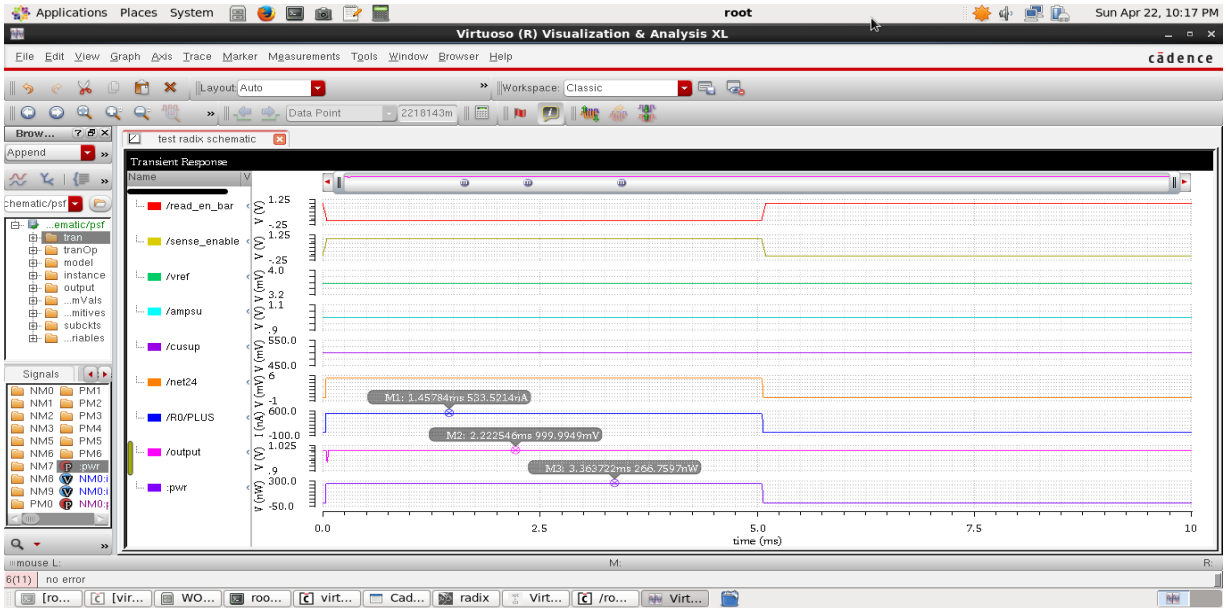

Figure: Waveforms for 10k ohm resistance

2) Layout of topology:-3

For drawing the layout, Resistor will be designed using transistor in the sense amplifier.

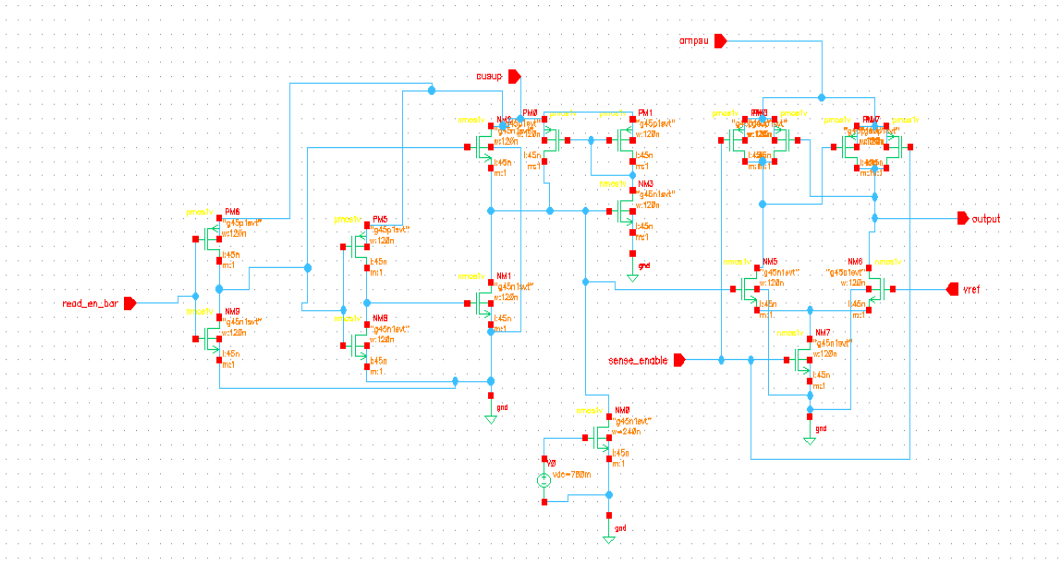

Figure: Schematic for 5k ohm

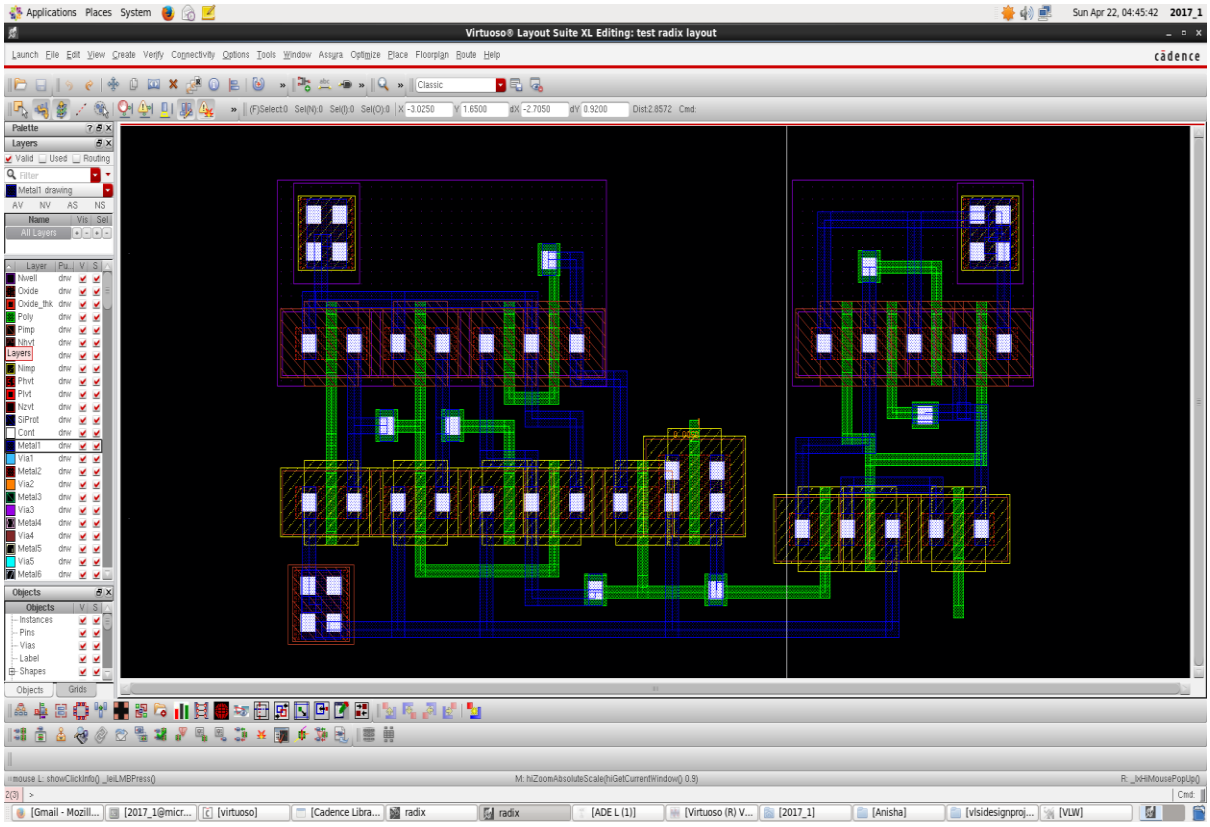

Figure: layout for 5k ohm

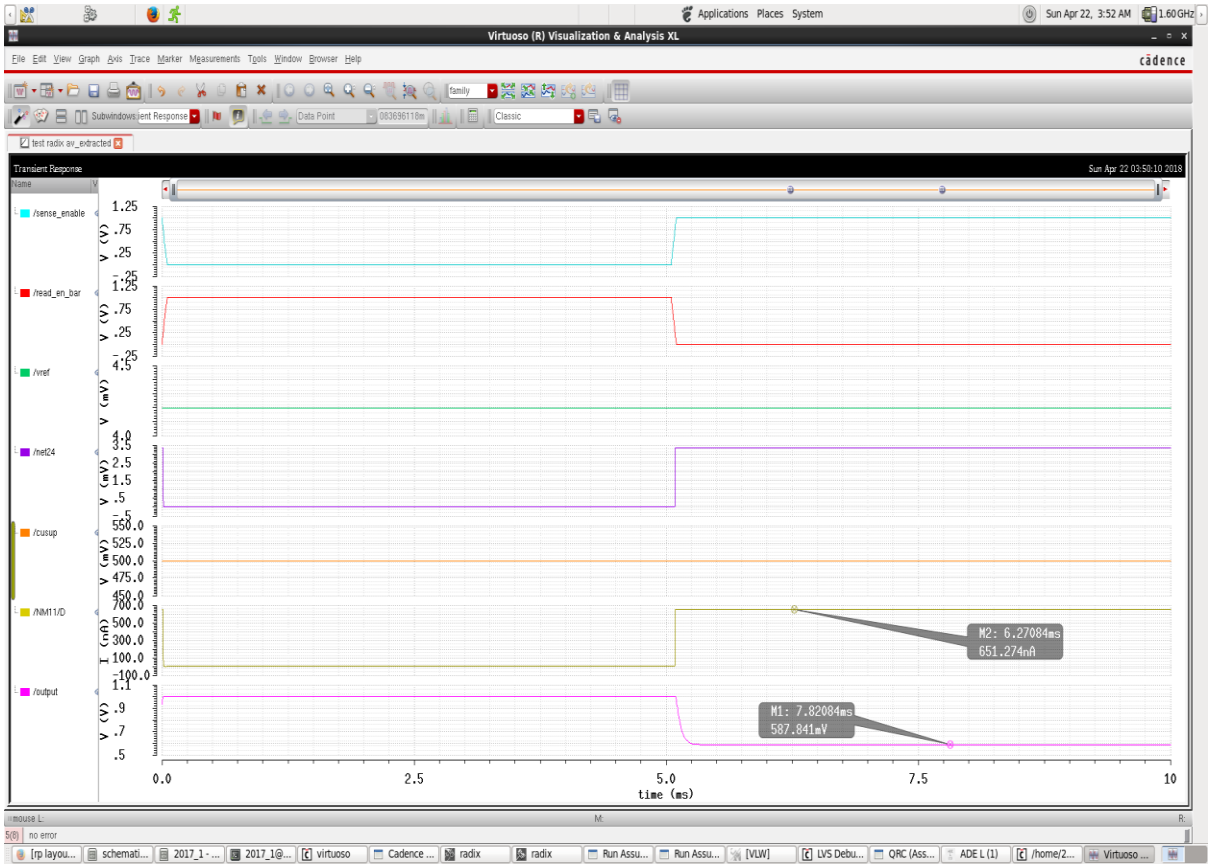

Figure: Waveforms for 5k ohm resistance

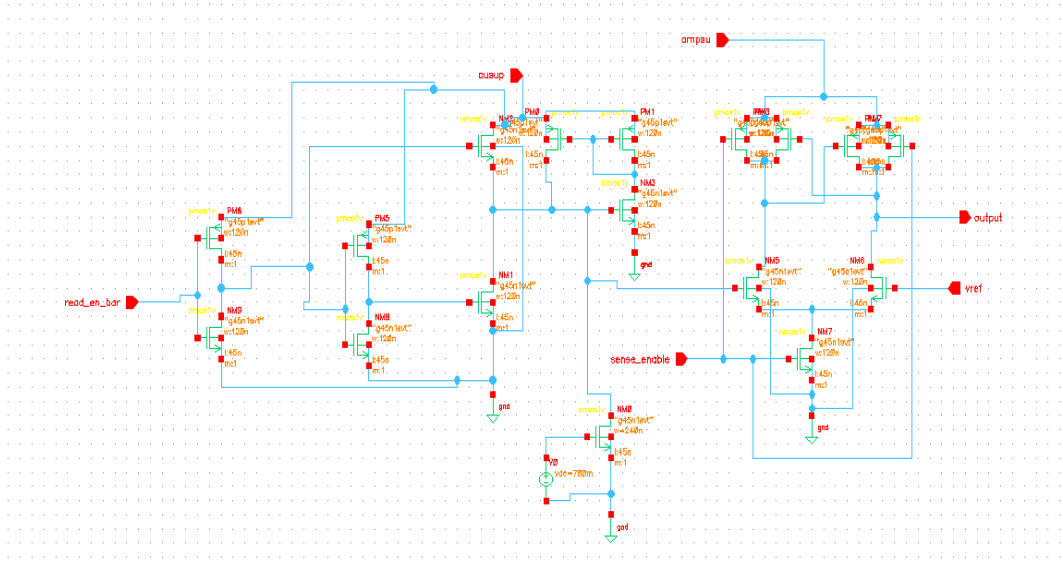

Figure: Schematic for 10k ohm

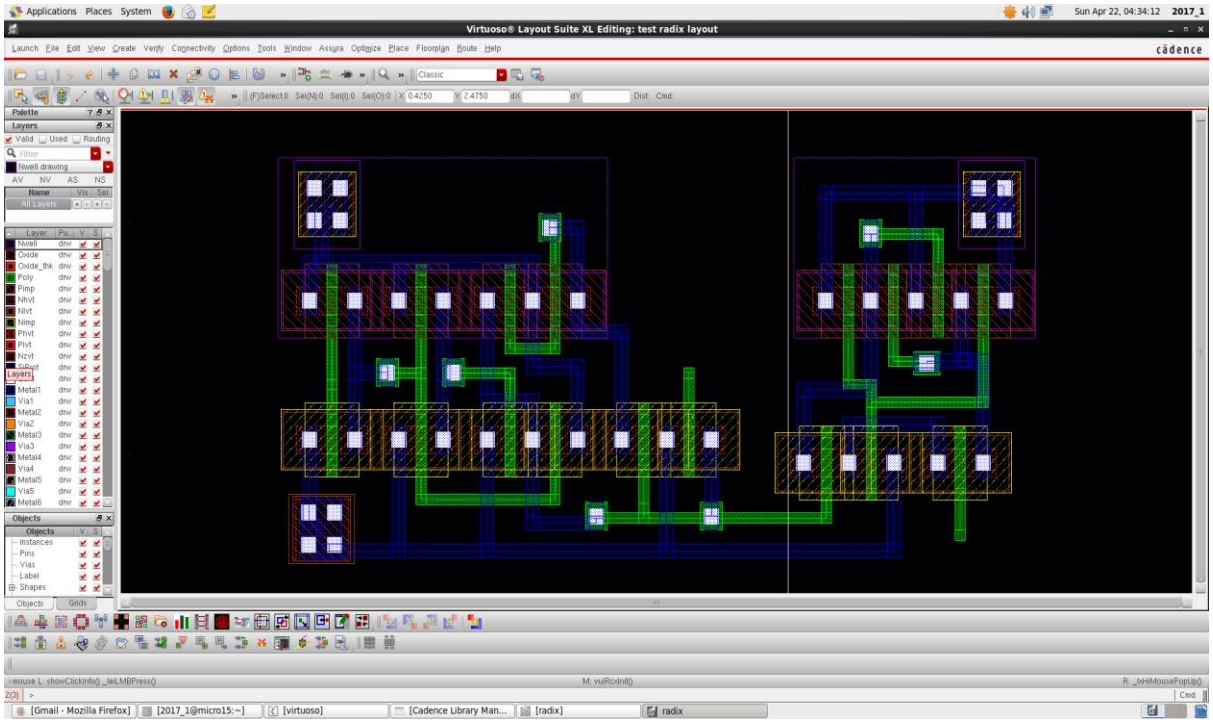

Figure: layout for 10k ohm

Figure: Waveforms for 10k ohm resistance

MTJ resistance (ohm)	Output voltage(volt.)	Power consumption(w)
5k	587m	289n
10k	1	282n

4) topology:- 4

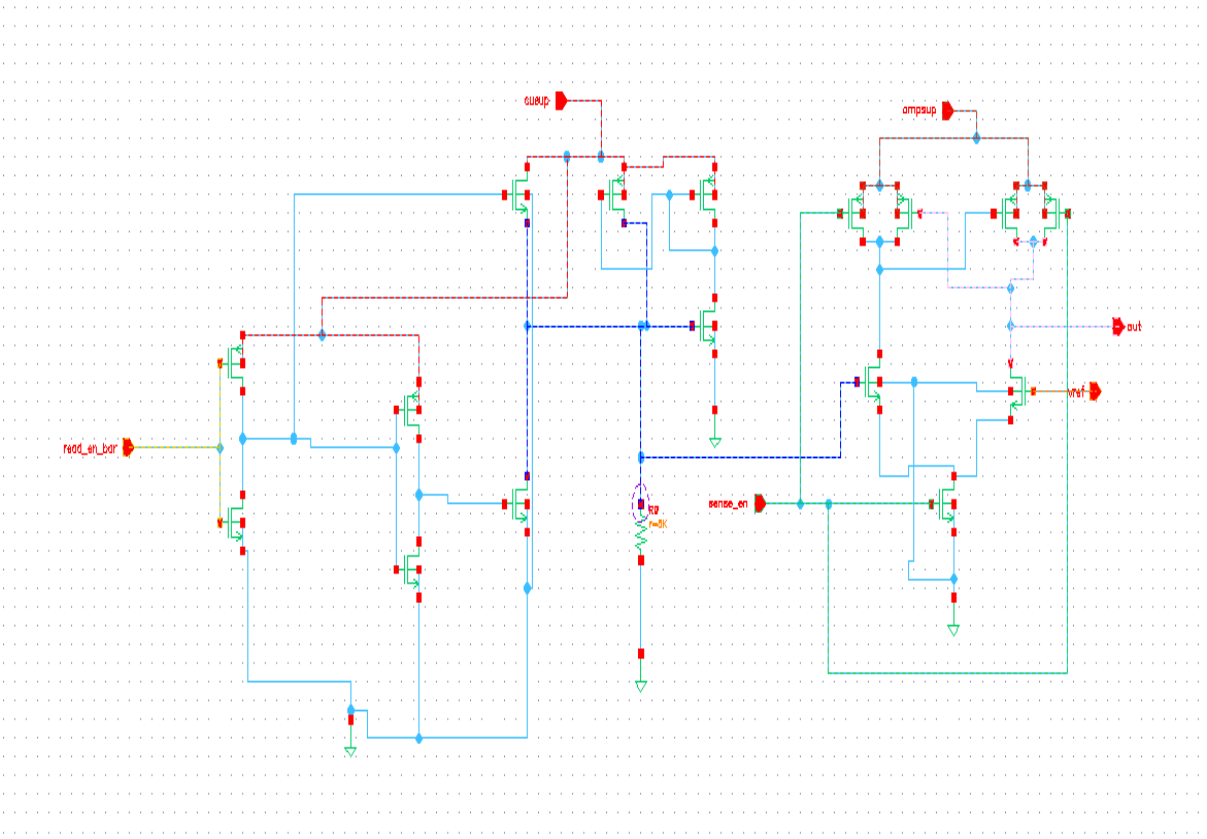

Figure: Schematic for 5k ohm

This topology is same as topology 3 but this topology is designed using the finfet 15 nm technology. Input stimuli kept same as cmos technology. In this sense amplifier, bandwidth is around 2MHz and read margin is around 0.6 V.

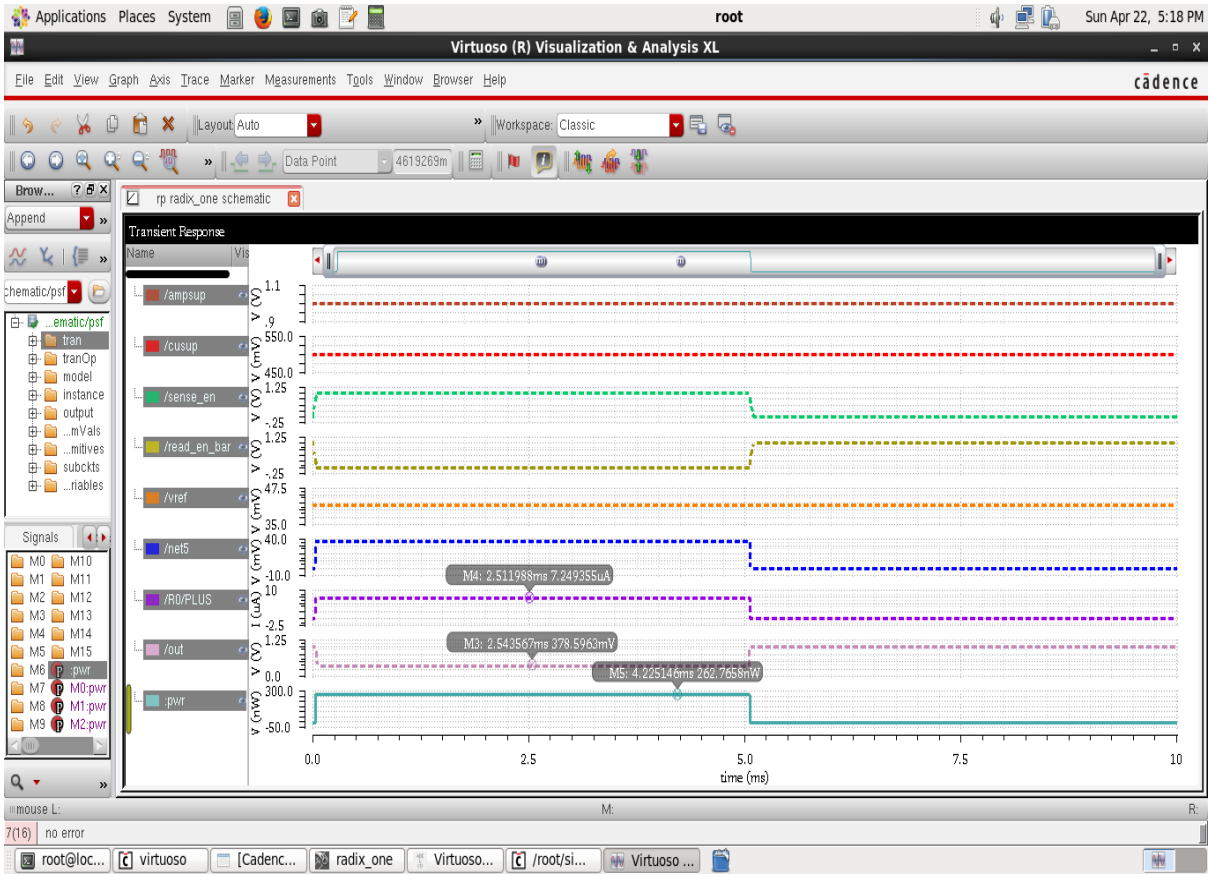

Figure: Waveforms for 5k ohm resistance

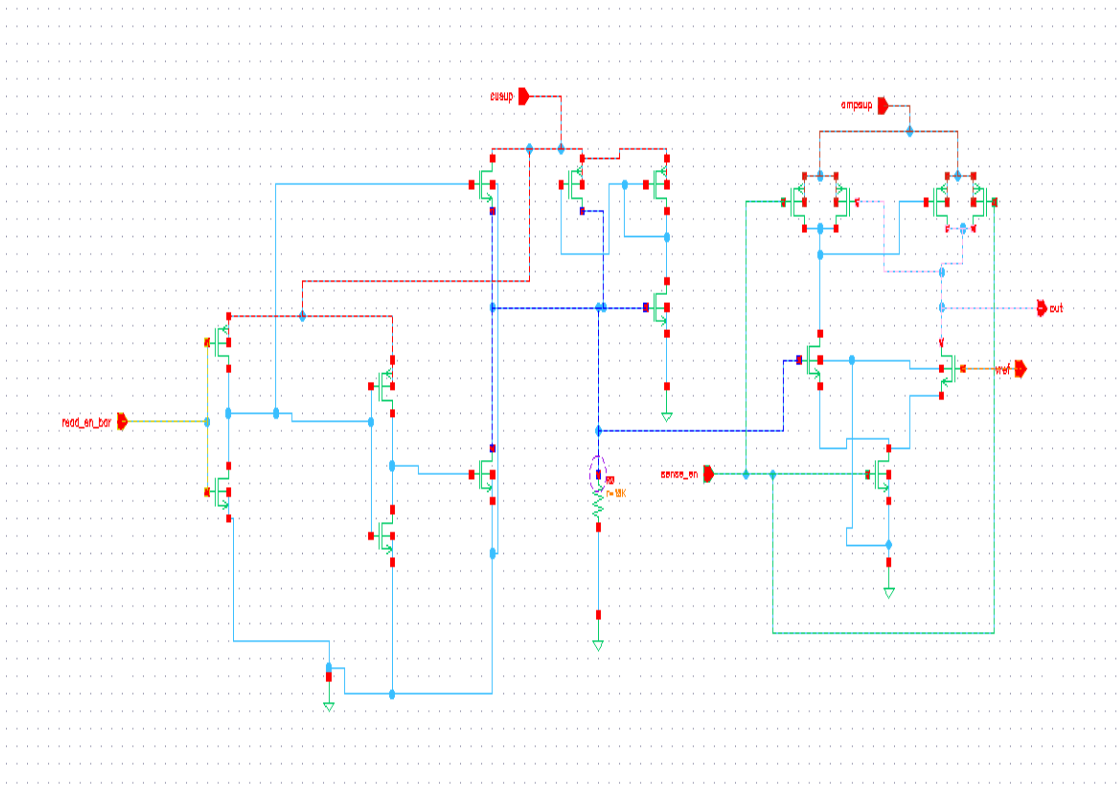

Figure: Schematic for 10k ohm

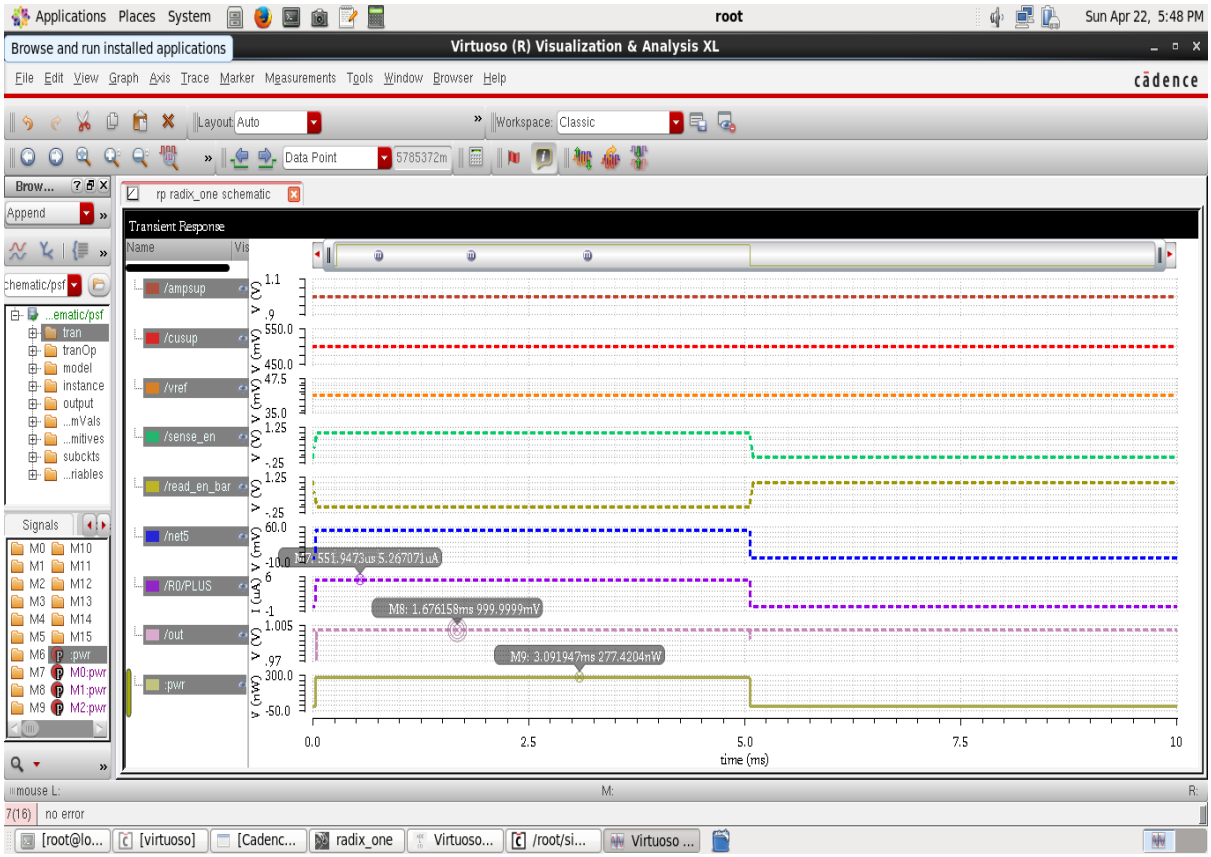

Figure: Waveform for 10k ohm resistance

MJT resistance	Output voltage	Power consumption
5k ohm	378 mV	262 nW
10k ohm	1 V	277 nW

Conclusion :-

Because of the finfet characteristics, read margin and speed of the circuit are better than the other topologies which is designed using cmos technology.

	Read margin	Bandwidth
Topology3	0.345 V	25 KHz
Topology4	0.622 V	2 MHz

Due to the presence of two gate terminals, power dissipation is more in FinFET but that can be reduced by scaling down the power supply with gate length. But in topology 4(using Finfet tech.), power consumption are almost same as topology3(using cmos tech.) for the same stimuli. Henceforth FinFET bids to be a frontrunner in adapting an alternative technology to MOSFET to substitute the device in the nanometre regime where MOSFETs encounter short channel effects.

References :-

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- Self-Timed Read and Write Operations in STT-MRAM Rajendra Bishnoi, Fabian Oboril, Mojtaba Ebrahimi, and Mehdi B. Tahoori, Senior Member, IEEE transaction on very large scale (VLSI) system, VOL. 24, NO. 5, MAY 2016