ADDV Assignment-2 (2025)

Objective

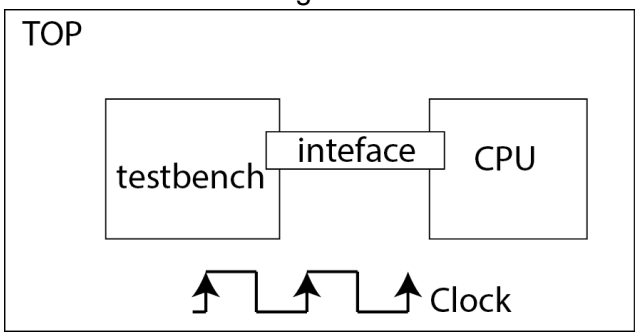
The objective of this assignment is to gain hands-on experience on functional verification using coverage-driven constrained-random testing and SystemVerilog Assertions

Instructions

- Each group will submit only one zipped folder
- The zipped folder will contain files mentioned in the **Question** section below.
- Demo will be taken and marks of student in the same group may vary depending on the effort and understanding of individual
- **Copying/Plagiarism is strictly prohibited. Institute copying/plagiarism policy will apply with no exception.**

Question

1. Using **ChatGPT or any LLM**: Generate Verilog codes for a CPU with a 10-15 instructions. Report the screenshot of the prompts and the generated code.
2. Create a SystemVerilog testbench to functionally test the above CPU as shown below with the following features.



   a. At the TOP: interface, testbench and CPU must be instantiated
   b. Testbench should be implemented as program and contain the above interface
   c. Testbench program should be connected to CPU module in the TOP module using the above interface (CPU can have interface or it can be a purely Verilog model with ports).
   d. The interface should have synchronous signals defined with respect to a clocking block
   e. Clock should be generated in the module TOP
   f. A coverage model should be defined for the CPU (you may define coverpoints and bins appropriately)

    g. The testbench program should generate random stimuli

3. Perform simulation of the above testbench using any tool and carry out functional coverage analysis. Report the results and your analysis.
4. Constrain the random stimuli generation in step 2 and improve the coverage from what you obtained in step 3. Report the results and your analysis.
5. Write SVA (you may write as many assertions as you want) that ensures that:
    a. All instructions get executed in Maximum 5 clock cycles
    b. Run the above SVA using Jasper or any formal analysis tool and report the result (It is OK to have failures and unsolved assertions. You need not try to fix them. You need to analyze and provide an explanation of the result).