EE 105: **Semiconductor Devices**
Resources and Worksheets

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Contents

1 Online resources (expanded)

Below is a curated list of quality online resources that you may find helpful for learning, exploring, and practicing a variety of concepts related to semiconductor devices.

1.1 Tutorials and reference websites

- **All About Circuits**: This website features extensive text-based tutorials that cover DC/AC circuits, semiconductor devices, and more. Every topic also includes a forum at the bottom of the page where students can ask questions and interact with the community to give and receive help. A comprehensive, hyperlinked table of contents on semiconductor devices is available here, and an online textbook on analog devices may be found here, with a corresponding table of contents toward the bottom of the page. For additional practice, select a topic to explore and challenge yourself in the Worksheets section.
- **Electronics-Tutorials** (*corrected hyperlink*): This is a fantastic organized collection of tutorials covering a myriad of topics in circuits with tons of diagrams and worked-out examples featuring step-by-step derivations. For semiconductor devices, relevant sections include semiconductor basics, diodes, and transistors.
- **Khan Academy**: Features a collection of short video lessons and practice problems on the fundamentals of circuit basics, signals, and systems with a user-friendly approach suitable for beginners. In regard to semiconductor devices, a set of video lectures on diodes may be found here.
- **LibreTexts**: LibreTexts is a fantastic online textbook resource for a variety of topics, including theory and worked out examples. A section on the basic physics concepts behind semiconductor devices may be found here, while a set of general textbook modules on semiconductors, including band theory, extrinsic vs. intrinsic semiconductors, metal-oxide-semiconductors (MOS), and diodes, may be found here.
- **MIT OpenCourseWare (OCW)**: Free, self-paced course materials available from MIT, including detailed lecture notes, problem sets, exams with solutions, and video lectures. For semiconductor devices, courses **6.002** (*Circuits and Electronics*, link here) and **6.012** (*Microelectronic Devices and Circuits*, links here, here, and here).
- **Selected problems by BarcelonaTech**: A collection of solved examples on semiconductor and electronic device physics, suitable for practice and deeper understanding.
- **Wikipedia**: A great resource for introductory and surface-level overviews of topics related to electronics and semiconductor devices. Examples of entries relevant to semiconductor devices include MOSFET, CMOS, and subthreshold conduction.

1.2 Simulation tools

- **Tinkercad Circuits**: A browser-based circuit design and simulation tool from Autodesk. This is a great tool for beginners to visualize and interact with circuits in a simulated fashion. It includes basic electronic components, measurement tools, and real-time simulation. For some introductory tutorials to get you started, check out the official playlist on YouTube.
- **Falstad Circuit Simulator**: A web-based real-time simulation interface with helpful visualizations of voltages and currents which allows students to see waveforms change dynamically. A large variety of preset examples (such as RLC circuits, op-amps, and digital logic circuits) are included for students to explore with a user-friendly drag-and-drop interface.
- **LTspice**: An excellent freeware circuit simulator developed by Analog Devices which is widely used in both academia and industry. It has a slightly steeper learning curve than the other simulators but it is capable of simulating many different types of complex circuits, making it a useful tool for learning schematic capture, waveform analysis, and advanced circuit behavior. For some introductory tutorials to get started, check out the following YouTube tutorial playlist.
- **PhET Simulations**: For absolute beginners who are particularly visual learners and are looking for hands-on learning to aid conceptual understanding, this website includes many interactive demos and simulation tools for DC and AC circuit basics. Students are able to manipulate variables in real time (e.g., resistor values, battery voltage, etc.) and see immediate effects.

- **CircuitLab**: Another browser-based circuit simulator with built-in analysis tools. Featuring a library of example circuits, it can be useful for practicing circuit design and learning how measurement tools work, such as oscilloscopes.

1.3 Discussion and forum communities

- **Electronics Stack Exchange**: A Q&A format discussion forum with a broad community of hobbyists, students, and professionals. It can be a great resource for well-structured answers to specific, technical circuit questions.
- **r/ElectricalEngineering**: An electrical engineering subreddit forum featuring discussions on coursework, textbooks, career advice, and circuit troubleshotting. It can be a good place to ask questions and see how others approach similar problems.

2 Brief overview of semiconductor devices

A semiconductor device is any electronic component made from semiconductor materials (typically silicon, but also germanium, gallium arsenide, etc.) that exploit the material's unique electrical properties—namely, that its conductivity can be controlled and varied between that of a conductor (metal) and an insulator. Semiconductor devices underpin all modern electronics, from diodes to transistors and integrated circuits, enabling logic operations, amplification, and signal processing in everything from computers to smartphones. This section covers a basic overview of semiconductor devices and the concepts that form their foundation.

2.1 Semiconductors vs. Conductors and Insulators

- **Conductors** (e.g., metals) have a large number of free charge carriers (electrons) available for conduction, resulting in low resistance.
- **Insulators** have very few free charge carriers and high resistance.
- **Semiconductors** lie in between: in their pure (intrinsic) form, they have moderate conductivity. Crucially, *doping* and external factors (like electric fields, temperature, and light) can modify this conductivity dramatically.

2.2 Doping (n-type and p-type)

- **Intrinsic semiconductor**: Pure crystal (e.g., pure silicon) with relatively few charge carriers (electrons/holes).
- **Doping**: Adding small amounts of impurity atoms to control the number and type of charge carriers:
  - **n-type doping**: Introduces extra electrons (negative charges). A common dopant for silicon is phosphorus or arsenic, which adds free electrons to the conduction band.
  - **p-type doping**: Creates "holes" (positively charged carriers). A common dopant is boron, which introduces deficiencies of electrons in the valence band (thus creating holes).

2.3 Electrons, Holes, and Energy Bands

- In a crystalline semiconductor, *electrons* occupy allowed energy bands (valence band, conduction band) separated by a band gap.
- **Conduction band**: Electrons in this band are free to move and conduct current.
- **Valence band**: Electrons here are bound to atoms and not free to conduct.
- **Band gap**: Energy difference between the valence band and conduction band. In semiconductors, this gap is small enough ($\sim$1 eV for silicon) that electrons (or holes) can be excited into conduction by doping or applied voltages.

2.4 The p–n Junction (Diode)

- A **p–n junction** forms when p-type and n-type regions meet in a single crystal.
- At the junction, electrons diffuse from n-type to p-type and holes diffuse from p-type to n-type, creating a **depletion region**.
- **Diodes** exploit this junction to allow current to flow primarily in one direction:
  - **Forward bias** (p-side positive relative to n-side) lets current flow easily.
  - **Reverse bias** blocks current, aside from a small leakage, until breakdown at a high reverse voltage.

2.5 Transistors

Transistors are the fundamental building blocks of modern electronics, acting as switches or amplifiers. They come in several types:

1. **Bipolar Junction Transistor (BJT)**
   - Made of p–n–p or n–p–n layers.
   - Current flows between the collector and emitter, controlled by the base current.

- Used historically in amplifiers and logic circuits, now often found in analog/low-power applications.

2. **Field-Effect Transistor (FET)**
   - Controlled by an electric field rather than base current.
   - **MOSFET** (Metal–Oxide–Semiconductor FET) is the most widely used transistor in modern digital circuits.
   - Has three terminals: Gate, Source, Drain (with a Body or Substrate often tied to a reference).
   - A gate voltage modulates a conductive channel that either allows or blocks current between source and drain.
     - **NMOS**: Channel formed by electrons, activated by a positive gate voltage.
     - **PMOS**: Channel formed by holes, activated by a negative gate voltage.
     - **CMOS** (Complementary MOS) combines NMOS and PMOS devices for efficient logic design (very low power consumption).

2.6 Threshold and Sub-Threshold (MOSFET Focus)

- **Threshold voltage** (V_{th}): The minimum gate-to-source voltage (for enhancement-mode MOSFETs) needed to form an inversion layer (conductive channel).
- **Above threshold**: The MOSFET behaves like a voltage-controlled current source or, in linear region, a resistor whose value depends on gate voltage.
- **Sub-threshold**: When $V_{\text{GS}} < V_{\text{th}}$, a small exponential current flows. In modern ultra-low-power applications, sub-threshold operation is sometimes exploited deliberately.

2.7 Why Semiconductor Devices Matter

1. **Applications**
   - **Logic Gates**: CMOS technology (using NMOS and PMOS transistors) underpins nearly all modern digital ICs (microprocessors, memory chips).
   - **Analog Circuits**: Transistors used as amplifiers, current sources, mixers, oscillators, etc.
   - **Power Electronics**: High-voltage devices (MOSFETs, IGBTs) in motor drives, power supplies, electric vehicles.
   - **Optoelectronics**: Semiconductor diodes and transistors can emit or detect light (LEDs, laser diodes, photodiodes).
2. **Importance**
   - **Scalability**: Continual transistor shrinking in integrated circuits (Moore's law) drives exponential increases in computing power.
   - **Versatility**: By controlling doping profiles, geometries, and materials, engineers tailor semiconductors for everything from tiny ultra-low-power sensors to high-power industrial inverters.
   - **Innovation Driver**: Semiconductors enable modern communications, computing, automotive electronics, renewable energy systems, and more.

2.8 Summary

1. **Semiconductors** are materials whose electrical conductivity can be precisely controlled via doping and electric fields.
2. **Diodes** and **transistors** are the two cornerstone devices:
   - **Diodes** allow current in one direction and form the basis of rectifiers, regulators, and many sensor circuits.
   - **Transistors** (BJT, MOSFET, etc.) act as switches and amplifiers; MOSFETs dominate modern digital circuits due to efficiency and scalability.
3. **Threshold voltage** and **sub-threshold conduction** are vital to understanding power consumption and switching behavior in MOSFET-based circuits.
4. **CMOS** (complementary MOS) technology combines NMOS and PMOS transistors for highly efficient digital logic, minimizing static power consumption.

By mastering these fundamentals—band theory, doping, p–n junctions, diode equations, MOSFET operation modes—you gain the foundation to tackle more advanced topics like integrated circuit design, analog/mixed-signal systems, and emerging semiconductor technologies.

3 Resistivity in semiconductor devices

A **resistor** is usually viewed as a simple, linear circuit element where current and voltage maintain a proportional relationship (Ohm's Law: $V = IR$). However, many **semiconductor devices** can behave like *non-linear* or *tunable* resistors, meaning their resistance changes with applied voltage, current, temperature, or other factors. Below is an overview of the following listed topics along with how these concepts manifest in semiconductor devices:

1. **Non-Linear Resistors** (e.g., diodes, varistors, thermistors, etc.)
2. **Tunable Resistors** (e.g., FETs in the "triode" region, digital potentiometers, special doping structures)
3. **Typical Applications** in circuits.
4. **Wire resistance formula**
5. **Resistivity**
6. **Carrier density**

3.1 Non-Linear Resistors

A **non-linear resistor** is any device whose voltage–current (V–I) relationship is not simply a straight line. In other words, its resistance ($R = V/I$) changes depending on the voltage across it or the current passing through it.

3.1.1 Common Examples

The following elements fall under *non-linear* because their operating principle involves changes in carrier concentration, doping behavior, or conduction mechanisms that vary as voltage, current, temperature, or light changes.

1. **Diodes**
   - **p–n junction diodes** exhibit a very non-linear V–I characteristic: negligible current below a certain forward voltage (0.7 V for silicon), and then exponential growth of current above that voltage.
   - Diodes in **reverse bias** pass only leakage current until breakdown occurs at a high reverse voltage.
2. **Varistor** (Voltage-Dependent Resistor, MOV)
   - Primarily used for **surge protection**.
   - Exhibits very high resistance up to a certain "clamping" voltage, then rapidly decreases its resistance to clamp high-voltage transients (e.g., lightning surges).
3. **Thermistor** (Temperature-Dependent Resistor)
   - Resistance changes significantly with temperature.
   - **NTC** (Negative Temperature Coefficient) thermistors decrease in resistance with increasing temperature; used in temperature sensing or inrush current limiting.
   - **PTC** (Positive Temperature Coefficient) thermistors increase in resistance with temperature; used in over-current protection.
4. **Photoresistor** (Light-Dependent Resistor, LDR)
   - Semiconducting material (like CdS) whose resistance decreases with higher light intensity.
   - Widely used in light sensors, automatic night lights, etc.

3.2 Tunable (Voltage-Controlled) Resistors

A *tunable resistor* is a device whose effective resistance can be actively controlled, typically by an external voltage or current. The simplest forms use semiconductor transistor devices (FETs) operated in certain bias regions to mimic a variable resistor.

3.2.1 Common Implementations

1. **MOSFET in Triode (Linear) Region**
   - In the low ($V_{DS} < V_{GS} - V_{th}$) region, a MOSFET behaves like a resistor whose value depends on the gate voltage V_{GS}.
   - By adjusting V_{GS}, you effectively "tune" the channel conductivity, changing the on-resistance r_{on}.
   - Used in analog circuits for voltage-controlled resistors or "electronic potentiometers."
   - Also found in some filter circuits, amplitude modulators, or gain stages requiring variable resistance.
2. **JFET as a Voltage-Controlled Resistor**
   - Similar principle but controlled by the gate–source voltage in a junction field-effect transistor.
   - Common in older or simpler designs before MOSFETs became prevalent.
3. **Digital Potentiometers (DigiPots)**
   - Typically implemented with *CMOS switch arrays* internally, stepping between discrete resistor taps.
   - Controlled via a digital interface (SPI, I^2C).
   - Often used where a microcontroller sets an analog level (e.g., volume control, calibration).
4. **Special Doping Structures / MEMS**
   - Certain advanced processes create doping gradients or micro-electromechanical (MEMS) variable resistors.
   - Applications might include sensor calibration, precision tuning, etc.

3.3 Summary of non-linear and tunable resistors

Tunable and non-linear resistors expand the functionality of basic resistive elements by leveraging *semiconductor properties*—such as carrier concentration, doping profiles, and gate voltages—to produce devices with voltage-/current-dependent resistance. From thermistors and varistors (passive, non-linear resistors) to actively controlled MOSFET-based variable resistors, these components appear in countless circuit applications: sensor reading, dynamic filtering, gain control, and overvoltage protection. Understanding their operation and limitations is a core part of designing robust, versatile electronic systems.

3.3.1 Use of non-linear/tunable resistors in semiconductor devices

1. **Wave Shaping and Clamping**
   - Non-linear resistors such as diodes and varistors clamp or shape waveforms.
   - Surge protectors (MOVs) protect circuits from high-voltage spikes.
2. **Sensing and Feedback**
   - Thermistors measure temperature; LDRs measure light.
   - These resistors often form part of a *voltage divider*, producing an output voltage that indicates the sensed parameter (temp or light).
3. **Filters and Signal Processing**
   - Tunable resistors (FETs in the triode region) create *voltage-controlled filters* or amplitude modulators.
   - Analog multipliers or variable gain amplifiers can incorporate a MOSFET-based resistor to set gain dynamically.
4. **Automatic Gain Control (AGC)**
   - Some designs use a FET as a dynamic resistor in the feedback path of an amplifier, controlling gain in response to signal amplitude.
5. **Calibration and Trimming**
   - Circuits might include a digitally adjustable resistor (a "digital pot") for fine-tuning or trimming offsets, calibrations, or bias currents post-manufacturing.

6. **Low-Power Applications**
   - Sub-threshold MOSFET operation can act as a very high-value tunable resistor, sometimes leveraged in ultra-low-power analog circuits.

3.3.2 Key points to remember

- **Non-Linear Resistive Elements**
  - Have I–V characteristics that deviate from a straight line (Ohm's Law is no longer a single constant ratio).
  - Often used for protection, sensor interfaces, or waveform shaping.
- **Tunable Resistors**
  - Usually implemented with transistors (FETs, JFETs) or digital resistor arrays.
  - Provide a voltage or digitally controlled resistance, crucial for adaptive circuits, filters, or user-adjustable functions.
- **Advantages**
  - Offer dynamic control over circuit behavior (gain, filtering, sense thresholds) without physically swapping components.
  - Enable miniaturization and integration, particularly in large-scale or microelectronic systems.
- **Considerations**
  - Non-linearities can cause distortion if not managed (important in analog signal paths).
  - Temperature dependence and parasitics can influence accuracy, especially at small geometries or low currents.
  - Maximum current/voltage ratings must be observed (e.g., MOVs for surges, FET-based tunable resistors for device safe operating area).

3.4 Resistivity

Resistivity (ρ) is an intrinsic material property that describes how strongly the material opposes current flow. It is independent of the physical dimensions of a sample and depends instead on material composition, temperature, and impurity/defect levels.

- Low $\rho \rightarrow$ "Good conductor" (e.g., metals like copper or aluminum).
- High $\rho \rightarrow$ "Poor conductor" or insulator (e.g., glass, ceramics).
- Semiconductors (like silicon) have ρ values between those of conductors and insulators.

In *semiconductor materials* (e.g., silicon, germanium, gallium arsenide):

- Resistivity is highly temperature-dependent.
- Adding **dopants** (e.g., phosphorus, boron) changes carrier concentration, drastically altering resistivity.
- Semiconductors can be *tuned* to have very high or moderate conductivity by controlling doping levels, giving them tremendous versatility in electronic devices.

3.5 Wire Resistance Formula

For a uniform, cylindrical wire of length L and cross-sectional area A, made from a material with resistivity ρ, the *resistance* R is:

$$\boxed{R = \frac{\rho\, L}{A}}.$$

- R: Resistance (in ohms, Ω).
- ρ: Resistivity of the material (in $\Omega \cdot \text{m}$ or $\Omega \cdot \text{cm}$). A *lower-resistivity* material (ρ smaller) *lowers* resistance.

- L: Length of the wire (m, cm, etc.). A *longer* wire (L is large) *increases* resistance.
- A: Cross-sectional area (m^2, cm^2, etc.). A *thicker* wire (A is large) *lowers* resistance.

As an example, copper wires have $\rho \approx 1.68 \times 10^{-8}\,\Omega \cdot \text{m}$. This low resistivity means copper is an excellent conductor, so short, thick copper wires have very low resistance and minimal power loss.

3.6 Carrier Density

3.6.1 Electrons vs. Holes

In a semiconductor, two types of **charge carriers** typically dominate conduction:

1. **Electrons** in the conduction band (negatively charged).
2. **Holes** in the valence band (effectively positively charged "vacancies" where an electron is missing).

3.6.2 Intrinsic vs. Extrinsic Carrier Density

1. Intrinsic Carrier Density (n_i)
   - The number of electrons (and holes) in a pure, undoped semiconductor due to thermal energy alone.
   - For silicon at room temperature (300 K), $n_i \approx 10^{10}\,\text{cm}^{-3}$.
2. Extrinsic Carrier Density
   - Achieved by **doping** the semiconductor with donor (n-type) or acceptor (p-type) impurities, which increases either electron or hole concentrations.
   - If N_D (donor concentration) $\gg n_i$, then $n \approx N_D$ (for n-type).
   - If N_A (acceptor concentration) $\gg n_i$, then $p \approx N_A$ (for p-type).

3.6.3 Impact on Resistivity

The *resistivity* of a semiconductor ρ is inversely related to the *carrier concentration* (n or p) and **mobility** (μ):

$$\sigma = \frac{1}{\rho} = q\,(n\mu_n + p\mu_p),$$

where:

- σ = conductivity,
- q = electron charge ($\approx 1.602 \times 10^{-19}$ C),
- μ_n, μ_p = electron and hole mobilities, respectively.

Key Point: Increasing the doping (and thus carrier density) typically lowers the semiconductor's resistivity, making it more conductive.

3.7 Applications to Semiconductor Devices

1. Interconnects and Metal Layers (Wires On-Chip)
   - In integrated circuits (ICs), "wires" are often metal interconnect layers (e.g., aluminum, copper). Designers calculate line resistance using $R = \rho L/A$ to ensure signal integrity and manage power dissipation.
   - As device dimensions shrink (in advanced technology nodes), wire thickness and width also reduce, which can *increase* resistance and lead to design challenges (e.g., RC delays).
2. Resistors On-Chip
   - Sometimes **poly-silicon** (heavily doped) or **diffused** regions in silicon are used as on-chip resistors.
   - Their resistivity depends on doping, which can be adjusted to achieve a target resistance.

3. p–n Junctions and Diodes
   - The **resistivity** and doping levels in p- and n-regions define *depletion region* widths, junction barriers, and diode I–V characteristics.
   - Carrier densities influence forward current magnitude ($I \propto e^V$ in diode equations).
4. Transistors (MOSFETs, BJTs)
   - **MOSFET** conduction: The *channel* between source and drain forms (or doesn't form) depending on the gate voltage. The channel's effective resistivity (and thus current) can be tuned by doping profiles and gate fields.
   - **BJT** conduction: Depends on doping gradients in the emitter, base, and collector. Carrier densities in each region determine the current gain and saturation/forward-active characteristics.
5. Power Devices
   - **High-power semiconductors** (e.g., IGBTs, power MOSFETs) use doping profiles carefully engineered to handle large currents while maintaining a certain ρ or breakdown voltage.

3.7.1 Key Takeaways

1. **Wire Resistance Formula**: $R = \frac{\rho L}{A}$ is fundamental for *conductors*, but also shows up in *semiconductor* "wires" or resistors fabricated on chips, where dimensions and resistivity are carefully controlled.
2. **Resistivity**: Intrinsic property of a material, dependent on *material structure, temperature, doping.* Metals have very low resistivity; insulators have very high; *semiconductors* can vary over a wide range.
3. **Carrier Density**:
   - Determines how many free electrons/holes are available for conduction.
   - **Doping** manipulates carrier density and thus *conductivity.*
   - Intrinsic vs. extrinsic doping heavily affects the *device operation region* (e.g., conduction, depletion, inversion).
4. **Device Application**: All these concepts—resistance, resistivity, carrier density—come together in p–n junctions, transistor channels, interconnects, and on-chip resistors, influencing design trade-offs, device speed, power dissipation, and scalability.

In summary, **wire resistance** is a classical formula that underpins how interconnects and on-chip resistors behave electrically. **Resistivity** is the intrinsic property that sets a baseline for conduction or insulation, and **carrier density** is the handle by which semiconductor device engineers tune conduction characteristics—giving semiconductors the unique "variable conductivity" property central to modern electronics.

4 Semiconductor physics and diodes

Electrons, holes, energy bands, and band gaps form the foundation of semiconductor physics. They explain how materials like silicon, germanium, or gallium arsenide can act as conductors, insulators, or lie in-between — as semiconductors — depending on temperature, doping, and applied fields. Below is a basic overview of these concepts and how they underlie modern semiconductor devices.

4.1 Energy Bands in Solids

4.1.1 Formation of Bands

In a solid, each atom's electron orbitals overlap with those of neighboring atoms, forming **bands** of allowed energy levels:

- **Valence Band (VB)**: Lower-energy band where electrons are bound more tightly to atoms.
- **Conduction Band (CB)**: Higher-energy band where electrons can move more freely and conduct current.

Between these two bands lies the **band gap** — an energy range in which no electron states exist.

4.1.2 Metals, Insulators, and Semiconductors

1. **Metals**: The valence band and conduction band overlap or are only partially filled, allowing many free electrons for conduction.
2. **Insulators**: The band gap is so large that electrons in the valence band cannot easily jump to the conduction band at ordinary temperatures, resulting in almost no free charge carriers.
3. **Semiconductors**: The band gap is moderate (e.g., 1.12 eV for silicon). At room temperature, some electrons gain enough energy to transition from the valence band to the conduction band, yielding moderate conductivity. The conductivity can be *enhanced* or *reduced* via doping or external fields.

4.2 Electrons and Holes

- Electrons in the Conduction Band
  - When an electron gains sufficient energy (e.g., from thermal agitation, doping, or light absorption), it can move from the valence band to the conduction band, leaving behind a vacancy in the valence band.
  - **Conduction electrons** are relatively free to move under an electric field, contributing to current flow.
- Holes in the Valence Band
  - The vacancy left in the valence band is called a **hole**—it behaves like a positively charged carrier.
  - A hole can move when adjacent electrons "hop" into the hole, effectively shifting the vacancy in the opposite direction.
  - In **p-type** (positively doped) semiconductors, holes dominate conduction.

4.3 Band Gap

The *band gap* is the energy difference (E_g) between the top of the valence band and the bottom of the conduction band. It determines:

- How easily electrons can be excited to the conduction band.
- The *temperature dependence* of carrier concentration and conductivity.
- The semiconductor's *optical absorption* and emission characteristics.

4.3.1 Intrinsic vs. Extrinsic Semiconductors

- **Intrinsic**: Pure semiconductor with no deliberate doping. The number of electrons equals the number of holes.
- **Extrinsic**: Doped semiconductor:
  - **n-type**: Doping with donor atoms (extra electrons).
  - **p-type**: Doping with acceptor atoms (creates holes).

By carefully controlling doping, engineers manipulate the **Fermi level** (chemical potential for electrons) within the band gap, shifting electron/hole concentrations dramatically.

4.4 Applications to Semiconductor Devices

1. **p–n Junction (Diode)**
   - A p–n junction is formed by joining p-type and n-type semiconductors.
   - Electrons and holes diffuse across the junction, creating a *depletion region* and built-in potential.
   - Under *forward bias*, electrons and holes recombine across the junction, allowing current flow (the diode "turns on").
   - Under *reverse bias*, very little current flows, except for tiny leakage or breakdown at high reverse voltage.
2. **Bipolar Junction Transistor (BJT)**
   - Consists of n–p–n or p–n–p layers.
   - Small changes in base current cause large changes in collector–emitter current due to electron–hole injection across junctions.
   - Widely used for amplification and switching (though less dominant in digital ICs than MOSFETs).
3. Field-Effect Transistor (FET)
   - **MOSFET** (Metal–Oxide–Semiconductor FET) is the cornerstone of modern electronics.
   - A *gate voltage* modulates the concentration of carriers in a channel region (between source and drain), turning conduction on or off.
   - **NMOS**: Electrons are the majority carriers; a positive gate voltage inverts the p-type substrate locally to form an n-type channel.
   - **PMOS**: Holes are the majority carriers; a negative gate voltage inverts the n-type substrate region to form a p-type channel.
4. LEDs and Laser Diodes
   - In Light-Emitting Diodes (LEDs), electrons recombine with holes across a p–n junction, releasing photons.
   - The *band gap* influences the color of emitted light (e.g., GaAs has a direct gap suitable for efficient light emission).
5. Photodiodes and Solar Cells
   - Photodiodes convert light to electrical current.
   - Photons with energy above the band gap excite electrons into the conduction band, creating electron–hole pairs that generate current in a reversed p–n junction.

4.4.1 Key Takeaways

1. **Energy Bands** and the **Band Gap** determine whether a material is metallic, insulating, or semiconducting.
2. **Electrons** in the conduction band and **holes** in the valence band serve as the primary charge carriers in semiconductors.
3. **Doping** shifts the Fermi level, controlling electron or hole concentration to create n-type or p-type regions.
4. By carefully designing structures (p–n junctions, transistors), engineers harness electron–hole dynamics for rectification, amplification, switching, and light emission/detection.

5. **Semiconductor devices** rely on these fundamental band and carrier concepts to power virtually all modern electronics: from microprocessors and memory to optoelectronic sensors and communication systems.

Understanding electrons, holes, energy bands, and band gaps is crucial to grasp *how semiconductors function*. Mastering these concepts sets the stage for deeper study of specific devices (diodes, transistors, MOSFETs, etc.) and advanced applications (integrated circuits, photovoltaics, LED technology, and more).

5 Introduction to Diodes

Diodes are essential two-terminal semiconductor devices that allow current flow primarily in one direction. They are formed by a *p–n junction*, combining p-type and n-type semiconductor materials. Below is an introduction to the concepts of diodes, including ideal vs. non-ideal behavior, the diode current equation, and how these devices appear in practical applications.

5.1 The Basic p–n Junction Diode

5.1.1 p–n Junction Structure

- A **p–n junction** is created by joining p-type (excess holes) and n-type (excess electrons) semiconductor regions.
- Near the boundary, electrons from the n-side diffuse into the p-side, and holes from the p-side diffuse into the n-side, creating a **depletion region** with ionized donors/acceptors.
- A *built-in potential* forms, opposing further carrier diffusion.

5.1.2 Forward vs. Reverse Bias

- **Forward Bias**: p-side is at a higher potential than the n-side. The depletion region narrows, allowing significant current to flow once the voltage exceeds roughly 0.7 V in silicon diodes (or 0.3 V in germanium, etc.).
- **Reverse Bias**: n-side is at a higher potential than the p-side. The depletion region widens, and only a tiny leakage current flows, until a large reverse voltage causes breakdown.

5.2 Ideal Diode Model

5.2.1 Characteristics

In an *ideal diode*:

1. **Forward conduction**: Zero voltage drop when forward biased, so $V \approx 0$ for $I > 0$.
2. **Reverse conduction**: Zero current (aside from a theoretical negligible leakage) in reverse bias, so $I \approx 0$ for $V < 0$.

5.2.2 Ideal Diode Symbol and Equation

Symbolically, one often writes:

$$I_D = \begin{cases} 0, & V_D < 0 \quad \text{(reverse)} \\ \text{unlimited}, & V_D > 0 \quad \text{(forward)} \end{cases}$$

In practice, "unlimited" forward current is constrained by external circuit elements, but the diode itself has no forward voltage drop in this ideal model.

5.2.3 Applications

Applications include:

- **Rectifiers**: Diodes in power supplies to convert AC to DC.
- **Clipping/Clamping**: Ideal diodes model perfect conduction in one direction.
- **Simple Logic Gates** (in older diode-logic circuits).

5.3 Non-Ideal (Real) Diodes

5.3.1 The Diode Equation

A more accurate model for a silicon diode's forward current (assuming it's above threshold and ignoring high-level injection or breakdown) is:

$$\boxed{I_D = I_s\left(e^{\frac{V_D}{n\,V_T}} - 1\right),}$$

where:

- I_s: **Saturation current** (on the order of 10^{-14} to 10^{-9} A for a small-signal diode), depends on doping and junction area.
- V_D: **Diode voltage** (forward bias voltage).
- V_T: **Thermal voltage** (≈ 25 mV at 300 K).
- n: **Ideality factor**, typically between 1 and 2, capturing recombination and other non-ideal processes.

5.3.2 Forward Bias Behavior

- For $V_D \gg V_T$, $e^{\frac{V_D}{n V_T}}$ becomes large, so $I_D \approx I_s\, e^{\frac{V_D}{n\,V_T}}$.
- A real silicon diode typically drops 0.7 V at a reasonable forward current (like 1–10 mA).

5.3.3 Reverse Bias and Breakdown

- In reverse bias, $V_D < 0$, the current is near $-I_s$, very small.
- *Breakdown* can occur if the reverse voltage exceeds the diode's rating:
  - **Zener Breakdown** (heavily doped diodes at <5–6 V range).
  - **Avalanche Breakdown** (higher voltages, doping arrangement differs).

5.4 Non-Ideal Effects and Additional Parameters

- Series Resistance (R_s)
  - Real diodes have a *bulk or contact resistance* in series.
  - At high forward current, $I_D \cdot R_s$ adds to the diode drop.
- Shunt Resistance (R_{sh})
  - Leakage paths or imperfections can create a small parallel conduction route, noticeable in reverse bias.
- Temperature Effects
  - Higher temperature typically increases I_s and lowers the forward voltage drop.
  - Diodes are often used in temperature sensing (e.g., diode-based thermal sensors).

5.5 Common Diode Types

1. **Signal Diodes (Small-Signal)**: Low current rating, used in RF, high-speed switching. Examples: 1N4148.
2. **Power Diodes**: Large junction area for higher current/voltage. Examples: 1N400x series for rectifiers.
3. **Zener Diodes**: Designed to operate in *reverse breakdown* region to provide voltage regulation or reference.
4. **Schottky Diodes**: Metal–semiconductor junction, lower forward voltage (0.2–0.4 V), faster switching.
5. **Light-Emitting Diodes (LEDs)**: Emit light when electrons recombine with holes across the junction.

5.6 Role in Semiconductor Devices

1. **Rectification and Power Conversion**
   - **Diode bridges** or **half-wave rectifiers** convert AC to DC in power supplies.
   - **Voltage regulators**: Zener diodes clamp voltage to a set level.

2. **Signal Processing**
   - **Clippers** and **Clampers** shape waveforms in analog circuits.
   - **Mixers, Detectors** in radio-frequency (RF) front-ends utilize diodes to demodulate signals.
3. **Protection**
   - **Transient Voltage Suppression (TVS) diodes** protect circuits from electrostatic discharges (ESD) and voltage spikes.
4. **Integrated Circuits (ICs)**
   - Diodes often appear as *body diodes* in MOSFETs or as *parasitic diodes* in bipolar processes. They can also be deliberately integrated for ESD protection, biasing networks, or bandgap references.
   -

5.6.1 Key Takeaways

1. An **ideal diode** is a simple conceptual tool: no forward drop, infinite reverse resistance.
2. A **non-ideal (real) diode** follows the *diode current equation*, exhibiting exponential I–V behavior in forward bias and minimal reverse current until breakdown.
3. Practical diodes have *series resistance*, *shunt leakage*, and can experience *breakdown* under large reverse bias.
4. These diode concepts extend beyond simple discrete devices to the *junctions* in transistors (both BJT and MOS) and integrated circuits.
5. Understanding diode operation—forward conduction, reverse blocking, breakdown—is crucial for power electronics, signal processing, switching circuits, and protective components.

Diodes represent *the simplest p–n junction device*, fundamental to all semiconductor technology. From an *ideal* perspective, they act as one-way current valves. In real-world applications, their *non-ideal* behavior—including a finite forward drop, saturation current, and reverse breakdown—forms the basis for rectifiers, voltage clamps, power regulators, signal detectors, and more. Mastering diode theory lays a foundation for understanding more complex devices like transistors, integrated circuits, and other semiconductor components critical to modern electronics.

5.7 Problem Worksheets

Click here to access a set of problems on the basics of semiconductor devices, resistivity, semiconductor physics, and diodes. Click here to access a second set of problems covering the basics of semiconductor devices, semiconductor physics, and diodes.

6 Introduction and overview of transistors

A *transistor* is a three-terminal semiconductor device that can amplify or switch electronic signals. Transistors come in several types—the most common in modern digital electronics being the MOSFET (Metal–Oxide–Semiconductor Field-Effect Transistor). This overview focuses on MOSFETs, including the differences between NMOS (n-channel) and PMOS (p-channel) devices, how they combine to form CMOS technology, key current–voltage relationships, and the concept of *threshold* vs. *subthreshold* conduction.

6.1 Basic MOSFET Structure

- **MOSFET** stands for Metal–Oxide–Semiconductor Field-Effect Transistor.
- Consists of four terminals: **Gate (G)**, **Source (S)**, **Drain (D)**, and **Body (B)** (or Substrate). In many cases, the body is tied internally or externally to a reference voltage (e.g., ground for NMOS or supply for PMOS).
- A thin insulating layer (oxide) separates the Gate from the semiconductor channel region.

6.1.1 N-channel (NMOS) vs. P-channel (PMOS)

1. **NMOS (n-channel)**
   - Built on a p-type substrate (body).
   - A *positive* Gate–Source voltage (V_{GS}) inverts the surface beneath the gate to create an *n-type channel* for electrons.
   - Conduction occurs primarily via electrons.
2. **PMOS (p-channel)**
   - Built on an n-type substrate (well).
   - A *negative* Gate–Source voltage (V_{GS}) creates a *p-type channel* for holes.
   - Conduction occurs primarily via holes.

6.2 Regions of Operation

A MOSFET can operate in several "regions," depending on the voltages V_{GS} (gate–source), V_{DS} (drain–source), and the *threshold voltage* V_{th}.

6.2.1 Threshold Voltage

- The minimum V_{GS} for strong inversion (creating a conductive channel).
- For **NMOS**: You need $V_{GS} > V_{th}$ (positive) to "turn on" the channel.
- For **PMOS**: You need V_{GS} to be *less than* $-V_{th}$ (i.e., sufficiently negative) to form the p-channel.
- V_{th} can be adjusted via doping, oxide thickness, and workfunction engineering.

6.2.2 MOSFET Operating Regions

1. **Cutoff (Off Region)**
   - $|V_{GS}|$ less than $|V_{th}|$.
   - No conductive channel forms; only a small leakage current flows.
2. **Linear (or Triode) Region**
   - $|V_{GS} - V_{th}| > 0$ (channel formed), but $|V_{DS}| < |V_{GS} - V_{th}|$.
   - The device behaves *somewhat* like a *voltage-controlled resistor* with R_{on} set by $(V_{GS} - V_{th})$.
3. **Saturation Region**
4. $|V_{GS} - V_{th}| > 0$ and $|V_{DS}| \geq |V_{GS} - V_{th}|$.
5. The channel "pinches off" near the drain; the transistor behaves more like a *current source* controlled by V_{GS}.

6.3 MOSFET Current–Voltage Relationships

6.3.1 Ideal Long-Channel Model (Ignoring Channel-Length Modulation)

1. **Linear (Triode) Region**:
   - $$I_D = \mu C_{\text{ox}} \frac{W}{L} \Big[(V_{GS} - V_{th}) V_{DS} - \tfrac{V_{DS}^2}{2} \Big],$$
   - μ is carrier mobility (μ_n for NMOS or μ_p for PMOS), C_{ox} is gate oxide capacitance per unit area, and W/L is the device width over length ratio.
2. **Saturation Region**:
   - $$I_D \;=\; \tfrac{1}{2}\, \mu C_{\text{ox}} \tfrac{W}{L}\, (V_{GS} - V_{th})^2.$$
   - The current is set primarily by $(V_{GS} - V_{th})$.
   - Once in saturation, increasing V_{DS} further has minimal effect (in the ideal model).

6.3.2 N-MOSFET vs. P-MOSFET

- Both follow similar equations, but for *PMOS* the voltage polarities and sign conventions are reversed.
- Typically, $\mu_n > \mu_p$ in silicon, meaning electrons (NMOS) have higher mobility than holes (PMOS).
- Hence, for the same W/L and $|V_{GS} - V_{th}|$, an NMOS usually carries more current than a PMOS.

6.4 Threshold vs. Subthreshold Current

- **Strong Inversion and Threshold**
  - Above the threshold voltage ($V_{GS} > V_{th}$ for NMOS), the device enters *strong inversion*, and the standard quadratic MOSFET models apply.
  - This is typically how MOSFETs are driven in digital logic (fully on or fully off).
- **Subthreshold (Below Threshold)**
  - If $|V_{GS}| < |V_{th}|$, only a small **subthreshold current** flows, described by an exponential relationship:

    $$I_D \approx I_0 \exp\Big(\tfrac{V_{GS} - V_{th}}{n\, V_T} \Big),$$
  - where n is the subthreshold slope factor (1.1 to 2), $V_T \approx 25\,\text{mV}$ at room temperature.
  - **Subthreshold conduction** can be *significant* in very low-power circuits or in advanced technology nodes with high leakage.

6.5 CMOS (Complementary MOS)

6.5.1 NMOS + PMOS

CMOS technology pairs an **n-channel MOSFET (NFET)** and a **p-channel MOSFET (PFET)** in complementary configurations. A standard **CMOS inverter** uses one NMOS (pull-down) and one PMOS (pull-up):

- **Input**: Both gates tied together.
- **Output**: Connected to both drains.
- The PMOS source is typically at V_{DD}, and the NMOS source at ground.

6.5.2 CMOS Inverter Operation

- When the input is *low* (0 V):
  - NMOS is off, PMOS is on → Output is pulled up to V_{DD}.
- When the input is *high* (close to V_{DD}):
  - NMOS is on, PMOS is off → Output is pulled down to 0 V.

- CMOS inverters have *low static power* consumption (only a small leakage current flows when inputs are not switching).
- This principle extends to all CMOS logic gates—AND, OR, NAND, NOR, etc.—using transistor networks arranged in pull-up and pull-down logic.

6.6 Applications to Semiconductor Devices

1. **Digital Logic**
   - CMOS circuits form the backbone of microprocessors, memory, and digital integrated circuits thanks to low power and high density.
   - **Transistor scaling** (Moore's Law) continuously reduces channel lengths for higher speed and density.
2. **Analog Circuits**
   - MOSFETs used in amplifiers, current mirrors, filters, etc.
   - Designers exploit the transistor's linear region (as tunable resistors) or saturation region (as current sources).
3. **Power Electronics**
   - **Power MOSFETs** handle high currents and voltages in motor drivers, power supplies, converters.
   - Lateral vs. vertical MOSFET designs allow for efficient conduction at different voltage/current scales.
4. **Specialized Devices**
   - **FinFETs**, **SOI MOSFETs**, and **Multi-Gate devices**: used in advanced CMOS processes for reduced leakage and improved performance.
   - **Subthreshold operation**: used in ultra-low power designs (e.g., certain sensor nodes or wearable electronics).

6.6.1 Key Takeaways

1. **MOSFET Basics**: Gate voltage controls a conductive channel; "threshold" is the minimum required to form a strong channel.
2. **NMOS vs. PMOS**: NMOS typically offers higher electron mobility, but PMOS complements it in CMOS for efficient logic gates.
3. **CMOS**: The combination of n-channel and p-channel devices results in robust, low-power digital logic (inverters, gates, etc.).
4. **Current–Voltage Behavior**: Above threshold, a MOSFET follows quadratic-like or linear relationships in different regions; below threshold, conduction is exponentially small (but not zero).
5. **Significance**: Transistors, especially MOSFETs, are fundamental building blocks of all modern electronics, enabling everything from microprocessors to power converters.

Transistors — particularly **MOSFETs** — are at the heart of nearly all semiconductor devices today. By understanding *how gate voltages create or block conductive channels*, how **NMOS** and **PMOS** differ, and how they *combine in CMOS* to form energy-efficient logic, engineers can design and optimize circuits that power the digital age. Whether in microchips, analog amplifiers, or power switches, transistors remain the indispensable cornerstone of electronic technology.

6.7 Problem Worksheets

Click here to access a set of problems on the basics of transistors, including MOSFET, CMOS, and threshold vs. subthreshold current. Click here to access a second set of problems covering the basics of transistors.

7 Problems

7.1 Semiconductor Basics: Problem Set 1 [return to TOC]

The following problems focus on the fundamentals of semiconductor devices and include a mix of theoretical and computational exercises covering semiconductor physics and devices, resistivity, doping, band gaps, and diode behavior.

7.1.1 Problem 1: Resistivity and Carrier Density Relationship

Explain how increasing or decreasing charge carrier density affects the resistivity of a semiconductor. Provide a qualitative discussion.

7.1.2 Problem 2: Calculating the Resistivity of a Semiconductor

Given a semiconductor with electron mobility $\mu_n = 1350$ cm^2/Vs and hole mobility $\mu_p = 480$ cm^2/Vs, and intrinsic carrier concentration $n_i = 1.5 \times 10^{10}$ cm^{-3}, calculate the intrinsic resistivity of silicon at room temperature.

7.1.3 Problem 3: Calculating Conductivity for Doped Silicon

A silicon sample is doped with 10^{16} donors per cm^3. Assuming complete ionization and $\mu_n = 1350$ cm^2/Vs, find the conductivity.

7.1.4 Problem 4: Band Gap Calculation from Optical Absorption

A semiconductor absorbs light with a wavelength of 870 nm. Calculate its band gap energy E_g.

7.1.5 Problem 5: Energy Band Diagrams Interpretation

Describe the significance of the conduction band, valence band, and band gap in a semiconductor.

7.1.6 Problem 6: Doping and Fermi Level Shifts

Explain how doping affects the position of the Fermi level in n-type and p-type semiconductors.

7.1.7 Problem 7: Diode Ideal Current Equation Verification

Verify the ideal diode equation for $V = 0.7V$ with $I_0 = 1$ nA, $kT/q = 25$ mV.

7.1.8 Problem 8: Plotting the I-V Characteristics of a Diode

Plot the diode current as a function of voltage in the range $-0.2\text{V} \leq V \leq 0.8\text{V}$, for saturation current $I_0 = 1$ nA and thermal voltage $V_\text{T} = 25$ mV.

7.1.9 Problem 9: Reverse Bias in a Diode

Explain what happens when a diode is reverse biased.

7.1.10 Problem 10: Zener Breakdown Calculation

If a Zener diode has a breakdown voltage of 5.1V and is connected to a 10V supply through a 1kΩ resistor, find the current through the diode.

7.1.11 Problem 11: Carrier Concentration Calculation

A silicon semiconductor is doped with 5×10^{16} donors per cm^3. Assuming complete ionization and an intrinsic carrier concentration $n_i = 1.5 \times 10^{10}$ cm^{-3}, determine the electron and hole concentrations using the mass action law.

7.1.12 Problem 12: Diode Small-Signal Resistance

Derive the small-signal resistance r_d of a diode at $V = 0.7V_{\mathrm{T}}$ with $I_0 = 1$ nA, assuming $V_{\mathrm{T}} = kT/q = 25$ mV.

7.1.13 Problem 13: Temperature Dependence of Band Gap

The band gap of silicon varies with temperature as:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta}$$

where $E_g(0) = 1.17$ eV, $\alpha = 4.73 \times 10^{-4}$ eV/K, and $\beta = 636$ K. Plot $E_g(T)$ from 200K to 400K.

7.1.14 Problem 14: PN Junction Capacitance

A PN junction has a built-in voltage of 0.7V and a depletion width of 200 nm. Compute the junction capacitance per unit area assuming a dielectric constant $\epsilon = 11.7\epsilon_0$.

7.1.15 Problem 15: MOSFET Threshold Voltage

Derive the threshold voltage equation for a MOSFET:

$$V_T = V_{FB} + 2\phi_F + \frac{Q_d}{C_{ox}}$$

where V_{FB} is the flatband voltage, ϕ_F is the Fermi potential, Q_d is the depletion charge, and C_{ox} is the oxide capacitance.

7.1.16 Problem 16: Bipolar Junction Transistor Current Gain

For a BJT, the current gain is defined as:

$$\beta = \frac{I_C}{I_B}$$

If $I_C = 5$ mA and $I_B = 50$ µA, calculate β.

7.1.17 Problem 17: LED Emission Wavelength

An LED has a band gap of 2.0 eV. Find the corresponding emission wavelength.

7.1.18 Problem 18: Solar Cell Efficiency Calculation

A silicon solar cell receives 1000 W/m^2 of sunlight and generates 200 W/m^2 of electrical power. Calculate the efficiency.

7.1.19 Problem 19: Schottky Diode Behavior

Explain how a Schottky diode differs from a PN junction diode.

7.1.20 Problem 20: Semiconductor Fabrication Process

List and briefly describe the major steps in semiconductor fabrication.

7.1.21 Problem 21: Computing and Plotting MOSFET Threshold Voltage

Consider an n-channel MOSFET with a p-type silicon substrate that has an acceptor doping concentration of $N_A = 5 \times 10^{16}$ cm^{-3}. The oxide layer has a thickness of 10 nm, and the oxide permittivity is $\epsilon_{ox} = 3.9\epsilon_0$, where $\epsilon_0 = 8.85 \times 10^{-12}$ F/m. The semiconductor permittivity is $\epsilon_s = 11.7\epsilon_0$, and the flatband voltage is given as $V_{FB} = -0.9$ V.

1. **Compute** the threshold voltage V_T at room temperature (300K).
2. **Plot** V_T as a function of the doping concentration N_A ranging from 10^{15} cm^{-3} to 10^{18} cm^{-3}.
3. **Analyze** the trend of V_T with increasing doping concentration.

7.2 Semiconductor Basics: Problem Set 2

[return to TOC]

The following problems focus on the fundamentals of semiconductor devices. They span conceptual and quantitative aspects of semiconductor device physics, focusing on carrier densities, diode equations (ideal and non-ideal), wire and resistor formulas, and special diode types (Zener, tunneling). Problems 1–10 include Python snippets to reinforce computational skills, while Problems 11–20 address core semiconductor concepts qualitatively.

7.2.1 Problem 1: Wire Resistance Calculation

A copper wire of length $L = 2$ m and cross-sectional area $A = 1 \times 10^{-6}$ m^2 is used to connect a circuit. Copper has a resistivity $\rho = 1.68 \times 10^{-8}\,\Omega \cdot$ m.

1. Calculate the resistance of the wire.
2. If the current flowing through the wire is $I = 1$ A, find the voltage drop across it.

7.2.2 Problem 2: Intrinsic Carrier Concentration and Doping

Silicon at room temperature ($T = 300$ K) has an intrinsic carrier concentration $n_i = 1 \times 10^{10}\,\text{cm}^{-3}$. Consider an n-type silicon doped with donor atoms at a concentration $N_D = 1 \times 10^{16}\,\text{cm}^{-3}$. Assume complete ionization of donors.

1. Find the electron concentration $n \approx N_D$ (for $N_D \gg n_i$).
2. Using the mass action law $n \cdot p = n_i^2$, find the hole concentration p.
3. Convert the units of electron concentration n to m^{-3}.

7.2.3 Problem 3: Determining Fermi Level Shift with Doping

In intrinsic silicon at 300 K, the Fermi level is approximately in the middle of the band gap. When doped n-type to a concentration $N_D = 10^{15}\,\text{cm}^{-3}$, the Fermi level E_F moves closer to the conduction band. The intrinsic Fermi level E_{Fi} is at $E_g/2$ from the valence band, with $E_g = 1.12$ eV. Using the relation

$$E_F - E_{Fi} = k_B T \ln\left(\frac{N_D}{n_i}\right),$$

where $k_B T \approx 0.0259$ eV at 300 K and $n_i = 10^{10}\,\text{cm}^{-3}$, calculate $E_F - E_{Fi}$.

7.2.4 Problem 4: Diode I–V Characteristic (Ideal Diode)

An ideal silicon diode has a saturation current $I_s = 10^{-14}$ A. At room temperature ($k_B T/q \approx 25$ mV), use the ideal diode equation

$$I_D = I_s\left(e^{\frac{V_D}{V_T}} - 1\right)$$

where $V_T = 25$ mV, to:

1. Calculate the diode current at $V_D = 0.7$ V.
2. Plot the diode's I–V characteristic from $V_D = 0$ V to 1 V.

7.2.5 Problem 5: Non-Ideal Diode with Ideality Factor

A silicon diode has a saturation current $I_s = 10^{-14}$ A and an ideality factor $n = 2$. At room temperature (25 mV thermal voltage), the diode equation becomes

$$I_D = I_s \left(e^{\frac{V_D}{nV_T}} - 1 \right).$$

1. Calculate the current at $V_D = 0.7$ V.
2. Compare the result with the ideal diode (where $n = 1$).

7.2.6 Problem 6: Series Resistance Effect in a Diode

A diode has a series resistance $R_s = 10\,\Omega$. Its intrinsic diode saturation current is $I_s = 10^{-14}$ A, and the ideality factor is $n = 1$. At room temperature ($V_T = 25$ mV), the I–V relation becomes

$$I_D = I_s \left(\exp\left[\frac{V_D - I_D R_s}{nV_T} \right] - 1 \right).$$

1. Use numerical iteration to estimate the current at $V_D = 0.65$ V.
2. Plot I_D vs. V_D from 0 to 0.65 V, taking R_s into account.

7.2.7 Problem 7: Carrier Density vs. Temperature

Consider intrinsic silicon with $n_i(T)$ given (approximately) by

$$n_i(T) = 5.2 \times 10^{15} \times T^{3/2} \exp\left(-\frac{E_g}{2k_B T} \right) \text{ cm}^{-3},$$

where $E_g = 1.12$ eV (for silicon), $k_B = 8.617 \times 10^{-5}$ eV/K. Plot $n_i(T)$ from $T = 300$ K to $T = 600$ K.

7.2.8 Problem 8: Measuring Resistivity with Four-Point Probe

You perform a four-point probe measurement on a silicon sample. The measurement yields a sheet resistance $R_s = 200\,\Omega/\square$. The wafer thickness is $t = 500\,\mu\text{m} = 5 \times 10^{-2}$ cm. Compute the bulk resistivity ρ.

$$\rho = R_s \times t.$$

7.2.9 Problem 9: Tunneling Diode Current Approximation

A tunneling diode exhibits negative differential resistance in a certain region. Assume an approximate peak current density J_p of 100 A/cm^2 at $V_p = 0.3$ V. If the diode cross-sectional area is 0.01 cm^2, estimate the peak current (I_p) and the power at peak voltage.

7.2.10 Problem 10: Non-Linear (Tunable) Resistor Model

A "tunable" semiconductor resistor has a voltage-dependent resistance given by

$$R(V) = \frac{R_0}{1 + \alpha V^2},$$

where $R_0 = 1\,\text{k}\Omega$ and $\alpha = 5\,\text{V}^{-2}$.

1. Calculate and plot $R(V)$ for V from 0 to 10 V.
2. Find the current when a 10 V source is applied across this resistor.

7.2.11 Problem 11: Qualitative: Electrons vs. Holes in Semiconductors

Explain the difference between electrons and holes in a semiconductor and why the effective mass and mobility of holes are often different (and typically lower mobility) compared to electrons.

7.2.12 Problem 12: Band Gap Types: Direct vs. Indirect

Compare direct band gap and indirect band gap semiconductors, giving one example of each. Why are direct band gap semiconductors typically used for optoelectronic devices such as LEDs?

7.2.13 Problem 13: Zener Diode Breakdown

Describe how a Zener diode achieves voltage regulation through breakdown. Why does the Zener breakdown voltage typically lie between 2 V to a few hundred volts?

7.2.14 Problem 14: LED vs. Normal Diode

An LED (Light Emitting Diode) and a normal (signal) diode both use a p–n junction. Explain why one emits light while the other does not.

7.2.15 Problem 15: Forward and Reverse Bias in a p–n Junction

Describe what happens to the depletion region and current flow in forward bias vs. reverse bias for a basic p–n junction diode.

7.2.16 Problem 16: Ideal vs. Real Diode Equation Parameters

Discuss the difference between the ideal diode equation and the real diode equation which includes parameters such as series resistance (R_s) and shunt resistance (R_{sh}).

7.2.17 Problem 17: Depletion Capacitance in a Diode

Explain how the depletion region in a reverse-biased diode creates a junction capacitance. How does this capacitance vary with reverse bias voltage?

7.2.18 Problem 18: Short vs. Long Diodes (Diode Length Effects)

Consider a diode with a very short p–region relative to its diffusion length. Explain how diode length impacts carrier injection and the resulting I–V characteristics.

7.2.19 Problem 19: Non-Idealities: Recombination–Generation Currents

In a real diode, recombination–generation currents in the depletion region can significantly affect the I–V curve. Which part of the I–V characteristic is most influenced by these processes, and why?

7.2.20 Problem 20: Tunable Resistor vs. Diode Behavior

A semiconductor device can behave like a tunable resistor under certain doping profiles or external control (e.g., a field-effect resistor), whereas a diode allows current primarily in one direction. Conceptually compare why a "tunable resistor" does not rectify current, but a diode does.

7.3 Transistor Basics: Problem Set 3 [return to TOC]

The following problems focus on the fundamentals of transistors and cover key topics such as MOSFET characteristics, CMOS circuits, threshold voltage, and subthreshold current.

7.3.1 Problem 1: History of the Transistor

Briefly describe the significance of the invention of the transistor and its impact on modern electronics.

7.3.2 Problem 2: MOSFET Structure and Operation

Explain the basic structure of a MOSFET and describe its three operational regions.

7.3.3 Problem 3: CMOS Inverter Logic

Explain how a CMOS inverter works using an nMOS and pMOS transistor pair.

7.3.4 Problem 4: Calculating MOSFET Drain Current in the Linear Region

A MOSFET has parameters: $V_G = 2.5V$, $V_T = 1V$, $V_{DS} = 0.5V$, $\mu_n C_{ox} = 100\ \mu A/V^2$, $L = 0.2\ \mu m$, and $W = 10\ \mu m$. Compute I_D.

7.3.5 Problem 5: Plotting MOSFET I-V Characteristics

Plot I_D vs. V_{DS} for a MOSFET in the linear and saturation regions for $V_G = 2.5\text{V}, 3.5\text{V}, 4.5\text{V}$.

7.3.6 Problem 6: Threshold Voltage and Scaling

Explain how reducing MOSFET channel length affects threshold voltage and leakage current.

7.3.7 Problem 7: Subthreshold Current Calculation

For a MOSFET with $V_T = 0.4V$, $V_{DS} = 1.2V$, and subthreshold slope $S = 80mV/decade$, estimate I_D at $V_G = 0.3V$ given $I_{D0} = 1\ \mu A$ at $V_G = 0.4V$.

7.3.8 Problem 8: Comparing NMOS and PMOS Characteristics

Explain why PMOS transistors generally have lower current than NMOS transistors for the same device size.

7.3.9 Problem 9: Calculating Drain Current in the Saturation Region

A MOSFET operates in the saturation region with parameters:

- $V_G = 3.3V$,
- $V_T = 1.2V$,
- $L = 0.25\ \mu m$,
- $W = 5\ \mu m$,
- $\mu_n C_{ox} = 80\ \mu A/V^2$.

Compute I_D.

7.3.10 Problem 10: CMOS Power Consumption

A CMOS inverter is supplied with $V_{DD} = 5V$ and a clock frequency of 10 MHz. The load capacitance is $C_L = 10pF$. Compute the dynamic power consumption.

7.3.11 Problem 11: CMOS Inverter Transfer Characteristics

Plot the transfer characteristics of a CMOS inverter, assuming $V_{DD} = 5V$.

7.3.12 Problem 12: Short-Channel vs. Long-Channel MOSFET Effects

Explain why short-channel MOSFETs experience increased leakage current and lower threshold voltage compared to long-channel MOSFETs.

7.3.13 Problem 13: Leakage Currents in Modern MOSFETs

List the primary sources of leakage current in MOSFETs and explain their impact.

7.3.14 Problem 14: Effect of Temperature on MOSFET Performance

MOSFETs are tested at two temperatures: 300K and 350K. Assuming V_T decreases with temperature, plot I_D as a function of T.

7.3.15 Problem 15: Body Effect in MOSFETs

Explain the body effect and derive the equation for the modified threshold voltage.

7.3.16 Problem 16: Oxide Thickness and Threshold Voltage

The value of V_{T0} (the threshold voltage when t_{ox} is at a reference thickness and $V_{SB} = 0$) should be defined based on typical MOSFET operating conditions. A *common assumption* for silicon MOSFETs is that V_{T0} ranges between 0.6V and 1.2V for long-channel devices. For modern *short-channel* MOSFETs, V_{T0} can be lower (e.g., 0.3V to 0.6V). For this problem, assume $V_{T0} = 0.7$V, which is reasonable for a *moderately scaled* MOSFET. Compute V_T for different oxide thicknesses (t_{ox}) ranging from 1 nm to 5 nm.

7.3.17 Problem 17: Subthreshold Slope Plot

For a MOSFET with:

- Subthreshold slope $S = 80$ mV/decade
- Threshold voltage $V_T = 0.4V$
- Off-current $I_{D0} = 1$ nA at $V_GS = 0.4V$

Plot the subthreshold current I_D for V_GS ranging from 0V to 1V.

7.3.18 Problem 18: CMOS vs. NMOS Logic

Explain why CMOS logic is preferred over NMOS-only logic.

7.3.19 Problem 19: Body Effect Equation Derivation

Derive the body effect equation for threshold voltage.

7.3.20 Problem 20: Drain Current for Different Oxide Thicknesses

For an n-channel MOSFET, compute and plot drain current I_D in saturation as a function of oxide thickness t_{ox}. Assume:

- **Gate voltage**: $V_G = 2.5$V
- **Threshold voltage**: $V_T = 0.7$V
- **Oxide permittivity**: $\epsilon_{ox} = 3.9\epsilon_0$
- **Gate oxide thickness range**: 1 nm to 5 nm
- **Mobility-capacitance product**: $\mu_n C_{ox} = 80\ \mu$A/V^2 when $t_{ox} = 2.5$ nm
- **Channel width**: $W = 10\ \mu$m
- **Channel length**: $L = 0.2\ \mu$m

Compute and plot I_D in saturation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_G - V_T)^2$$

7.4 Transistor Basics: Problem Set 4 [return to TOC]

The following problems focus on the fundamentals of transistors and address both *quantitative* and *qualitative* aspects of MOSFETs and CMOS circuits. Focus is on MOSFET topics such as NMOS vs. PMOS, N-channel vs. P-channel devices, CMOS inverters, current–voltage (I–V) relationships (including sub-threshold behavior), threshold voltage, and more. This problem set is suitable for undergraduate electrical engineering students studying semiconductor devices.

7.4.1 Problem 1: NMOS Drain Current in Saturation

An NMOS transistor operates in the saturation region (neglect channel-length modulation). Its drain current is given by:

$$I_D = \frac{1}{2}\mu_n C_{\text{ox}} \frac{W}{L}(V_{GS} - V_{th})^2,$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W is the channel width, L is the channel length, V_{GS} is the gate-to-source voltage, and V_{th} is the threshold voltage.

Given:

- $\mu_n = 400\,\text{cm}^2/\text{V}\cdot\text{s} \approx 0.04\,\text{m}^2/\text{V}\cdot\text{s}$
- $C_{\text{ox}} = 10^{-2}\,\text{F/m}^2$
- $W/L = 10$
- $V_{GS} = 2.5\,\text{V}, \quad V_{th} = 1.0\,\text{V}$

1. Calculate I_D.
2. Plot I_D as a function of $(V_{GS} - V_{th})$ ranging from 0 to 2 V (i.e., V_{GS} from 1 V to 3 V).

Note: Assume the device remains in saturation for these voltages.

7.4.2 Problem 2: Threshold Voltage with Body Effect

The threshold voltage V_{th} of an NMOS transistor can increase if the source–bulk voltage V_{SB} is non-zero. The modified threshold voltage is often modeled as:

$$V'_{th} = V_{th0} + \gamma\left[\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right],$$

where:

- V_{th0} is the threshold voltage when $V_{SB} = 0$,
- γ is the body-effect coefficient,
- ϕ_F is the Fermi potential (on the order of 0.3 to 0.5 V in silicon).

Given:

- $V_{th0} = 0.7\,\text{V}$
- $\gamma = 0.4\,\text{V}^{1/2}$
- $\phi_F = 0.4\,\text{V}$

1. Calculate V'_{th} for $V_{SB} = 0.5\,\text{V}$.
2. Plot V'_{th} vs. V_{SB} for $V_{SB} \in [0, 2]$ V.

7.4.3 Problem 3: NMOS I–V Characteristics (Linear/Triode vs. Saturation)

An NMOS transistor has the following parameters:

- $\mu_n C_{\text{ox}} = 50\,\mu\text{A/V}^2$,
- $W/L = 5$,
- $V_{th} = 1.0\,\text{V}$.

For a given $V_{GS} = 3\,\text{V}$, plot the drain current I_D versus V_{DS} from 0 V to 5 V, distinguishing between the triode (linear) region and the saturation region. Use the standard piecewise equations:

1. **Triode region** ($V_{DS} < V_{GS} - V_{th}$):

$$I_D = \mu_n C_{\text{ox}} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right].$$

2. **Saturation region** ($V_{DS} \geq V_{GS} - V_{th}$):

$$I_D = \frac{1}{2} \mu_n C_{\text{ox}} \frac{W}{L} (V_{GS} - V_{th})^2.$$

7.4.4 Problem 4: PMOS Drain Current (Enhancement Mode)

A PMOS transistor (enhancement mode) has the current equation in saturation (neglecting channel-length modulation):

$$I_D = \frac{1}{2} \mu_p C_{\text{ox}} \frac{W}{L} (|V_{SG}| - |V_{thp}|)^2,$$

where μ_p is the hole mobility, V_{SG} is the source-to-gate voltage, and V_{thp} is the (negative) threshold voltage of the PMOS device.

Given:

- $\mu_p = 200\,\text{cm}^2/\text{V}\cdot\text{s} \approx 0.02\,\text{m}^2/\text{V}\cdot\text{s}$ $C_{\text{ox}} = 8 \times 10^{-3}\,\text{F/m}^2$
- $W/L = 10$
- $|V_{thp}| = 1.0\,\text{V}$
- $|V_{SG}| = 2.0\,\text{V}$

1. Compute the PMOS drain current I_D in saturation.
2. Compare the magnitude of this current to that of an NMOS with the same geometry and $\mu_n = 0.04\,\text{m}^2/\text{V}\cdot\text{s}$, $C_{\text{ox}} = 8 \times 10^{-3}\,\text{F/m}^2$, and threshold $V_{thn} = 1.0\,\text{V}$ at the same overdrive of 1.0 V.

7.4.5 Problem 5: CMOS Inverter Switching Threshold

A CMOS inverter is composed of an NMOS and a PMOS transistor. The switching (inversion) threshold V_M occurs approximately when the NMOS and PMOS devices have equal currents (in the simple static analysis). Assuming both transistors operate in saturation at the switching point, the condition for the currents to match is:

$$\frac{1}{2} k_n (V_M - V_{thn})^2 \;=\; \frac{1}{2} k_p (V_{DD} - V_M - |V_{thp}|)^2,$$

where

- $k_n = \mu_n C_{\text{ox}} (W/L)_n$,
- $k_p = \mu_p C_{\text{ox}} (W/L)_p$,
- V_{DD} is the supply voltage,
- V_{thn} and $|V_{thp}|$ are the NMOS and PMOS threshold magnitudes.

Given:

- $k_n = 3 \times 10^{-4}\,\text{A/V}^2$, $\quad k_p = 2 \times 10^{-4}\,\text{A/V}^2$
- $V_{thn} = 0.8\,\text{V}$, $\quad |V_{thp}| = 1.0\,\text{V}$
- $V_{DD} = 5\,\text{V}$

Find the inverter switching threshold V_M. (You can assume the solution is in a range where both transistors are saturated.)

7.4.6 Problem 6: Subthreshold Conduction in MOSFET

Below the threshold voltage ($V_{GS} < V_{th}$), the drain current of an NMOS transistor exhibits an exponential dependence on V_{GS}. A simplified subthreshold current model is:

$$I_D = I_0 \exp\Big(\frac{V_{GS} - V_{th}}{n\, V_T}\Big),$$

where n is the subthreshold slope factor (often 1.1–1.5), and $V_T = k_B T/q \approx 25\,\text{mV}$ at room temperature. Assume $I_0 = 1\,\text{nA}$, $V_{th} = 0.7\,\text{V}$, $n = 1.2$.

1. Plot I_D vs. V_{GS} for $V_{GS} \in [0, 0.8]$.
2. Find I_D at $V_{GS} = 0.6\,\text{V}$.

7.4.7 Problem 7: Channel-Length Modulation

Even in saturation, a MOSFET's current can increase slightly with V_{DS} due to channel-length modulation. A simple model extends the saturation current equation to:

$$I_D \approx \frac{1}{2} k (V_{GS} - V_{th})^2 \big(1 + \lambda\, V_{DS}\big),$$

where λ is the channel-length modulation parameter. Assume an NMOS transistor has:

- $k = 100\,\mu\text{A/V}^2$,
- $V_{GS} - V_{th} = 2\,\text{V}$,
- $\lambda = 0.02\,\text{V}^{-1}$,
- and V_{DS} in saturation from 3 V to 10 V.

1. Calculate I_D at $V_{DS} = 3$ V and $V_{DS} = 10$ V.
2. Plot I_D vs. V_{DS} for $V_{DS} \in [0, 10]$ V, but use the above expression only for $V_{DS} \geq (V_{GS} - V_{th}) = 2\,\text{V}$. (For $V_{DS} < 2\,\text{V}$, the device is not in saturation.)

7.4.8 Problem 8: Transconductance g_m for an NMOS

The small-signal transconductance g_m in saturation (ignoring channel-length modulation) is:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{2 k I_D},$$

where $k = \mu_n C_\text{ox}(W/L)$. If an NMOS has $k = 400\,\mu\text{A/V}^2$, and the DC operating point drain current is $I_D = 1\,\text{mA}$, find g_m. Then, plot g_m vs. I_D for I_D from 0.1 mA to 5 mA.

7.4.9 Problem 9: MOSFET Sizing in a CMOS Inverter

A CMOS inverter has an NMOS of size $(W/L)_n = 5$ and a PMOS of size $(W/L)_p = 10$. Assume:

- $\mu_n = 2.5\,\mu_p$,
- Both transistors have the same gate oxide (C_ox),
- Threshold magnitudes are equal ($|V_{thp}| = V_{thn}$).

Show that at a given overdrive ($V_{GS} - V_{th}$), the PMOS current roughly matches the NMOS current due to sizing and mobility ratio. Then, compute the ratio $\frac{(W/L)_p}{(W/L)_n}$ needed if $\mu_n = 3\,\mu_p$, to keep the same symmetry.

Note: No Python needed for the final ratio; you may still provide a code snippet for demonstration.

7.4.10 Problem 10: PMOS vs. NMOS Sizing to Achieve Balanced Delay

Consider a CMOS inverter with supply voltage $V_{DD} = 1.8\,\text{V}$. For a target rise and fall time to be equal, you size the PMOS to be 2.5× larger (in W/L) than the NMOS because $\mu_n \approx 2.5\,\mu_p$. Suppose the NMOS device has $(W/L)_n = 2$.

1. Determine $(W/L)_p$.
2. Assuming each device is in saturation at the switching instant and ignoring channel-length modulation, compute the drain current if $(V_{GS} - V_{th}) = 0.8\,\text{V}$ for both. Assume $k_n = \mu_n C_{\text{ox}} = 50\,\mu\text{A/V}^2$; hence $k_p = k_n \times \frac{\mu_p}{\mu_n} = 50/2.5 = 20\,\mu\text{A/V}^2$.
3. Show that the two currents match if sized appropriately.

7.4.11 Problem 11: Enhancement vs. Depletion MOSFETs

Explain the difference between *enhancement-mode* and *depletion-mode* MOSFETs. Why are enhancement-mode transistors more commonly used in modern CMOS processes?

7.4.12 Problem 12: Body Effect vs. Source Tied to Substrate

Discuss how tying the source and substrate together eliminates the body effect in an NMOS transistor. Under what conditions might a designer allow a non-zero V_{SB}?

7.4.13 Problem 13: Short-Channel Effects

As MOSFET channel lengths shrink below a micron, short-channel effects become significant. List two short-channel effects and briefly describe how they impact device operation.

7.4.14 Problem 14: PMOS in a Well (Twin-Well Processes)

Describe why in a typical CMOS twin-well (or twin-tub) process, the PMOS device is placed in an n-well while the NMOS is placed in a p-substrate. How does this arrangement help with isolating the devices?

7.4.15 Problem 15: Threshold Voltage Variation with Temperature

Qualitatively discuss how the MOSFET threshold voltage varies with temperature and the typical impact on circuit performance.

7.4.16 Problem 16: Differences Between NMOS and PMOS Body Diodes

Each MOSFET inherently has a body diode between the source and substrate (and between drain and substrate if source and substrate are tied). Compare why the NMOS body diode is forward-biased with negative substrate potential, whereas the PMOS body diode is forward-biased with positive substrate potential.

7.4.17 Problem 17: Subthreshold Slope

Define the subthreshold slope S in an MOSFET and explain how it relates to the factor n in the subthreshold current equation. Why is there a fundamental limit on how small the subthreshold slope can be at room temperature?

7.4.18 Problem 18: Channel Formation in NMOS vs. PMOS

Explain how channel formation differs between an NMOS and a PMOS transistor in enhancement mode. Specifically, what type of carriers form the channel in each device, and from which doping region do they originate?

7.4.19 Problem 19: MOSFET as a Voltage-Controlled Current Source

Why is the MOSFET often described as a voltage-controlled current source in saturation? Under what condition does it behave more like a resistor?

7.4.20 Problem 20: Impact of Gate Oxide Thickness on MOSFET Operation

Discuss how reducing the gate oxide thickness t_{ox} in a MOSFET affects:

1. The gate capacitance C_{ox}.
2. The threshold voltage.
3. Short-channel effects (qualitatively).

8 Solutions to problems

8.1 Semiconductor Basics: Solution Set 1

8.1.1 Solution 1: Resistivity and Carrier Density Relationship

From the resistivity equation:

$$\rho = \frac{1}{q\mu n}$$

where:

- q is the charge of an electron,
- μ is the mobility of carriers,
- n is the carrier concentration.

If n increases (more free carriers), the resistivity ρ decreases. Conversely, if n decreases, ρ increases. This tunability is a key feature of semiconductors.

8.1.2 Solution 2: Calculating the Resistivity of a Semiconductor

Intrinsic conductivity:

$$\sigma = q(n_i\mu_n + n_i\mu_p)$$

Resistivity:

$$\rho = \frac{1}{\sigma}$$

See Python script `set1_prob2.py`.

8.1.3 Solution 3: Calculating Conductivity for Doped Silicon

Use:

$$\sigma = qN_D\mu_n$$

See script `set1_prob3.py` for solution.

8.1.4 Solution 4: Band Gap Calculation from Optical Absorption

Use:

$$E_g = \frac{hc}{\lambda}$$

See script `set1_prob4.py` for solution.

8.1.5 Solution 5: Energy Band Diagrams Interpretation

- The **valence band** contains bound electrons.
- The **conduction band** contains free electrons available for conduction.
- The **band gap** is the energy required for an electron to move from the valence band to the conduction band.

8.1.6 Solution 6: Doping and Fermi Level Shifts

- **N-type**: Fermi level moves closer to the conduction band.
- **P-type**: Fermi level moves closer to the valence band.

8.1.7 Solution 7: Diode Ideal Current Equation Verification

Use:

$$I = I_0 \left(e^{V/V_T} - 1 \right)$$

See script `set1_prob7.py` for solution.

8.1.8 Solution 8: Plotting the I-V Characteristics of a Diode

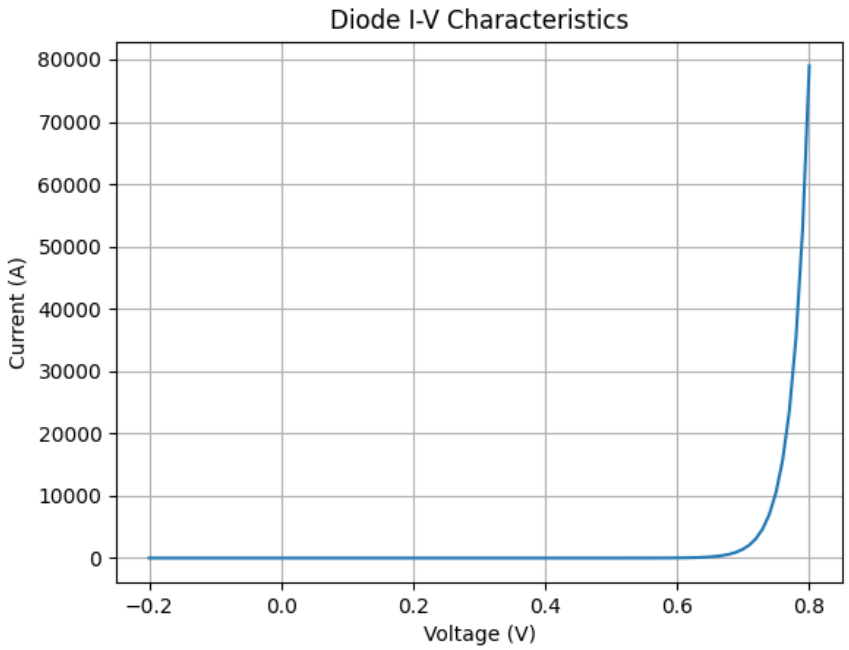

Figure 1: Solution for problem 8. See script `set1_prob8.py` for solution details.

8.1.9 Solution 9: Reverse Bias in a Diode

A reverse-biased diode blocks current, with only a small leakage due to minority carriers.

8.1.10 Solution 10: Zener Breakdown Calculation

Use:

$$I = \frac{(V_{supply} - V_Z)}{R}$$

See script `set1_prob10.py` for solution.

8.1.11 Solution 11: Carrier Concentration Calculation

The mass action law states:

$$np = n_i^2$$

For n-type material:

$$n \approx N_D, \quad p = \frac{n_i^2}{N_D}$$

See script `set1_prob11.py` for solution.

8.1.12 Solution 12: Diode Small-Signal Resistance

Small-signal resistance:

$$r_d = \frac{V_T}{I}$$

See script `set1_prob12.py` for solution.

8.1.13 Solution 13: Temperature Dependence of Band Gap

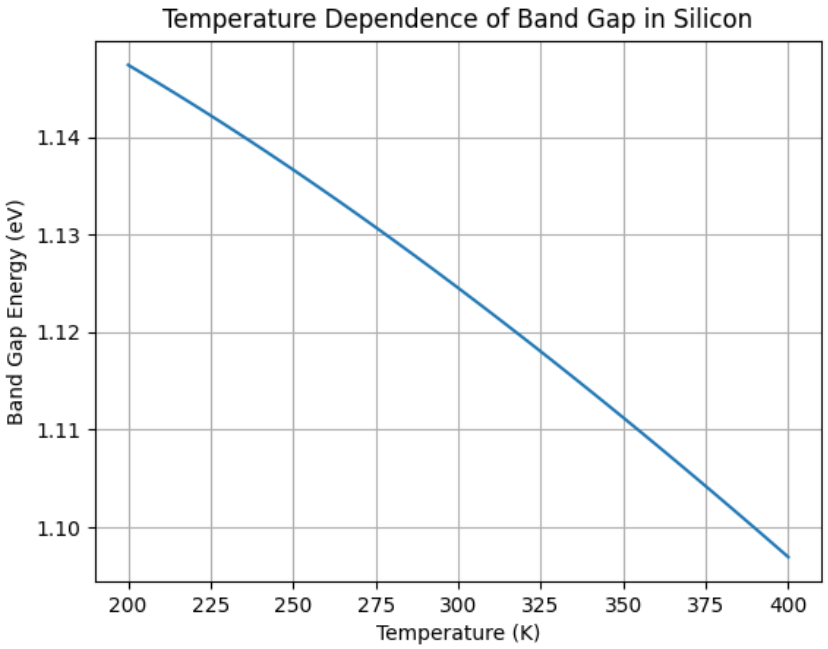

Figure 2: Solution for problem 13. See script `set1_prob13.py` for solution details.

8.1.14 Solution 14: PN Junction Capacitance

Use:

$$C_j = \frac{\epsilon}{W}$$

See script `set1_prob14.py` for solution.

8.1.15 Solution 15: MOSFET Threshold Voltage

This equation models the voltage needed to create an inversion layer in a MOSFET.

Derivation of the MOSFET Threshold Voltage Equation:

The threshold voltage V_T of a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is the minimum gate-to-source voltage (V_{GS}) required to form a conductive inversion layer at the semiconductor-oxide interface. It is derived as follows:

Step 1: Define the Energy Bands and Work Functions

A MOS capacitor consists of a metal, an insulator (oxide), and a semiconductor. The work function difference between the metal and the semiconductor determines the *flatband voltage* (V_{FB}), which is given by:

$$V_{FB} = \Phi_M - \Phi_S$$

where:

- Φ_M is the metal work function,
- Φ_S is the semiconductor work function.

Step 2: Define the Fermi Potential (ϕ_F)

The Fermi potential ϕ_F describes the difference in energy between the intrinsic Fermi level and the Fermi level in a doped semiconductor:

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \quad \text{(for p-type)}$$

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right) \quad \text{(for n-type)}$$

where:

- k is Boltzmann's constant,
- T is temperature,
- q is the electron charge,
- N_A and N_D are the acceptor and donor concentrations,
- n_i is the intrinsic carrier concentration.

For an *n-channel MOSFET*, which uses a p-type substrate, inversion occurs when the surface potential ψ_S reaches $2\phi_F$, where

$$\psi_S = 2\phi_F$$

This condition ensures that the surface electron concentration equals the bulk hole concentration, forming an inversion layer.

Step 3: Depletion Charge (Q_d)

The depletion charge per unit area Q_d arises due to the ionized acceptors in the depletion region. Using Gauss's law, it is given by:

$$Q_d = \sqrt{2q\epsilon_s N_A 2\phi_F}$$

where ϵ_s is the permittivity of the semiconductor.

Step 4: Gate-Oxide Capacitance (C_{ox})

The gate-oxide capacitance per unit area is:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

where:

- ϵ_{ox} is the permittivity of the oxide layer,
- t_{ox} is the oxide thickness.

Step 5: Expressing the Threshold Voltage

The threshold voltage V_T must account for:

1. Flatband Voltage (V_{FB}): The voltage required to align the bands.
2. Surface Potential ($2\phi_F$): The potential needed to invert the surface.
3. Charge Influence (Q_d/C_{ox}): The effect of the depletion charge.

Thus, the total threshold voltage is:

$$V_T = V_{FB} + 2\phi_F + \frac{Q_d}{C_{ox}}$$

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2q\epsilon_s N_A 2\phi_F}}{C_{ox}}$$

Conclusion

This equation expresses the threshold voltage in terms of fundamental material and process parameters, showing how the work functions, Fermi potential, depletion charge, and oxide capacitance contribute to determining the voltage required to turn on a MOSFET.

8.1.16 Solution 16: Bipolar Junction Transistor Current Gain

Use:

$$\beta = \frac{5 \times 10^{-3}}{50 \times 10^{-6}} = 100$$

See script `set1_prob16.py` for solution.

8.1.17 Solution 17: LED Emission Wavelength

Use:

$$\lambda = \frac{hc}{E_g}$$

See script `set1_prob17.py` for solution.

8.1.18 Solution 18: Solar Cell Efficiency Calculation

Use:

$$\eta = \frac{P_{out}}{P_{in}} \times 100\%$$

See script `set1_prob18.py` for solution.

8.1.19 Solution 19: Schottky Diode Behavior

Compared to a PN junction diode,

- The Schottky diode forms a junction between a metal and a semiconductor.
- It has a lower forward voltage drop (0.3V vs. 0.7V for Si).
- Faster response time due to majority carrier conduction.

8.1.20 Solution 20: Semiconductor Fabrication Process

1. **Lithography**: Defines circuit patterns on a wafer.
2. **Oxidation**: Grows SiO_2 for insulation.
3. **Doping**: Introduces impurities to alter carrier concentration.
4. **Etching**: Removes unwanted material.
5. **Deposition**: Adds metal or dielectric layers.
6. **Packaging**: Encapsulates the chip for protection.

8.1.21 Solution 21: Computing and Plotting MOSFET Threshold Voltage

Step 1: Compute the Fermi Potential ϕ_F

The Fermi potential for a p-type semiconductor is:

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

where:

- $k = 1.38 \times 10^{-23}$ J/K (Boltzmann's constant),
- $T = 300$ K,
- $q = 1.6 \times 10^{-19}$ C (electron charge),
- $n_i = 1.5 \times 10^{10}$ cm^{-3} (intrinsic carrier concentration for Si).

Step 2: Compute the Depletion Charge Q_d

$$Q_d = \sqrt{2q\epsilon_s N_A 2\phi_F}$$

Step 3: Compute the Oxide Capacitance per Unit Area C_{ox}

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

Step 4: Compute the Threshold Voltage V_T

$$V_T = V_{FB} + 2\phi_F + \frac{Q_d}{C_{ox}}$$

Discussion:

- The plot shows how V_T increases with increasing doping concentration N_A.
- Higher doping leads to a larger depletion charge Q_d, requiring a higher gate voltage to induce inversion.
- This trend is crucial in **MOSFET design**, as adjusting N_A allows engineers to *tune* V_T for different applications.

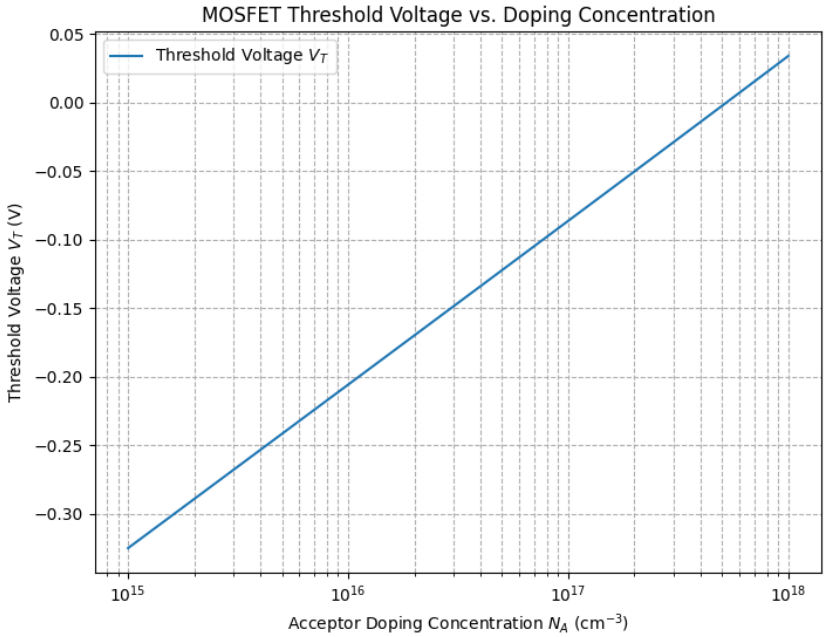

Figure 3: Solution for problem 21. See script `set1_prob21.py` for solution details.

8.2 Semiconductor Basics: Solution Set 2

8.2.1 Solution 1: Wire Resistance Calculation

Use the following formulas:

Wire Resistance:

$$R = \frac{\rho L}{A} = \frac{(1.68 \times 10^{-8}\,\Omega \cdot \text{m})(2\text{ m})}{1 \times 10^{-6}\text{ m}^2} = 3.36 \times 10^{-2}\,\Omega.$$

Voltage Drop:

$$V = IR = (1\text{ A})(0.0336\,\Omega) = 0.0336\text{ V}.$$

See script `set2_prob1.py` for solution.

8.2.2 Solution 2: Intrinsic Carrier Concentration and Doping

1. **Electron Concentration** (approx.)

$$n \approx N_D = 1 \times 10^{16}\,\text{cm}^{-3}.$$

2. **Hole Concentration**

$$p = \frac{n_i^2}{n} = \frac{(1 \times 10^{10})^2}{1 \times 10^{16}} = \frac{1 \times 10^{20}}{1 \times 10^{16}} = 1 \times 10^4\,\text{cm}^{-3}.$$

3. Convert n to m^{-3}

$$1\,\text{cm}^{-3} = 10^6\,\text{m}^{-3}.$$

$$n = 1 \times 10^{16}\,\mathrm{cm}^{-3} \times 10^{6}\,\mathrm{m}^{-3}/\mathrm{cm}^{-3} = 1 \times 10^{22}\,\mathrm{m}^{-3}.$$

See script `set2_prob2.py` for solution.

8.2.3 Solution 3: Determining Fermi Level Shift with Doping

$$E_F - E_{Fi} = 0.0259 \times \ln\left(\frac{10^{15}}{10^{10}}\right) = 0.0259 \times \ln(10^5).$$

$$\ln(10^5) = 5\ln(10) \approx 5 \times 2.3026 = 11.513.$$

$$E_F - E_{Fi} \approx 0.0259 \times 11.513 = 0.298\ \mathrm{eV}\ (\text{approximately}).$$

See script `set2_prob3.py` for solution.

8.2.4 Solution 4: Diode I–V Characteristic (Ideal Diode)

1. Diode Current at $V_D = 0.7$ V

$$I_D = 10^{-14}\left(e^{\frac{0.7}{0.025}} - 1\right).$$

Numerically, $\frac{0.7}{0.025} = 28$. Thus,

$$I_D \approx 10^{-14}\left(e^{28} - 1\right).$$

$e^{28} \approx 1.446 \times 10^{12}$, so

$$I_D \approx 10^{-14} \times 1.446 \times 10^{12} = 1.446 \times 10^{-2}\,\mathrm{A} = 0.01446\,\mathrm{A}.$$

2. Plotting I–V

We vary V_D from 0 to 1 V, compute I_D, and plot.

8.2.5 Solution 5: Non-Ideal Diode with Ideality Factor

1. Current with $n = 2$

$$I_D = 10^{-14}\left(e^{\frac{0.7}{2\times 0.025}} - 1\right).$$

$\frac{0.7}{0.05} = 14$. Hence,

$$e^{14} \approx 1.2026 \times 10^{6},$$

so

$$I_D \approx 10^{-14}\left(1.2026 \times 10^{6} - 1\right) \approx 1.2026 \times 10^{-8}\,\mathrm{A}.$$

2. Comparison with $n = 1$

From Problem 4, the current was about 0.01446 A at the same voltage. We see the non-ideal diode (with $n = 2$) has a *much smaller* current at the same forward voltage.

See script `set2_prob5.py` for solution.

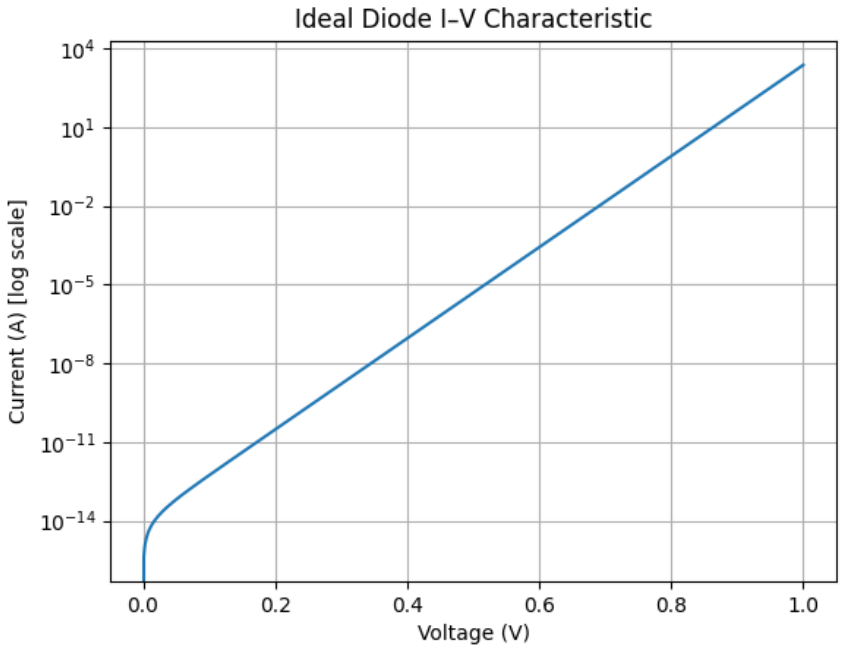

Figure 4: Solution for problem 4. See script `set2_prob4.py` for solution details.

8.2.6 Solution 6: Series Resistance Effect in a Diode

We must solve for I_D in the equation

$$I_D = I_s \left(e^{\frac{V_D - I_D R_s}{V_T}} - 1 \right).$$

This is implicitly defined because I_D appears on both sides. We can do a simple iterative approach or use a root-finding method.

In practice, you might use a more sophisticated solver like *scipy.optimize* to converge more reliably.

8.2.7 Solution 7: Carrier Density vs. Temperature

- Compute $n_i(T)$ at each temperature point.
- Use appropriate constants in eV and convert to correct units if needed.
- Plot on a linear or log scale.

8.2.8 Solution 8: Measuring Resistivity with Four-Point Probe

Use:

$$\rho = 200\,\Omega/\square \times 5 \times 10^{-2}\ \text{cm} = 10\,\Omega \cdot \text{cm}.$$

See script `set2_prob8.py` for solution.

8.2.9 Solution 9: Tunneling Diode Current Approximation

1. **Peak Current**

$$I_p = J_p \times \text{Area} = 100\,\frac{\text{A}}{\text{cm}^2} \times 0.01\,\text{cm}^2 = 1\ \text{A}.$$

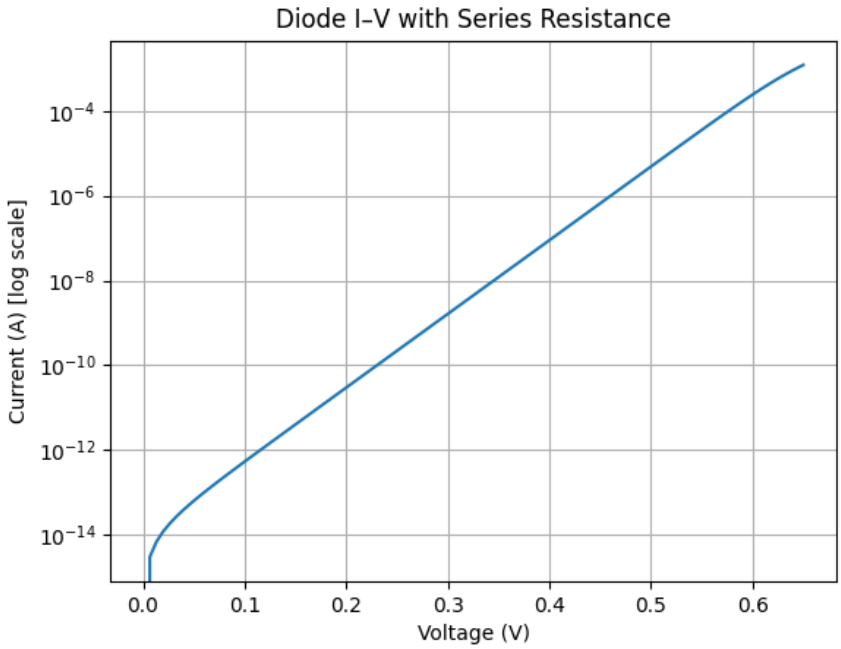

Figure 5: Solution for problem 6. See script `set2_prob6.py` for a solution.

2. **Power at Peak Voltage**

$$P_p = I_p \times V_p = 1\text{ A} \times 0.3\text{ V} = 0.3\text{ W}.$$

See script `set2_prob9.py` for solution.

8.2.10 Solution 10: Non-Linear (Tunable) Resistor Model

1. **Resistance vs. Voltage**

$$R(V) = \frac{1000\,\Omega}{1 + 5V^2}.$$

2. **Current at 10 V**

$$R(10) = \frac{1000}{1 + 5 \times 10^2} = \frac{1000}{1 + 500} = \frac{1000}{501} \approx 1.996\,\Omega.$$

$$I = \frac{V}{R(10)} = \frac{10}{1.996} \approx 5.01\text{ A}.$$

8.2.11 Solution 11: Qualitative: Electrons vs. Holes in Semiconductors

- **Electrons** are negative charge carriers residing in the conduction band. Holes are the absence of electrons in the valence band and act as positive charge carriers.
- The **effective mass** depends on the curvature of the energy bands; the valence band's curvature often leads to a larger effective mass for holes, leading to lower mobility compared to electrons in many semiconductors.
- **Mobility** also depends on scattering mechanisms; holes (in the valence band) generally encounter different scattering processes and have lower mobility than electrons.

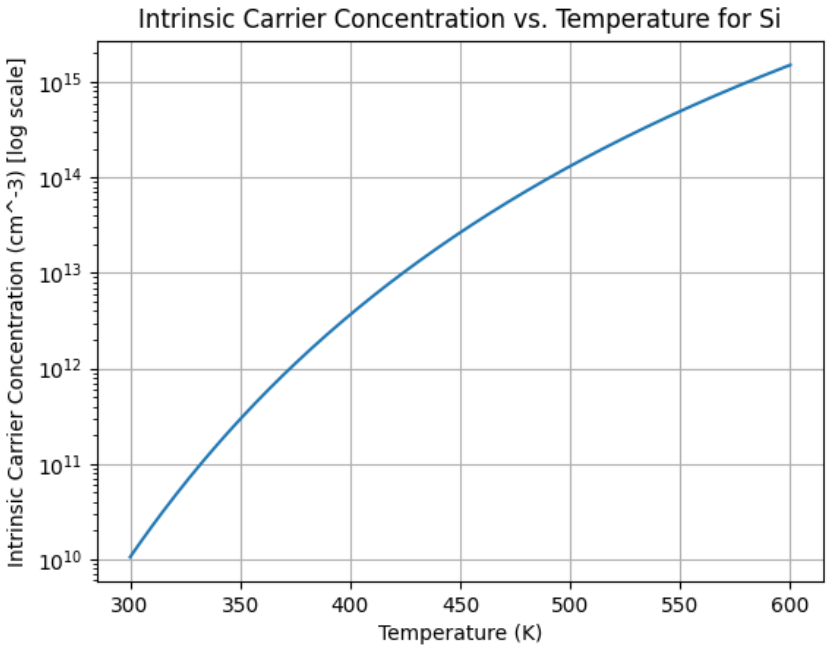

Figure 6: Solution for problem 7. See script `set2_prob7.py` for solution details.

8.2.12 Solution 12: Band Gap Types: Direct vs. Indirect

- **Direct band gap**: Conduction band minimum and valence band maximum occur at the same crystal momentum (k). Example: Gallium arsenide (GaAs). Efficient radiative recombination → used in LEDs, lasers.
- **Indirect band gap**: Conduction band minimum and valence band maximum occur at different k-values. Example: Silicon. Less efficient light emission → commonly used for electronic, not for bright LEDs.

8.2.13 Solution 13: Zener Diode Breakdown

- **Zener diodes** are heavily doped p–n junctions that exhibit a sharp breakdown at a well-defined reverse voltage (the Zener voltage).
- In **Zener breakdown** (<5–6 V typically), quantum tunneling of electrons from the valence band of the p-side to the conduction band of the n-side dominates.
- The doping levels set the electric field needed for breakdown, leading to a stable, repeatable breakdown voltage. Higher doping lowers breakdown voltage. Thus, typical Zener diodes range from about 2 V up to a few hundred volts.

8.2.14 Solution 14: LED vs. Normal Diode

- An **LED** is made from direct band gap materials (e.g., GaAs, GaN). Electron-hole recombination releases energy as photons.
- A **normal diode** (often silicon) has an indirect band gap; most recombinations are non-radiative (heat). Hence, no visible light is emitted.

8.2.15 Solution 15: Forward and Reverse Bias in a p–n Junction

- **Forward Bias**: p-side is at higher potential. Depletion region narrows, carriers are injected across the junction, significant current flows once above the threshold ($\sim 0.7\,\text{V}$ in silicon).
- **Reverse Bias**: n-side is at higher potential. Depletion region widens, only a small leakage current flows. Above a large reverse voltage, breakdown can occur (Zener or avalanche).

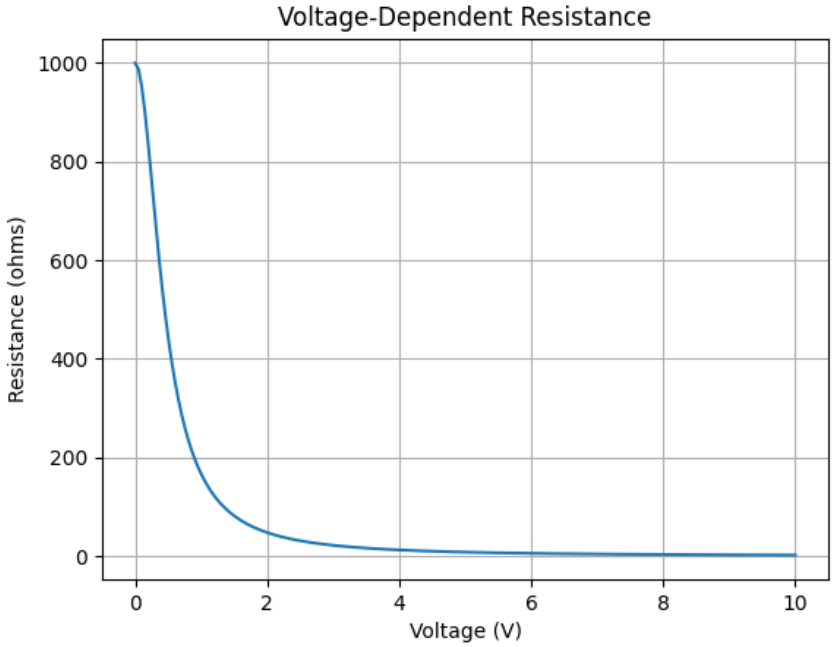

Figure 7: Solution for problem 10. See script `set2_prob10.py` for solution details.

8.2.16 Solution 16: Ideal vs. Real Diode Equation Parameters

- **Ideal diode equation**: $I_D = I_s(\exp(V_D/V_T) - 1)$.
- **Real diode** adds:

  Series resistance (R_s) from bulk semiconductor and contacts, reducing current at higher forward bias. **Shunt resistance** (R_{sh}) modeling leakage pathways that increase reverse current. **Ideality factor** (n) > 1 to account for recombination and other non-ideal effects.

8.2.17 Solution 17: Depletion Capacitance in a Diode

- In **reverse bias**, the diode forms a capacitor-like structure with the depletion region acting as the dielectric. The p- and n-regions form the capacitor plates.
- **Capacitance** is inversely proportional to the width of the depletion region. As reverse bias increases, depletion width grows and capacitance *decreases*. Typically described by $C_j \propto \frac{1}{\sqrt{V_{bias}}}$ for abrupt junctions.

8.2.18 Solution 18: Short vs. Long Diodes (Diode Length Effects)

- If the p–region is *shorter* than the carrier diffusion length, carriers injected from the n–region can easily reach the ohmic contact on the p–side without recombining, reducing series resistance and potentially affecting the forward conduction.
- *Longer* diodes have more recombination within the neutral regions, which can alter the ideality factor and the saturation current.

8.2.19 Solution 19: Non-Idealities: Recombination–Generation Currents

- **Recombination–generation** (R–G) currents dominate the *mid-voltage* range (forward bias less than 0.5–0.6 V in silicon) and also contribute to reverse leakage.
- In the depletion region, carriers can recombine via mid-gap states, affecting the diode's slope in that intermediate bias region. Hence, the ideality factor n can be closer to 2 instead of 1 in that regime.

8.2.20 Solution 20: Tunable Resistor vs. Diode Behavior

- A **tunable resistor** typically maintains a symmetrical conduction path—its operation changes resistance with a control parameter (voltage on a gate, doping level, etc.) but does not create a p–n junction asymmetry.
- A **diode** has a built-in asymmetry (p–n junction) that allows current to flow readily in one direction (forward) and restricts current in the opposite (reverse). This asymmetry is the hallmark of rectification.

8.3 Transistor Basics: Solution Set 3

8.3.1 Solution 1: History of the Transistor

The invention of the transistor revolutionized electronics by enabling miniaturization, lower power consumption, and higher reliability compared to vacuum tubes. The first transistor was created in 1947 by Bardeen, Brattain, and Shockley at Bell Labs, leading to the 1956 Nobel Prize in Physics. The later development of MOSFETs enabled the creation of CMOS technology, which forms the foundation of modern digital circuits.

8.3.2 Solution 2: MOSFET Structure and Operation

A MOSFET consists of a **gate**, **source**, **drain**, and **substrate**. The three operational regions are:

- **Cutoff region**: $V_G < V_T$, no conduction.
- **Linear region**: $V_G > V_T$ and V_{DS} is small, where current increases linearly with V_{DS}.
- **Saturation region**: $V_G > V_T$ and $V_{DS} > V_{DS,sat}$, where current is constant.

8.3.3 Solution 3: CMOS Inverter Logic

A CMOS inverter consists of:

- **pMOS transistor**: Conducts when $V_{in} = 0$.
- **nMOS transistor**: Conducts when $V_{in} = V_{DD}$.
- When $V_{in} = 0$, pMOS is ON and nMOS is OFF, output $V_{out} = V_{DD}$.
- When $V_{in} = V_{DD}$, pMOS is OFF and nMOS is ON, output $V_{out} = 0$.

8.3.4 Solution 4: Calculating MOSFET Drain Current in the Linear Region

Using the linear region equation:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_G - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

See script `set3_prob4.py` for solution.

8.3.5 Solution 5: Plotting MOSFET I-V Characteristics

8.3.6 Solution 6: Threshold Voltage and Scaling

Reducing channel length leads to:

- **Lower threshold voltage** due to drain-induced barrier lowering (DIBL).
- **Increased leakage current** due to subthreshold conduction.

8.3.7 Solution 7: Subthreshold Current Calculation

Use:

$$I_D = I_{D0} \times 10^{(V_G - V_T)/S}$$

See script `set3_prob7.py` for solution.

8.3.8 Solution 8: Comparing NMOS and PMOS Characteristics

Electron mobility (μ_n) is typically 2-3 times higher than hole mobility (μ_p), leading to lower current in PMOS for the same W/L.

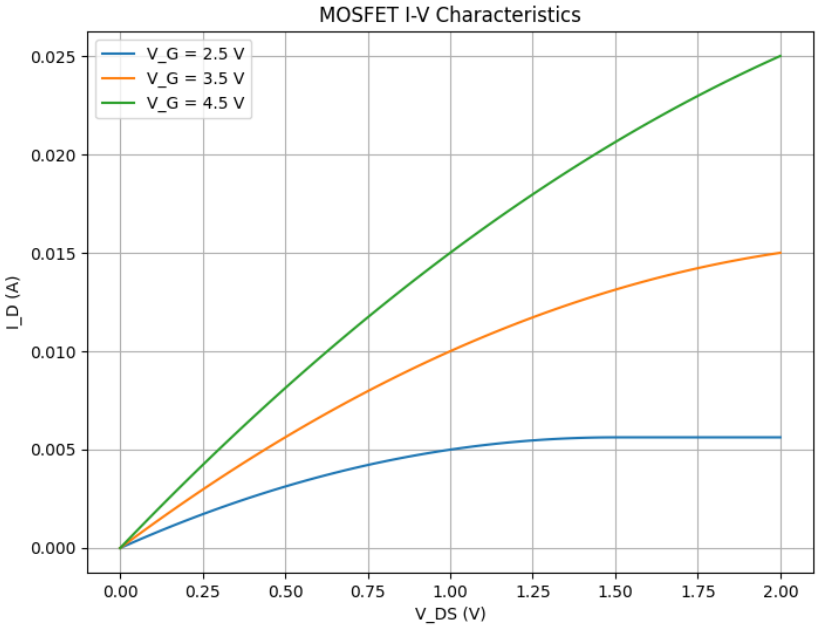

Figure 8: Solution for problem 5. See script `set3_prob5.py` for solution details.

8.3.9 Solution 9: Calculating Drain Current in the Saturation Region

Using the saturation current equation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_G - V_T)^2$$

See script `set3_prob9.py` for solution.

8.3.10 Solution 10: CMOS Power Consumption

Dynamic power is given by:

$$P = C_L V_{DD}^2 f$$

See script `set3_prob10.py` for solution.

8.3.11 Solution 11: CMOS Inverter Transfer Characteristics

8.3.12 Solution 12: Short-Channel vs. Long-Channel MOSFET Effects

- **Short-Channel Effects (SCE)** reduce threshold voltage due to Drain-Induced Barrier Lowering (DIBL).
- Increased electric fields cause velocity saturation and leakage currents, leading to higher off-state power consumption.
- Long-channel MOSFETs do not suffer from these issues and operate closer to the ideal square-law model.

8.3.13 Solution 13: Leakage Currents in Modern MOSFETs

- **Subthreshold leakage**: Exponential dependence on V_G.
- **Gate leakage**: Due to quantum tunneling through the gate oxide.

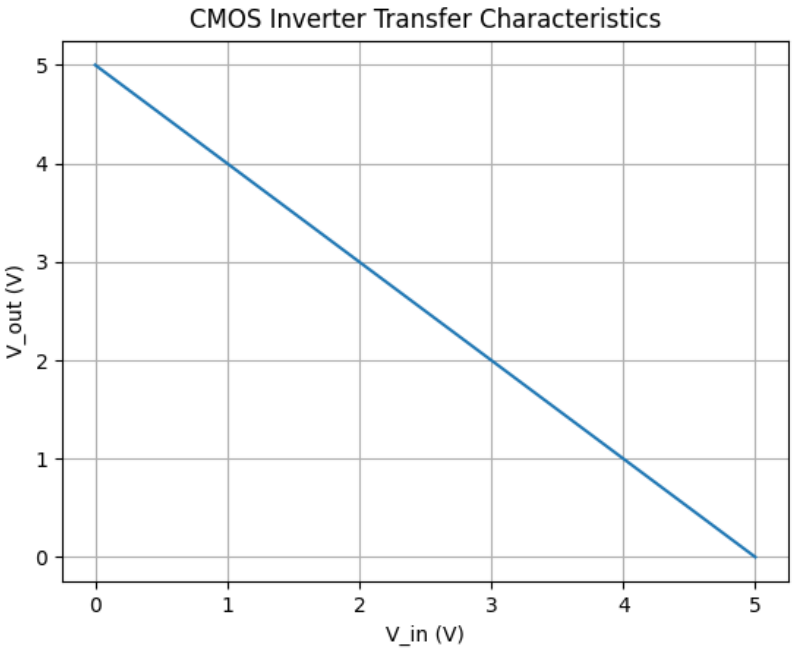

Figure 9: Solution for problem 11. See script `set3_prob11.py` for solution details.

- **Junction leakage**: Due to reverse bias of source/drain junctions.
- **Drain-induced barrier lowering (DIBL)**: Reduces V_T and increases leakage.

8.3.14 Solution 14: Effect of Temperature on MOSFET Performance

8.3.15 Solution 15: Body Effect in MOSFETs

The body effect describes how V_T increases with V_{SB}.

$$V_T' = V_T0 + \gamma(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F})$$

where:

- V_T0 is the threshold voltage at $V_{SB} = 0$,
- γ is the body effect coefficient.

In greater detail, the *body effect* describes how the threshold voltage (V_T) of a MOSFET changes due to a nonzero source-to-body voltage (V_{SB}). This occurs because the depletion region of the MOSFET depends on the *potential difference* between the source and the substrate.

Step 1: Understanding the Threshold Voltage

The threshold voltage of a MOSFET is given by:

$$V_T = V_{FB} + 2\phi_F + \frac{Q_d}{C_{ox}}$$

where:

- V_{FB} is the flat-band voltage,
- ϕ_F is the Fermi potential,

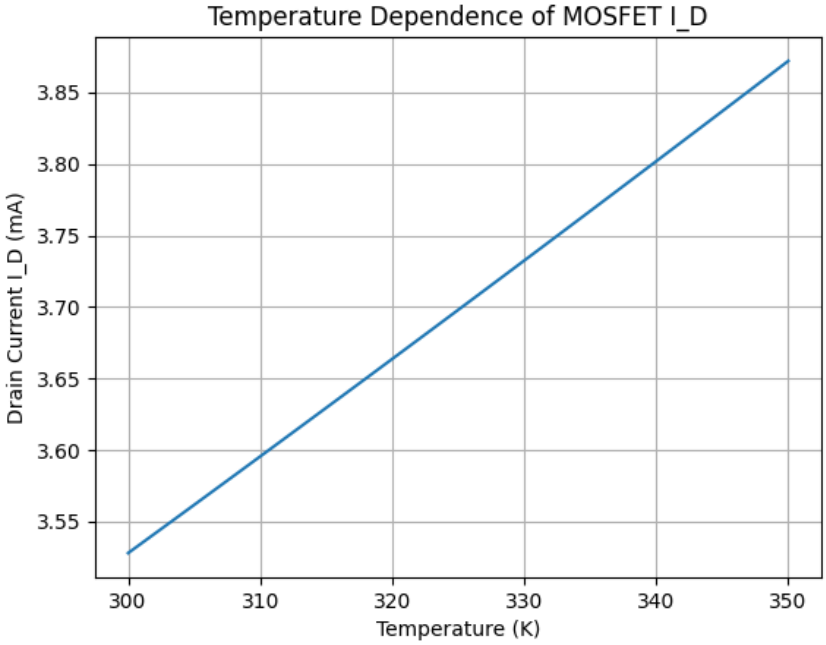

Figure 10: Solution for problem 14. See script `set3_prob14.py` for solution details.

- Q_d is the depletion charge per unit area,
- C_{ox} is the oxide capacitance per unit area.

Step 2: Depletion Charge Approximation

The depletion charge per unit area is given by:

$$Q_d = \sqrt{2q\epsilon_s N_A(2\phi_F + V_{SB})}$$

where:

- q is the electron charge,
- ϵ_s is the permittivity of the semiconductor,
- N_A is the acceptor doping concentration,
- $2\phi_F$ is the built-in potential of the depletion region,
- V_{SB} is the source-to-body voltage.

Since the depletion charge appears in the threshold voltage equation:

$$V_T' = V_T0 + \frac{\sqrt{2q\epsilon_s N_A(2\phi_F + V_{SB})}}{C_{ox}}$$

where V_T0 is the threshold voltage when $V_{SB} = 0$.

Step 3: Defining the Body Effect Coefficient

We define the body effect coefficient γ as:

$$\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}}$$

Using this definition, we rewrite the threshold voltage equation:

$$V_T' = V_T0 + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

Step 4: Interpretation of the Equation

- γ determines how *strongly* the substrate affects V_T.
- V_T *increases* as V_{SB} increases (stronger inversion is needed).
- The term $\sqrt{2\phi_F + V_{SB}}$ accounts for the *increased depletion width* at the interface.

This equation is widely used in MOSFET modeling to determine how changes in the substrate bias impact transistor operation.

Conclusion

The final equation for the body effect is:

$$V_T' = V_T0 + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

This describes how the threshold voltage increases when a positive source-to-body bias is applied (in n-channel MOSFETs), or decreases for a negative bias (in p-channel MOSFETs).

8.3.16 Solution 16: Oxide Thickness and Threshold Voltage

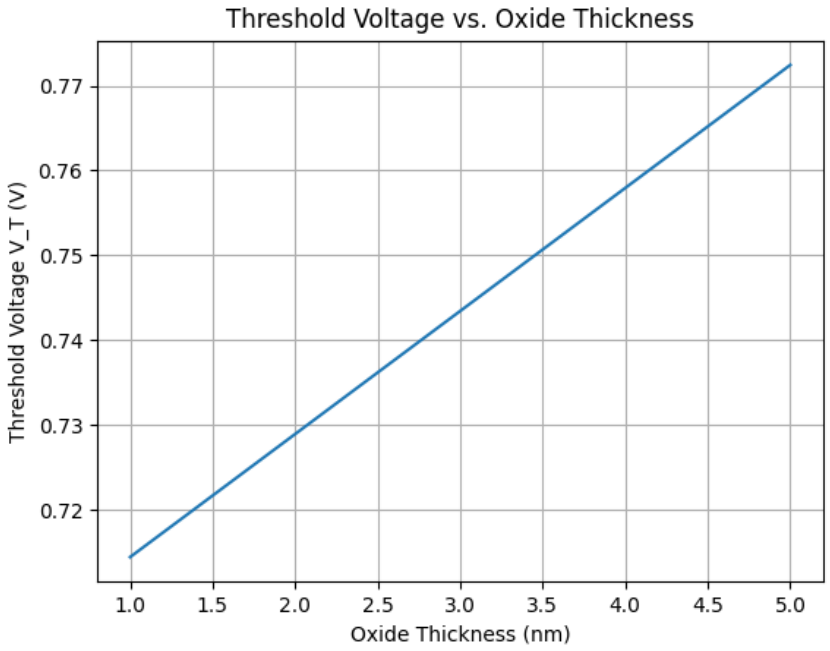

Figure 11: Solution for problem 16. See script `set3_prob16.py` for solution details.

Some notes:

- The choice of V_{T0} depends on device scaling and doping.
- *Smaller* t_{ox} results in *higher* C_{ox}, thereby *reducing* V_T.
- This trend is essential for understanding MOSFET scaling in modern IC design.

8.3.17 Solution 17: Subthreshold Slope Plot

The **subthreshold current** follows an *exponential* relationship:

$$I_D = I_{D0} \times 10^{(V_{GS}-V_T)/S}$$

where:

- I_D0 = Drain current at $V_{GS} = V_T$,
- S = Subthreshold slope in volts (converted to natural log base),
- V_GS = Gate-source voltage.

Since $S = 80$ mV/decade, we convert it to natural log (ln) form:

$$I_D = I_{D0} \times e^{\frac{(V_{GS}-V_T)}{S'}}$$

where:

$$S' = \frac{S}{\ln(10)}$$

$$S' = \frac{80 \times 10^{-3}}{\ln(10)} = 34.7 \text{ mV}$$

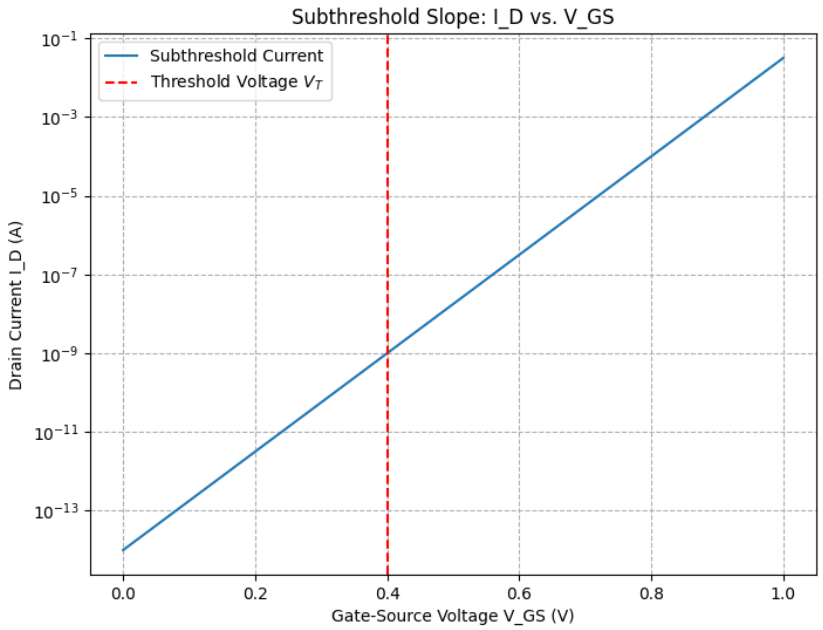

Figure 12: Solution for problem 17. See script `set3_prob17.py` for numerical solution details.

8.3.18 Solution 18: CMOS vs. NMOS Logic

- **Lower power consumption**: CMOS has no static power dissipation.
- **Better noise margins**: Symmetric pull-up and pull-down networks.
- **Higher packing density**: Less area than NMOS-only logic.

8.3.19 Solution 19: Body Effect Equation Derivation

Using depletion charge analysis:

$$V_T' = V_T0 + \gamma(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F})$$

where:

- $\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}}$,
- $\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$.

The *body effect* describes how the threshold voltage (V_T) of a MOSFET changes due to a nonzero source-to-body voltage (V_{SB}). This occurs because the depletion region of the MOSFET depends on the *potential difference* between the source and the substrate.

Step 1: Understanding the Threshold Voltage

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where:

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- Q_d is the depletion charge per unit area,
- C_{ox} is the oxide capacitance per unit area.

Step 2: Depletion Charge Approximation

The depletion charge per unit area is given by:

$$Q_d = \sqrt{2q\epsilon_s N_A(2\phi_F + V_{SB})}$$

where:

- q is the electron charge,
- ϵ_s is the permittivity of the semiconductor,
- N_A is the acceptor doping concentration,
- $2\phi_F$ is the built-in potential of the depletion region,
- V_{SB} is the source-to-body voltage.

Since the depletion charge appears in the threshold voltage equation:

$$V_T' = V_T0 + \frac{\sqrt{2q\epsilon_s N_A(2\phi_F + V_{SB})}}{C_{ox}}$$

where V_T0 is the threshold voltage when $V_{SB} = 0$.

Step 3: Defining the Body Effect Coefficient

We define the body effect coefficient γ as:

$$\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}}$$

Using this definition, we rewrite the threshold voltage equation:

$$V_T' = V_T0 + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

Step 4: Interpretation of the Equation

- γ determines how *strongly* the substrate affects V_T.
- V_T *increases* as V_{SB} increases (stronger inversion is needed).
- The term $\sqrt{2\phi_F + V_{SB}}$ accounts for the *increased depletion width* at the interface.

This equation is widely used in MOSFET modeling to determine how changes in the substrate bias impact transistor operation.

Conclusion

The final equation for the body effect is:

$$V_T' = V_T0 + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

This describes how the threshold voltage increases when a positive source-to-body bias is applied (in n-channel MOSFETs), or decreases for a negative bias (in p-channel MOSFETs).

8.3.20 Solution 20: Drain Current for Different Oxide Thicknesses

- **Smaller oxide thickness t_{ox}** → **Higher C_{ox}** → **Increased I_D**. - **Larger oxide thickness t_{ox}** → **Lower C_{ox}** → **Reduced I_D**.

This matches **MOSFET scaling trends**, where **reducing t_{ox}** improves drive current but increases leakage concerns.

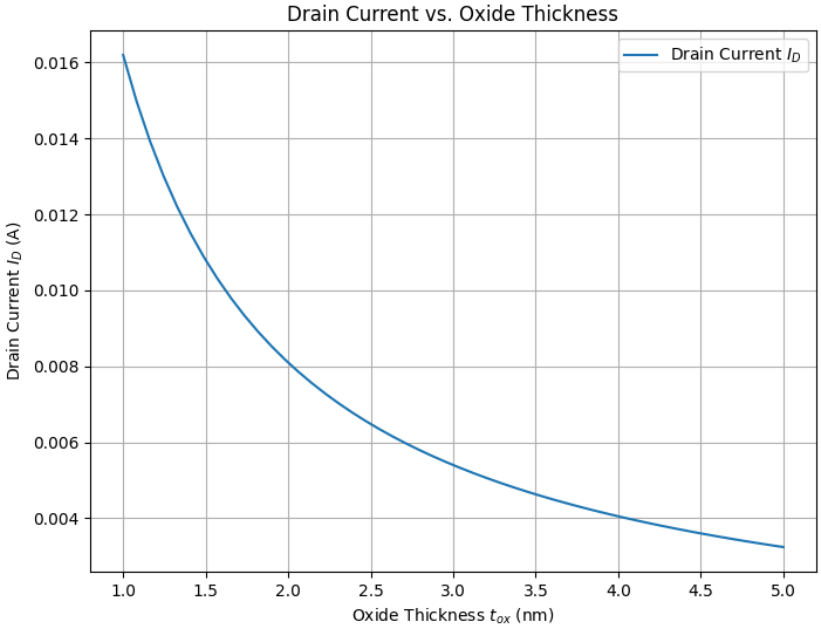

Figure 13: Solution for problem 20. See script `set3_prob20.py` for solution details.

8.4 Transistor Basics: Solution Set 4

8.4.1 Solution 1: NMOS Drain Current in Saturation

1. Drain Current Calculation

$$(V_{GS} - V_{th}) = (2.5 - 1.0) = 1.5\,\text{V}.$$

$$I_D = \frac{1}{2} \times 0.04\,\text{m}^2/\text{V}\cdot\text{s} \times 10^{-2}\,\text{F/m}^2 \times \left(\frac{W}{L}\right) \times (1.5)^2.$$

Plugging in numbers carefully (note the unit conversions):

- $\mu_n = 0.04\,\text{m}^2/\text{V}\cdot\text{s}$
- $C_{\text{ox}} = 10^{-2}\,\text{F/m}^2$
- $W/L = 10$
- $(1.5)^2 = 2.25$

$$I_D = \frac{1}{2} \times 0.04 \times 10^{-2} \times 10 \times 2.25 = 0.5 \times 0.04 \times 10^{-2} \times 10 \times 2.25.$$

First simplify inside:

- $0.04 \times 10^{-2} = 0.04 \times 0.01 = 4 \times 10^{-4}$.
- $4 \times 10^{-4} \times 10 = 4 \times 10^{-3}$.
- $4 \times 10^{-3} \times 2.25 = 9 \times 10^{-3} = 0.009$.

Now include the factor $\frac{1}{2} = 0.5$:

$$I_D = 0.5 \times 0.009 = 0.0045\,\text{A} = 4.5\,\text{mA}.$$

2. Plot I_D vs. $(V_{GS} - V_{th})$

We vary $(V_{GS} - V_{th})$ from 0 to 2 V. The formula in saturation (neglecting channel-length modulation) is:

$$I_D(\Delta V) = \frac{1}{2}\mu_n C_{\text{ox}} \frac{W}{L} (\Delta V)^2, \quad \text{where } \Delta V = V_{GS} - V_{th}.$$

We can plot for $\Delta V \in [0, 2]$ V.

8.4.2 Solution 2: Threshold Voltage with Body Effect

1. Numerical Calculation

$$V'_{th} = 0.7 + 0.4\left[\sqrt{2 \times 0.4 + 0.5} - \sqrt{2 \times 0.4}\right].$$

Evaluate inside terms: - $2\phi_F = 2 \times 0.4 = 0.8$. - So $\sqrt{0.8 + 0.5} = \sqrt{1.3} \approx 1.140$. - $\sqrt{0.8} = 0.8944$.

Hence:

$$V'_{th} = 0.7 + 0.4 \times (1.140 - 0.8944) = 0.7 + 0.4 \times 0.2456 = 0.7 + 0.09824 \approx 0.798\,\text{V}.$$

2. Plot V'_{th} vs. V_{SB}

Vary V_{SB} from 0 to 2 V in small increments and compute:

$$V'_{th}(V_{SB}) = V_{th0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right).$$

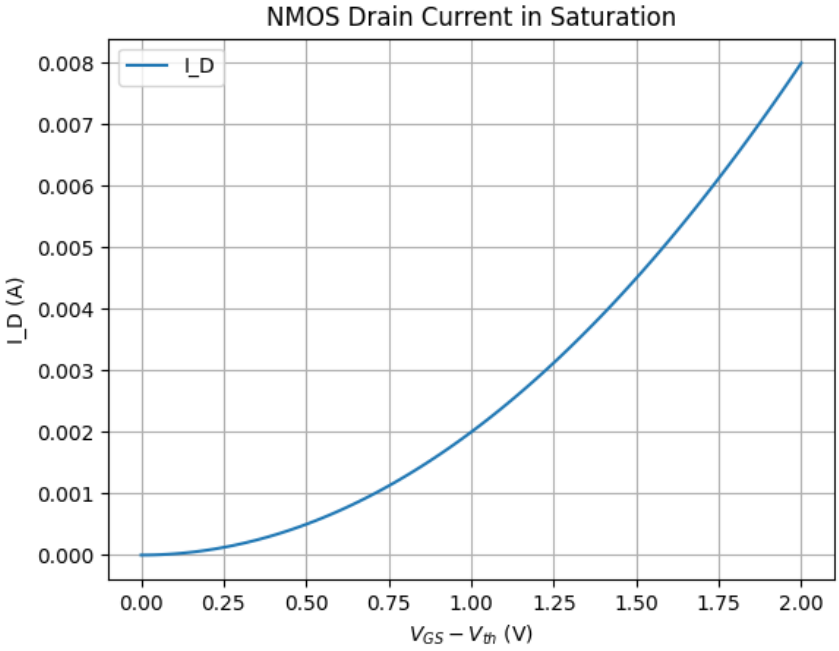

Figure 14: Solution for problem 1. See script `set4_prob1.py` for solution details.

8.4.3 Solution 3: NMOS I–V Characteristics (Linear/Triode vs. Saturation)

- For $V_{GS} = 3$ V and $V_{th} = 1$ V, $(V_{GS} - V_{th}) = 2$ V.
- The boundary between triode and saturation occurs at $V_{DS} = V_{GS} - V_{th} = 2\,\text{V}$.
- **Triode region**: $0 \leq V_{DS} < 2\,\text{V}$.
- Saturation region: $V_{DS} \geq 2\,\text{V}$.

Key parameters:

$\mu_n C_{\text{ox}}(W/L) = 50\,\mu\text{A/V}^2 \times 5 = 250\,\mu\text{A/V}^2 = 2.5 \times 10^{-4}\,\text{A/V}^2$.

1. **In Triode** (for $V_{DS} < 2\,\text{V}$):

$$I_D = (2.5 \times 10^{-4})\big[(2)\,V_{DS} - \tfrac{V_{DS}^2}{2}\big].$$

2. **In Saturation** (for $V_{DS} \geq 2\,\text{V}$):

$$I_D = \tfrac{1}{2}(2.5 \times 10^{-4})(2)^2 = 0.5 \times 2.5 \times 10^{-4} \times 4 = 0.5 \times 10^{-3} = 5 \times 10^{-4} = 0.0005\,\text{A} = 0.5\,\text{mA}.$$

So once V_{DS} reaches 2 V, I_D saturates at 0.5 mA.

8.4.4 Solution 4: PMOS Drain Current (Enhancement Mode)

1. PMOS Drain Current

Overdrive $(|V_{SG}| - |V_{thp}|) = (2.0 - 1.0) = 1.0\,\text{V}$.

$$\mu_p C_{\text{ox}} \frac{W}{L} = 0.02\,\text{m}^2/\text{V}\cdot\text{s} \times 8 \times 10^{-3}\,\text{F/m}^2 \times 10.$$

Simplify step by step: - $0.02 \times 8 \times 10^{-3} = 0.02 \times 0.008 = 1.6 \times 10^{-4}$. - Multiply by 10 $\Rightarrow 1.6 \times 10^{-3}\,\text{A/V}^2$.

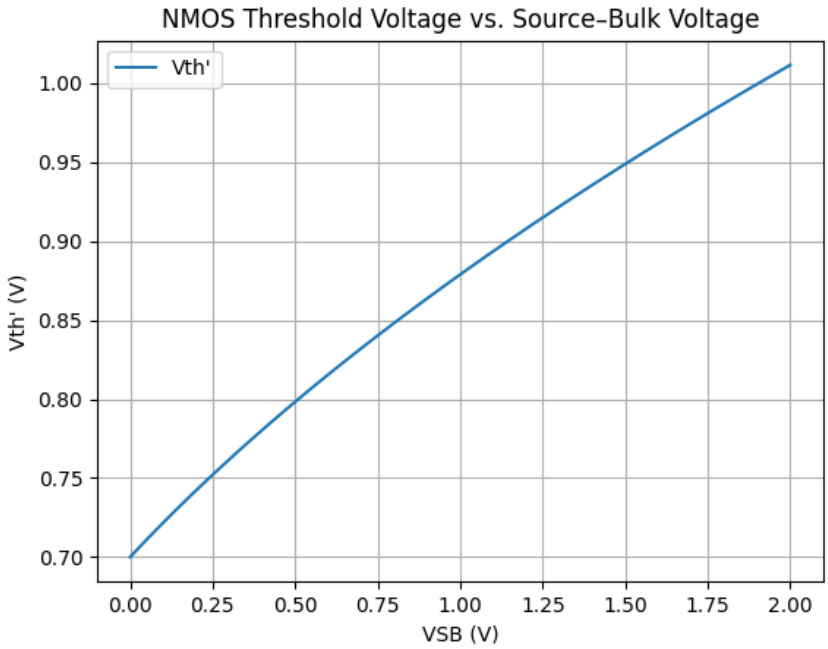

Figure 15: Solution for problem 2. See script `set4_prob2.py` for solution details.

Hence,

$$I_D = \frac{1}{2} \times 1.6 \times 10^{-3} \times (1.0)^2 = 0.8 \times 10^{-3}\,\text{A} = 0.8\,\text{mA}.$$

2. NMOS Comparison

For an NMOS with $\mu_n = 0.04\,\text{m}^2/\text{V}\cdot\text{s}$, same C_{ox}, same W/L, and the same overdrive $(V_{GS} - V_{thn}) = 1.0\,\text{V}$:

$$\mu_n C_{\text{ox}} \frac{W}{L} = 0.04 \times 8 \times 10^{-3} \times 10 = 3.2 \times 10^{-3}\,\text{A/V}^2.$$

$$I_{D,\text{NMOS}} = \frac{1}{2} \times 3.2 \times 10^{-3} \times (1.0)^2 = 1.6 \times 10^{-3}\,\text{A} = 1.6\,\text{mA}.$$

Thus, under the same overdrive voltage (1 V), the NMOS current (1.6 mA) is *about twice* the PMOS current (0.8 mA), mainly because $\mu_n > \mu_p$.

See script `set4_prob4.py` for solution.

8.4.5 Solution 5: CMOS Inverter Switching Threshold

We want V_M satisfying:

$$k_n(V_M - 0.8)^2 = k_p(5 - V_M - 1.0)^2,$$

dropping the factor $\frac{1}{2}$ from both sides.

That is:

$$3 \times 10^{-4}(V_M - 0.8)^2 = 2 \times 10^{-4}(4 - V_M)^2.$$

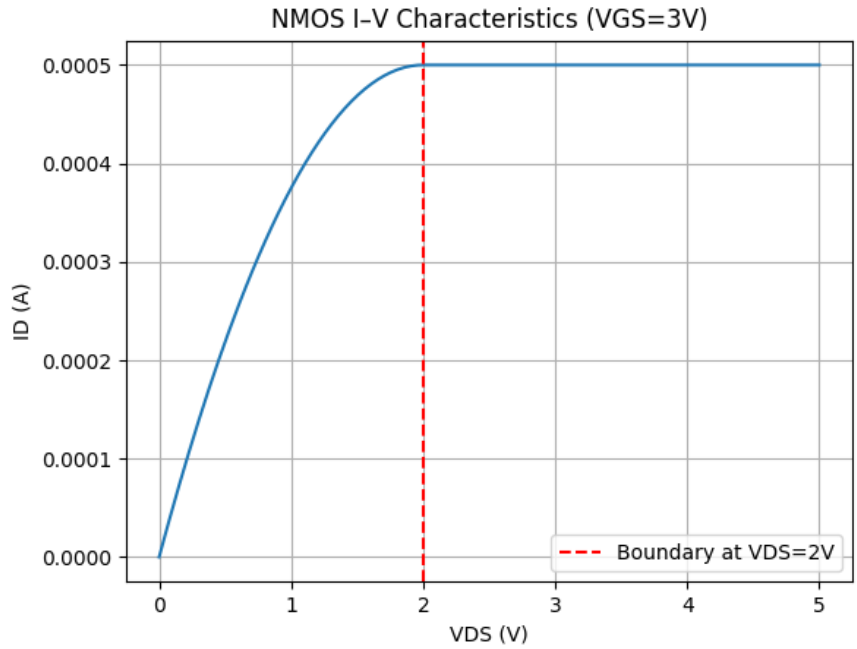

Figure 16: Solution for problem 3. See script `set4_prob3.py` for solution details.

1. Rearrange:

$$\frac{(V_M - 0.8)^2}{(4 - V_M)^2} = \frac{2 \times 10^{-4}}{3 \times 10^{-4}} = \frac{2}{3}.$$

2. Taking square roots:

$$\frac{|V_M - 0.8|}{|4 - V_M|} = \sqrt{\frac{2}{3}} \approx 0.8165.$$

We can solve numerically. Alternatively, rearrange and solve:

$$|V_M - 0.8| = 0.8165\,|4 - V_M|.$$

We can solve for V_M in a standard algebraic way (assuming $V_M < 4$, so $4 - V_M > 0$, also $V_M > 0.8$ is typical for a typical switching threshold with these parameters, but we'll do the full approach).

Let's remove absolute values in a likely scenario:

$$V_M - 0.8 = 0.8165(4 - V_M).$$

$$V_M - 0.8 = 3.266 - 0.8165\,V_M.$$

$$V_M + 0.8165\,V_M = 3.266 + 0.8.$$

$$1.8165\,V_M = 4.066.$$

$$V_M \approx 2.24\,\text{V}.$$

We check if that is consistent with our assumption: $V_M = 2.24$ is indeed less than 4 and greater than 0.8, so it makes sense physically.

Hence, $V_M \approx 2.24\,\text{V}$.

See script `set4_prob5.py` for numerical solution. In practice, one might use a root-finding algorithm like *scipy.optimize.fsolve*. The direct approach yields $\approx 2.24\,\text{V}$.

8.4.6 Solution 6: Subthreshold Conduction in MOSFET

1. Subthreshold I–V Plot

We use the equation

$$I_D = 1\,\text{nA}\ \exp\Big(\frac{V_{GS} - 0.7}{1.2 \times 0.025}\Big),$$

for $V_{GS} \leq 0.7\,\text{V}$. Even slightly above 0.7 V, in practice, the device may enter moderate conduction, but we'll still plot up to 0.8 V.

2. Evaluate at $V_{GS} = 0.6\,\text{V}$

$$V_{GS} - V_{th} = -0.1\,\text{V}. \quad n\,V_T = 1.2 \times 0.025 = 0.03\,\text{V}.$$

$$\frac{-0.1}{0.03} \approx -3.33.$$

Hence,

$$I_D \approx 1\,\text{nA} \times e^{-3.33} \approx 1 \times 10^{-9}\,\text{A} \times 0.0356 \approx 3.56 \times 10^{-11}\,\text{A} = 35.6\,\text{pA}.$$

8.4.7 Solution 7: Channel-Length Modulation

1. Drain Current

Base saturation current without channel-length modulation:

$$I_{D0} = \frac{1}{2}k(V_{GS} - V_{th})^2 = \frac{1}{2} \times (100 \times 10^{-6}) \times (2)^2.$$

$$= 50 \times 10^{-6} \times 4 = 200 \times 10^{-6} = 2 \times 10^{-4}\,\text{A} = 0.2\,\text{mA}.$$

(a) At $V_{DS} = 3\,\text{V}$:

$$I_D = I_{D0}(1 + \lambda \times 3) = 0.2\,\text{mA}\,[1 + 0.02 \times 3] = 0.2\,\text{mA}\,[1 + 0.06] = 0.2\,\text{mA} \times 1.06 = 0.212\,\text{mA}.$$

(b) At $V_{DS} = 10\,\text{V}$:

$$I_D = 0.2\,\text{mA}\,[1 + 0.02 \times 10] = 0.2\,\text{mA} \times 1.2 = 0.24\,\text{mA}.$$

2. Plot

- For $V_{DS} < 2$ V: device not in saturation (would use triode equation).
- For $V_{DS} \geq 2$ V: use $I_{D0}[1 + \lambda V_{DS}]$. We can show a piecewise plot (0–2 V in triode, 2–10 V in saturation with channel-length modulation).

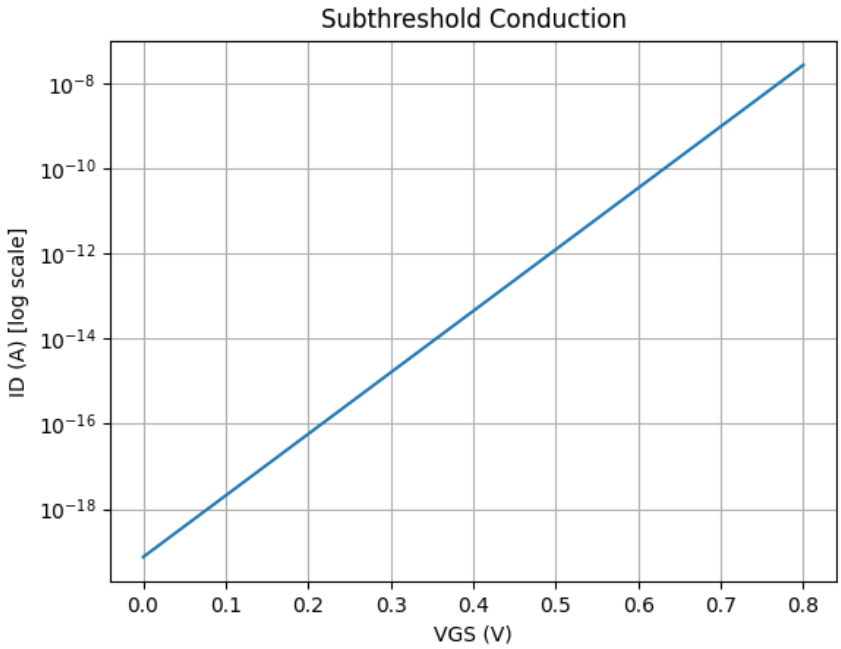

Figure 17: Solution for problem 6. See script `set4_prob6.py` for solution details.

8.4.8 Solution 8: Transconductance g_{m} for an NMOS

1. Calculate g_m at $I_D = 1\,\mathbf{mA}$

$$g_m = \sqrt{2 \times 400 \times 10^{-6}\,\mathrm{A/V^2} \times 1 \times 10^{-3}\,\mathrm{A}}.$$

Inside the square root:

- $2 \times 400 \times 10^{-6} = 800 \times 10^{-6} = 8 \times 10^{-4}$.
- Multiply by 10^{-3} A $\rightarrow 8 \times 10^{-4} \times 10^{-3} = 8 \times 10^{-7}$.

$$\sqrt{8 \times 10^{-7}} = \sqrt{8} \times 10^{-3.5}.$$

$\sqrt{8} \approx 2.828$. Also, $10^{-3.5} = 10^{-3} \times 10^{-0.5} = 10^{-3} \times 0.316 \approx 3.16 \times 10^{-4}$. Let's do it more systematically:

$$\sqrt{8 \times 10^{-7}} = \sqrt{8} \times 10^{-3.5} \approx 2.828 \times 3.162 \times 10^{-4} \approx 8.94 \times 10^{-4} = 0.000894\,\mathrm{S}.$$

A simpler numeric approach:

- $2 \times 400 \times 10^{-6} = 8 \times 10^{-4}$.
- Multiply by $1 \times 10^{-3} \rightarrow 8 \times 10^{-7}$.
- $\sqrt{8 \times 10^{-7}} \approx 2.828 \times 10^{-3.5}$.
- $10^{-3.5} = 3.162 \times 10^{-4}$.
- Product $\approx 2.828 \times 3.162 \times 10^{-4} \approx 8.95 \times 10^{-4}$.

So,

$$g_m \approx 0.000894\,\mathrm{S} = 0.894\,\mathrm{mS}.$$

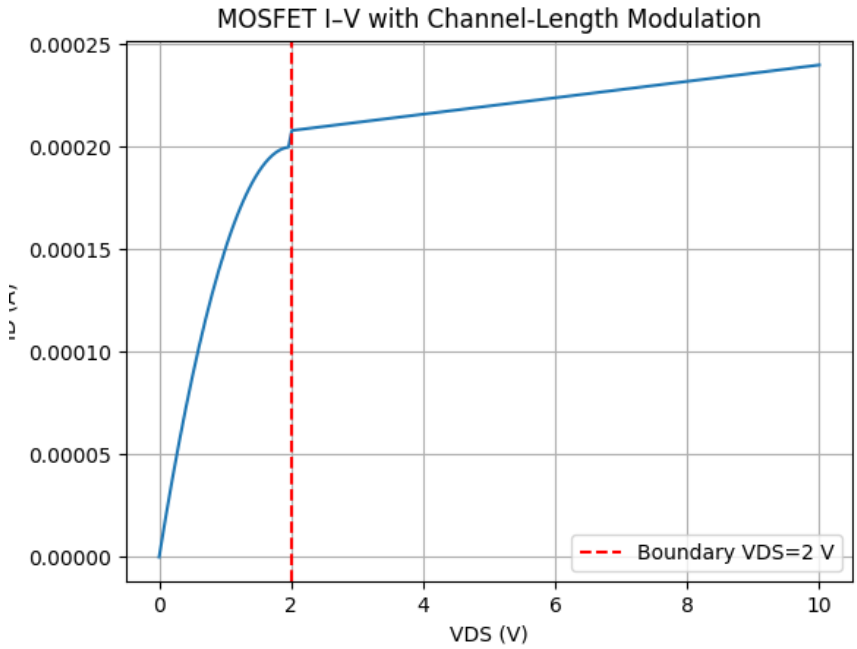

Figure 18: Solution for problem 7. See script `set4_prob7.py` for solution details.

2. Plot

For $I_D \in [0.1, 5]$ mA:

$$g_m(I_D) = \sqrt{2kI_D}.$$

8.4.9 Solution 9: MOSFET Sizing in a CMOS Inverter

- **NMOS current** scale factor: $k_n \sim \mu_n \, (W/L)_n \, C_{\text{ox}}$.
- **PMOS current** scale factor: $k_p \sim \mu_p \, (W/L)_p \, C_{\text{ox}}$.

We want $k_n \approx k_p$. If $\mu_n = 2.5\,\mu_p$, and $(W/L)_n = 5$, $(W/L)_p = 10$, then:

$$k_n = \mu_n \times 5, \quad k_p = \mu_p \times 10.$$

$$\text{Ratio } \frac{k_n}{k_p} = \frac{\mu_n \times 5}{\mu_p \times 10} = \frac{\mu_n}{\mu_p} \times \frac{5}{10} = 2.5 \times 0.5 = 1.25.$$

Strictly, that's not exactly 1.0, but indicates we're in the ballpark (1.25 suggests the PMOS is still a bit weaker). Designers might refine to get perfect matching.

For $\mu_n = 3\,\mu_p$, to get $k_n = k_p$, we require:

$$\mu_n \times (W/L)_n = \mu_p \times (W/L)_p \quad \Longrightarrow \quad 3 \times 5 = 1 \times (W/L)_p \quad \Longrightarrow \quad (W/L)_p = 15.$$

Hence, if $\mu_n = 3\,\mu_p$, we'd pick $(W/L)_p = 15$ to balance the drive currents with $(W/L)_n = 5$.

8.4.10 Solution 10: PMOS vs. NMOS Sizing to Achieve Balanced Delay

1. **PMOS Size**: $(W/L)_p = 2.5 \times (W/L)_n = 2.5 \times 2 = 5$.

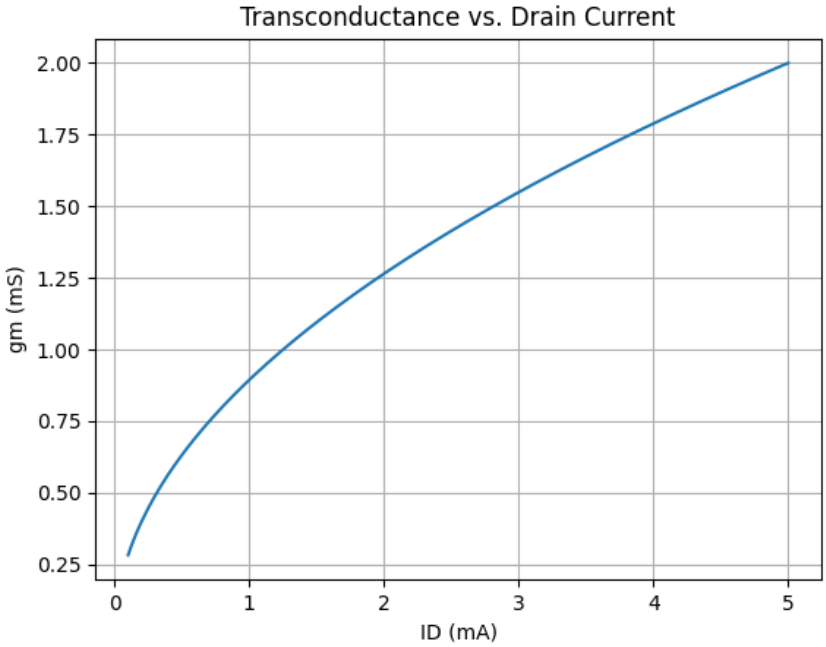

Figure 19: Solution for problem 8. See script `set4_prob8.py` for solution details.

2. **Drain Currents**:

NMOS: $k_n' = k_n(W/L)_n = 50 \times 10^{-6}\,\text{A/V}^2 \times 2 = 100 \times 10^{-6}\,\text{A/V}^2$.

$$I_{D,n} = \tfrac{1}{2}k_n'(V_{GS} - V_{th})^2 = 0.5 \times 100 \times 10^{-6} \times 0.8^2$$

$$= 50 \times 10^{-6} \times 0.64 = 32 \times 10^{-6}\,\text{A} = 32\,\mu\text{A}.$$

PMOS: $k_p' = k_p(W/L)_p = 20 \times 10^{-6}\,\text{A/V}^2 \times 5 = 100 \times 10^{-6}\,\text{A/V}^2$.

$$I_{D,p} = 0.5 \times 100 \times 10^{-6} \times 0.8^2 = 32\,\mu\text{A},$$

the same as the NMOS, as designed.

3. **Matching**: Both drain currents are 32 µA with the chosen sizing ratio.

8.4.11 Solution 11: Enhancement vs. Depletion MOSFETs

- **Enhancement-mode** MOSFET: By default (at $V_{GS} = 0$), the device channel is non-existent (off). A sufficiently positive V_{GS} (for NMOS) or sufficiently negative V_{GS} (for PMOS) is required to "enhance" or create the channel.
- **Depletion-mode** MOSFET: The channel is already formed at $V_{GS} = 0$; applying a certain gate voltage "depletes" the channel.
- **Modern CMOS** typically uses enhancement-mode because it's easier to ensure zero current draw at zero gate voltage, simpler to integrate for logic, and is the standard for scaling and low-power design.

8.4.12 Solution 12: Body Effect vs. Source Tied to Substrate

- **Body effect** arises when $V_{SB} \neq 0$, which increases the threshold voltage.
- By *tying source to substrate* (in an NMOS, substrate is typically p-type), $V_{SB} = 0$, so no body effect. This is standard in discrete transistors or many digital CMOS circuits.

- In analog circuits or certain high-voltage or level-shifting blocks, a non-zero V_{SB} might be used intentionally (e.g., to shift thresholds or isolate wells).

8.4.13 Solution 13: Short-Channel Effects

1. **Drain-Induced Barrier Lowering (DIBL)**: High V_{DS} lowers the channel potential barrier, effectively reducing V_{th} and increasing off-current.
2. **Velocity Saturation / Mobility Degradation**: Carriers cannot accelerate indefinitely, limiting current and altering the I–V characteristic from the long-channel quadratic forms.

8.4.14 Solution 14: PMOS in a Well (Twin-Well Processes)

- **Twin-well process** uses an n-well region to host the p-channel transistor (PMOS) so that its body (p-type region) can be at a desired potential (often tied to V_{DD}). The NMOS resides in the p-substrate.
- Each well isolates the device bodies from the main substrate or from each other, preventing undesirable conduction paths and enabling independent body connections if needed.

8.4.15 Solution 15: Threshold Voltage Variation with Temperature

- As temperature *increases*, the intrinsic carrier concentration rises, effectively reducing the bandgap and lowering the threshold voltage. Also, carrier mobility decreases with higher temperature, somewhat countering this effect.
- Overall, many CMOS circuits exhibit slower operation at higher temperatures (due to decreased mobility), and slightly lower threshold voltages can increase subthreshold leakage.

8.4.16 Solution 16: Differences Between NMOS and PMOS Body Diodes

- The **body diode** arises from the p–n junction between the MOSFET body region (substrate) and the source/drain diffusion. For an NMOS in a p-substrate, the source/drain n-region forms a p–n junction. It's forward-biased if the source is at a higher potential than the substrate (p–n diode direction).
- For a PMOS in an n-well, the well is typically at V_{DD}; the p-source region forms a diode to the n-well. It's forward-biased if the source p-region is more positive (close to V_{DD}) than the well (also near V_{DD} or higher potential).

8.4.17 Solution 17: Subthreshold Slope

The **subthreshold slope** S is usually expressed in mV/decade, indicating how many mV of V_{GS} are needed to change I_D by one decade in the subthreshold region:

$$S = (n \times 60)\,\text{mV/decade at } T \approx 300\,\text{K}.$$

The factor $n \geq 1$ accounts for non-idealities, body effect, etc. The Boltzmann distribution and thermal voltage set a fundamental limit of 60 mV/decade at room temperature for an ideal transistor.

8.4.18 Solution 18: Channel Formation in NMOS vs. PMOS

- **NMOS**: The substrate is p-type, so the channel forms by inverting the surface to n-type. Electrons are the majority carriers in the channel. They come from the n+ source/drain regions.
- **PMOS**: The substrate (or well) is n-type, so a negative gate voltage inverts the surface to p-type. Holes are the majority carriers in the channel, originating from the p+ source/drain regions.

8.4.19 Solution 19: MOSFET as a Voltage-Controlled Current Source

In **saturation**, the drain current I_D is (to first order) set by $V_{GS} - V_{th}$ and largely independent of V_{DS}, akin to a controlled current source. At *low* V_{DS} (i.e., triode region), the device behaves like a resistor whose value depends on $(V_{GS} - V_{th})$.

8.4.20 Solution 20: Impact of Gate Oxide Thickness on MOSFET Operation

1. **Gate Capacitance** ($C_{\text{ox}} \propto 1/t_{\text{ox}}$) *increases* as t_{ox} shrinks, improving gate control.
2. **Threshold Voltage** can decrease because the stronger gate electric field can invert the channel more easily (though doping and workfunction engineering also matter).
3. **Short-channel effects** often *worsen* at the same channel length if the device is not scaled properly in other dimensions. Thinner oxide helps in controlling the channel, but at very short lengths, additional measures (halo implants, higher doping, etc.) are needed to mitigate SCEs.