Name: USC ID#:

I hereby affirm that all the answers below are my own. I have neither searched online nor taken assistance from any external entity.

Student Signature Above

EE105 – Spring 2025

Final

Time Limit: 2 hours

Max Points: 125

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# Section A (25 points)

**Question 1 (25 points)**

The current source at the top of this circuit is a 1 A current source

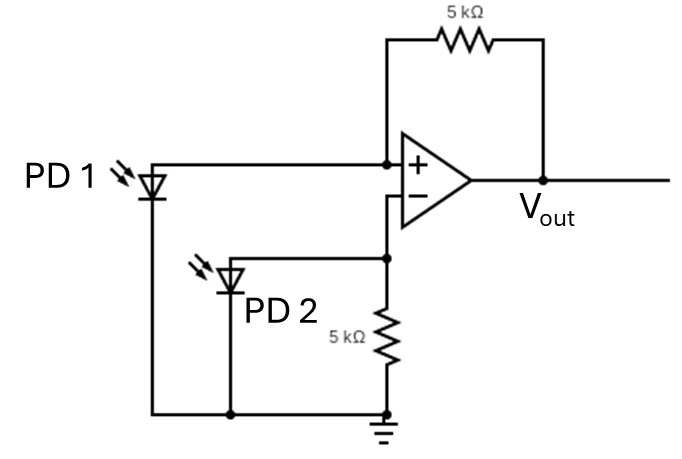
A diagram of a circuit

AI-generated content may be incorrect.

1. What is the equivalent resistance of this network of resistors?
2. Identify the nodes and the loops in the circuit. Then write the KVL and KCL equations for each node and loop. Choose your own current direction but make sure to be consistent.
3. What are the voltages dropped across each resistor? Include both voltage drop magnitude and the sign.

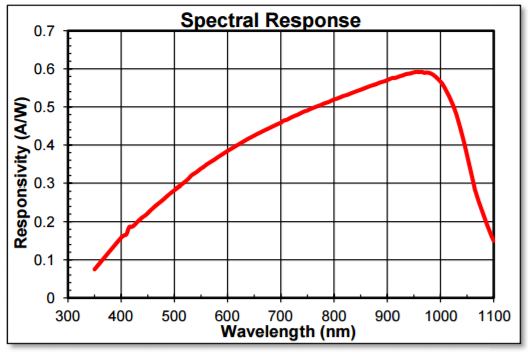
# Question 2 (25 points)

An operational amplifier (Op-Amp) is connected with resistors as shown below. Two photodiodes, PD 1 and PD 2, are connected to this op amp.



1. Derive the expression for the output voltage (Vout) in terms of the photocurrent of PD 1 and PD 2, which you can call IPD1 and IPD2. Make sure to remember which direction current flows in a photodetector when light is shining on it.
2. Assume a bandwidth of 100 KHz and room temperature (300 K). Calculate the noise voltage due to each resistor and each photodetector. For the photodetector, assume 10 mA of photocurrent is flowing through PD 1 and 1 mA of photocurrent is flowing through PD 2. Ignore flicker noise.
3. Find the total noise voltage on the output due to the noise of the resistors and photodiodes. Make sure you add it properly.
4. What is the signal to noise ratio for the case when the system is at room temperature, with a 100 KHz bandwidth, and the currents flowing through PD 1 and PD 2 as stated in part b?

# Question 3 (10 points)

Imagine you have a green LED (emission wavelength = 532 nm), and a silicon photodetector with a responsivity as shown below.

Your LED has a diode I-V curve as shown below. Assume a quantum efficiency of current to photon generation of 21.5%. For the purposes of the questions below, assume 100% of the emitted light falls on the photodetector.  
  
A graph of a green line

AI-generated content may be incorrect.

1. Design an LED driver circuit using a tunable voltage source, a 100 Ohm resistor, and the LED. By tuning the voltage source in this circuit, you should be able to control the current in the LED. What is the minimum and maximum voltage you will need the tunable voltage source to output if you want to be able to control the current in the LED between 0 mA and 10 mA? Solve the diode equation and be precise with the voltage required.
2. Now use op amps, ONLY 100 ohm resistors (any number of them), and the photodetector to build a readout circuit. Assume the output of this detection circuit goes to an analog to digital converter (ADC), and this analog to digital converter can accept a maximum signal of 10 V and a minimum signal of 0 V. In order for us to maximize the use of this (ADC) we want to create a photodetector readout circuit that outputs 10 V when we are flowing max current through our LED (i.e. 10 mA). Design an amplifier circuit that outputs 10 V at max LED brightness (i.e. when flowing max current through the LED).

# Question 4 ( 25 points)

1. Assume you have a fully connected neural network with:
   1. Input layer: 500 neurons
   2. Hidden layer 1: 128 neurons
   3. Hidden layer 2: 64 neurons
   4. Hidden layer 3: 32 neurons
   5. Output layer: 10 neurons

Calculate the total number of multiply and addition operations (floating point operations) needed for a single inference using this neural network.

1. Sketch the training and test accuracy vs epoch for a case where your neural network is underfitting the data and a case where your neural network is overfitting the data?
2. What is the mathematical rule for the original perceptron neuron?
3. Why were the original perceptrons difficult to train?

# Question 5 ( 15 points)

1. Design a CMOS digital logic gate for a nand gate using nmos and pmos devices only. This gate should take in two logical inputs (A and B), and then output 0 only if both inputs are 1. Label both VDD and ground
2. Assume that for your CMOS logic gate the following is true:

|  |  |  |
| --- | --- | --- |
|  | pmos | nmos |
| On-state resistance | 2100 ohms | 700 ohms |
| Off-state resistance | 1 Megaohm | 1 Megaohm |

If the supply voltage, VDD, is 2 V, what will the EXACT output voltage be for all the input cases? Fill in the table below

|  |  |  |  |
| --- | --- | --- | --- |
| Input A | Input B | Logical Output | Actual Voltage Out |
| 0 | 0 | 1 | ? |
| 0 | 1 | 1 | ? |
| 1 | 0 | 1 | ? |
| 1 | 1 | 0 | ? |