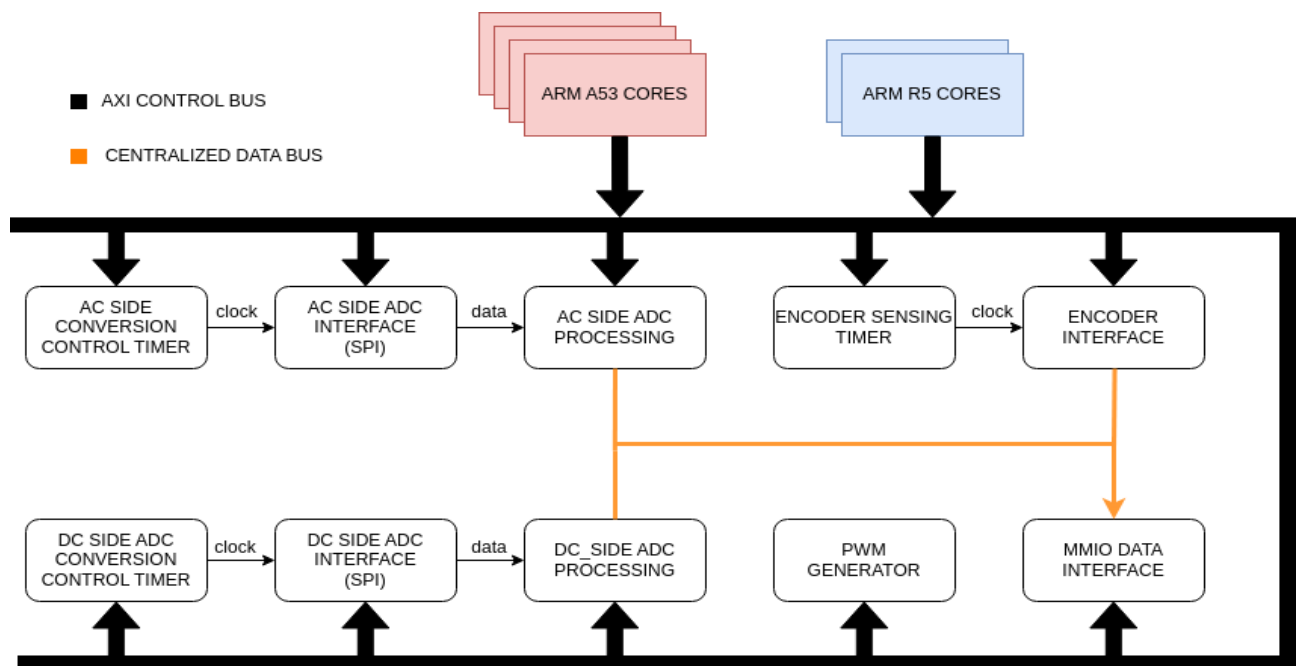# LAB FPGA platform Hardware

The FPGA portion of the experimental platform designed for the HPED Lab exercises is designed to handle all real-time hardware interfacing tasks and exposes a high level memory mapped interface to the code running on the ARM cores.

The overall structure of the FPGA implemented logic, shown in the figure below, consists of a series of peripherals connected to the ARM core clusters (Both cortex A53 and R5) with an AMBA AXI bus. Analog data sensing for the DC and AC side is handled by two identical logic pipelines composed of the following:

- **CONVERSION CONTROL TIMER:** Simple 16 Bit timer running at a fixed 100MHz clock frequency that can be used to control sampling frequency and phase

- **ADC SPI INTERFACE:** A multichannel SPI interface capable of simultaneously reading the connected ADC sensorS:

- **ADC POST-PROCESSING:** Post processing block capable of offset correction, filtering averaging and decimation.

Rotor sensing is handled directly in FPGA with both speed and angle being directly measured from the incremental encoder signal. The first is done through counting of both rising and falling edges of both A and B signals. Shaft speed is independently digitized by measuring the period of the A signal, thus avoiding the need for digital differentiation (which is prone to noise amplification)
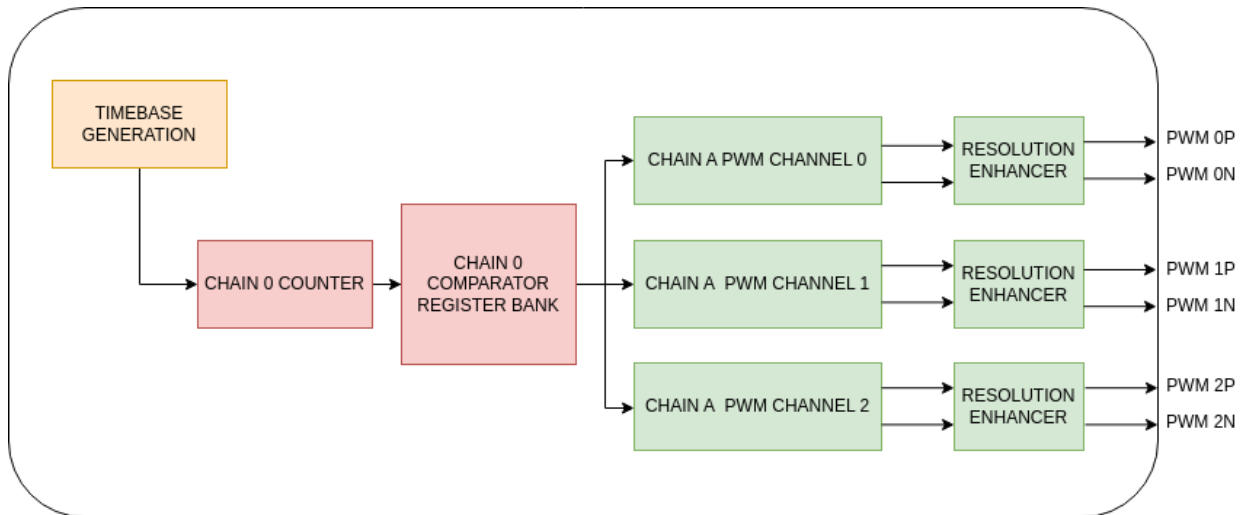
Finally an advanced PWM generator can be used to produce the desired output gating signals.

Each peripheral is directly mapped in the address space of the ARM cores, thus the control register can be accessed by reading and writing to the correct memory address. Each peripheral occupies a contiguous block of addresses starting from the base address from the table below.

Peripheral	Peripheral type	Base address	Number of registers
PWM GENERATOR	PWM GENERATOR	0xA0000000	18
GLOBAL CONTROL	GPIO	0xA0010000	2
AC SIDE TIMER	ENABLE GENERATOR	0xA0020000	4
DC SIDE TIMER	ENABLE GENERATOR	0xA0030000	4
AC SIDE SPI	SPI ADC INTERFACE	0xA0040000	4
DC SIDE SPI	SPI ADC INTERFACE	0xA0050000	4
AC SIDE PROCESSING	ADC PROCESSING	0xA0060000	13
DC SIDE PROCESSING	ADC PROCESSING	0xA0070000	13
ENCODER TIMER	ENABLE GENERATOR	0xA0080000	4
ENCODER INTERFACE	ENCODER INTERFACE	0xA0090000	5
MMIO DATA	MEMORY	0xA00A0000	10
IRQ CONTROLLER	IRQ CONTROLLER	0xA00B0000	1

The following sections will briefly show the peripherals structure and register maps.

PWM GENERATOR

This peripheral is a highly capable PWM modulator that supports many advanced carrier based modulation techniques. It can be configured to generate N_c carriers each one has an associated bank of compare registers that can handle up to N_M modulating signals generating N_{PWM} pwm channels.
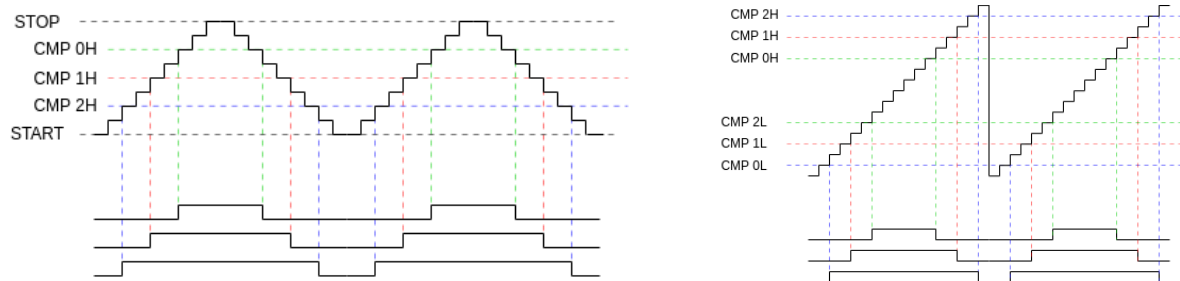
$$N_{PWM} = N_C N_M$$

Other advanced features of this modulator are:

- Dynamically configurable phase shift between carriers

- Automatic deadtime insertion

- Configurable default pin state

- Asymmetric pwm capability

- multiphase edge shifter for enhanced resolution.
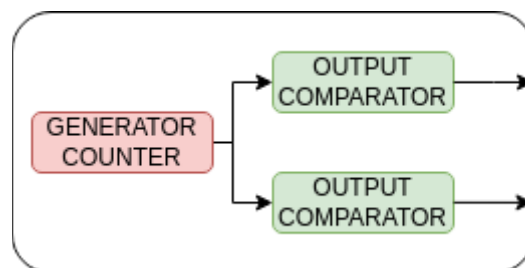
- Selectable and delayable synchronization out event

Register Name	Description	Offset
Global control	• Bit[0:2]: PWM timebase frequency divisor • Bit 3: Timebase enable • Bit 4: External timebase enable • Bit 5: Enable all counters • Bit 6: Instant counter reload (used in distributed system synchronization) • bit[7:17] default pin state	0
Sync Out select	Index of the chain used to generate the output synchronization signal	0x4
Sync out delay	Programmable delay between counter reload and sync event generation	0x8
Threshold low[0]	Value of the comparator low treshold for channel 0	0x100
Threshold low[1]	Value of the comparator low treshold for channel 1	0x104
Threshold low[2]	Value of the comparator low treshold for channel 2	0x108
Threshold high[0]	Value of the comparator high threshold for channel 0	0x10C
Threshold high[1]	Value of the comparator high threshold for channel 1	0x110
Threshold high[2]	Value of the comparator high threshold for channel 2	0x114
deadtime[0]	Deadtime for channel 0	0x108
deadtime[1]	Deadtime for channel 1	0x10C
deadtime[2]	Deadtime for channel 2	0x110
Carrier low	Lower value of the carrier waveform	0x114
Carrier high	Higher value of the carrier waveform	0x118
Carrier phase	Phase of the carrier	0x11C
Output enable	• Bit[0:1]: Enable channel 0P and 0N gates • Bit[2:3]: Enable channel 1P and 1N gates • Bit[4:5]: Enable channel 2P and 2N gates	0x120
Deadtime enable	• Bit 0: Enable deadtime insertion for channel 0 • Bit 1: Enable deadtime insertion for channel 1 • Bit 2: Enable deadtime insertion for channel 2	0x124

Control	• Bit[0:2] Counter mode selection:
	  ○ 0: up counters
	  ○ 1: down counter
	  ○ 2: up-down counter
		0x128

This peripheral can generate a pwm signal using either a sawtooth (up count) or triangular (up-down count). The threshold registers are used to control the output signal state as shown in the following diagrams
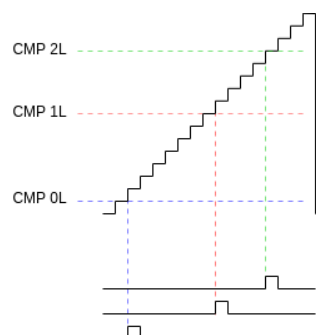

ENABLE GENERATOR

This peripheral can generate one or more enable pulses that are used throughout the whole FPGA each generator consists of a single 32 bit timer setting the event frequency and a bank of comparators, which fires the appropriate enable pulse each time the counter value crosses a threshold, ths controlling the relative phase of the output signals.

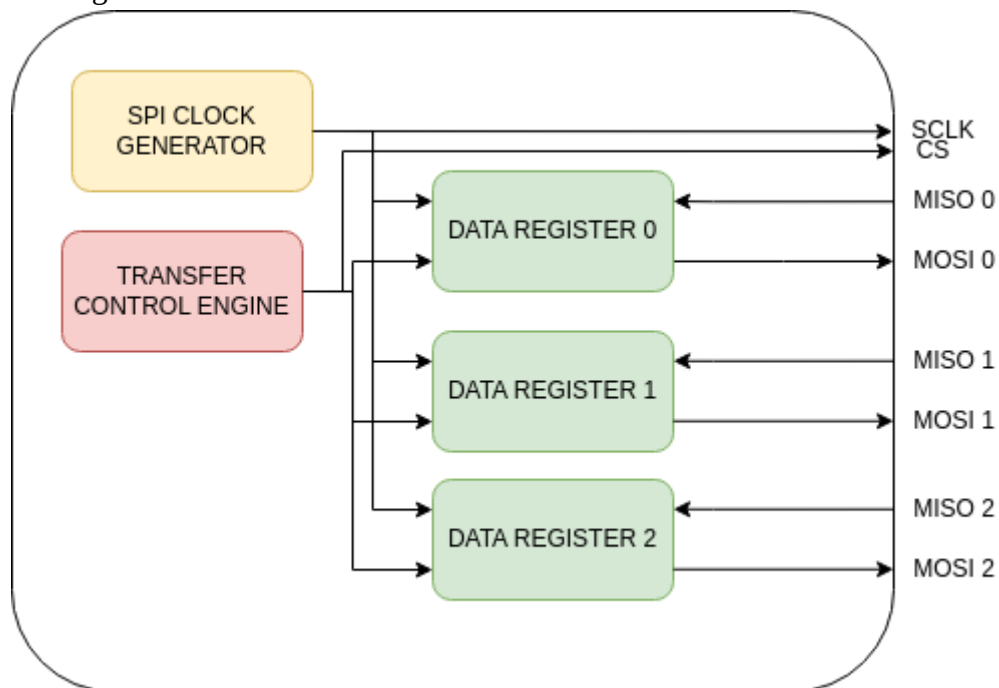| Register Name	Description	Offset
enable	0: generator disabled 1: generator enabled	0
Period	Period of the outputs (in clock cycles)	0x4
Threshold [0]	Phase of Enable 0 with respect to counter reload (in clock cycles)	0x8
Threshold [1]	Phase of Enable 1 with respect to counter reload (in clock cycles)	0xC

The internal waveforms of the modules are as follows

SPI ADC INTERFACE

This peripheral implements a multichannel interface capable of reading the sample data from a bank of externaol SPI interfaced ADCs. To reduce resource usage, only a single the serial clock (SCLK) and chip select line are used, enforcing fully simultaneous sampling. Each SPI channel is served by its own shift register allowing for fully paralled data input and output on the MISO and MOSI signals.

Each communication cycle is started with a trigger signal coming from external logic or by writing to the appropriate register

Register Name	Description	Offset
Control	Bit 0: deprecated Bit [1:3]: SCLK divider setting Bit [4:7]: Transfer length Bit 9: deprecated Bit 12: deprecated Bit 13: CS polarity Bit 14: add cs_delay between transfer end CS deassertion Bit 15: select between external and bus controlled transfer length Bit 16: Select shift register latching edge (0 rising edge, 1 falling edge) Bit 17: Clock polarity (0 for active high 1 for active low)	0
cs_delay	Delay (in clock cycles) between chip select assertion and transfer start	0x4

Reserved	Do not write here	0x8
Trigger	Writing to this register will trigger an SPI transfer cycle	0xC

ENCODER INTERFACE

This peripheral handles automatically the acquisition of motor shaft speed and angle through an incremental encoder.

Register Name	Description	Offset
Angle address	Address of the angle data on the output bus (write 0 to this)	0
Speed address	Address of the speed data on the output bus (write 1 to this)	0x4
Encoder pulses	Number of encoder edges per encoder revolution	0x8
Angle out	Read current angle value	0xC
Speed out	Read current speed value	0x10

GLOBAL CONTROL

This GPIO peripheral allow read and write access to a 32 bit word containing flags that manage the global state of the FPGA based logic:

Flag name	Description	Bit
Gates enable	Enable the pwm modulation	0
AC sensing enable	Enable sensing AC currents and voltages (also mapped to user led A)	1
DC sensing enable	Enable sensing DC voltages and currents (also mapped to user led B)	2

MMIO DATA AREA

In this area the DATA from the sensors will be deposited in this memory area.

Register Name	Description	Offset
Angle	Encoder Angle	0
Speed	Encoder Speed	0x4
ac_va	AC side voltage of phase A	0x8
ac_vb	AC side voltage of phase B	0xC
ac_vc	AC side voltage of phase C	0x10
ac_ia	AC side current on phase A	0x14
ac_ib	AC side current on phase B	0x18
ac_ic	AC side current on phase C	0x1C
dc_v	DC side voltage	0x20
dc_i	DC side current	0x24