November 2, 4:00PM: Discussed our general project objectives and divided work among us.
November 2, 5:00PM: Assembled existing modules from lab.
November 2, 6:00PM: Converted data memory and instruction memory to be byte addressable.

November 3, 12:00PM: Created table of ALU select signals
November 3, 1:00PM: Completed ALU Control Unit
November 3, 10:00PM: New shifter module completed

November 4, 4:00PM: Completed top module connections (datapath)
November 4, 6:00PM: Created all test cases
November 4, 10:00PM: Tested all instructions apart from I-Type and R-Type

November 5, 4:30PM: Tested remaining instructions
November 5, 8:00PM: Wrote report and readme.txt