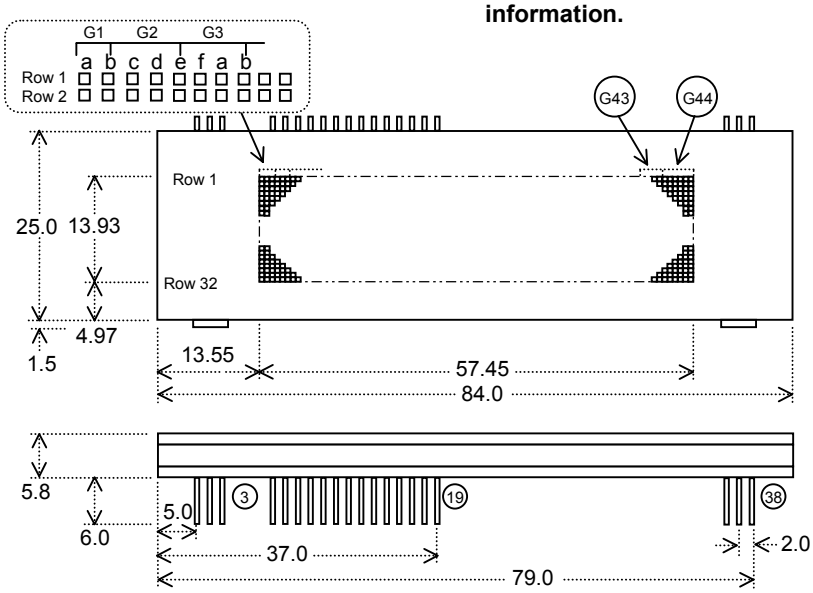
Graphic Dot Matrix Chip In Glass VFD MN12832L

- **128 x 32 Graphic Dot Matrix**
- **Chip in Glass Driver IC**
- **8 Level Grey Scale**
- **High Brightness Blue Green Display**
- **Synchronous Serial Interface**
- **Wide Operating Temperature**

This VF glass includes 2x 240 bit serial shift registers, PWM decoder and latched driver which connects to the anode and grid electrodes. An external host is required to provide a multiplexing data stream to refresh the display. The signal inputs can be connected to the ports of a CMOS microprocessor. The a.c. filament supply (F1, F2) can be derived from a source of 10KHz to 200KHz. Consult our application notes for further information.



Dimensions in mm
See full spec for tolerances

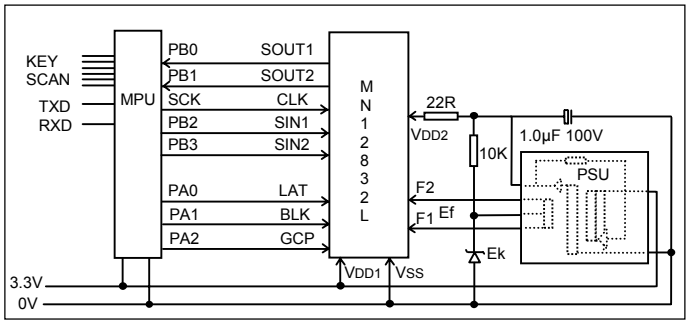
PIN OUT

Pin	Sig
1	F1
2	F1
3	F1
6	V_{DD2}
7	V_{SS}
8	V_{SS}
9	V_{DD1}
10	BLK
11	LAT
12	GCP
13	SOUT2
14	SOUT1
15	CLK
16	SIN1
17	SIN2
36	F2
37	F2
38	F2

ELECTRICAL SPECIFICATION

Parameter	Sym	Min	Typ	Max	Unit	Condition
Logic Voltage	V_{DD1}	3.0	3.3	3.7	V	V_{SS}=0V
Logic Current	I_{DD1}	-	1.0	2.0	mA	VDD1=3.3V
Filament Voltage	E f	2.6	2.9	3.2	Vac	V_{DD2}=0V
Filament Current	I f	135.0	150.0	165.0	mAac	V_{DD2}=0V
Display Voltage	V_{DD2}	-	45.0	50.0	V	V_{SS}=0V
Display Current	I_{DD2}	-	10.0	15.0	mA	V_{DD2}=55V
Filament Bias	E_K	3.5	4.0	4.5	V	V_{SS}=0V
Logic High Input	V_{IH}	$V_{DD1+2.4}$	-	V_{DD1}	V	V_{SS}=0V
Logic Low Input	V_{IL}	V_{ss}	-	+0.7	V	V_{SS}=0V
Logic High Input	I_{IH}	-	-	5.0	µA	VDD1=3.3V
Logic Low Input	I_{IL}	-250	-70	-35	µA	VDD1=3.3V

INTERFACE EXAMPLE

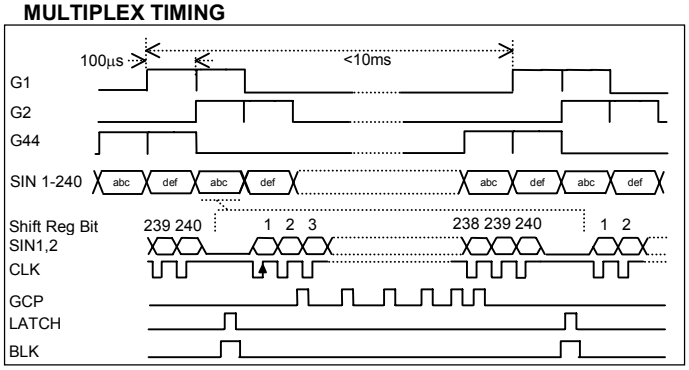


ENVIRONMENTAL and OPTICAL SPECIFICATION

Parameter	Value
Display Area (XxY mm)	57.45 x 13.93
Dot Size/Pitch (XxY mm)	0.3 x 0.29/0.45 x 0.44
Luminance	800 cd/m^2 Typ.
Colour of Illumination	Blue-Green (Filter for colours)
Operating Temperature	-40°C to +85°C
Storage Temperature	-50°C to +85°C
Operating Humidity (non condensing)	5 to 95% @ 25°C

1. The power on rise time should be less than 50ms.
2. The 22R resistor at the V_{DD2} input is required to prevent current surge during switching.
3. If scanning of the display stops with V_{DD2} applied, the BLK input must be set high to prevent damage to the display.
4. The GCP line is the counter clock for the PWM decoder.

MULTIPLEX TIMING



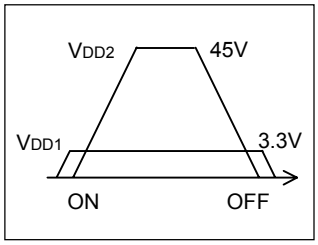
SHIFT REGISTER ASSIGNMENT

Electrode	Bit Numbers
Row 1 'afbecd'	1-6
Row 2 'afbecd'	7-12
Row 3 'afbecd'	13-18
:	:
Row 30 'afbecd'	175-180
Row 31 'afbecd'	181-186
Row 32 'afbecd'	187-192
Grid G1-G44	193-236

INTERFACE TIMING

Parameter	Time
CLK Cycle	400ns min
CLK High	200ns min
CLK Low	200ns min
SIN Setup	40ns min
SIN Hold	30ns min
LAT High	300ns min
CLK then LAT	250ns min
BLK Hold	10µs min

POWER SEQUENCE



CONTACT

Noritake Sales Office Tel Nos
Nagoya Japan: +81 (0)52-561-9867
Canada: +1-416-291-2946
Chicago USA: +1-847-439-9020
Munchen (D): +49 (0)89-3214-290
Itron UK: +44 (0)1493 601144
Rest Europe: +49 (0)61-0520-9220
www.noritake-itron.com

Subject to change without notice.
Doc Ref:3772 Iss.1 31 January 2002