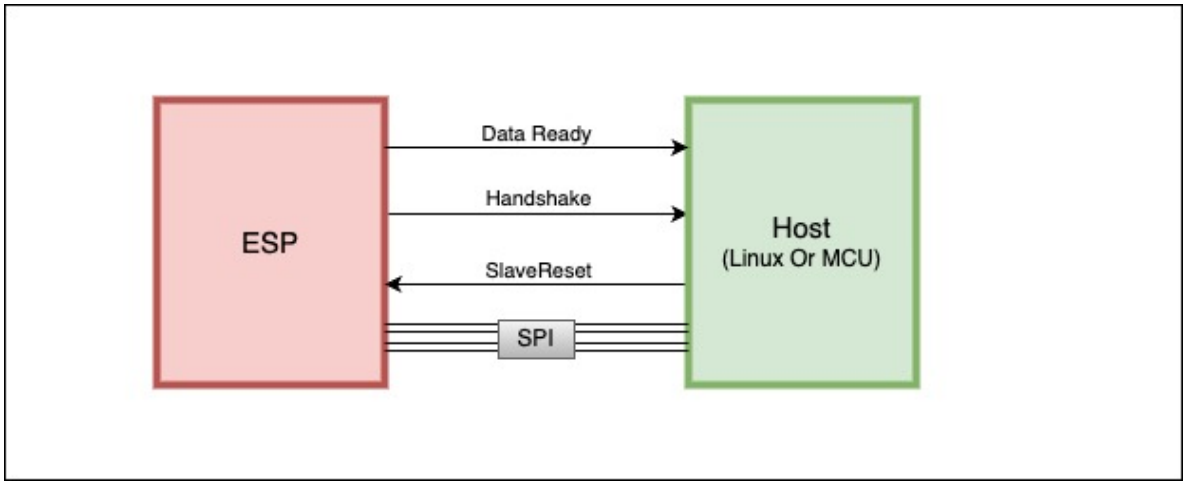
Why Extra GPIO for Handshake, DataReady & SlaveReset

Pins perspective



Handshake pin

Output pin for ESP. Idle state of this Pin is high.
Can be understood as CTS (ClearToSend) to signal host for next transaction.
ESP peripheral makes use of this pin to convey its readiness for execution of SPI transaction.
The host is not supposed to initiate SPI transaction if ESP peripheral has not indicated its readiness.
Pin will be low when ESP is not ready. Host can start transaction any time only if this pin is current value is high.

Data Ready Pin

Output pin for ESP.
This pin is used to indicate host that the ESP peripheral wants to send a data packet to it (ESP has Tx packet pending).
This pin stays high till the host reads this data packet.
Idle state of this pin is low (when ESP doesn't have any packet)

Reset/EN pin

Input pin for ESP.
Host while restarting ESP-Hosted software, resets the slave for getting into consistent state before starting.

SPI bus understanding

A. When Either party is not having any packet to send, there will not be any activity on SPI (SPI bus will be idle and would save some power)

B. Host has some packet to send, it doesn't need Data Ready pin check. I will simply need to schedule the SPI. Here it will only check if Handshake is obtained (ESP is ready) or not (ESP is still in progress for earlier SPI transaction).

C. ESP has some packet to send. It will set Data ready high, which will make host mandate SPI transaction using riding edge interrupt.
At this time, If host any pending packet, will go on MOSI, whereas MISO will receive packet from ESP.
If in case Host doesn't have any packet to send, it will send **dummy** data, which ESP will discard once received.

D. SPI bus is always used in duplex mode.
Transmit: Either party has valid data, will fill the Tx buffer. If no valid data, dummy data will be filled.
Receive: Either party received data will check the validity of the data. If incorrect framed data (using checksum) or dummy data, will be simply discarded.
If valid data, will push for further RX processing.

E. The state where both parties do not have either Tx or Rx any valid data, SPI bus will not have any transactions, till either party has any valid data.