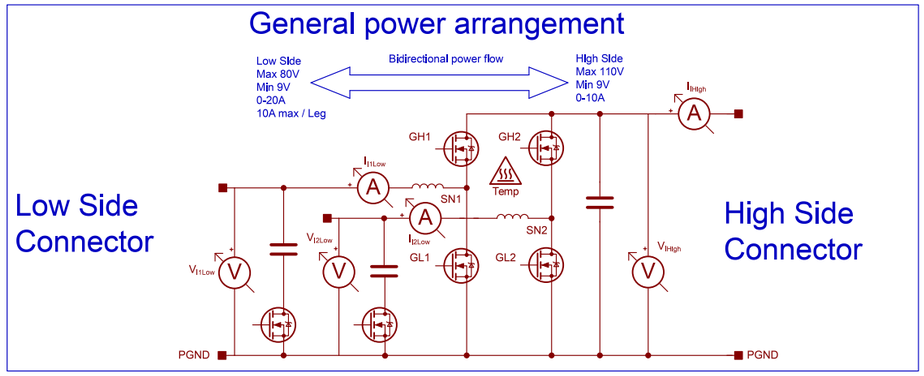
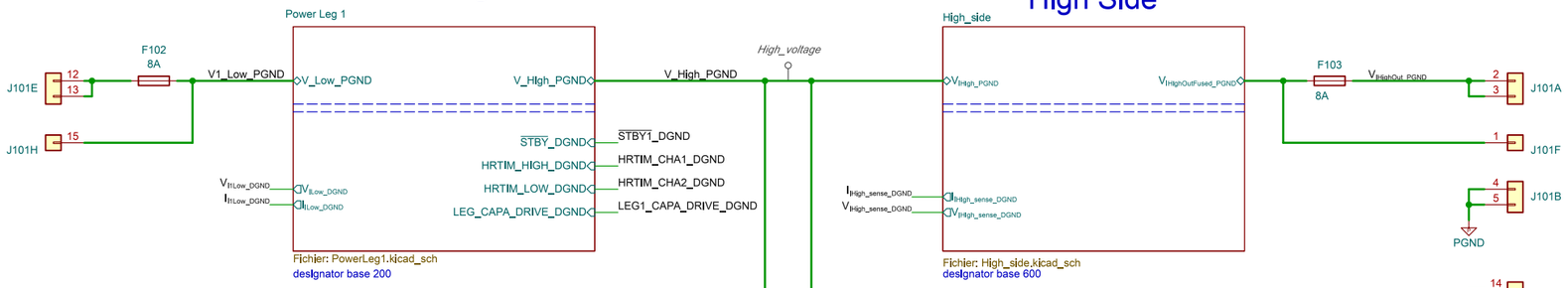
General power arrangement

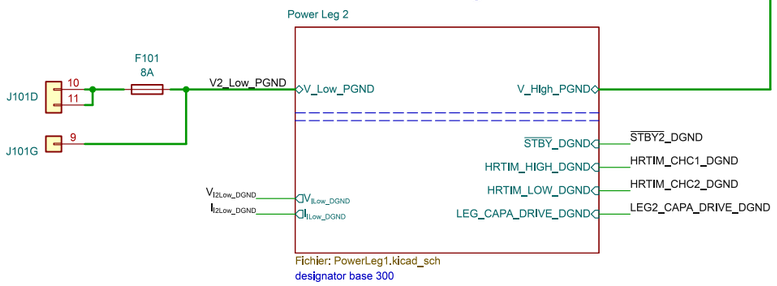


Power Leg 1

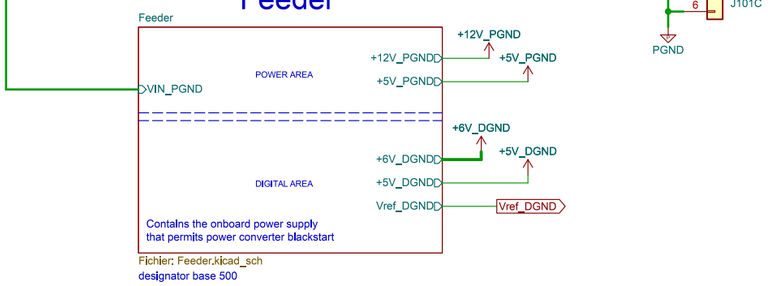


High Side

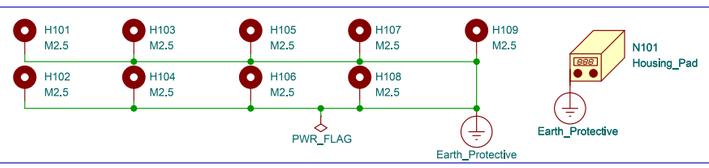
Power Leg 2



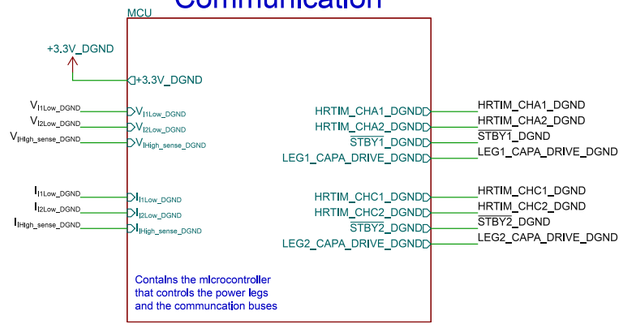
Feeder



Mechanical housing and heatsink holes



Microcontroller and Communication



NOTES :

All ceramic capacitor are 0805 X7R 50V unless specified
All resistor are 0805 thick film unless specified

Source repository : https://gitlab.laas.fr/owntech/1leg/-/tree/V1.1.2

Preliminary PREL, Good For Execution, GFE, As Built ASB
Major revisions are to be described thoroughly when pushed with git push command

Date	Rev.	Creator	Reviewer	Approver	Status
	B				
	A				
2023-10-11	-	WALTER			

Title: TWIST 1.4

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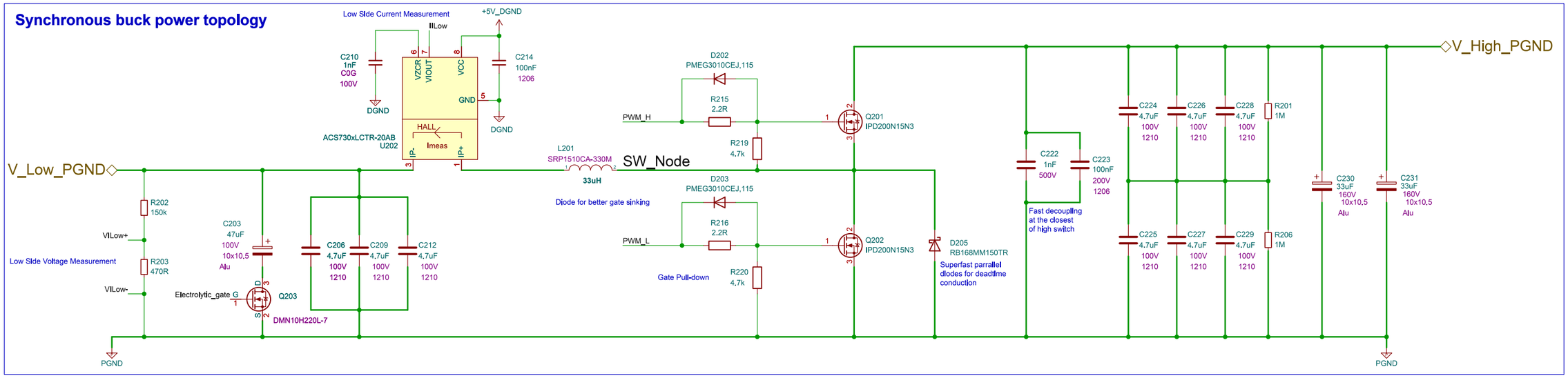
File: Power.kicad_sch

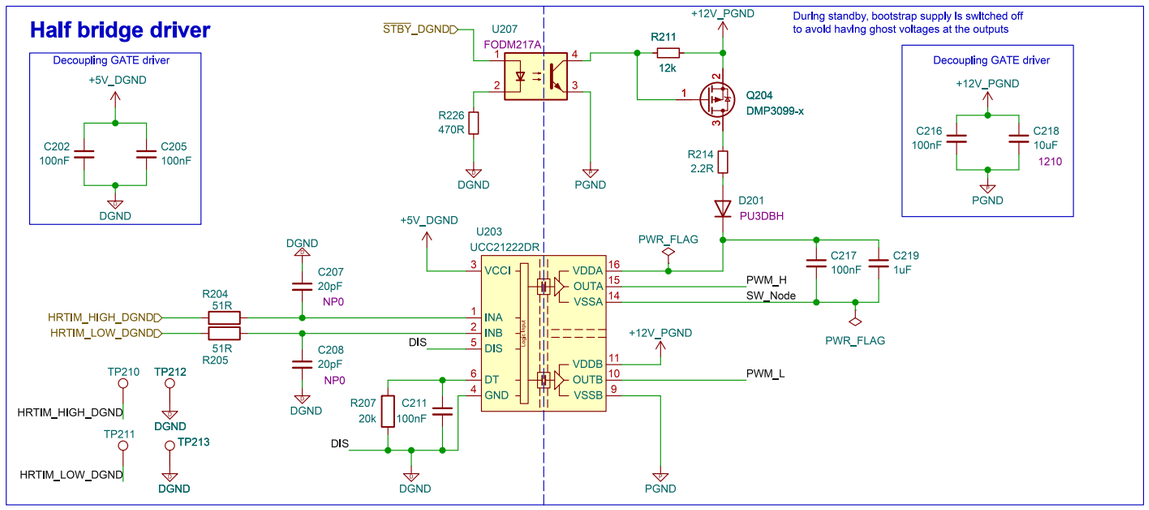
Size: A3 | Scale: | Sheet: /

KiCad E.D.A. 8.0.0 | Id: 1/6

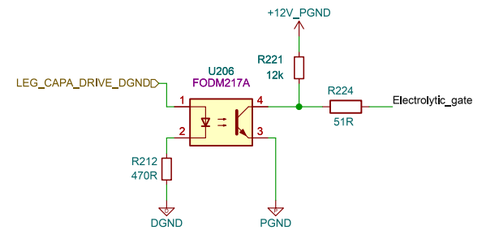
Synchronous buck power topology



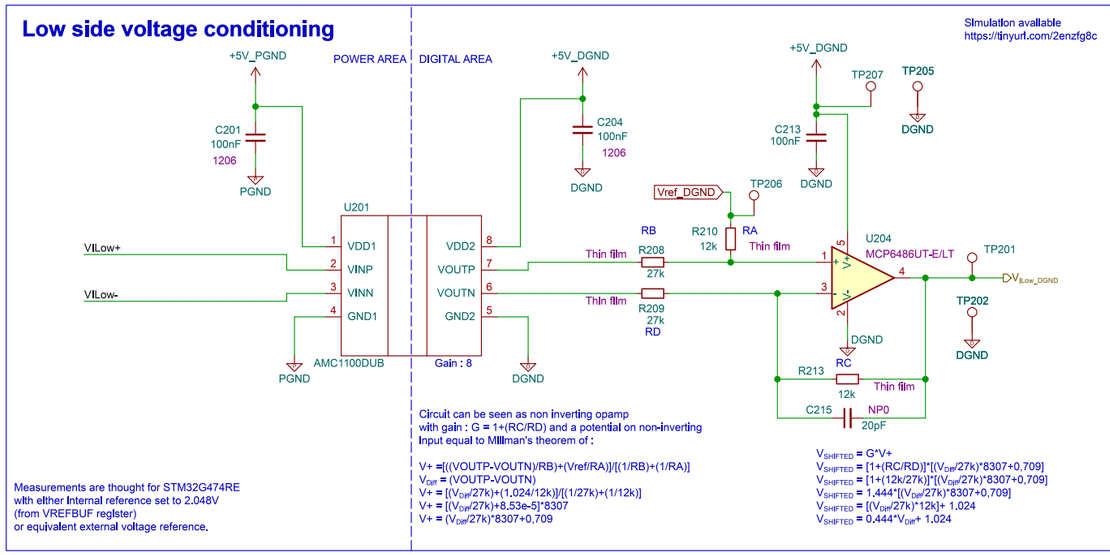
Half bridge driver



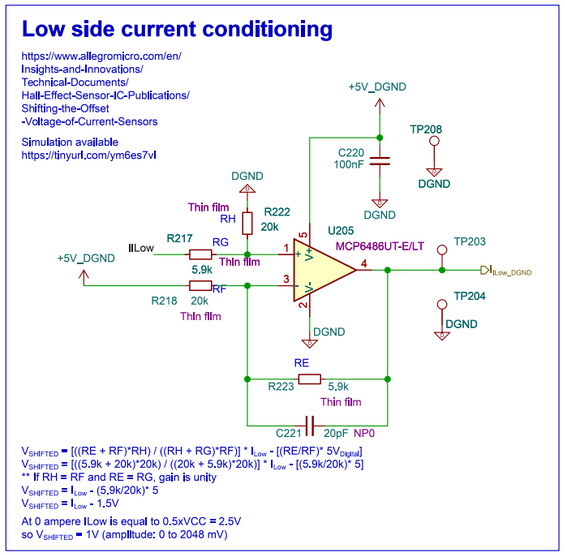
Low side electrolytic capacitor ground connection control



Low side voltage conditioning



Low side current conditioning



NOTES :

Source repository : https://gitlab.laas.fr/owntech/1leg/-/tree/V1.1.2

Preliminary PREL, Good For Execution, GFE, As Built ASB
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Date	Rev.	Creator	Reviewer	Approver	Status
	B				
	A				
2023-10-11	-	WALTER			

Title: TWIST 1.4

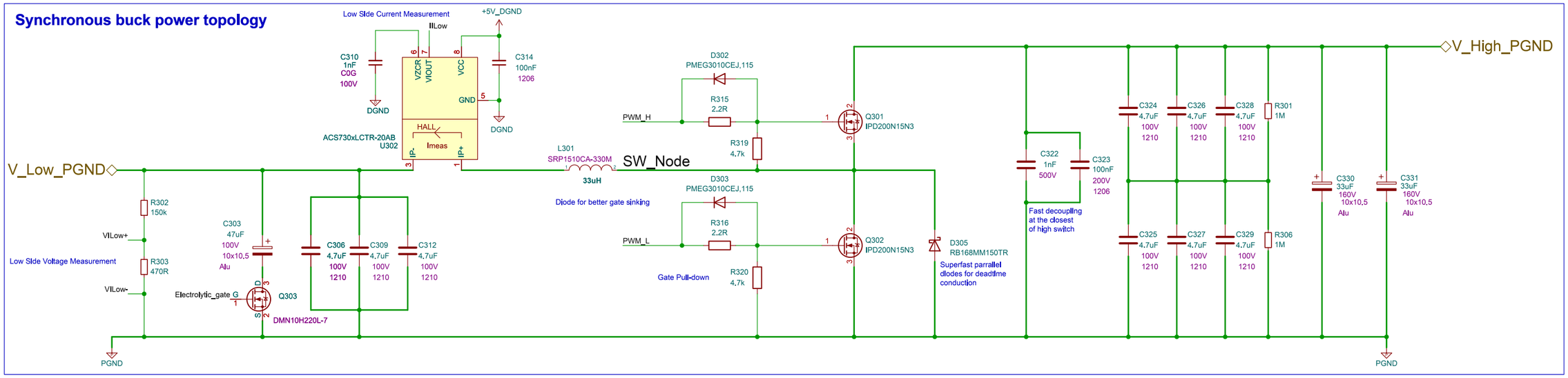
OwnTech Open Digital Power

File: PowerLeg1.kicad_sch

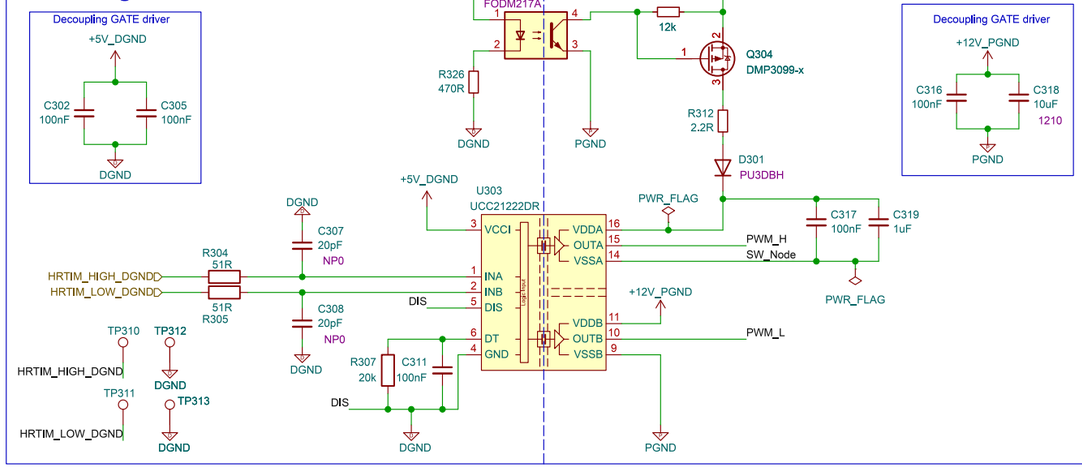
Size: A3 | Scale: | Sheet: /Power Leg 1/

KiCad E.D.A. 8.0.0 | Id: 2/6

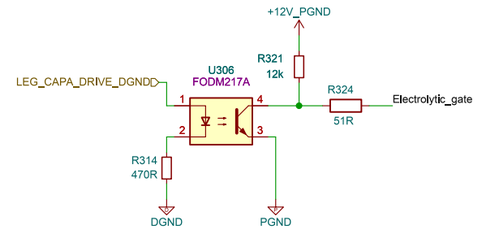
Synchronous buck power topology



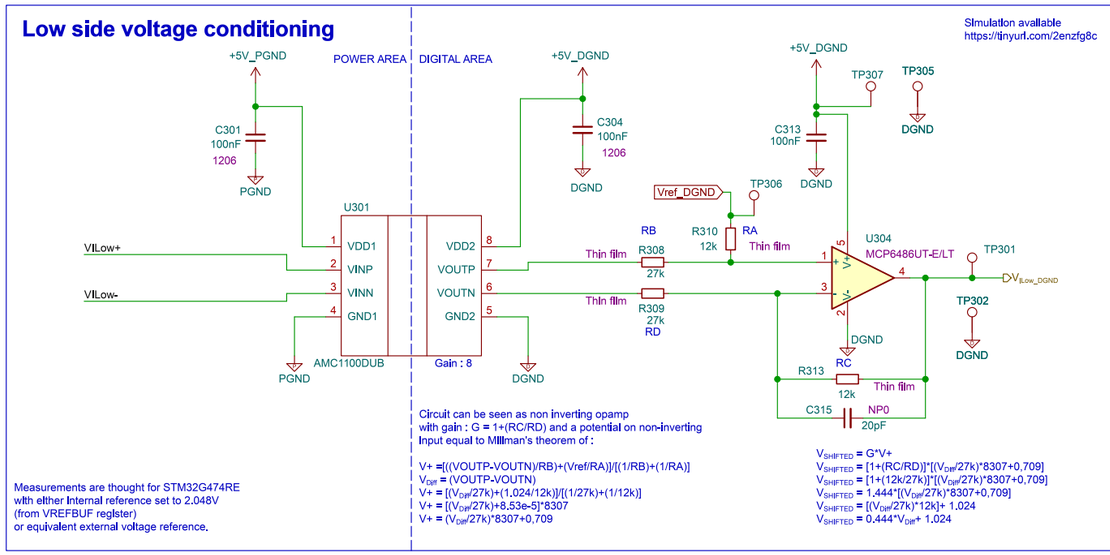
Half bridge driver



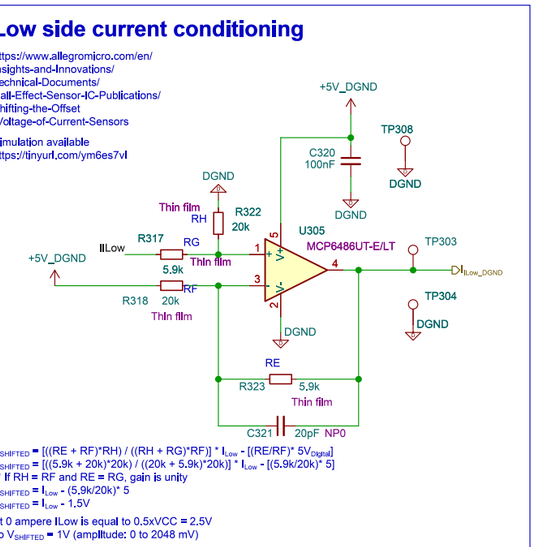
Low side electrolytic capacitor ground connection control



Low side voltage conditioning



Low side current conditioning



NOTES :

Source repository : https://gitlab.laas.fr/owntech/1leg/-/tree/V1.1.2

Preliminary PREL, Good For Execution, GFE, As Built ASB
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Date	Rev.	Creator	Reviewer	Approver	Status
	B				
	A				
2023-10-11	-	WALTER			

Title: TWIST 1.4

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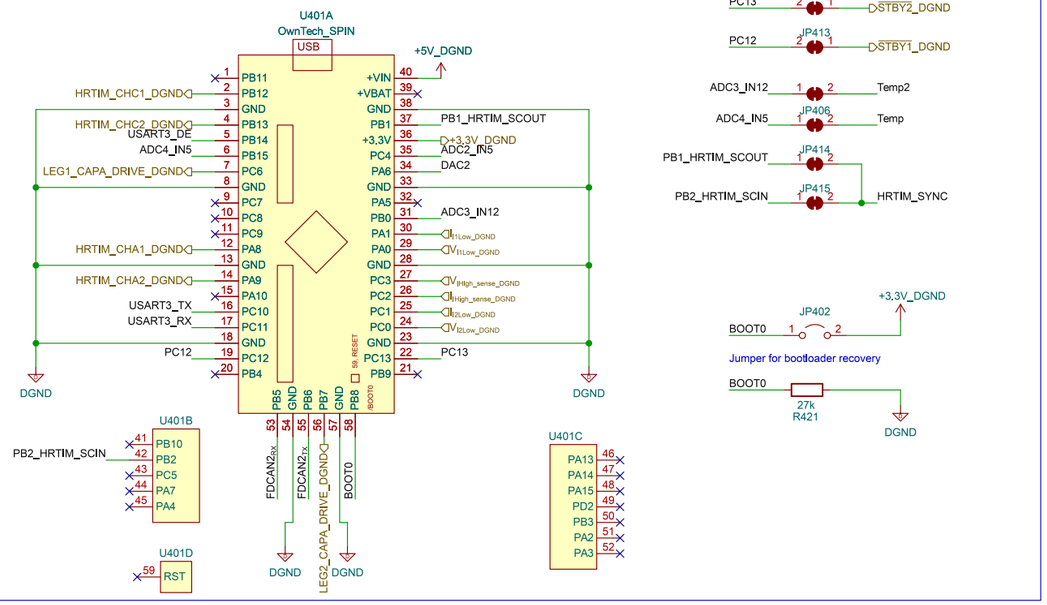
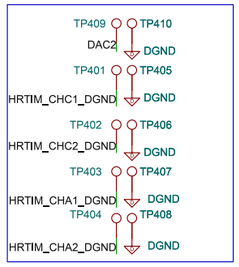
File: PowerLeg1.kicad_sch

Size: A3 | Scale: | Sheet: /Power Leg 2/

KiCad E.D.A. 8.0.0 | Id: 3/6

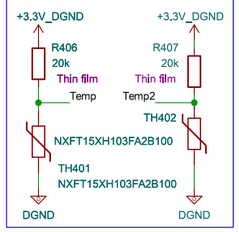
SPIN pinout





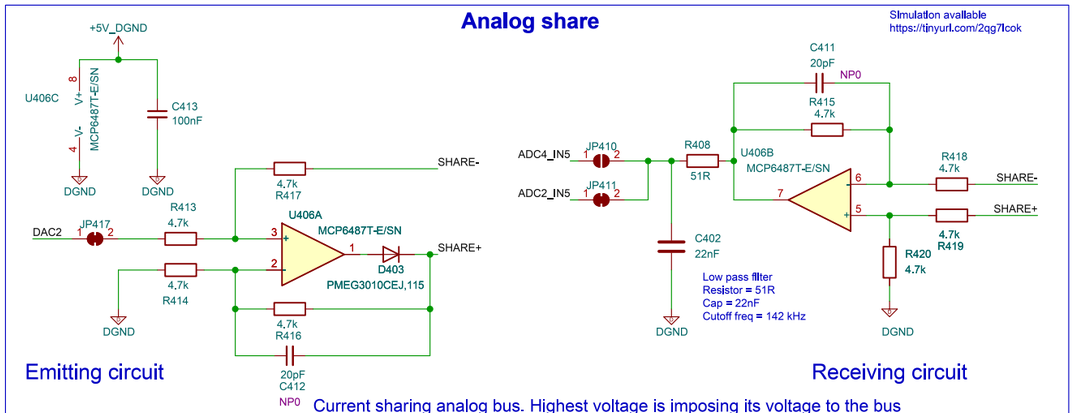
Temperature sensor is wired
to a flexible temp probe
attached to the heatsink
Range : -5°C to +125°C
Max current flowing: 0.16mA@125°C
R0 = 10kOhm @T0 = 25°C
B = 3450
R = R0 * exp[B(T0-T)/T0*T]
Temp expressed In °K

FALSTAD
https://tinyurl.com/2262hpg6



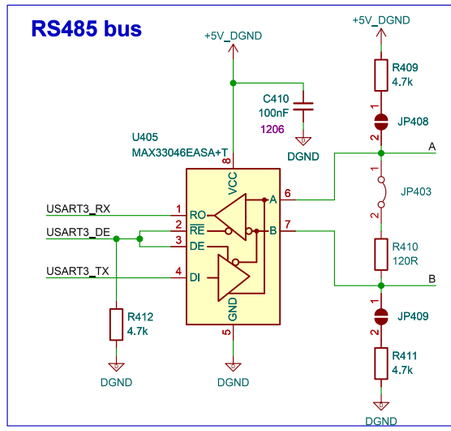
Analog share

Simulation available
https://tinyurl.com/2qg7lcok

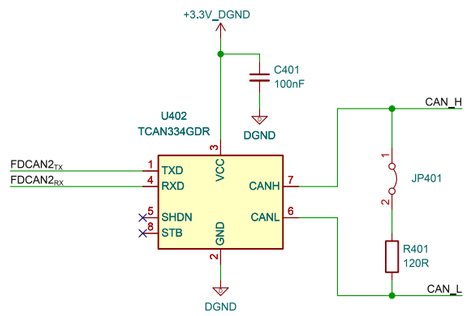


Current sharing analog bus. Highest voltage is imposing its voltage to the bus

RS485 bus

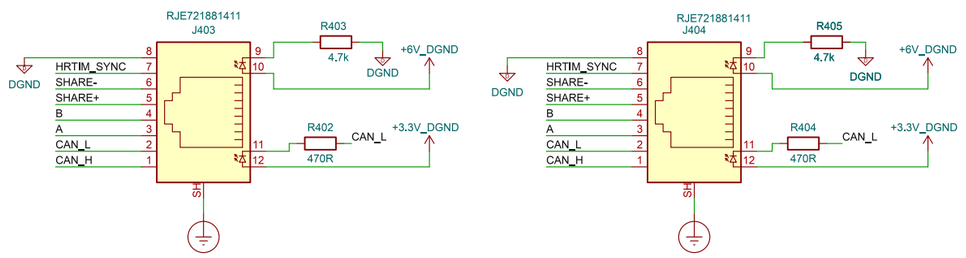


CAN bus



CopyLeft LibreSolar

Communication RJ45 terminals



Communication link encompasses
- Analog bus
- CAN bus
- HRTIM sync
- RS485 20Mbps bus

NOTES :

Source repository : https://gitlab.laas.fr/owntech/1leg/-/tree/V1.1.2

Preliminary PREL, Good For Execution, GFE, As Built ASB
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Date	Rev.	Creator	Reviewer	Approver	Status
	B				
	A				
2023-10-11	-	WALTER			

Title: TWIST 1.4

OwnTech
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File: Microcontroller.kicad_sch

Size: A3	Scale:	Sheet: /MCU/
KiCad E.D.A. 8.0.0		Id: 4/6

Jumper that permits
to isolate the feeder supply
if faulty

Input 10-110V
@600mA max

VIN_PGND
JP5001
L5001
10uH
High_voltage
input
PWR_FLAG

C5002 470nF
C5003 470nF
C5005 4.7uF 100V 1210
C5006 4.7uF 100V 1210
C5008 4.7uF 100V 1210
C5009 4.7uF 100V 1210
HV
HV
PGND

Added inductor
and extra capacitors
for the input filter
as per application note

UVLO is the feeder
start-up threshold.
Configured for 9,7V
start-up.

Once started it will
operate for any VIN
higher than 8,9V

D5 is the
overvoltage
protection
that sense
the Aux voltage
NTC1 is the over
temperature
protection

Do not populate
these parts for
initial testing.
As Fault pin is
not necessary at
first

TP5001
PGND

PWR_FLAG
VBoost

R5003 47k
R5004 4.7k
VAUX
D5001 6.2V
C5010 22nF
NTC5001 100kNTC
C5011 22nF
R5005 100k
C5013 1nF C0G 100V
PGND

22nF means
~20ms soft start

100k means
100kHz switching
frequency

U5003
NCP12700ADNR2G
UVLO
FLT
SS
RT
COMP
VIN
DRV
CS
VCC
GND

C5015 100nF 250V X7T
R5008 2.2R
R5010 10R
D5003 PMEG3010CEJ,115
Q5002 TK13P25D,RQ(S
R5012 12k
R5009 470R
C5016 100pF 1kV 1206 C0G
R5014 240m 1210
R9 is the current
sensing resistor.
240m should give
Ipeak ~2A

Snubber circuit
As per Application
Note DN05109-D

R5013 330k
C5021 6,8nF 630V
D5004 PU3DBH
C5022 100pF 1kV 1206 C0G DNP
MOSD
MOSS

VBoost
D5002 PMEG3010CEJ,115
L5002 100uH
VAUX
R5015 10R
D5005 BAS20HT1G
D5006 BAS20HT1G
C5019 1uF
Q5001
DMN10H220L-7
R5007 1.4k
C5017 1uF
R5016 1.4k
Aux

T5001
PA2467NL
37uH

ISat for PA2467NL
is about 2.85A

C5024 2.2nF 1812 2.5kV
C5025 2.2nF 1812 2.5kV
PGND
DGND

C5026 1nF 500V
R5017 10R 1W 2010
D5007 PU3DBH
C5028 10uF 1210
TP5002
DGND

Jumper that permits
to isolate the feeder if needed
External supply can provide +6V from pin 2 and 3

+6VJP
J5003
Header_2_54_01x03
PWR_FLAG
+6V_DGND
C5031 100uF 6.3x7.7 25V Alu
DGND
DGND

R5020 10R

Type 2 Isolated feedback network with TL431
As per Application note DN05109-D

Explanation
https://www.onsemi.com/pub/Collateral/TND381-D.PDF

RB is the value to change the output voltage
It should be 27K to stabilize it to 6.05V

TL431 give Vo = 6.05V
with Vo = Vref(1 + RA/RB)
6.05V = 2,5V * (1 + 38,3K/27K)

RA
R5021 38.3k
R5018 1.4k
R5019 12k
C5030 6,8nF 630V
TL431
U5006
TL431MFDT,215
REF
RB
R5022 27k Thin film
DGND

U5005
FODM217A

Passive unregulated
boost permits to supply
control IC from auxiliary
as output voltage is below 9V

PGND

NOTES :

This feeder design is based on a Flyback DCM design largely inspired from Application Note DN05109-D

Targeted SPEC:
11-110V Input
6V Output @ 0.5A
DCM boundary @ 70% max load

Source repository : https://gitlab.laas.fr/owntech/1leg/-/tree/V1.1.2

Preliminary PREL, Good For Execution, GFE, As Built ASB
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Date	Rev.	Creator	Reviewer	Approver	Status
	B				
	A				
2023-10-11	-	WALTER			

Title: TWIST 1.4

OwnTech
Open Digital Power

File: Feeder.kicad_sch

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Size: A3 | Scale: | Sheet: /Feeder/

KiCad E.D.A. 8.0.0 | Id: 5/6

+5V_DGND
C5004 100nF
R5001 47k Thin film
U5001
MCP6486UT-E/LT
C5001 20pF NP0
R5002 12k Thin film
C5007 20pF NP0 DNP
DGND
Vref_DGND
JP5002

1,024V reference for measurement offset
Simulation available
https://tinyurl.com/mtt5xsmv

External power supply
- 6V
- 100mA

Polyfuse to prevent
over-current in daisy-chained
bus with multiple sources and
sinks.

+6V_DGND
F5001 0ZCH0035FF2G 350mA 1210
F5002 0ZCH0035FF2G 350mA 1210
PWR_COM1
PWR_COM2
J5001
J5002

Low Drop Out
Linear regulator to get
Noise free +5V

U5002
AZ1117CH-5.0TRG1
C5012 10uF 1210
C5014 10uF 1210
R5006 2.2R

Isolated DCDC blocks to have
+12V and +5V referenced to PGND

U5004
AZ1117CH-5.0TRG1
C5018 10uF 1210
R5011 2,2R
C5020 10uF 1210
C5023 10uF 1210
PS5001
IL0512S
C5027 10uF 1210
L5003 22uH
C5029 10uF 1210

IHigh and VHigh sense

PIN 6 (Filter) of ACS712 is designed to connect a capacitor to ground to form low pass RC filter with an internal capacitor of 1.7kOhm

According to formula theoretical cutoff frequency is calculted like so :

fc = 1/(2*pi*R*C)

Here we have some examples of cutoff frequency for different values of capacitor

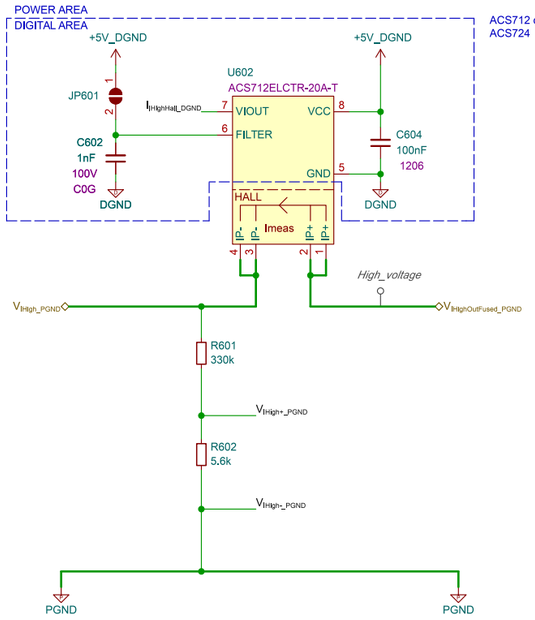
C (nF)	fc (kHz)
1	93.6
10	9.36
100	0.936

But in datasheet it is written 80kHz (-3dB) for 1nF...

ACS723 is pin to pin compatible with ACS712. If ACS723 is used, disconnect CA and tie pin 6 to either +5V or GND for wanted BW

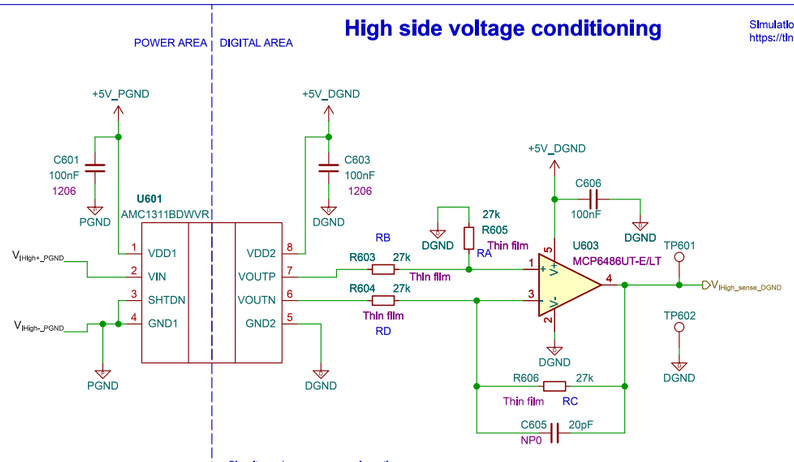
ACS723 pin 6 BW_SELECT :
- tie to ground for 80kHz BW.
- tie to VCC for 20kHz bandwidth.

ACS712 direct equivalence: ACS724



High side voltage conditioning

Simulation avallable
https://tinyurl.com/yodepbhp



Circuit can be seen as non inverting opamp with gain : G = 1+(RC/RD) and a potential on non-inverting input equal to :

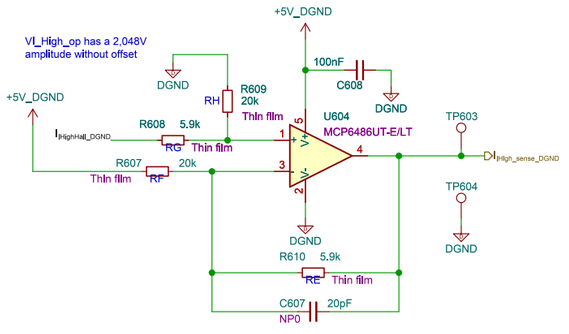
V+ =(VOUTP-VOUTN)*(RA/(RA+RB))

V_{Diff} = (VOUTP-VOUTN)

V+ = V_{Diff}*(RA/(RA+RB))
V+ = V_{Diff}*(27k/(27k+27k))
V+ = V_{Diff}*0.5

$V_{SHIFTED}$ = G*V+
$V_{SHIFTED}$ = [1+(RC/RD)]*0.5*V_{Diff}
$V_{SHIFTED}$ = [1+(27k/27k)]*0.5*V_{Diff}
$V_{SHIFTED}$ = 2*0.5*V_{Diff}
$V_{SHIFTED}$ = V_{Diff}

High side current conditioning



$V_{SHIFTED}$ = [((RE + RF)*RH) / ((RH + RG)*RF)] * I_{High} - [(RE/RF)* $5V_{Digital}$]
$V_{SHIFTED}$ = [((5.9k + 20k)*20k) / ((20k + 5.9k)*20k)] * I_{High} - [(5.9k/20k)* 5]
** If RH = RF and RE = RG, gain is unity
$V_{SHIFTED}$ = I_{High} - (5.9k/20k)* 5
$V_{SHIFTED}$ = I_{High} - 1.5V

At 0 ampere IHigh is equal to 0,5xVCC = 2,5V
so $V_{SHIFTED}$ = 1V (amplitude: 0 to 2048 mV)

Simulation avallable
https://tinyurl.com/ym6es7vl

NOTES :

Source repository : https://gitlab.laas.fr/owntech/1leg/-/tree/V1.1.2

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	B				
	A				
2023-10-11	-	WALTER			

Title: TWIST 1.4

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File: High_side.kicad_sch

Size: A3 | Scale: | Sheet: /High_side/

KiCad E.D.A. 8.0.0 | Id: 6/6