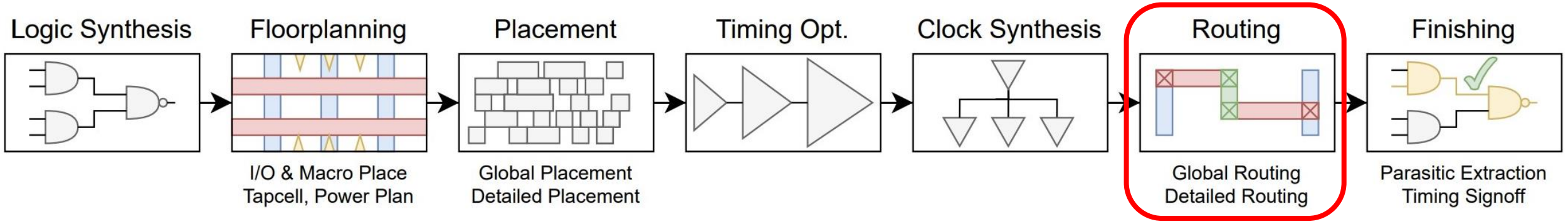
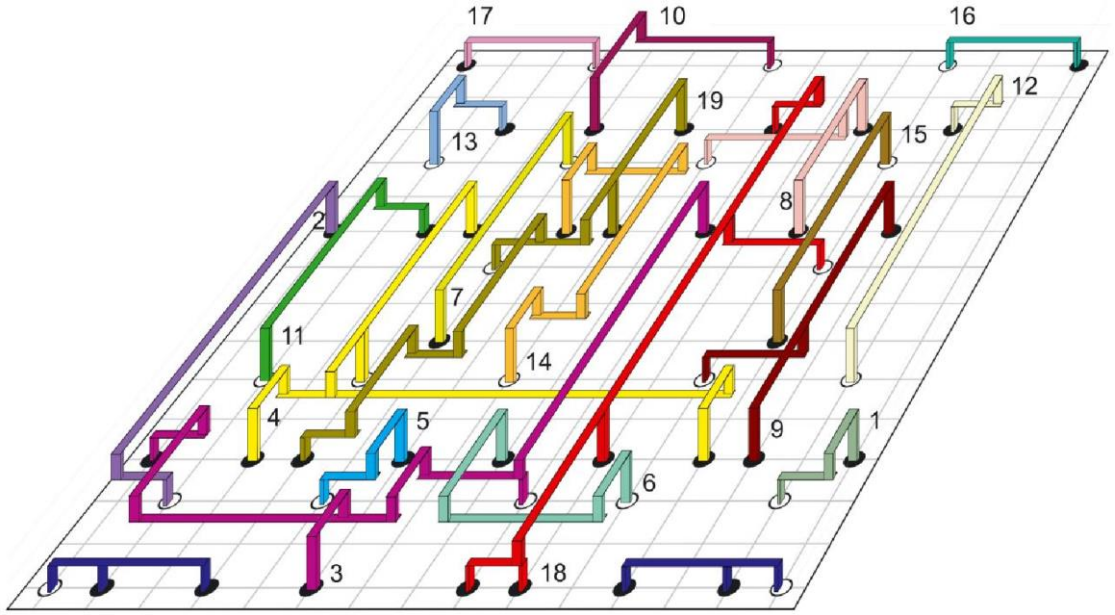
Routing


Logic Synthesis
Floorplanning
I/O & Macro Place
Tapcell, Power Plan
Placement
Global Placement
Detailed Placement
Timing Opt.
Clock Synthesis
Routing
Global Routing
Detailed Routing
Finishing
Parasitic Extraction
Timing Signoff

Routing

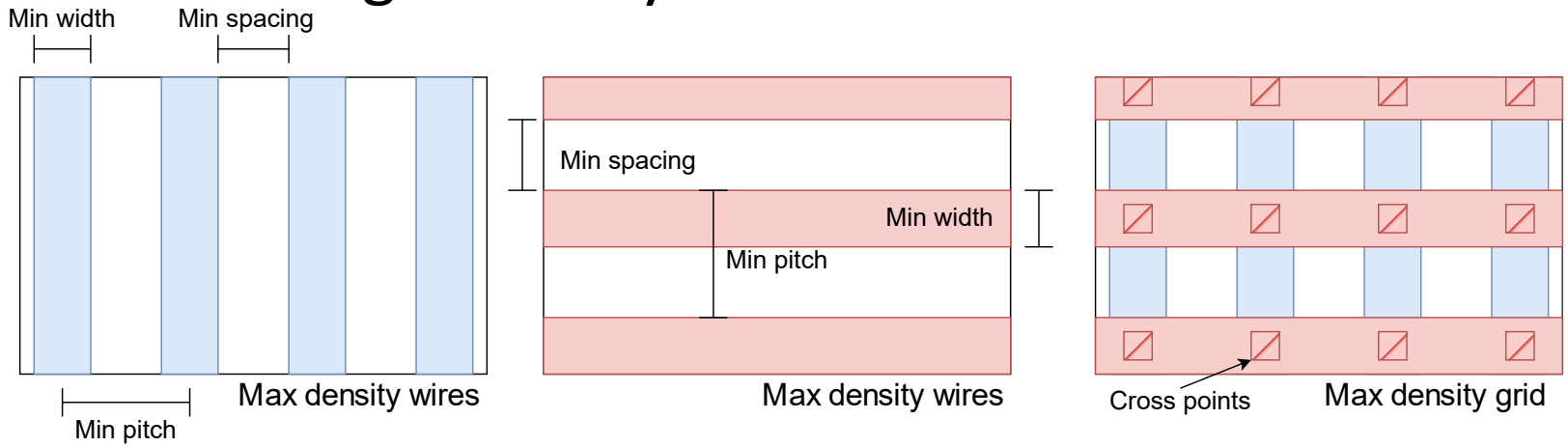
- Physically connect your circuit with wires
- Similar to placement, routing is a hard problem and broken into steps
- Steps
  - Track creation
  - Global routing
  - Detailed routing



Track Creation → Global Routing → Detailed Routing

Track Creation

- Reminder: metals have a min. width and min. spacing dictated by DRC
- Stacking min. width wires at min. pitch creates a **routing grid** which enables the max. number of routes on the chip possible
- Generate a grid of “routing tracks” that metals need to align to
- “Manhattan” routing: each layer is either all-vertical or all-horizontal

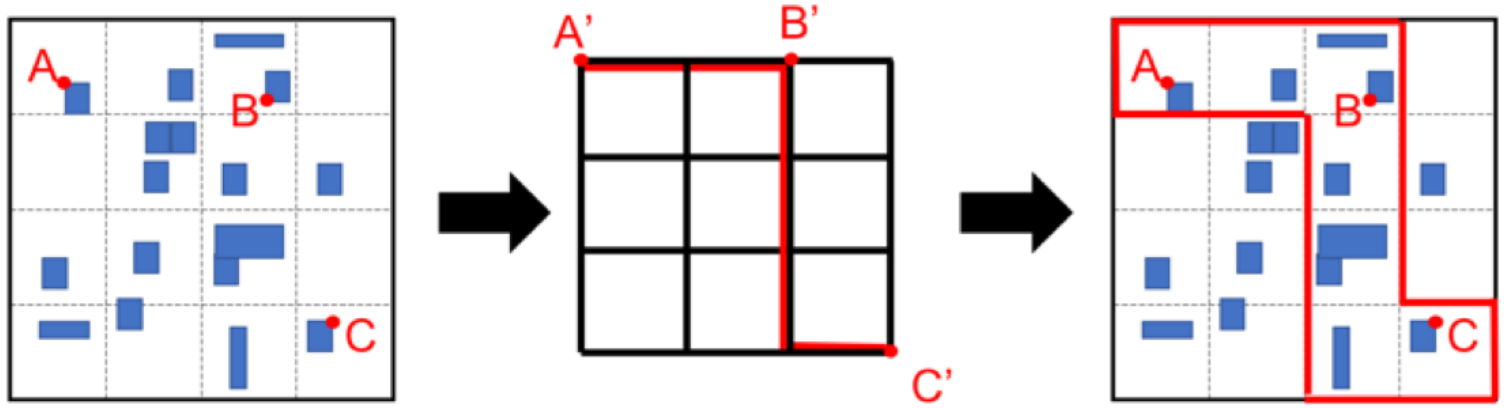


Track Creation > Global Routing > Detailed Routing

Routing

- Two main concerns in routing: **congestion** and **DRC violations**
- **Congestion**: too many routes per unit area means it will be impossible to route wires without shorts and/or violations
- **DRC violations**: routes must follow all design rules or chip can’t be fabricated
- Huge problem to address concurrently; solve individually

Global Routing



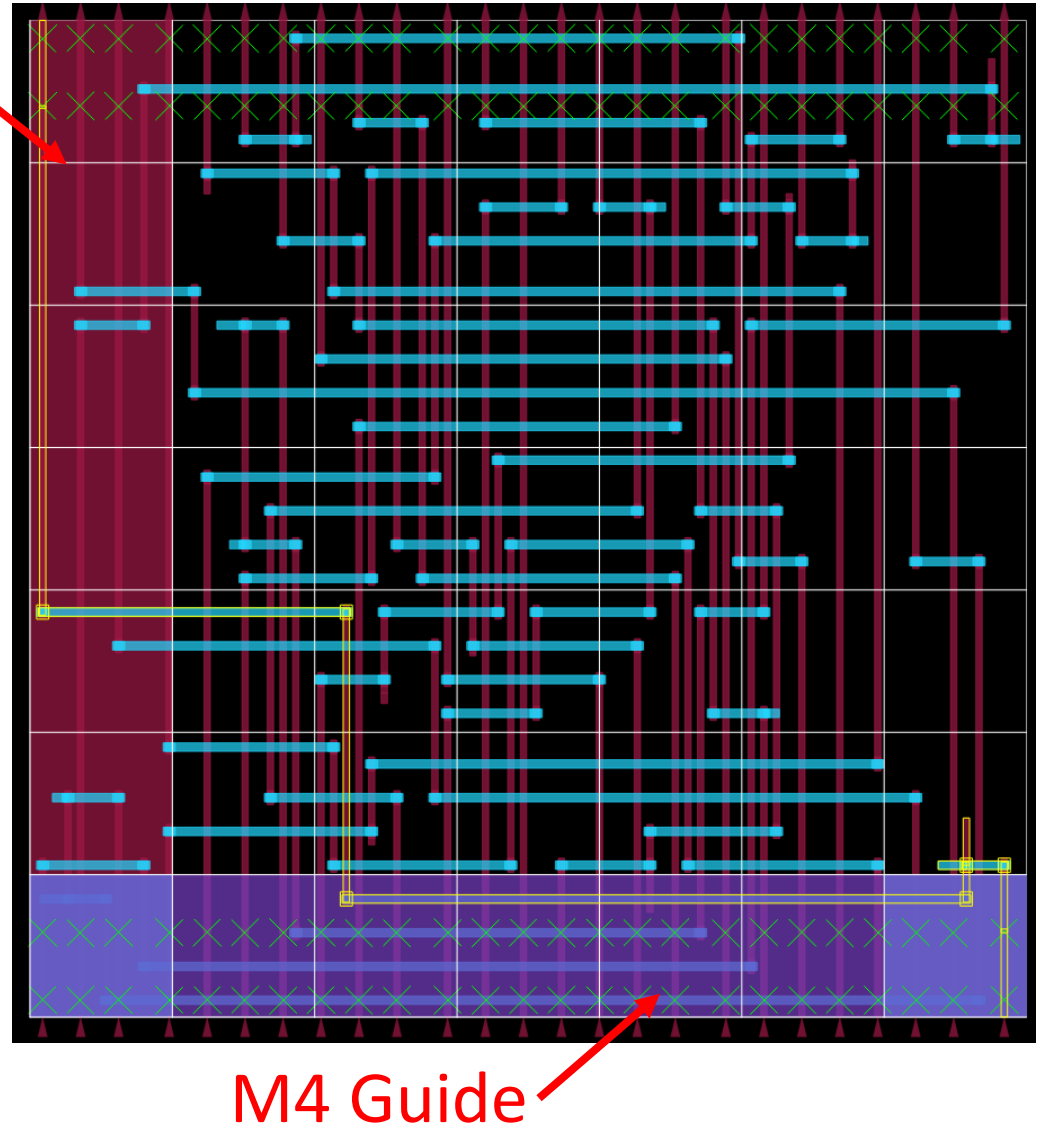
- Try to pre-allocate tracks so that no given area is over-congested
- Divide up the whole chip into partitions called Global Cells (**GCells**)
- Each GCell represents about 10-15 tracks
- Perform maze routing
- Each route through a GCell decrements # available tracks
- If a GCell has <0 tracks, it is over-congested and requires rerouting
- Output: **route guides** which are used in detail routing

Track Creation | **Global Routing** | Detailed Routing

Global Routing: User View

- Commercial tools don’t give as much info
- They like to bundle their global+detailed router together to hide things from the user, but they’re still there
- OpenROAD shows the process more clearly

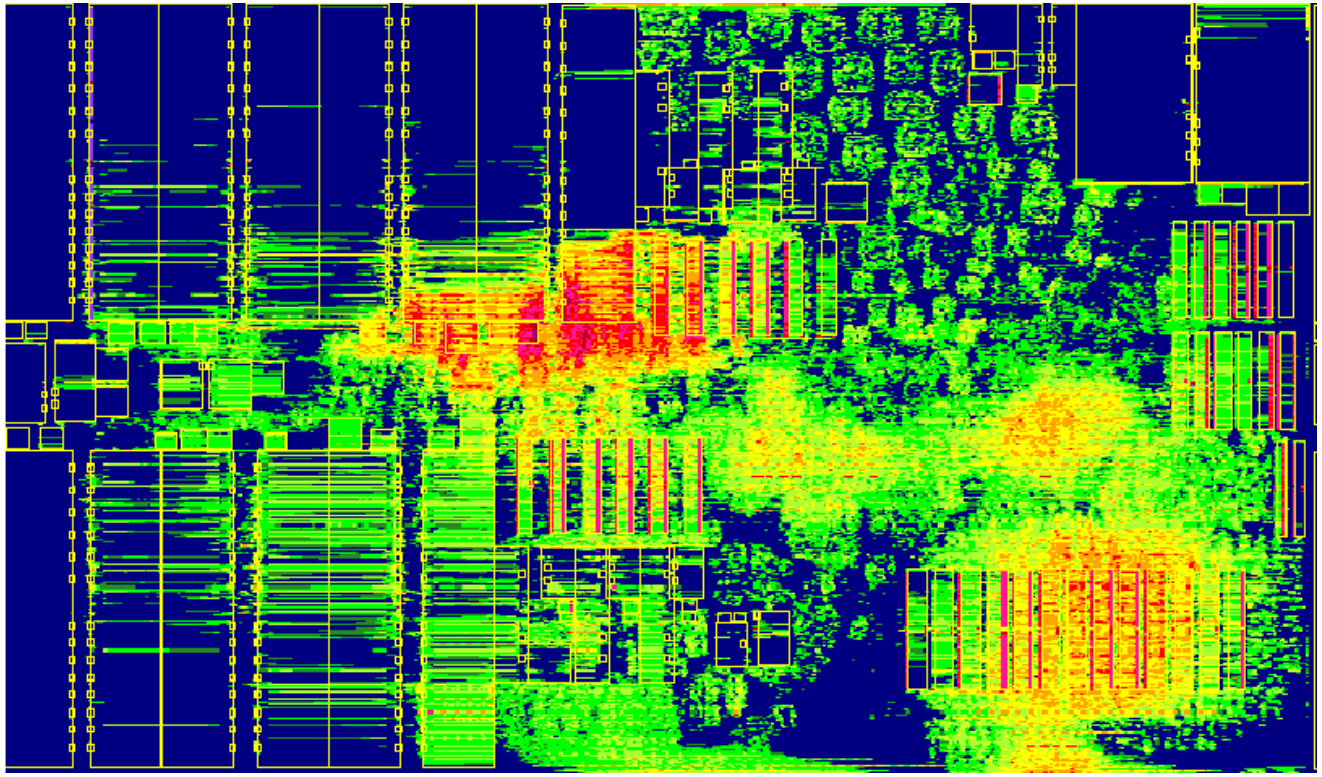
```
[INFO GRT-0096] Final congestion report:
Layer         Resource        Demand        Usage (%)    Max H / Max
------------------------------------------------------------------
metal1               0             0            0.00%             0 /
metal2            2464           489           19.85%             0 /
metal3            4704           677           14.39%             0 /
```



Track Creation | **Global Routing** | Detailed Routing

Global Routing: Common Problems

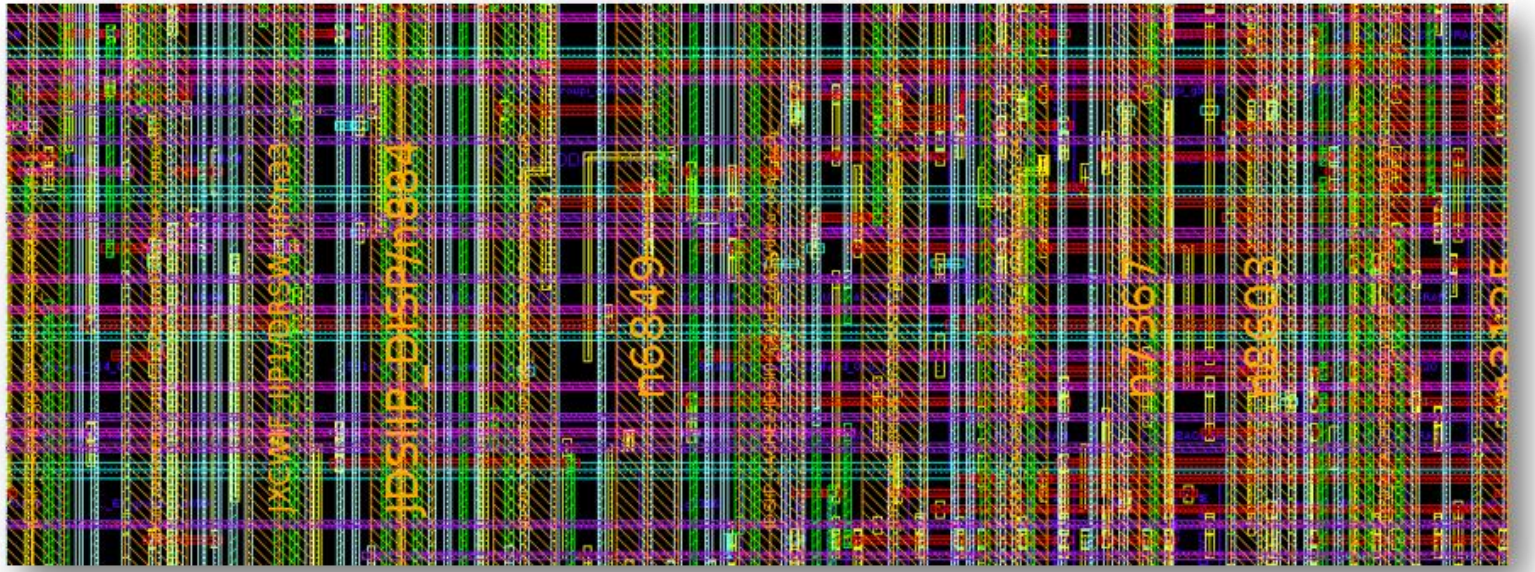
- Mainly congestion issues
- If you have a cell placement issue or a macro placement issue, it might show up now!
  - Ex. You have 100 routes that need to go between 2 macros but only 70 tracks
- Global routers might not know when to give up – excessive runtime



Track Creation | **Global Routing** | Detailed Routing

Detailed Routing

- Use route guides provided by global routing – constrained search
- Try to create physical wires which don't cross and don't violate DRC
- Perform finer-grain maze routing
- Check for DRC violations
- Iterate until solution has 0 violations (or max iterations)

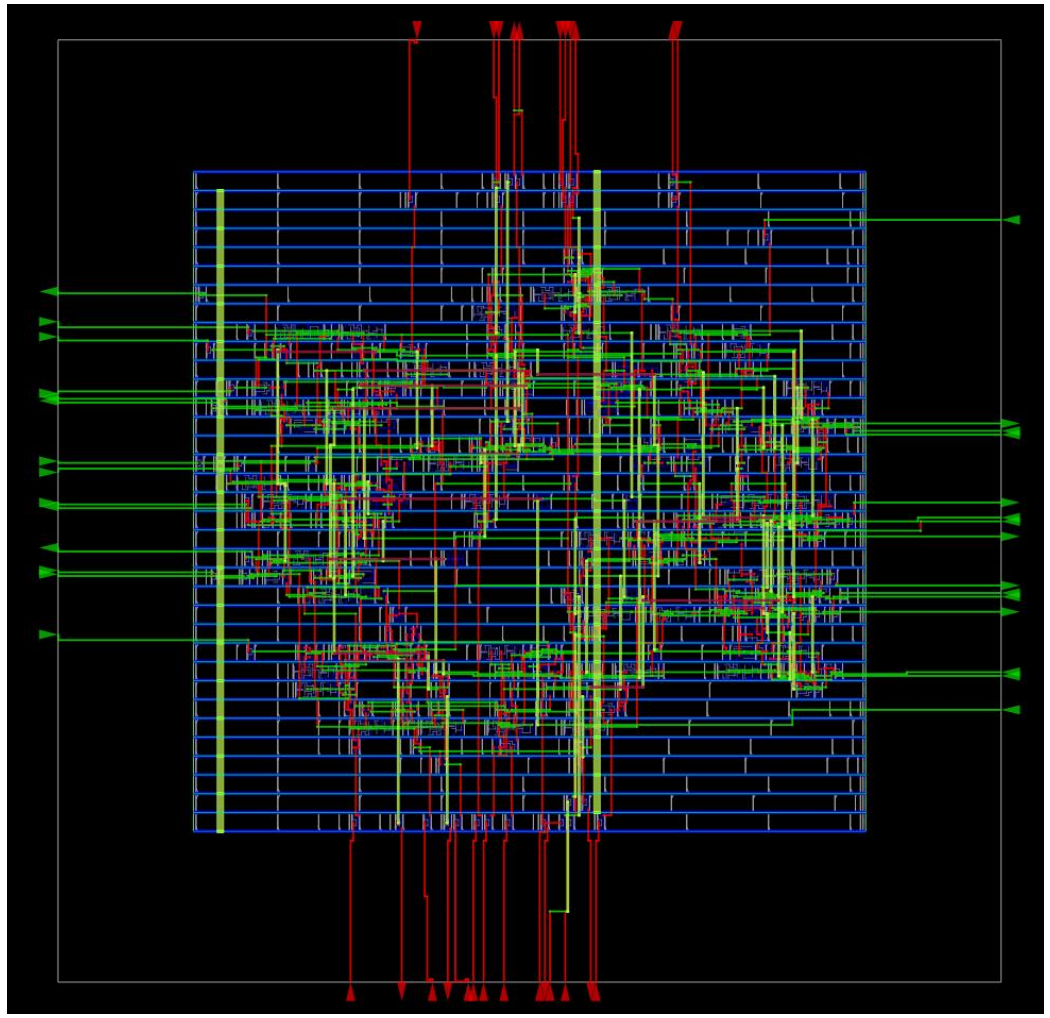


Track Creation → Global Routing → **Detailed Routing**

Detailed Routing: User View

- Detailed routing generally takes the longest of all steps
- Iterating to find a clean solution for 10k+ rules takes a while for large designs
- Looks like a real design now!

```
[INFO DRT-0194] Start detail routing.
[INFO DRT-0195] Start 0th optimization iteration.
    Completing 10% with 0 violations.
    elapsed time = 00:00:00, memory = 96.41 (MB).
    Completing 20% with 0 violations.
    elapsed time = 00:00:00, memory = 96.70 (MB).
```



Track Creation → Global Routing → **Detailed Routing**

Detailed Routing: Common Problems

- Basically all problems will manifest here (or in timing)
  - It's tough; may have to dig back several steps in the flow to ID root cause
- Global routing miscorrelation: predicted more resources available than actually possible
- Placement issues: a few specific cells (or macros) are placed together in a way that makes accessing the pins impossible
- Power grid issues: a poor power grid can make it impossible to access certain rows cleanly

Track Creation → Global Routing → **Detailed Routing**